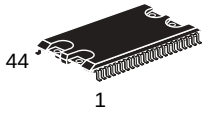
M616Z08

128 Kbit (8 Kbit x16) SRAM with Output Enable

FEATURES SUMMARY

- OPERATION VOLTAGE: 2.34V TO 3.6V
- 8 Kbit x16 SRAM
- EQUAL CYCLE and ACCESS TIMES: AS FAST AS 20ns
- TRI-STATE COMMON I/O
- TWO WRITE ENABLE PINS ALLOW WRITING TO UPPER AND LOWER BYTES

Figure 1. Package



SO44 (MH)
44-pin, Hatless SOIC

Figure 2. Logic Diagram

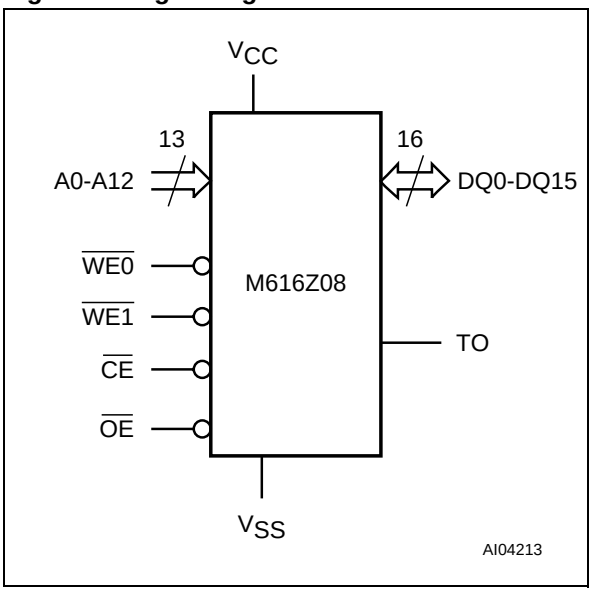


Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE0}$	WRITE Enable DQ 0-7
$\overline{WE1}$	WRITE Enable DQ 8-15
V_{CC}	Supply Voltage
V_{SS}	Ground
TO	Time-Out Pin

Note: TO Pin should be connected to V_{CC}.

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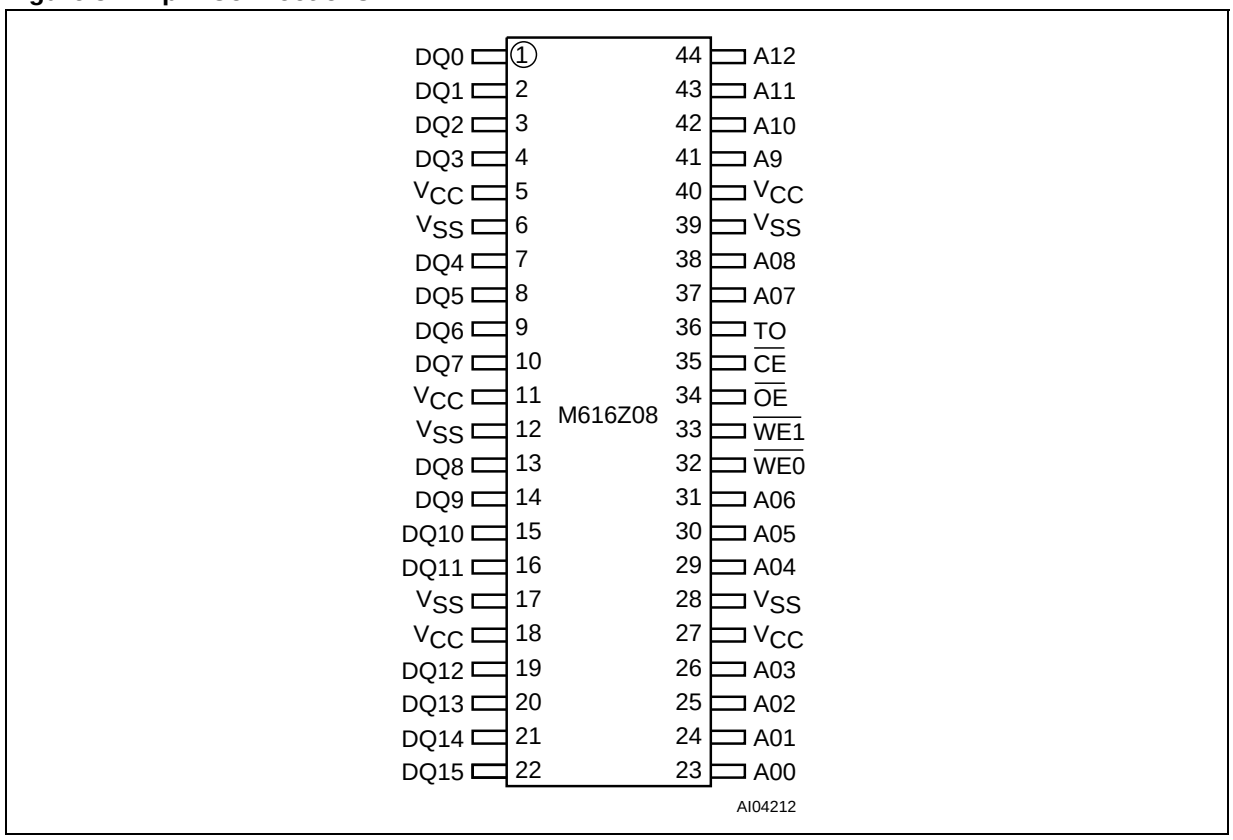
DESCRIPTION

The M616Z08 is a 128 Kbit (131,072 bit) CMOS SRAM, organized by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.6V ± 10% or 3.3V ± 10% supply, and all inputs and outputs are TTL compatible.

The M616Z08 is available in a 44-lead SOIC package.

Figure 3. 44-pin Connections



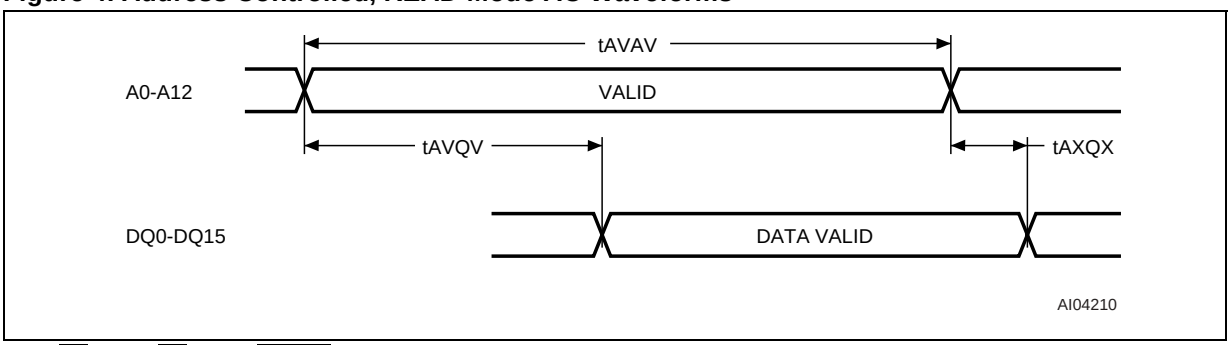
Note: TO Pin should be connected to V_{CC}.

OPERATION

READ Mode

The M616Z08 is in the READ Mode whenever WRITE Enable ($\overline{WE0}$ or $\overline{WE1}$) is High with Output Enable ($\overline{OE}$) Low, and Chip Enable ($\overline{CE}$) is asserted. This provides access to data from sixteen of the 131,072 locations in the static memory array, specified by the 13 address inputs. Valid data will be available at the sixteen output pins within t_{AVQV} after the last stable address, providing $\overline{OE}$ is Low and $\overline{CE}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

Figure 4. Address Controlled, READ Mode AC Waveforms



Note: $\overline{CE}$ = Low, $\overline{OE}$ = Low, $\overline{WE(0,1)}$ = High.

Figure 5. Chip Enable or Output Enable Controlled, READ Mode AC Waveforms

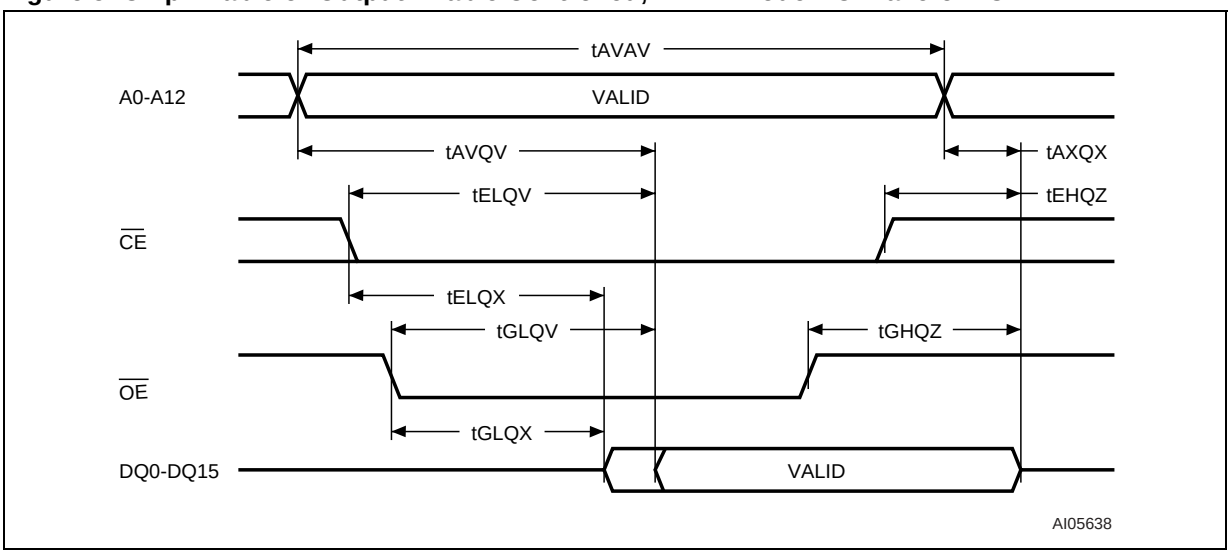


Table 2. READ Mode AC Characteristics

Symbol	Parameter[1]	M616Z08				Unit
		–20				
		2.34 to 3.0V		3.0 to 3.6V		
		Min	Max	Min	Max	
t_{AVAV}	READ Cycle Time	36		20		ns
t_{AVQV}	Address Valid to Output Valid		36		20	ns
t_{ELQV}	Chip Enable Low to Output Valid		36		20	ns
t_{GLQV}	Output Enable Low to Output Valid		20		10	ns
t_{ELQX}	Chip Enable Low to Output Transition	0		0		ns
t_{GLQX}	Output Enable Low to Output Transition	0		0		ns
t_{EHQZ}[2]	Chip Enable High to Output Hi-Z		10		10	ns
t_{GHQZ}[2]	Output Enable High to Output Hi-Z		10		10	ns
t_{AXQX}	Address Transition to Output Transition	0		0		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 125°C (except where noted).
2. C_L = 5pF.

WRITE Mode

The M616Z08 is in the WRITE mode whenever the WE0 (low memory addresses) or WE1 (high memory addresses) and CE pins are low (see Table 4., page 8). Either the Chip Enable input (CE) or the WRITE Enable input (WE0 or WE1) must be de-asserted during Address transitions for subsequent WRITE cycles. WRITE begins with the concurrence of Chip Enable being active with WE0 or WE1 low. Therefore, address setup time is referenced to WRITE Enable and Chip Enable as t_{AVWL} and t_{AVEH} respectively, and is determined by the latter occurring edge.

The WRITE cycle can be terminated by the earlier rising edge of CE, or WE0/WE1.

if the Output is enabled ($\overline{CE}$ = Low and $\overline{OE}$ = Low), then WE0 or WE1 will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of WRITE Enable, or for t_{DVEH} before the rising edge of $\overline{CE}$, whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

Note: When using MCP555 with TO Pin high, relaxed WRITE timing (CSNT = 1 in the chip select configuration register) should be selected.

Figure 6. WRITE Enable Controlled, WRITE Mode AC Waveforms

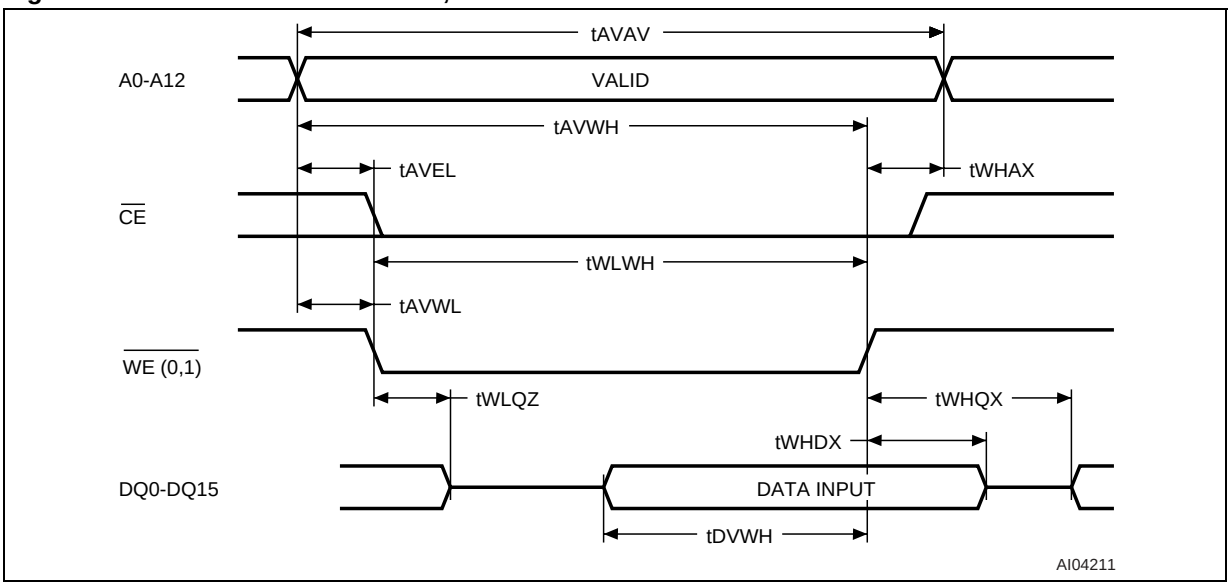
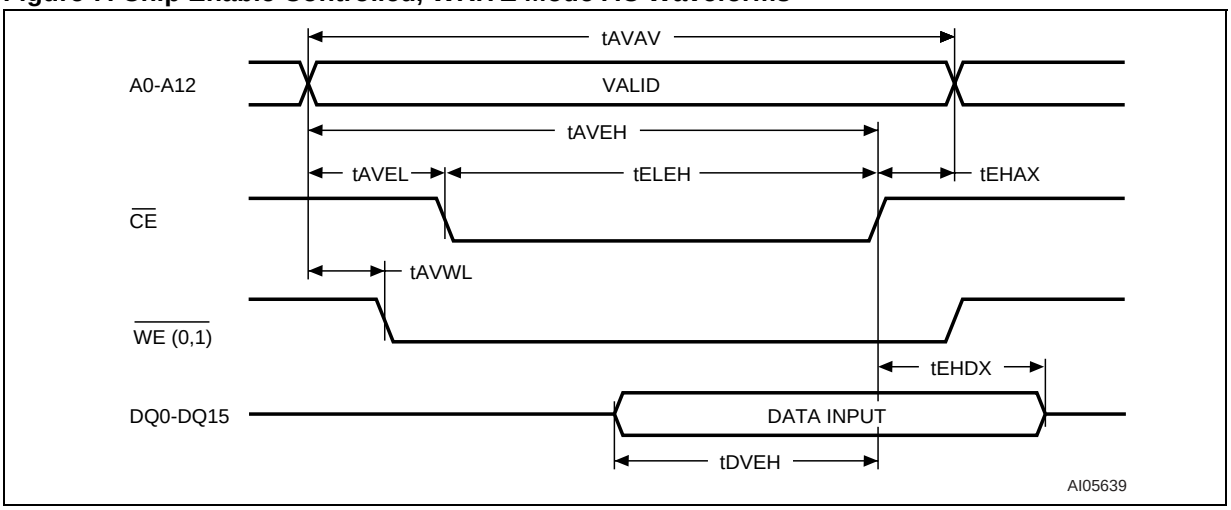


Figure 7. Chip Enable Controlled, WRITE Mode AC Waveforms



Note: 1. Output Enable ($\overline{OE}$) = High.
2. If $\overline{CE}$ goes High with $\overline{WE0}$ or $\overline{WE1}$ high, the output remains in a high-impedance state.

Table 3. WRITE Mode AC Characteristics

Symbol	Parameter[1]	M616Z08				Unit
		–20				
		2.34 to 3.0V		3.0 to 3.6V		
		Min	Max	Min	Max	
t_{AVAV}	WRITE Cycle Time	36		20		ns
t_{AVWL}	Address Valid to WRITE Enable Low	2		2		ns
t_{AVWH}	Address Valid to WRITE Enable High	34		18		ns
t_{AVEH}	Address Valid to Chip Enable High	34		18		ns
t_{WLWH}	WRITE Enable Pulse Width	25		11		ns
t_{WHAX}	WRITE Enable High to Address Transition	2		2		ns
t_{WHDX}	WRITE Enable High to Input Transition	2		2		ns
t_{WHQX}[3]	WRITE Enable High to Output Transition	0		0		ns
t_{WLQZ}[2,3]	WRITE Enable Low to Output Hi-Z		10		10	ns
t_{AVEL}	Address Valid to Chip Enable Low	2		2		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	25		11		ns
t_{EHAX}	Chip Enable High to Address Transition	2		2		ns
t_{EHDX}	Chip Enable High to Input Transition	2		2		ns
t_{DVWH}	Input Valid to WRITE Enable High	20		8		ns
t_{DVEH}	Input Valid to Chip Enable High	20		8		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 125°C (except where noted).
2. C_L = 5pF
3. At any given temperature and voltage condition, t_{WLQZ} is less than t_{WHQX} for any given device.

"Operational" Mode

The M616Z08 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted (CE = High). An Output Enable (OE) signal provides a high speed tri-state control, allowing fast READ/WRITE cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs WE0 or WE1 and CE as summarized in "Operating Modes" (see Tables 4 and 5).

Noise Immunity

When designing with high speed memory, proper power trace layout and capacitive decoupling must be maintained to ensure proper system operation. Power and ground line inductance should be reduced by providing separate power planes. The impedance of the decoupling path from the power pin through the decoupling capacitor should also be kept to a minimum. Small decoupling capacitors (10nF) should be located as close to the device pins as possible to limit the high frequency noise. Larger capacitor values (10uF and 1uF) are recommended to reduce low frequency noise and should be placed next to the power entry point of the board. Proper line termination should also be employed to minimize signal reflection.

See Motorola Semiconductor Application Note AN2127/D for additional Electromagnetic Compatibility (EMC) system design guidelines.

Table 4. $\overline{WE(0,1)}$ States during Access

WRITE Enable	Used during 16-bit Port Access
$\overline{WE0}$	WRITE Enable for DQ (0-7)
$\overline{WE1}$	WRITE Enable for DQ (8-15)

Table 5. Operating Modes

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE0}$	$\overline{WE1}$	DQ0–DQ7	DQ8–15
Deselect	V_{IH}	X(1)	X(1)	X(1)	Hi-Z	Hi-Z
Word WRITE	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Hi-Z	Hi-Z
Byte 0 WRITE	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Hi-Z	Hi-Z
Byte 1 WRITE	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Hi-Z	Hi-Z
Byte 0 WRITE, Byte 1 READ	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Hi-Z	Data
Byte 1 WRITE, Byte 0 READ	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Data	Hi-Z
Word READ	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data	Data

Note: 1. X = '1' or '0'

MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{SLD}(1,2)	Lead Solder Temperature for 10 seconds	260	°C
V_{IO}(3,4)	Input or Output Voltage	–0.3 to V_{CC} + 0.3	V
V_{CC}	Supply Voltage	–0.3 to 4.0	V
I_O(5)	Output Current	10	mA
P_D	Power Dissipation	270	mW

Note: 1. For standard (SnPb) lead finish: Reflow at peak temperature of 225°C (total thermal budget not to exceed 180°C for between 90 to 150 seconds).
2. For Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).
3. Up to a maximum operating V_{CC} of 3.6V only.
4. $V_{IL}(min) = V_{SS} – 2.0V$ AC (pulse width ≤ 10% $t_{AVAV}(min)$)
$V_{IH}(max) = V_{CC} + 2.0V$ AC (pulse width ≤ 10% $t_{AVAV}(min)$)
5. One output at a time, not to exceed 1 second duration.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. DC and AC Measurement Conditions

Parameter	M616Z08
V_{CC} Supply Voltage	2.34 to 3.0V or 3.0 to 3.6V
Ambient Operating Temperature	–40 to 125°C
Load Capacitance (C_L)	50pF
Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note: Output High Z is defined as the point where data is no longer driven.

Figure 8. AC Testing Load Circuit

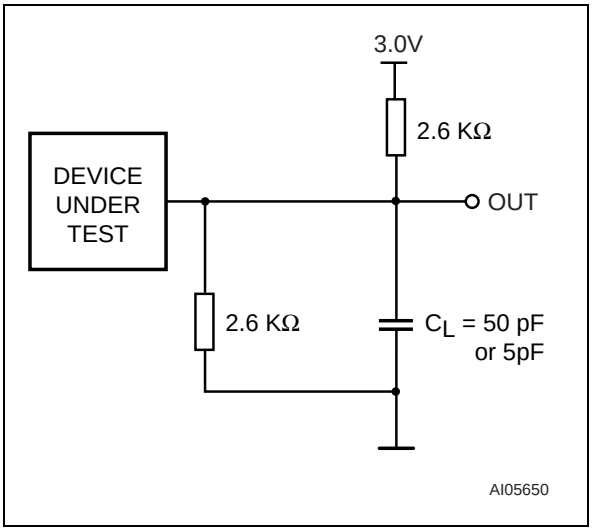


Table 8. Capacitance

Symbol	Parameter[1,2]	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)		10	pF
C_{OUT}[3]	Output Capacitance		10	pF

Note: 1. Effective capacitance measured with power supply at 3.3V; sampled only, not 100% tested.
2. At 25°C; f = 1MHz.
3. Outputs deselected.

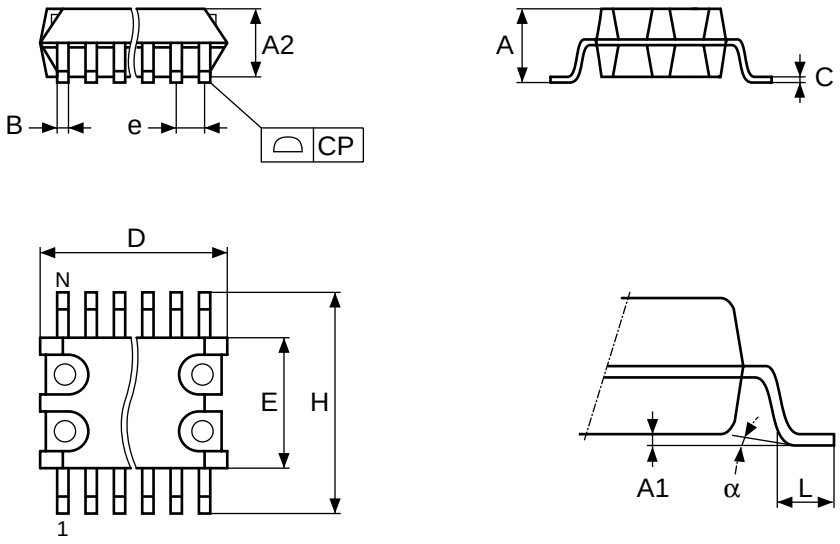
Table 9. DC Characteristics

Sym	Parameter	Test Condition(1)		Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le VIN \le V_{CC}$	TO Pin(2)		65	125	µA
			All other inputs			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$				±1	µA
I_{CC1}(3)	Supply Current	V_{CC} = 3.6V				75	mA
I_{CC3}(4)	Supply Current (Standby) CMOS	V_{CC} = 3.6V, $\overline{CE} \ge V_{CC} - 0.2V$, f = 0				1	mA
V_{IL}	Input Low Voltage			–0.3		$0.3V_{CC}$	V
V_{IH}	Input High Voltage			$0.7V_{CC}$		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1mA				0.2	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.34 to 3.0V	V_{CC}–0.2V			
			3.0 to 3.6V	V_{CC}–0.3V			V

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 125°C; V_{CC} = 3.0 to 3.6V or 2.34 to 3.0V (except where noted).
2. Input leakage on TO Pin due to internal pull-down to V_{SS}.
3. Average AC current, Outputs open, cycling at t_{AVAV} minimum.
4. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC}$ –0.2V.

PACKAGE MECHANICAL INFORMATION

Figure 9. SO44 – 44-Lead, Plastic, Hatless, Small Package Outline



SOH-C

Note: Drawing is not to scale.

Table 10. SO44 – 44-lead, Plastic, Hatless, Small Package Mechanical Data

Symb	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.46		0.014	0.018
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	0.81	–	–	0.032	–	–
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	44			44		
CP			0.10			0.004

PART NUMBERING

Table 11. Ordering Information Example

Example: M6 16Z08 –20 MH 3 F

Device Type

M6

Device Function

16Z08 = 128Kbit (8Kbit x16)

Speed

–20 = 20ns (3.0 to 3.6V)

Package

MH = 44-lead, Hatless SOIC

Temperature Range

3 = –40 to 125°C

Shipping Method

blank = Tubes (Not for New Design - Use E)

E = Lead-free Package (ECOPACK®), Tubes

F = Lead-free Package (ECOPACK®), Tape & Reel

TR = Tape & Reel (Not for New Design - Use F)

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

REVISION HISTORY

Table 12. Document Revision History

Date	Version	Revision Details
September 2001	1.0	First Issue
11/1901	2.0	Correction of Operating Modes text (Table 5); document status changed to “Data Sheet;” add text for Noise Immunity (page 10)
02/12/02	2.1	Add TO Pin (Figure 2, 3, Table 1); change WRITE Mode AC Characteristics (Table 3)
02/21/02	2.2	Changes for TO Pin (Table 9) and change characteristics (Table 2, 3)
05/13/02	2.3	Add reflow time and temperature footnote (Table 6)
07/22/02	2.4	Add “Hatless” to package description (Figure 1, 9 and Table 11, 10)
22-Mar-04	3.0	Reformatted; updated Lead-free information (Table 6, 11)