SONY

CXG1146EN

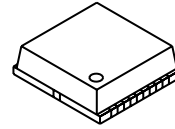## High Power SP3T Switch with Logic Control

Description

The CXG1146EN is a high power SP3T switch MMIC. This IC can be used in wireless communication systems, for example, W-CDMA handsets.

The CXG1146EN has on-chip logic for operation with 2 CMOS control inputs.

The Sony's J-FET process is used for low insertion loss and on-chip logic circuit.

10 pin VSON (Plastic)

Features

• Low insertion loss: 0.35dB @1.95GHz,
0.45dB @2.14GHz

• 2 CMOS compatible control line

• Small package size: 10-pin VSON

Applications

• Antenna switch for cellular handsets

• W-CDMA

Structure

GaAs J-FET MMIC
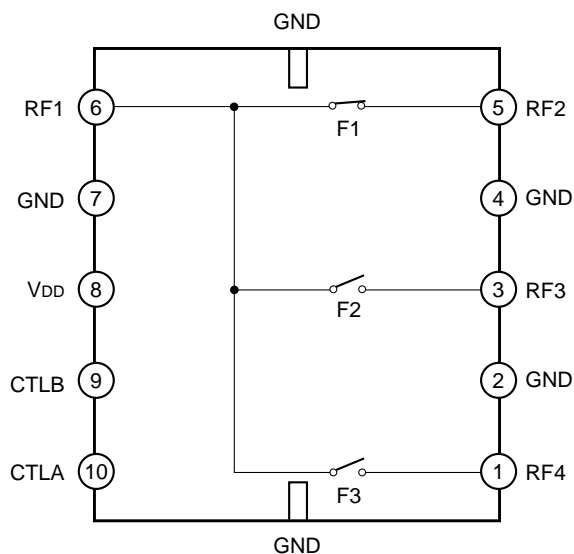
Absolute Maximum Ratings (Ta = 25°C)

• DC power supply voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operating temperature	Topr	−35 to +85	°C
• Storage temperature	Tstg	−65 to +150	°C

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

The actual ESD measurement data will be available later.

E02710-PS

Pin Configuration and Block Diagram

Pin Description

Pin No.	Symbol	Description
1	RF4	RF input/output. Connect capacitor (recommended value: 100pF) in use.
2	GND	GND
3	RF3	RF input/output. Connect capacitor (recommended value: 100pF) in use.
4	GND	GND
5	RF2	RF input/output. Connect capacitor (recommended value: 100pF) in use.
6	RF1	RF input/output. Connect capacitor (recommended value: 100pF) in use.
7	GND	GND
8	V_{DD}	DC power supply
9	CTLB	Logic control B
10	CTLA	Logic control A

Recommended Circuit
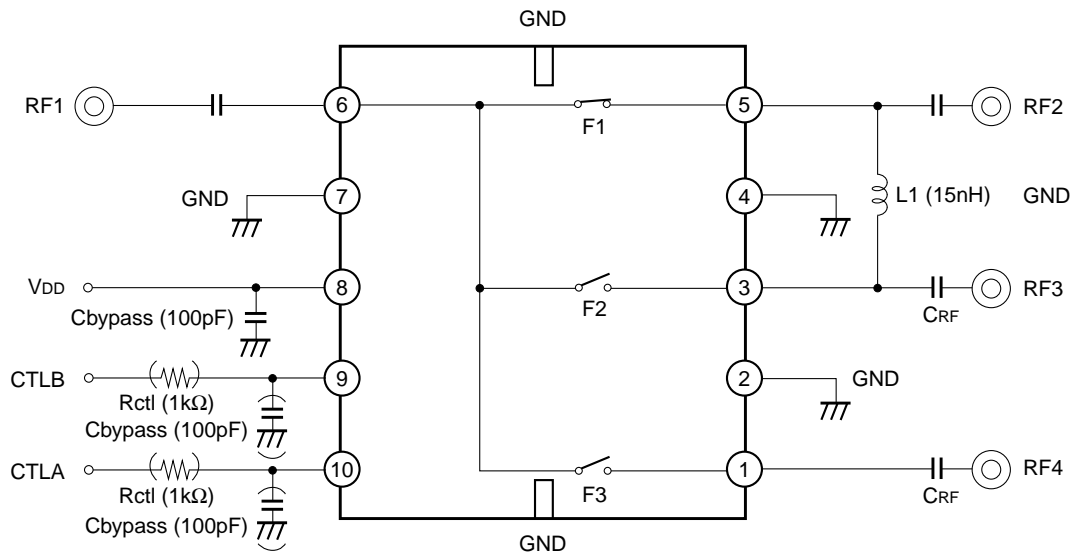
When using this IC, the following external components should be used:

Rctl: This resistor is used to improve ESD performance. 1kΩ is recommended.

C_{RF}: This capacitor is used for RF de-coupling and must be used for all applications.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

State	CTLA	CTLB	On state	F1	F2	F3
1	H	H	RF1 – RF2	ON	OFF	OFF
2	L	H	RF1 – RF3	OFF	ON	OFF
3	H/L	L	RF1 – RF4	OFF	OFF	ON

DC Bias Condition (Ta = 25°C)

| Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	3.0	3.6	V
Vctl (L)	0	—	0.4	V
V_{DD}	2.5	3.0	3.6	V

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Electrical Characteristics (Ta = 25°C)

Item	Symbol	State	Condition		Min.	Typ.	Max.	Unit
Insertion loss	IL	1	RF1 – RF2	1920MHz to 1980MHz[1]		0.35	0.55	dB
				2110MHz to 2170MHz[1]		0.45	0.65	dB
		2	RF1 – RF3	1920MHz to 1980MHz[1]		0.45	0.65	dB
				2110MHz to 2170MHz[1]		0.55	0.75	dB
		3	RF1 – RF4	1920MHz to 1980MHz[1]		0.90	1.10	dB
				2110MHz to 2170MHz[1]		1.00	1.20	dB
Isolation[1]	ISO.	2, 3	RF1 – RF2, 1920MHz to 2170MHz[1]		20	25		dB
		3, 1	RF1 – RF3, 1920MHz to 2170MHz[1]		20	30		dB
		1, 2	RF1 – RF4, 1920MHz to 2170MHz[1]		20	30		dB
VSWR	VSWR		50Ω			1.2	1.5	—
Switching speed	TSW		[1]			1	5	µs
ACLR	ACLR1	±5MHz	[2]			−60	−50	dBc
	ACLR2	±10MHz	[2]			−65	−55	dBc
Harmonics	2fo		[2]			−80	−55	dBc
	3fo		[2]			−80	−55	dBc
Bias current	IDD		VDD = 3.0V			0.25	0.42	mA
Control current	Ictl		Vctl (H) = 3V			30	70	µA

Condition

[1] Pin = 25dBm, 0/3V control, VDD = 3.0V

[2] Pin = 25dBm, 0/3V control, VDD = 3.0V, 1920MHz to 1980MHz, 50Ω

Note: Specification value is one on the IC terminal except for the specific description.

Package Outline   Unit: mm

10PIN VSON(PLASTIC)
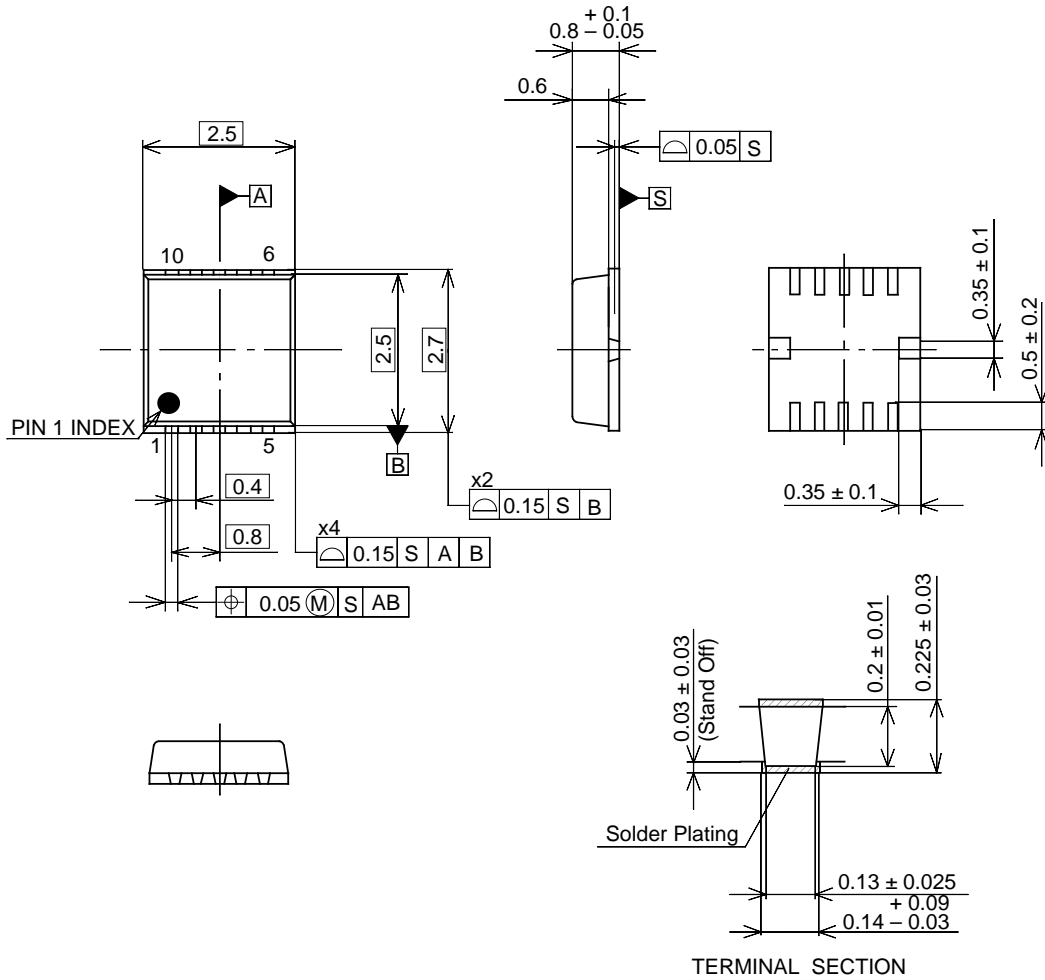
NOTE:1) The dimensions of the terminal section apply to the
ranges of 0.1mm and 0.25mm from the end of a terminal.

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

SONY CODE	VSON-10P-01
EIAJ CODE	———
JEDEC CODE	———

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm

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