PA7140 PEEL™ Array
Programmable Electrically Erasable Logic Array

Features

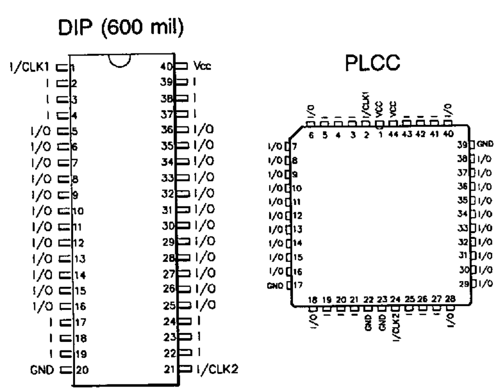
- **CMOS Electrically Erasable Technology**
  - Reprogrammable in 40-pin DIP and 44-pin PLCC packages
- **Versatile Logic Array Architecture**
  - 24 I/Os, 14 inputs, 60 registers/latches
  - Up to 72 logic cell output functions
  - PLA structure with true product-term sharing
  - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
  - Up to 3 output functions per logic cell
  - D,T and JK registers with special features
  - Independent or global clocks, resets, presets, clock polarity, and output enables
  - Sum-of-products logic for output enables
- **High-Speed Commercial and Industrial Versions**
  - As fast as 13ns/20ns (tpdi/tpd), 66.6MHz fmax
  - Industrial grade available for 4.5 to 5.5V Vcc and -40 to +85 °C temperatures
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
  - Integration of multiple PLDs and random logic
  - Buried counters, complex state-machines
  - Comparitors, decoders, other wide-gate functions
- **Development and Programmer Support**
  - ICT PLACE Development Software
  - Fitters for ABEL, CUPL and other software
  - Programming support by ICT PDS-3 and other popular 3rd party programmers

General Description

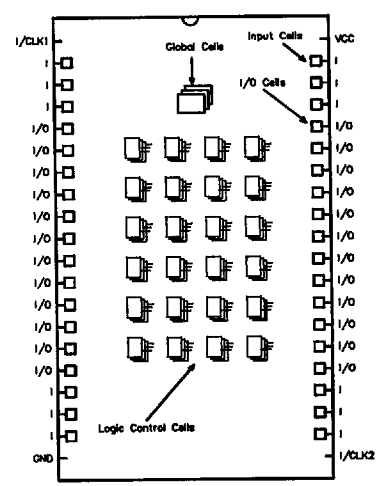
The PA7140 is a member of the Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's 1-micron CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7140 offers a versatile logic array architecture with 24 I/O pins, 14 input pins and 60 registers/latches (24 buried logic cells, 12 input reg/latches, 24 buried I/O reg/latches). Its logic array implements 100 sum-of-product logic functions divided into two groups each serving 12 logic cells. Each group shares half (60) of the 120 product-terms available for logic cells.

The PA7140's logic and I/O cells (LCCs, IOCs) are extremely flexible with up to three output functions per cell (a total of 72 for all 24 logic cells). Cells are configurable as D, T and JK registers with independent or global clocks, resets, presets, clock polarity, and other features, making the PA7140 suitable for a variety of combinatorial, synchronous, and asynchronous logic applications. The PA7140 supports speeds as fast as 13ns/20ns (tpdi/tpdx) and 66.6MHz (fmax) at moderate power consumption 100mA (80mA typical). Packaging includes 40-pin DIP and 44-pin PLCC. Development and programming support for the PA7140 is provided by ICT and popular third party development tool manufacturers.

Pin Configurations



Block Diagram



This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to Ground[1]	-0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T_A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T_R	Clock Rise Time	See Note 2		20	ns
T_F	Clock Fall Time	See Note 2		20	ns
T_{RVCC}	V_{CC} Rise Time	See Note 2		250	ms

D.C. Electrical Characteristics Over the operating range

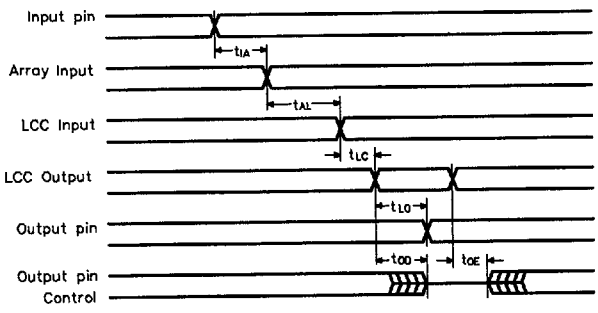
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage - CMOS	V_{CC} = Min, I_{OH} = -10µA		V_{CC} - 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage - CMOS	V_{CC} = Min, I_{OL} = 10µA			0.1	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			-0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current[4]	V_{CC} = 5V, V_O = 0.5V, T_A = 25°C		-30	-120	mA
I_{CC}	V_{CC} Current	V_{IN} = 0V or V_{CC}[3,11] f = 25MHz All outputs disabled	-20	80 (typ.)[19]	100	mA
			-25		100	
			I-25		110	
C_{IN}	Input Capacitance[5]	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT}	Output Capacitance[5]				12	pF

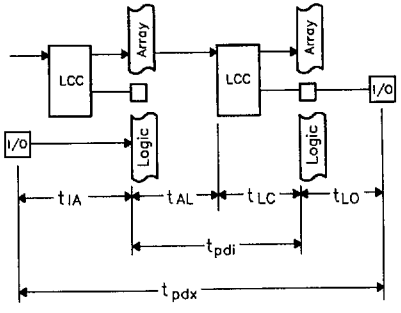
A.C. Electrical Characteristics Combinatorial

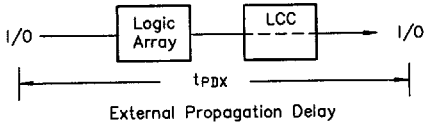
Over the Operating Range

Symbol	Parameter[6, 12]	-20[17]		-25 / I-25[17]		Unit
		Min	Max	Min	Max	
t_{PDI}	Propagation delay Internal (t_{AL} + t_{LC})		13		17	ns
t_{PDX}	Propagation delay External (t_{IA} + t_{AL} + t_{LC} + t_{LO})		20		25	ns
t_{IA}	Input or I/O pin to array input		2		2	ns
t_{AL}	Array input to LCC		12		16	ns
t_{LC}	LCC input to LCC output [10]		1		1	ns
t_{LO}	LCC output to output pin		5		6	ns
t_{OD}, t_{OE}	Output Disable, Enable from LCC output[7]		5		6	ns
t_{OX}	Output Disable, Enable from input pin[7]		20		25	ns

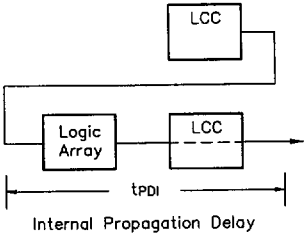
Combinatorial Timing - Waveforms and Block Diagram







External Propagation Delay



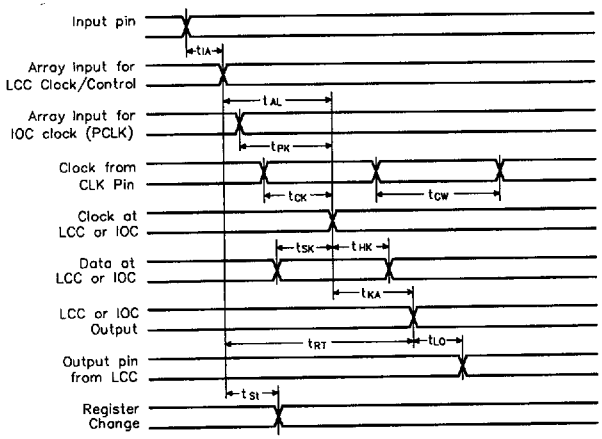
Internal Propagation Delay

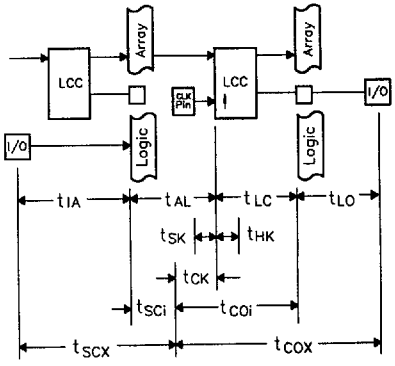
A.C. Electrical Characteristics Sequential

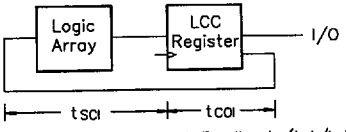
Over the Operating Range

Symbol	Parameter[6, 12]	-20[17]		-25 / I-25[17]		Unit
		Min	Max	Min	Max	
t_{SCI}	Internal set-up to system-clock[8] - LCC[14] ($t_{AL} + t_{SK} + t_{LC} - t_{CK}$)	8		11		ns
t_{SCX}	Input[16] (Ext.) set-up to system clock, -LCC ($t_{IA} + t_{SCI}$)	10		14		ns
t_{COI}	System-clock to Array Int. -LCC/IOC/INC[14] ($t_{CK} + t_{LC}$)		7		8	ns
t_{COX}	System-clock to Output Ext. - LCC ($t_{COI} + t_{LO}$)		12		14	ns
t_{HX}	Input hold time from system clock - LCC	0		0		ns
t_{SK}	LCC input set-up to async. clock [13] - LCC	1		1		ns
t_{AK}	Clock at LCC or IOC - LCC output	1		1		ns
t_{HK}	LCC input hold time from async. clock - LCC	4		4		ns
t_{SI}	Input set-up to system clock - IOC/INC[14] ($t_{SK} - t_{CK}$)	0		0		ns
t_{HI}	Input hold time from system clock - IOC/INC ($t_{CK} - t_{SK}$)	5		6		ns
t_{PK}	Array input to IOC PCLK clock		9		11	ns
t_{SPI}	Input set-up to PCLK clock[18]- IOC/INC (t_{SK}-t_{PK}-t_{IA})	0		0		ns
t_{HPI}	Input hold from PCLK clock[18] -IOC/INC (t_{PK}+t_{IA}-t_{SK})	10		12		ns
t_{SD}	Input set-up to system clock - IOC Sum-D[15] ($t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{CK}$)	10		13		ns
t_{HD}	Input hold time from system clock - IOC Sum-D	0		0		ns
t_{SDP}	Input set-up to PCLK clock ($t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{PK}$) - IOC Sum-D	7		9		ns
t_{HDP}	Input hold time from PCLK clock - IOC Sum-D	0		0		ns
t_{CK}	System-clock delay to LCC/IOC/INC		6		7	ns
t_{CW}	System-clock low or high pulse width	7		8		ns
f_{MAX1}	Max. system-clock frequency Int/Int 1/($t_{SCI} + t_{COI}$)		66.6		52.6	MHz
f_{MAX2}	Max. system-clock frequency Ext/Int 1/($t_{SCX} + t_{COI}$)		58.8		45.4	MHz
f_{MAX3}	Max. system-clock frequency Int/Ext 1/($t_{SCI} + t_{COX}$)		50.0		40.0	MHz
f_{MAX4}	Max. system-clock frequency Ext/Ext 1/($t_{SCX} + t_{COX}$)		45.4		35.7	MHz
f_{TGL}	Max. system-clock toggle frequency 1/($t_{CW} + t_{CW}$)[9]		71.4		62.5	MHz
t_{PR}	LCC preset/reset to LCC output		1		2	ns
t_{ST}	Input to Global Cell preset/reset ($t_{IA} + t_{AL} + t_{PR}$)		15		20	ns
t_{AW}	Asynch. preset/reset pulse width	8		8		ns
t_{RT}	Input to LCC Reg-Type (RT)		8		10	ns
t_{RTV}	LCC Reg-Type to LCC output register change		1		2	ns
t_{RTC}	Input to Global Cell register-type change ($t_{RT} + t_{RTV}$)		9		12	ns
t_{RW}	Asynch. Reg-Type pulse width	10		10		ns
t_{RESET}	Power-on reset time for registers in clear state[2]		5		5	µs

Sequential Timing - Waveforms and Block Diagram

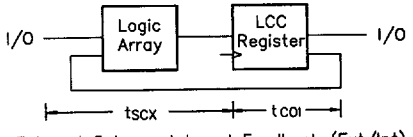






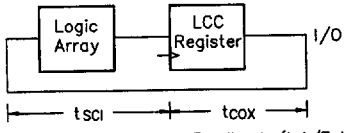
Internal Set-up, Internal Feedback (Int/Int)

$f_{MAX1} = 1/t_{SCI} + t_{COI}$



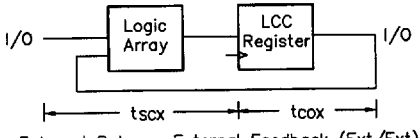
External Set-up, Internal Feedback (Ext/Int)

$f_{MAX2} = 1/t_{SCX} + t_{COI}$



Internal Set-up, External Feedback (Int/Ext)

$f_{MAX3} = 1/t_{SCI} + t_{COX}$



External Set-up, External Feedback (Ext/Ext)

$f_{MAX4} = 1/t_{SCX} + t_{COX}$

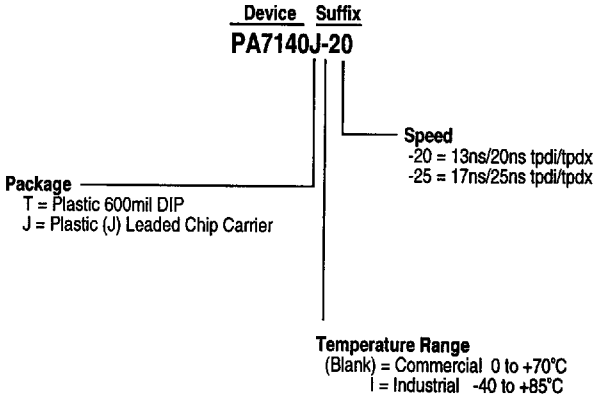
Notes:

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
3. I/O pins are 0V or V_{CC}.
4. Test one output at a time for a duration of less than 1 sec.
5. Capacitances are tested on a sample basis.
6. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
7. t_{OE} is measured from input transition to VREF ± 0.1V (See test loads at end of Section 6 for VREF value). t_{OD} is measured from input transition to VOH - 0.1V or VOL + 0.1V.
8. DIP: "System-clock" refers to pin 1/21 high speed clocks. PLCC: "System-clock" refers to pin 2/24 high speed clocks.
9. For T or JK registers in toggle (divide by 2) operation only.
10. For combinatorial and async-clock to LCC output delay.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D-type counter.
12. Test loads are specified in Section 6 of this Data Book.
13. "Async. clock" refers to the clock from the Sum term (OR gate).
14. The "LCC" term indicates that the timing parameter is applied to the LCC register. The "IOC" term indicates that the timing parameter is applied to the IOC register. The "LCC/IOC" term indicates that the timing parameter is applied to both the LCC and IOC registers. The "LCC/IOC/INC" term indicates that the timing parameter is applied to the LCC, IOC and INC registers.
15. This refers to the Sum-D gate routed to the IOC register for an additional buried register
16. The term "Input" without any reference to another term refers to an (external) input pin.
17. PA7140-1 is an alternate number for PA7140-20. PA7140-2 is an alternate number for PA7140-25.
18. The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (t_{SK} - t_{PK} - t_{IA}). This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
19. Typical (typ) ICC is measured at TA = 25°C, Freq = 25MHz, V_{CC} = 5V.

Ordering Information

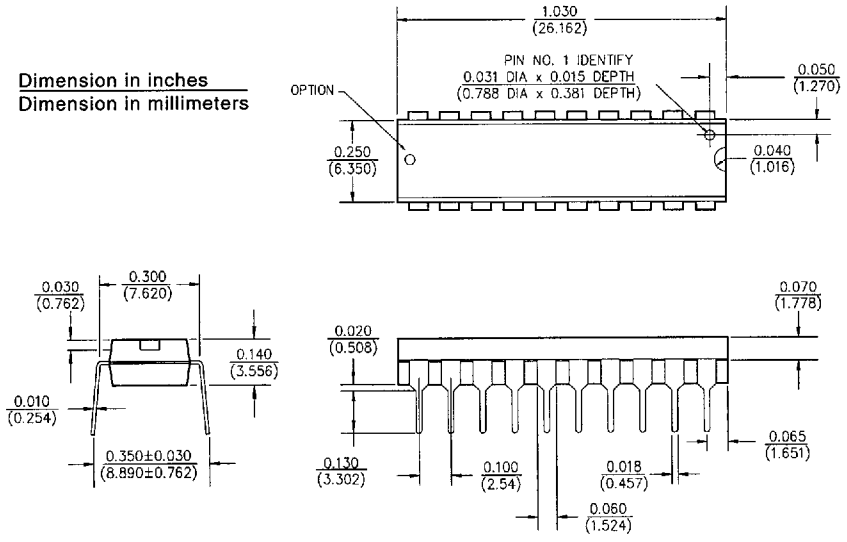
PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PA7140T-20	13/20ns	C	T40
PA7140J-20	13/20ns	C	J44
PA7140T-25	17/25ns	C	T40
PA7140TI-25	17/25ns	I	T40
PA7140J-25	17/25ns	C	J44
PA7140JI-25	17/25ns	I	J44

Part Number

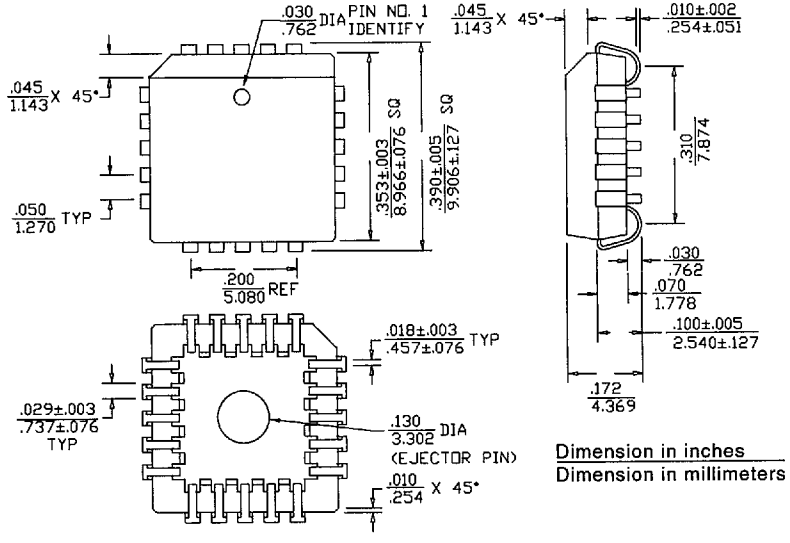


Package Diagrams (Drawings are not necessarily to scale.)

Dimension in inches
Dimension in millimeters

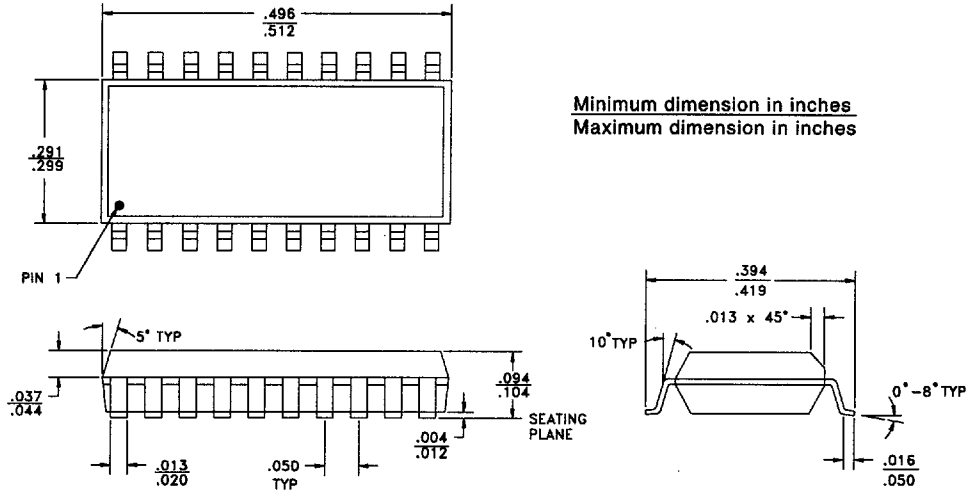


20-Pin Plastic DIP (P20)

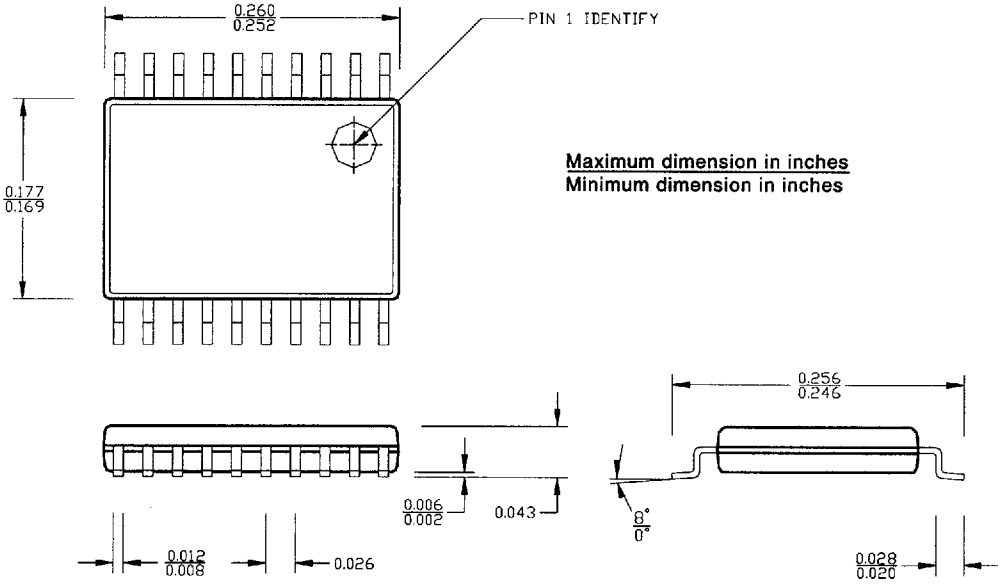


Dimension in inches
Dimension in millimeters

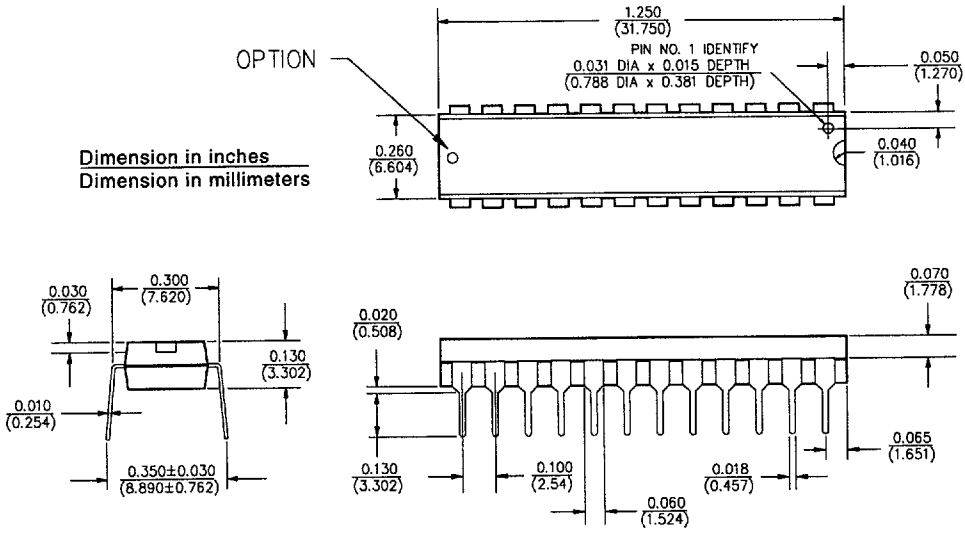
20-Pin PLCC (J20)



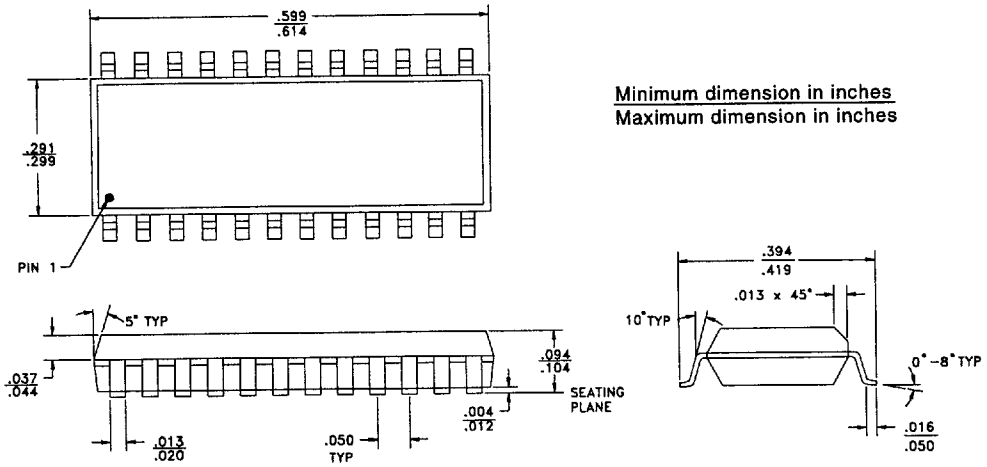
20-Pin SOIC (S20)



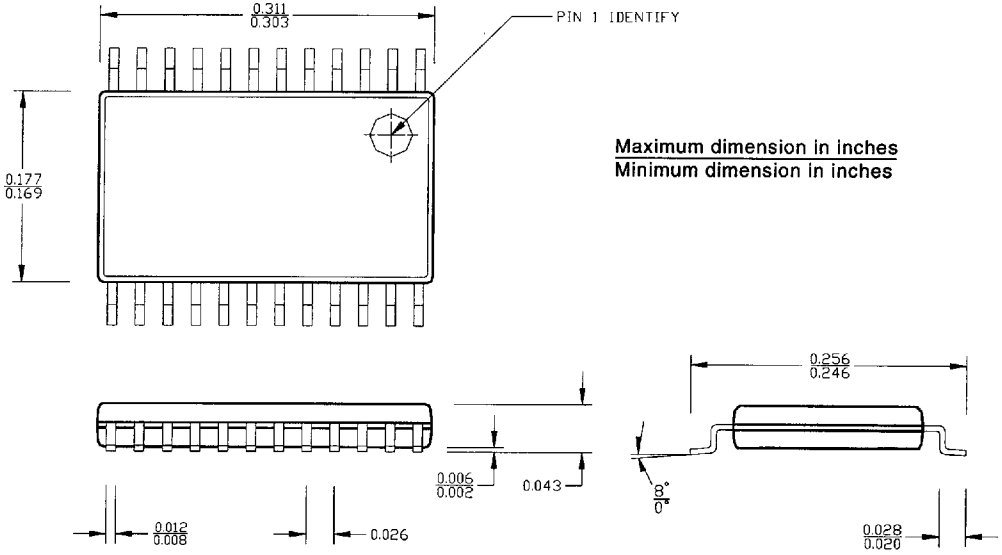
20-Pin TSSOP (T20)



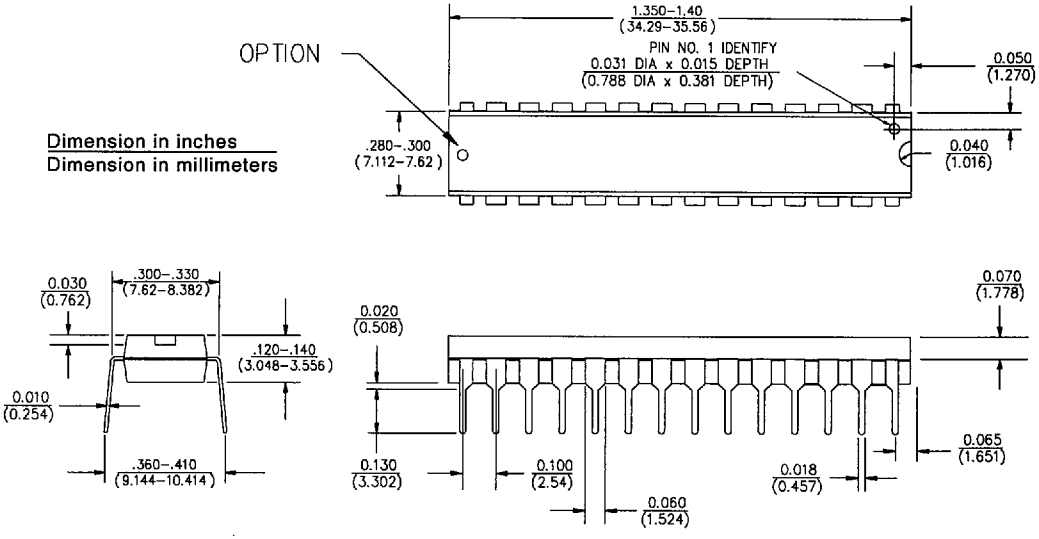
24-Pin Plastic DIP (P24)



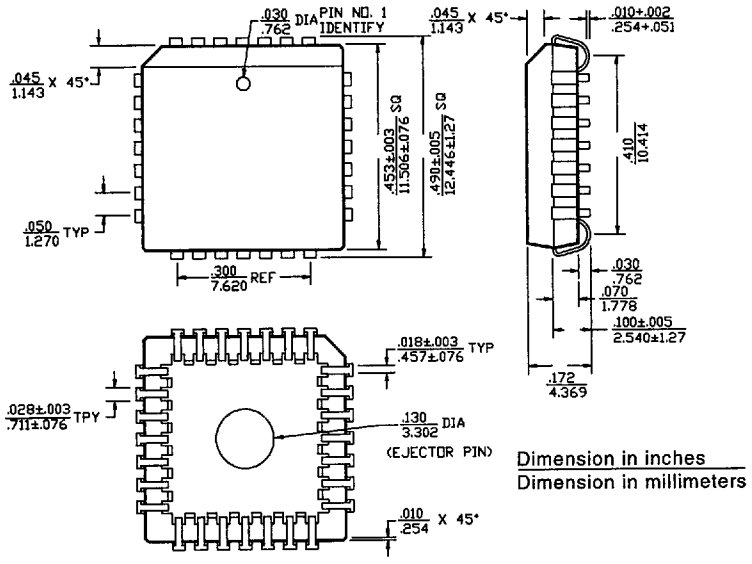
24-Pin SOIC (S24)



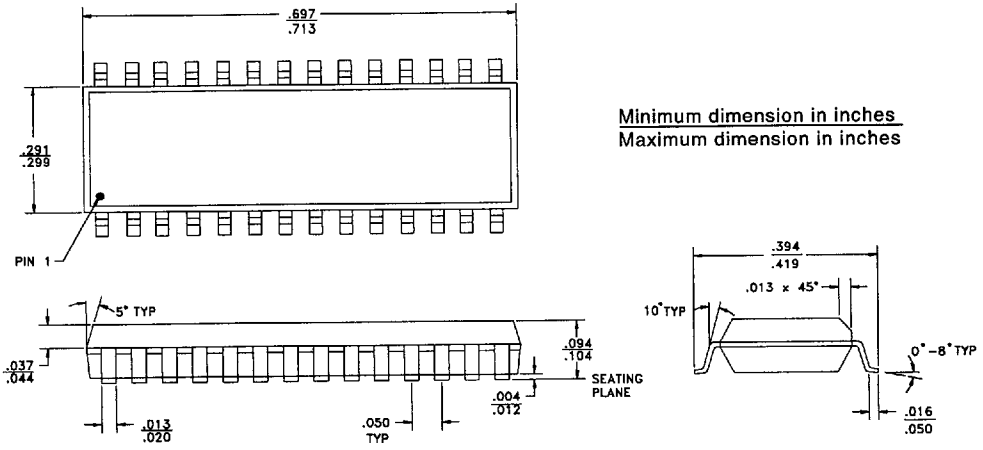
24-Pin TSSOP (T24)



28-Pin Plastic Dip (P28)

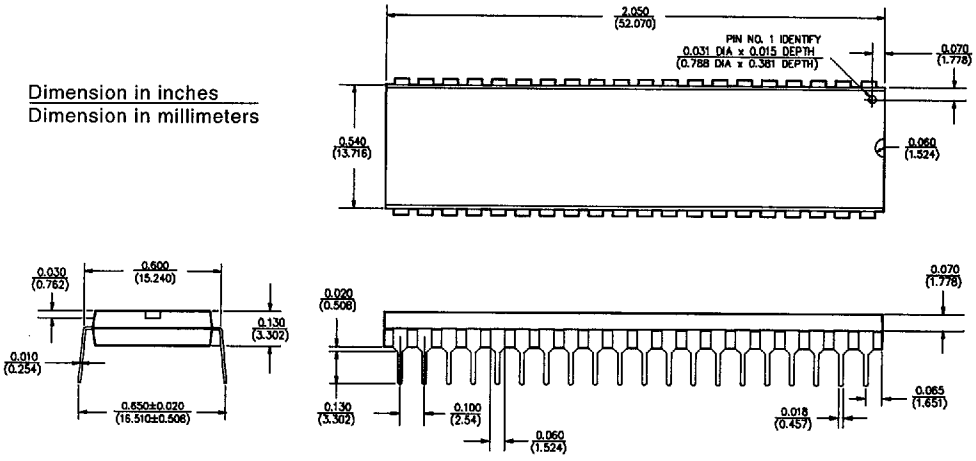


28-Pin PLCC (J28)

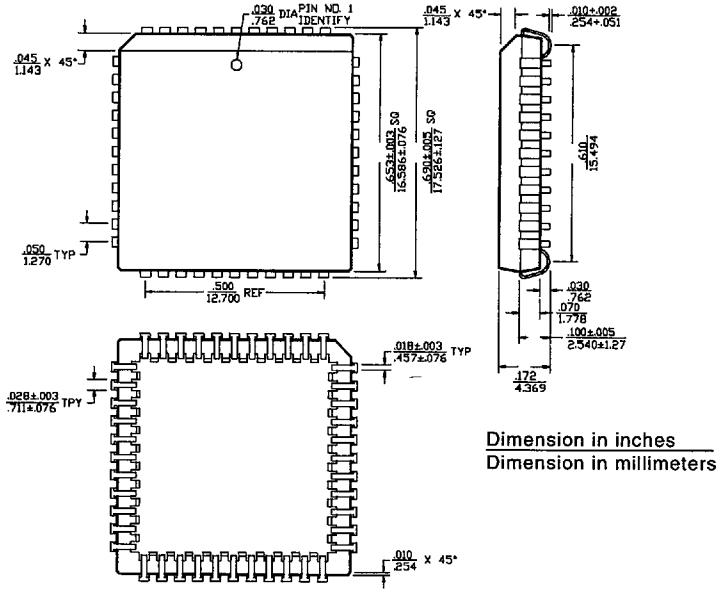


28-Pin SOIC (S28)

Dimension in inches
Dimension in millimeters



40-Pin Plastic DIP (T40)



Dimension in inches
Dimension in millimeters

44-Pin PLCC (J44)