High Speed, Current Feedback Operational Amplifier

OP-160

1.1 Scope.

This specification covers the detail requirement for a high speed, current feedback operational amplifier.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace specification control drawings.

1.2 Part Number.

The complete part numbers per Table 1 of this specification is as follows:

Device	Part Number	Package
−1	OP-160AZ/883	Z
−1	OP-160ARC/883	RC

1.2.3 Case Outline.

Letter	Case Outline (Lead Finish Per MIL-M-38510)
Z	8-Lead Ceramic Dual-in-Line Package (Cerdip)
RC	20-Contact Leadless Chip Carrier (LCC)

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage ..... ±18 V
Input Voltage ..... Supply Voltage
Differential Input Voltage ..... ±1 V
Inverting Input Current ..... ±7 mA Continuous ±20 mA Peak
Output Short-Circuit Duration ..... 10 Seconds
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$
Operating Temperature Range ..... $-55°C \leq T_A \leq +125°C$
Lead Temperature Range (Soldering 60 sec) ..... +300°C
Maximum Junction Temperature (T_J) ..... +175°C

1.5 Thermal Characteristics.

Thermal Resistance, Cerdip (Z) Package:
Junction-to-Case (θ_{JC}) = 16°C/W max
Junction-to-Ambient (θ_{JA}) = 148°C/W max

Thermal Resistance, LCC (RC) Package:
Junction-to-Case (θ_{JC}) = 38°C/W max
Junction-to-Ambient (θ_{JA}) = 98°C/W max

OP-160—SPECIFICATIONS

Table 1.

Test	Symbol	Device Types	Limits Min	Limits Max	Group A Subgroups	Test Condition[1]	Units
Input Offset Voltage[2]	V_{OS}	−1		±5	1	T_A = +25°C	mV
				±8	2, 3	T_A = −55°C, +125°C	
Noninverting Input Bias Current	I_{B+}	−1		±1	1	T_A = +25°C	μA
				±2	2, 3	T_A = −55°C, +125°C	
Inverting Input Bias Current	I_{B-}	−1		±20	1	T_A = +25°C	μA
				±30	2, 3	T_A = −55°C, +125°C	
Noninverting Input Bias Current Common-Mode Rejection Ratio	$CMRRI_{B+}$	−1		75	1	V_{CM} = ±11 V, T_A = +25°C	nA/V
				150	2, 3	V_{CM} = ±10 V; T_A = −55°C, +125°C	
Inverting Input Bias Current Common-Mode Rejection Ratio	$CMRRI_{B-}$	−1		75	1	V_{CM} = ±11 V, T_A = +25°C	nA/V
				150	2, 3	V_{CM} = ±10 V; T_A = −55°C, +125°C	
Noninverting Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B+}$	−1		5	1	V_S = ±9 V, ±18 V; T_A = +25°C	nA/V
				10	2, 3	V_S = ±9 V, ±18 V; T_A = −55°C, +125°C	
Inverting Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$	−1		50	1	V_S = ±9 V, ±18 V; T_A = +25°C	nA/V
				100	2, 3	V_S = ±9 V, ±18 V; T_A = −55°C, +125°C	
Common-Mode Rejection	CMR	−1	60		1	V_{CM} = ±11 V, T_A = +25°C	dB
			56		2, 3	V_{CM} = ±10 V; T_A = −55°C, +125°C	
Power Supply Rejection	PSR	−1	74		1	V_S = ±9 V, ±18 V; T_A = +25°C	dB
			70		2, 3	V_S = ±9 V, ±18 V; T_A = −55°C, +125°C	
Input Voltage Range[3]	IVR	−1	±11		1	T_A = +25°C	V
			±10		2, 3	T_A = −55°C, +125°C	
Output Voltage Swing	V_O	−1	±11		4	R_L = 500 Ω, T_A = +25°C	V
			±10		5, 6	R_L = 500 Ω; T_A = −55°C, +125°C	
Output Current	I_O	−1	±35		4	V_O = ±10 V, T_A = +25°C	mA
Transimpedance	R_T	−1	3		4	V_O = ±10 V; R_L = 500 Ω; T_A = +25°C	MΩ
			1.75		5, 6	V_O = ±10 V; R_L = 500 Ω; V_O = ±10 V; T_A = −55°C, +125°C	
Slew Rate	SR	−1	1000		7	A_V = +2, R_L = 500 Ω; T_A = +25°C V_O = ±10 V, Test at V_O = ±5 V	V/μs
Supply Current	I_{SY}	−1		8	1	No Load, T_A = +25°C	mA
				9	2, 3	No Load; T_A = −55°C, +125°C	

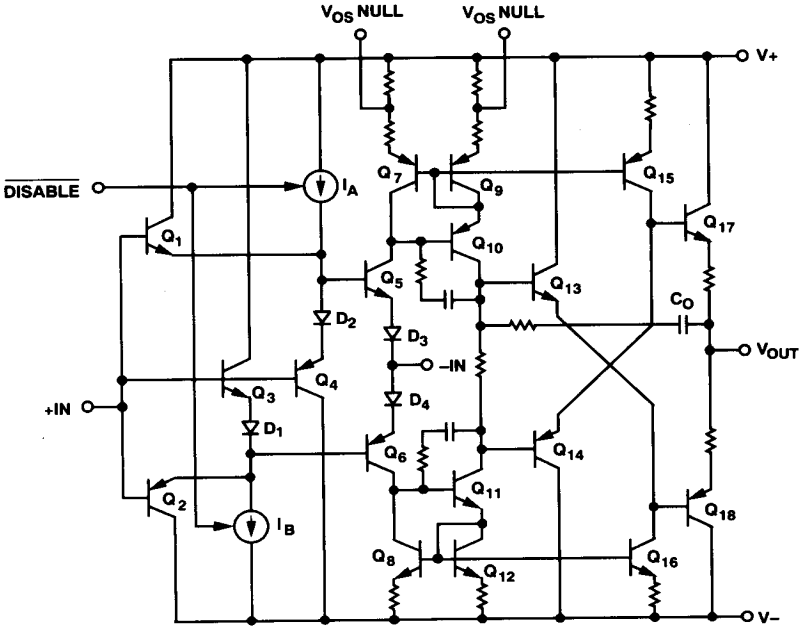
NOTES
[1]V_S = ±15 V, V_{CM} = 0 V, R_F = 820 Ω; unless otherwise specified.
[2]The input offset voltage (V_{OS}) and inverting bias current can be adjusted with an external 10 kΩ potentiometer between the NULL pins with wiper connected to V+ to make output offset voltage zero.
[3]Input voltage range (IVR) guaranteed by common-mode rejection (CMR) test.

Table 2. Electrical Test Requirements

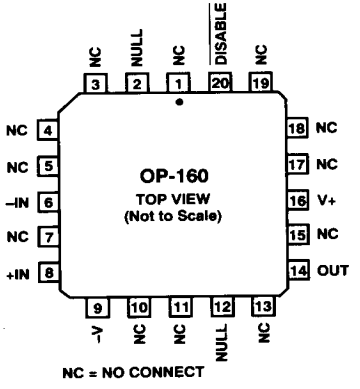
MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1,* 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

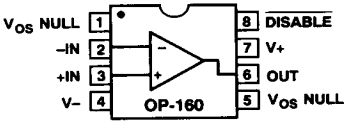
3.2.1 Functional Block Diagram and Terminal Assignments.



20-Position LCC (RC Suffix)



8-Pin Ceramic DIP (Z Suffix)



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in performed per MIL-STD-883 Method 1015 test condition (C).