PRELIMINARY

Spatializer® N-2-2™ Digital Audio Processor with BBE®

BBE SPATIALIZER® N-2-2™ VIRTUAL DOLBY SURROUND DOLBY SURROUND PRO • LOGIC

Description

The NJU25019 is a digital 3D surround sound processor which decodes surround information from a stereo audio source and produces a 3D sonic image from two speakers. This application specific 24-bit DSP can operate in both Dolby® Pro Logic™ and Virtual Dolby Surround (3D) mode. Based on Spatializer® Audio Laboratories Head Related Transfer Functions (HRTFs), N-2-2™ technology allows the listener to experience realistic 3D sound while just two front speakers are playing. Spatializer N-2-2 has the unique ability of creating a wide sweet spot of 3D sound that is well suited for near field applications such as desktop multimedia computers or for far field applications such as TV's, home theater and stereo music.

Digitally adjustable BBE® High Definition Sound processing is also incorporated in the NJU25019 which can be enabled on the output during any operating mode. BBE has the unique ability to dramatically improve the sound reproduced from loudspeakers by actively compensating for the increasing impedance inherent in loudspeakers as frequency increases. The BBE transfer function combines high and low frequency boost with phase correction, the combination of which greatly improves the transient response and clarity of loudspeakers.

The NJU25019 is also includes other system-level features not found in competing ICs: a full Dolby Pro Logic decoder, digital speaker crossover filters, and bass management. Home theater TVs, self-powered multimedia speakers for computers, and stereo systems can all benefit from the features and performance found in the NJU25019

Features

- Spatializer® N-2-2™ 3D Surround Sound Processing
  - 360° surround from two speakers
  - Wide and accurate 3D listening area
- BBE® High Definition Sound Enhancement
  - Programmable Lo Contour and Process levels
  - Digital adjustment 0 to +15 dB in 1 dB increments
- Dolby Pro Logic Decoder With Optional Subwoofer Output
  - 5.0 or 5.1ch output (L,R,SL,SR,C,SW)
  - On-chip digital delay, 30ms max.
- Dolby 3 Stereo Mode With Optional Subwoofer Output
- System Level Audio Management
  - Bass management
  - Subwoofer filter
  - Front high pass filters
  - Default or custom cutoff frequencies
  - Master Volume Control
  - Clipping Indicator
- A Complete DSP-based 3D Audio Solution
  - Includes on-chip surround time delay memory

Figure 1 NJU25019 Block Diagram

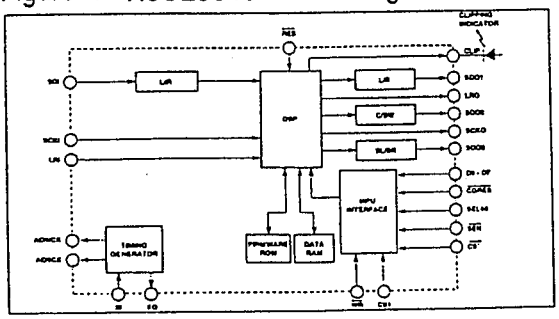


Figure 2 N-2-2 Virtual Surr ound Sound

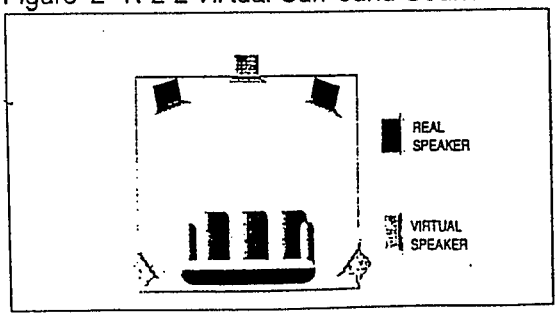


Figure 3 NJU25019 Pin Confi guration

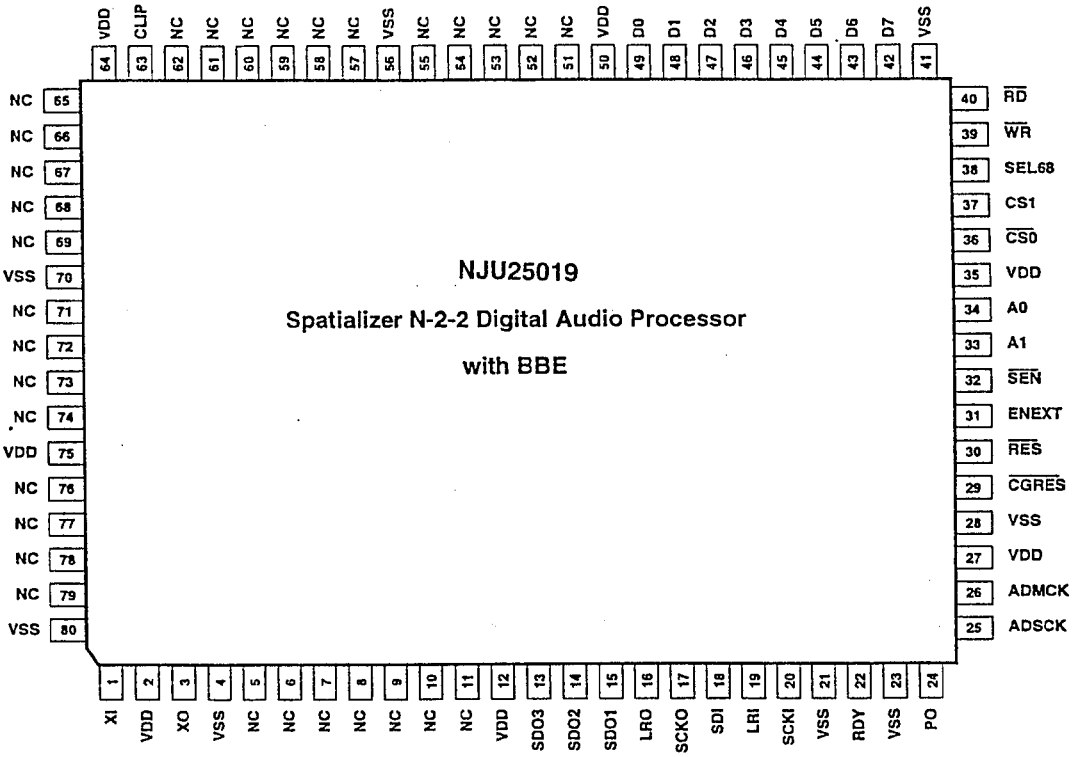


Figure 4 NJU25019 Functional Bloc k Diagram

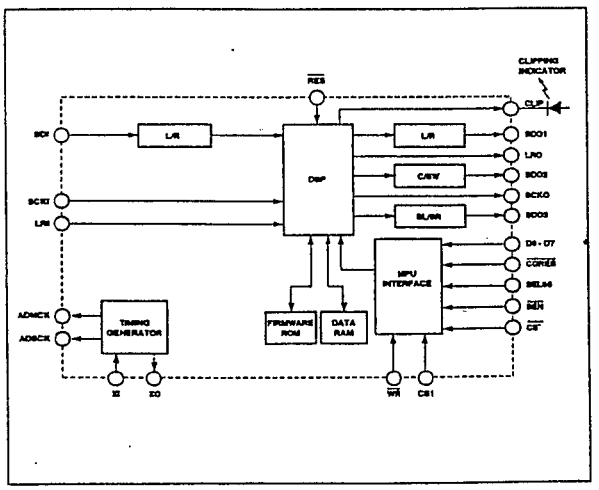
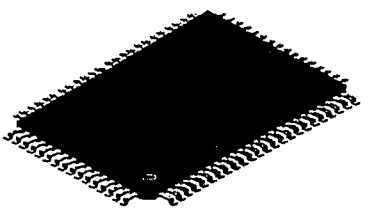


Figure 5 PQFP-80 Package



Plastic QFP-80

Table 1 Pin Description

No.	Symbol	I/O	Function	No.	Symbol	I/O	Function
1	XI	I	Crystal/External clock input	41	VSS	I	Ground
2	VDD	I	Power supply terminal: +5V	42	D7	I	MPU data, parallel input (MSB)
3	XO	O	Crystal	43	D6	I	MPU data, parallel input
4	VSS	I	Ground	44	D5	I	MPU data, parallel input
5	NC		No connect	45	D4	I	MPU data, parallel input
6	NC		No connect	46	D3	I	MPU data, parallel input
7	NC		No connect	47	D2	I	MPU data, parallel input
8	NC		No connect	48	D1		MPU data, parallel input
9	NC		No connect	49	D0	I	MPU data, parallel input (LSB), serial data input ($\overline{SEN}$ = 0)
10	NC		No connect	50	VDD	I	Power supply terminal: +5V
11	NC		No connect	51	NC		No connect
12	VDD	I	Power supply terminal: +5V	52	NC		No connect
13	SDO3	O	Digital audio serial data out, crossover output	53	NC		No connect
14	SDO2	O	Digital studio serial data out, PEQ output	54	NC		No connect
15	SDO1	O	Digital audio serial data out, full output	55	NC		No connect
16	LRO	O	Output left/right frame clock	56	VSS	I	Ground
17	SCKO	O	Output digital audio serial clock	57	NC		No connect
18	SDI	I	Input digital audio serial data	58	NC		No connect
19	LRI	I/O	Input left/right frame clock	59	NC		No connect
20	SCKI	I/O	Input digital audio serial clock	60	NC		No connect
21	VSS	I	Ground	61	NC		No connect
22	RDY	I	Test pin, high for normal operation	62	NC		No connect
23	VSS	I	Ground	63	CLIP	O	Clipping Indicator
24	PO	O	Test pin	64	VDD	I	Power supply terminal: +5V
25	ADSCK	O	32Fs/64Fs serial clock for A/D, D/A converters (default 32Fs)	65	NC		No connect
26	ADMCK	O	384Fs/256Fs master clock for A/D, D/A converters (default 384Fs)	66	NC		No connect
27	VDD	I	Power supply terminal: +5V	67	NC		No connect
28	VSS	I	Ground	68	NC		No connect
29	$\overline{CGRES}$	I	Test pin, normally high	69	NC		No connect
30	$\overline{RES}$	I	Reset, must be held low for at least two clock cycles after power on	70	VSS	I	Ground
31	$\overline{ENEXT}$	I	Test pin, normally low	71	NC		No connect
32	$\overline{SEN}$	I	MPU serial interface enable. Serial = L, parallel = H	72	NC		No connect
33	A1	I	Test pin. Low for normal operation	73	NC		No connect
34	A0	I	Test pin. Low for normal operation	74	NC		No connect
35	VDD	I	Power supply terminal: +5V	75	VDD	I	Power supply terminal: +5V
36	$\overline{CS0}$	I	Chip select, MPU interface enabled when $\overline{CS0}$ = 0 and CS1 = 1	76	NC		No connect
37	CS1	I	Chip select, MPU interface enabled when $\overline{CS0}$ = 0 and CS1 = 1	77	NC		No connect
38	SEL68	I	MPU interface mode: 68K = H, Z80 = L	78	NC		No connect
39	$\overline{WR}$	I	Write Strobe (Z80), Write Enable (68K)	79	NC		No connect
40	$\overline{RD}$	I	Write Strobe (68K)	80	VSS	I	Ground

Specifications

Table 2 Absolute Maximum Ratings [1] (V_{SS} = 0 V)

Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage (T_A = 25°C)	V_{DD}	-0.3	7	V
Input, Output Pin Voltage (T_A= 25°C)	V_x	-0.3	V_{DD} + 0.3	V
Operating Temperature	T_{OPR}	-25	85	°C
Storage Temperature	T_{STG}	-55	150	°C

1. Absolute maximum ratings are stress ratings only, and functional operation beyond these limits is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

Table 3 Electrical Characteristics (T_A = -20°C to +70°C)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Unit
Operating Voltage	V_{DD}	V_{DD} pins	4.75		5.25	V
Operating Current	I_{DD}	f_{osc} = 34 MHz	-	90	125	mA
High Level Input Voltage	V_{IH}		0.80 V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}		V_{SS}		0.10 V_{DD}	V
High Level Input Current	I_{IH}	V_{IN} = V_{DD}	-		10	µA
Low Level Input Current	I_{IL}	V_{IN} = V_{SS}	-		10	µA
High Level Output Voltage	V_{OH}	I_{OH} = 2 mA	V_{DD} - 1.0		-	V
Low Level Output Voltage	V_{OL}	I_{OH} = 2 mA	-		0.5	V
Input Capacitance	C_{IN}		-	10	20	pF
Clock Frequency[1]	f_{OSC}		20		34	MHz
Ext. System Clock Duty Cycle	r_{EC}		45		55	%

1. For operation with 37 MHz clock frequency, contact factory.

Timing Parameters and Timing Diagrams

Table 4 Serial Data Input Timing P arameter s (V_{DD} = 5V ± 5%, T_A = -20℃ to +70℃, f_{CLK} = 34MHz)

Parameter	Symbol	Minimum	Maximum	Unit
SCKI Period		160	-	ns
L Pulse Width	t_{SIL}	80	-	ns
H Pulse Width	t_{SIH}	80	-	ns
SCKI to LRI Time	t_{SLI}	50	-	ns
LRI to SCKI Time	t_{LSI}	75	-	ns
Data Setup Time	t_{DS}	10	-	ns
Data Hold Time	t_{DH}	10	-	ns

Figure 6 Serial Data Input Timing

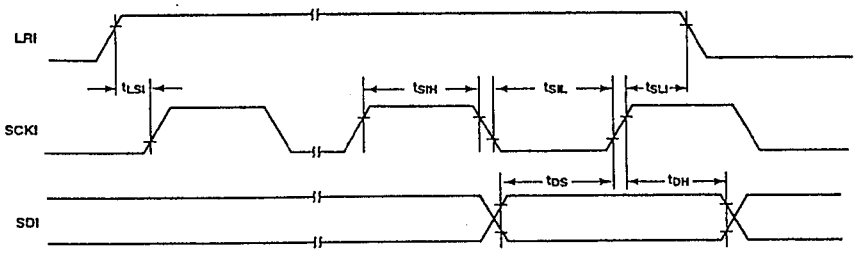


Table 5 Serial Data Output Timing P arameter s
(V_{DD} = 5V ± 5%, T_A = -20℃ to +70℃, f_{CLK} = 34MHz, CL: LRO, SCKO, SDO = 5 pF)

Parameter	Symbol	Minimum	Maximum	Unit
SCKO Period		160	-	ns
L Pulse Width	t_{SOL}	80	-	ns
H Pulse Width	t_{SOH}	80	-	ns
SCKO to LRO Time	t_{SLO}	-	5	ns
Data Output Delay	t_{DOD}	-	5	ns

Figure 7 Serial Data Output Timing

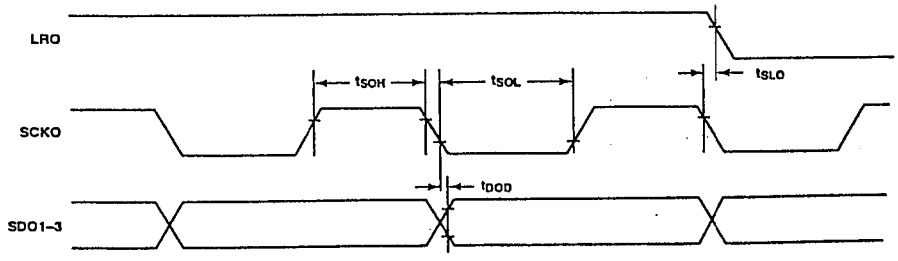


Table 6 Z80 Interface Timing P arameter s (V_{DD} = 5V ± 5%, T_A = -20°C to +70°C, f_{CLK} = 34MHz)

Parameter	Symbol	Minimum	Maximum	Unit
Address Setup Time	t_{AS8}	100	-	ns
Address Hold Time	t_{AH8}	100	-	ns
System Cycle Time	t_{CYC8}	1,000	-	ns
Read/Write Pulse Width	t_{CC8}	100	-	ns
Write Data Setup Time	t_{DS8}	10	-	ns
Write Data Hold Time	t_{DH8}	10	-	ns

Figure 8 Z80 Parallel Interface Timing (SEL68 Lo w)

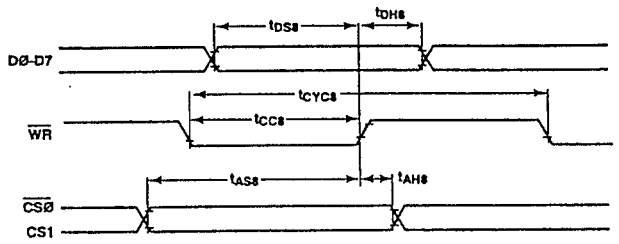


Figure 9 Z80 Serial Interface Timing (SEL68 Lo w)

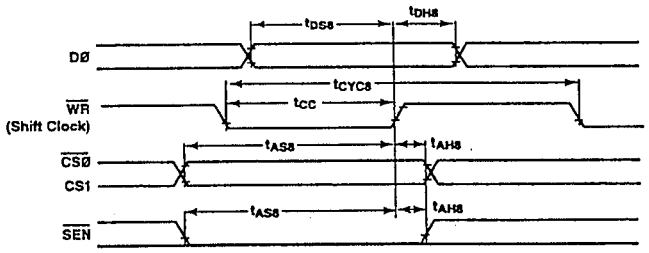


Table 7 68K Interface Timing P arameter s (V_{DD} = 5V ± 5%, T_A = -20°C to +70°C, f_{CLK} = 34MHz)

Parameter	Symbol	Minimum	Maximum	Unit
Address Setup Time	t_{AS6}	100	-	ns
Address Hold Time	t_{AH6}	100	-	ns
System Cycle Time	t_{CYC6}	1,000	-	ns
Read/Write Pulse Width	t_{CC6}	100	-	ns
Write Data Setup Time	t_{DS6}	10	-	ns
Write Data Hold Time	t_{DH6}	10	-	ns
Write-to-read Strobe Setup	t_{WRS}	100	-	ns
Read-to-write Strobe Setup	t_{WRH}	100	-	ns

Figure 10 68K Parallel Interface Timing (SEL68 High)

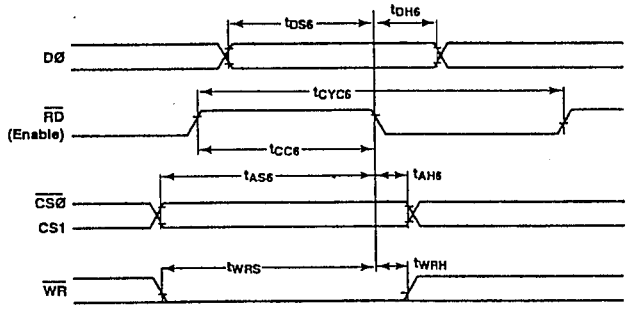
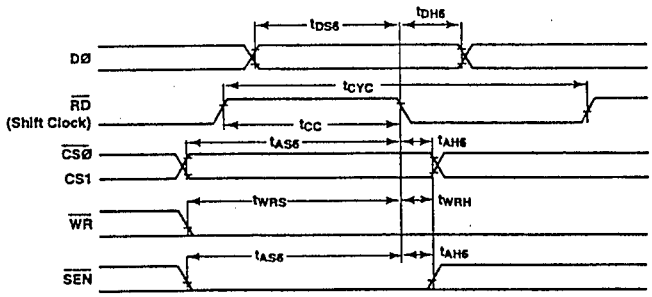


Figure 11 68K Serial Interface Timing (SEL68 High)



Functional Timing Diagrams

Figure 12 Left-Justified Data Format, ADSCK = 64 Fs, 18-bit Data

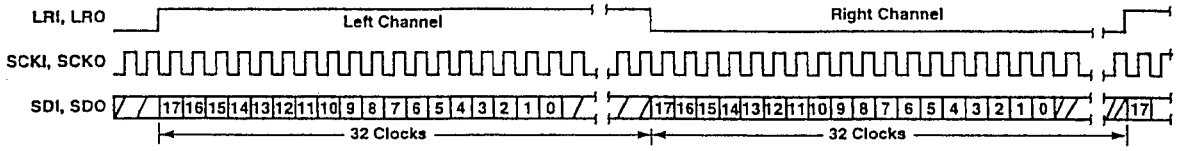


Figure 13 Right-Justified Data Format, ADSCK = 64 Fs, 18-bit Data

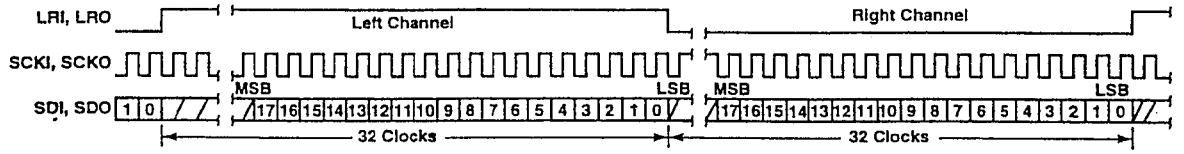


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Figure 14 I²S Data Format, ADSCK = 64 Fs, 18-bit Data

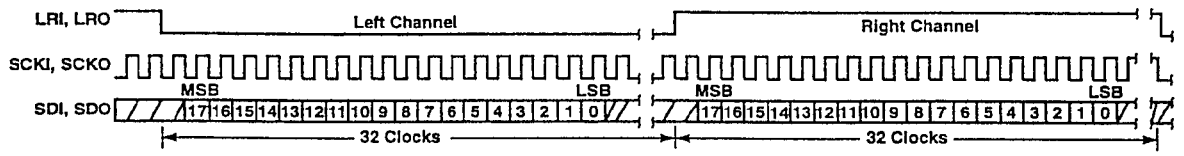


Figure 15 Right- and Left-Justified Data Formats, ADSCK = 32 Fs, 16-bit Data

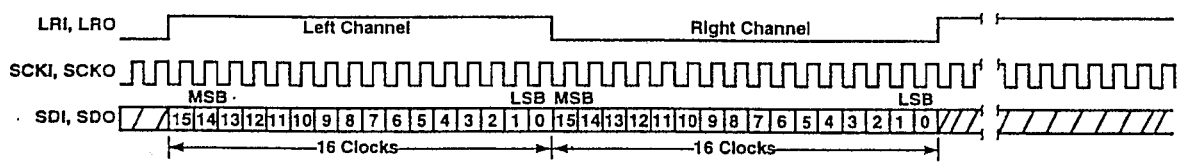
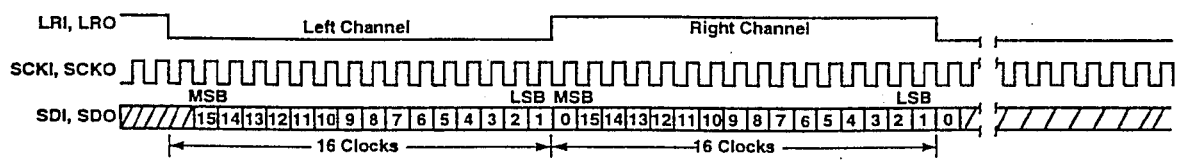


Figure 16 I²S Data Formats, ADSCK = 32 Fs, 16-bit Data



Functional Description

Spatializer N-2-2 Mode

Surround information from the audio source is extracted by the Dolby Pro Logic decoder processing in the NJU25019. Head Related Transfer Functions (HRTFs), based on the natural characteristics of the human hearing system, are used on both front and rear surround channels to synthesize virtual surround speakers to the side and rear of the listener. The Front HRTFs have frequency tailoring of the difference signals (L-R) to extend the sound image past the physical boundaries of the actual speakers. A different set of frequency coefficients are applied to the rear HRTFs that have much greater peak and valley differences. These coefficients are chosen so that the rear channels will virtualize behind the listener. The virtualized surround is then mixed into the left and right output. The center channel is also mixed into the left and right output. There is also a subwoofer output with low pass crossover filter that is active in all modes.

The NJU25019 initializes in N-2-2 mode with I^2S audio data format for use with a codec (A/D+D/A) and does not require a microprocessor for 2channel 3D surround sound operation.

Figure 17 Spatializ er N-2-2 Processing

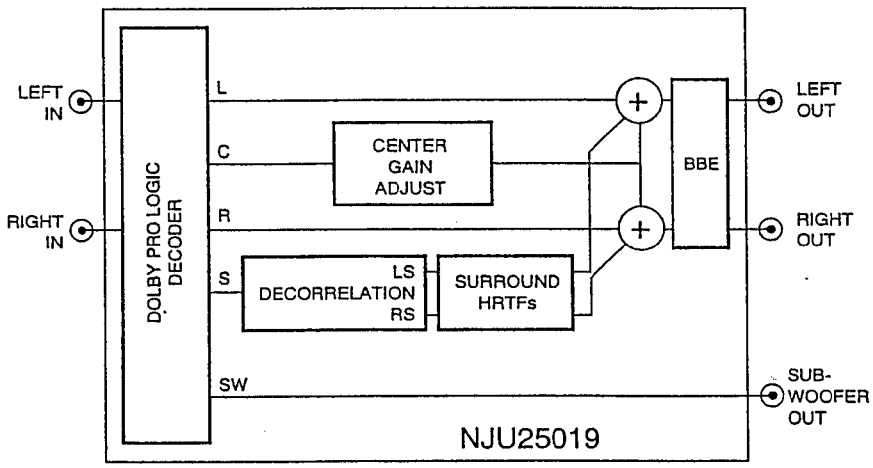


Figure 18 N-2-2 Listening Area

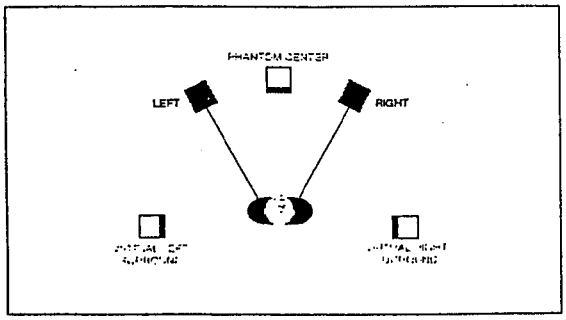
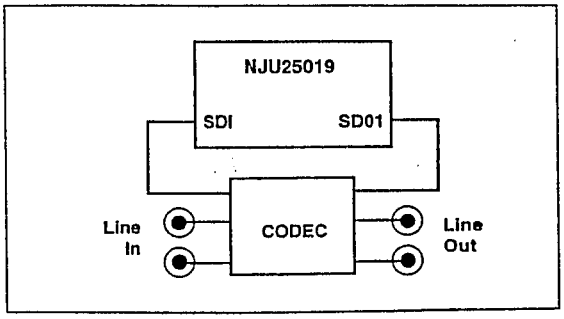


Figure 19 2-Channel Surr ound System

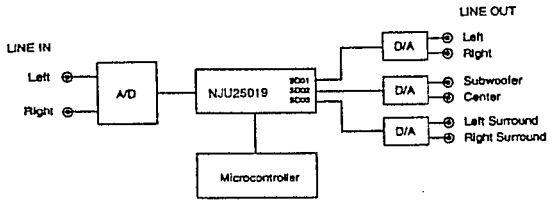


Dolby Pro Logic Mode

The NJU25019 can be switched from N-2-2 mode (2ch + optional subwoofer) to Dolby Pro Logic mode (5ch + optional subwoofer) using a microprocessor command. The NJU25019 has all the necessary controls to implement a complete Dolby Pro Logic system, including surround volume trim, surround delay using internal memory, noise sequencer, and center modes. Dolby 3 Stereo mode, Simulated Stereo mode for monophonic input sources, and Normal Stereo mode are also included in the chip.

Dolby Pro Logic processing with a DSP affords high performance with 24 bits of resolution and precise digital filtering for perfect matching between channels with exact consistency unit to unit. With the freedom to choose a wide variety of codecs, A/Ds, and D/As to fit the system cost and performance targets, the NJU25019 can be optimized for any market, from the most cost sensitive multimedia systems to audiophile equipment.

Figure 20 Typical NJU25019 5.1-Channel Dolby Pro Logic System



BBE®High Definition Audio

The BBE process is a proven method of improving the quality of any audio by restoring the transients lost in the dynamics of speakers, which create a progressively greater impedance with increasing frequencies. BBE compensates for the natural tendency of loudspeakers to add progressively longer delay times to the high frequencies. An equal and opposite delay curve of BBE for the low frequencies, delivers the high frequency transients first. At the same time, the digital process increases the amplitude of both high and low frequencies, resulting in boosted bass and treble. The result is a noticeable improvement in the presence and clarity of the audio, with the most accurate reproduction of live audio possible. Because BBE is a post virtualization audio enhancement, it does not alter the surround information or the 3D virtualization process. BBE's Lo Contour and Process can be adjusted by commands from the microprocessor, or it can be disabled entirely.

Figure 21 BBE Gain vs. Frequenc y

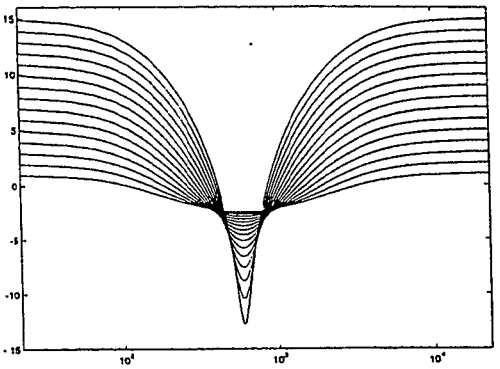
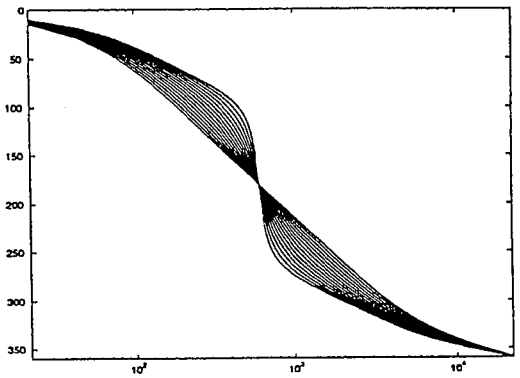


Figure 22 BBE Phase vs.Frequenc y



Digital Audio Data Interface

Three digital audio data formats are supported: left justified, right justified, and I²S. The data is always MSB first, 2's complement. Either 16-bit or 18-bit data can be accommodated. The polarities of the L/R clocks (LRI, LRO) are programmable, along with the active edge of the serial bit clocks (SCKI, SCKO). Master clock (ADMCK) and serial bit clock (ADSCK) outputs for the A/D and D/A converters are provided by an internal, programmable clock generator for synchronous operation with the DSP clock (768Fs). Asynchronous data rates are possible as long as the output is slaved to the input and it is close to the three supported sampling frequencies (32kHz, 44.1kHz, and 48kHz).

There is one stereo digital audio input and three stereo digital audio outputs for the L and R main channels, L and R surround

channels, Center, and Subwoofer. All three serial data outputs must have identical data formats. In each data format mode, SCLK and LRCLK polarities are independently programmable for input and output. Audio data width (16/18 bits), SCK and MCK frequencies (32/64Fs, 256/384Fs, respectively) must be the same for both input and output.

Clipping Indicator

Each audio sample is examined for over-range condition on both the stereo input and on each output. Any time the audio data reaches full scale, a Clipping Indicator flag is set in the DSP, and is output on pin 63 as an active-High logic level, which can be used to turn on an LED through a transistor. The Clipping Indicator remains High for approximately 4,000 samples, or about 0.1s after clipping is first detected in order to be visible. When this period (0.1 s) has been exceeded without any clipping, the Clipping Indicator pin is returned to logic Low. The Clipping Indicator may also be monitored by a microprocessor, which can take other appropriate action.

Serial Data Formats

There are three serial data formats supported for interfacing an A/D and three D/As to the digital audio interface. Either Left Justified, Right Justified, or I^2S mode is selected by the FMT0 and FMT1 bits in the second byte of the four-byte System State Download Command. In Left Justified mode, the MSB is aligned to the edge of LRI or LRO. The data is positioned at the left or "front" side of the L/R pulse (see Figure 12). In Right Justified mode, the LSB is aligned to the LRI or LRO edge. The data is at the right or "rear" of the L/R pulse (see Figure 13). Sometimes this mode is called Japanese mode or EIAJ mode. The I^2S mode is similar to Left Justified mode, except that the data is delayed one SCLK period and the sense of LRI and LRO is inverted (see Figure 14). In I^2S mode, LRI and LRO must be low for left channel data and high for right channel data, the opposite of other modes. The polarity of LRI and LRO can be inverted independently in any mode by the use of the LRI and LRO.

Normally, the serial data bits generated by a source change on the falling edge of the serial clock so that they can be easily clocked into a shift register on the rising clock edge. Considering an A/D as the source and the NJU25019 as a destination, the default setting is to clock the serial data input, SDI, in on the rising edge of SCKI. This can be changed to clock data in on the falling edge using the SCKI bit in the System Download Command.

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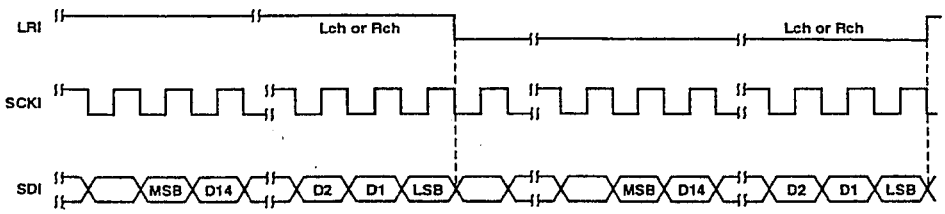
Figure 23 Serial Data Input Format



For the output serial data, the NJU25019 is considered the source and the D/As are considered the destination. The default interface setting is for data to be clocked out of SDO on the falling edge of SCKO so that the D/A clocks data in on the rising edge. This can be changed independently of the input and interface mode using the SCKO bit in the System Download Command.

The MS (Master/Slave) bit in the fourth System State Download Command byte selects either Master mode or Slave mode. In Right Justified mode, Master mode (MS = 0) is defined such that SCKO and LRO are generated from an internal divider derived from the 768Fs DSP clock (XI). In Slave mode (MS = 1) SCKO and LRO are the same as SCKI and LRI on the input. This mode should be used for asynchronous data rates, such as data from an S/PDIF receiver connected to the Digital Output from a laser disc player. The output D/A's must be synchronized to the input data by using the low jitter, recovered clock from the S/PDIF receiver to the D/A master clock. When an A/D is used, its master clock should be synchronous to the NJU25019 using ADMCK at 256Fs or 384Fs. In this case either Master mode or Slave mode will work. The default setting is Master mode (MS = 0).

In I^2S mode, Master and Slave modes have slightly different meanings. Relative to the NJU25019, Slave mode (MS = 1) is

defined as LRI and SCKI being inputs from the A/D. This means that the A/D must be in Master mode with L/R and SCLK outputs. Conversely, when the NJU25019 is in Master mode (MS = 0), LRI and SCKI are outputs that drive the L/R and SCLK inputs of an A/D operating in slave mode. SCKO and LRO to the D/As are always outputs. The D/A converters can run only in Slave mode, receiving both the L/R and SCLK from the NJU25019 LRO and SCKO are derived from the 768Fs DSP clock. When slave mode is selected, LRO and SCKO are generated by the LRI and SCKI inputs. Slave mode should be used for asynchronous audio data.

When using a codec in slave mode and operating the NJU25019 in I²S Master mode, the LRO signal must be used to drive the L/R input of the codec. Although LRI is not used, it must be programmed with the opposite polarity. This is the default setting upon initialization after reset (LRI=0, LRO=1) for typical 2-channel applications. For more details, refer to the Demonstration Board User's Guide. In all other modes or when using separate A/D and D/A converters that use both LRI and LRO, respectively, the polarity should be the same for LRI and LRO.

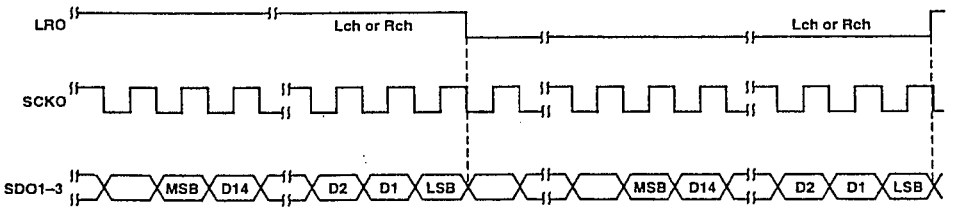
In Left Justified mode, only Slave mode (MS = 0) is allowed. The A/D is required to be in Master mode and supplies LRI and SCKI to the NJU25019 LRO and SCKO are generated from LRI and SCKI inputs.

For each data format, the serial clock frequency for SCKI and SCKO is selected using ADSCK in the System Download Command: either 32Fs (32-bit clocks per sample) or 64Fs (64-bit clocks per sample). SCKI and SCKO must be the same frequency. This clock is generated internally for the SCKI and SCKO in Master mode, but is also available as an output on the ADSCK pin. It is derived from the 768Fs Input Clock to the NJU25019

If SCKI and SCKO are selected to be 32Fs, the data length must be set to 16-bits (BIO = 0) because a stereo pair of 16-bit channels needs all 32 clocks per sample. In this case, both Left and Right Justified modes look exactly the same (see Figure 15), and either mode setting will work. In I²S mode, the data bits appear shifted by one SCLK and the L/R is inverted (see Figure 16).

An output clock, ADMCK, is derived from the NJU25019 768Fs Input Clock for use as an A/D or D/A master clock. ADMCK is set to 256Fs or 384Fs using the ADMCK bit in the System Download Command.

Figure 24 Serial Data Output Format



Microcontroller Interface

There are two microprocessor interface modes that can be used to work with a variety of microcontrollers, including 68000, Z80, or 8031 type interfaces. The primary difference between modes is that data is latched on the rising edge of $\overline{WR}$ in Z80 mode, while data is latched on the falling edge of $\overline{RD}$ in 68K mode. For 68K mode, SEL68 is set high, and for Z80 it is set low. The interface may be configured for 8-bit serial data by a logic low on $\overline{SEN}$, and clocking the data in using $\overline{WR}$ or $\overline{RD}$ as the serial bit clock, depending on the mode, Z80 (rising edge) or 68K (falling edge), respectively.

Figure 25 Z80 Interface

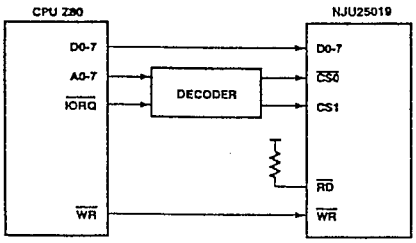
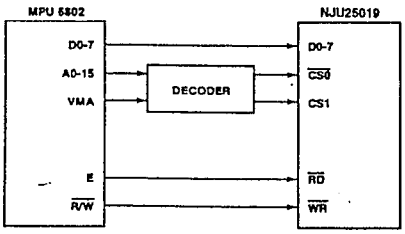


Figure 26 68K Interface



All of the microprocessor commands in the NJU25019 consist of multiple bytes of data. After the last byte is received, the DSP may use the available time at the end of audio processing during each audio sample to calculate coefficients required for the new parameters. Each command may take a different amount of time, depending on the parametric data to be calculated. Therefore, the NJU25019 has a pin that can be used for a handshake protocol using pin 62, HSHK, for optimum data transfer from the host to the DSP. The NJU25019 can accept data without using the Handshake pin as long as the worst case processing time, 5ms, is inserted between bytes and commands.

The HSHK pin toggles after each byte is received, processed, and the DSP is ready to receive the next byte. The procedure for the microprocessor is to read the state of the pin before sending a command byte to the NJU25019 Before the next byte can be sent, the microprocessor must wait for the pin to change state. The only exception is the first byte after the NJU25019 has been reset, either by turning the power on or with a hardware reset on pin 30, $\overline{RES}$. The microprocessor must not wait for a change of state before sending the first byte in this case. The initial state of HSHK is logic Low.

Parallel Interface—Z80 Mode

Writing commands to the NJU25019 from a Z80 type microprocessor is accomplished by setting SEL68 Low, placing data on the input data port, D0 to D7, setting the chip selects, and strobing $\overline{WR}$ Low then High. Successive writes, as in the four-byte System Download Command, can be done without resetting the chip select(s). It is recommended to return the Chip Select to the inactive state as soon as the command is sent. The recommended sequence for writing parallel data to the NJU25019 is:

1. Read state of HSHK (if using handshake interface).
2. Set $\overline{RD}$ High (can be tied to Vcc).
3. Place data on the data port, D0:7.
4. Assert chip selects, ($\overline{CS0}$ = 0 and CS1 = 1).
   One can be permanently tied to its active state, while the other is controlled.
5. Strobe $\overline{WR}$ Low, then High.
6. Deactivate chip selects.
7. Wait until HSHK changes state or 5 ms before sending next byte or command.

Parallel Interface—68K Mode

In 68K mode (SEL68 High) $\overline{RD}$ acts as a strobe for both read and write operations. $\overline{WR}$ defines whether a read or write is to be performed (L = write to NJU25019 H = there is no provision for reading from NJU25019). Since only write operations are allowed, $\overline{WR}$ can be tied Low. The recommended sequence to write parallel data to the NJU25019 in this mode is:

1. Read state of HSHK (if using handshake interface).
2. Set $\overline{WR}$ Low (can be tied to GND).
3. Place data on the data port, D0:7.
4. Assert chip selects, ($\overline{CS0}$ = 0 and CS1 = 1).
   One can be permanently tied to its active state, while the other is controlled.
5. Strobe $\overline{RD}$ High, then Low.

Serial Interface

In serial interface mode ($\overline{SEN}$ = 0), D0 is used for the serial data input. Two types of interface modes are supported. In Z80 mode (SEL68 Low) $\overline{WR}$ is used as a serial bit clock. In 68K mode (SEL68 High), $\overline{RD}$ is used to clock the serial data. Data is clocked in 8 bits at a time with a maximum data rate of 1 MHz. As in Parallel mode above, after each byte (8 serial data bits), HSHK must change state or a wait time of 5 ms must occur before the next byte or command is sent.

Serial Interface—Z80 Mode

When using a microprocessor with a Z80 type interface, writing serial data to the NJU25019 is done by clocking the data in on rising edges of the $\overline{WR}$, with $\overline{RD}$ held High (SEL68 = 0). The idle state of $\overline{WR}$ must be High when $\overline{CS0}$ and CS1 become active and return to inactive states. The recommended sequence is:

1. Read state of HSHK (if using handshake interface).
2. Set $\overline{SEN}$ = 0
3. Assert chip selects, ($\overline{CS0}$ = 0 and CS1 = 1).
4. Set $\overline{RD}$ High.
5. Clock in serial data with $\overline{WR}$ (rising edge).
6. Deactivate chip selects.
7. Wait until HSHK changes state or 5 ms before sending next byte or command.

Serial Interface—68K Mode

For 68K type microprocessors, the function of $\overline{RD}$ and $\overline{WR}$ is opposite of the Z80. Writing serial data to the NJU25019is done by setting $\overline{WR}$ Low and clocking the data in on rising edges of $\overline{RD}$ (SEL68 = 1). The idle state of $\overline{RD}$ must be Low when $\overline{CS0}$ and CS1 become active and return to inactive states. The recommended sequence is:

1. Read state of HSHK (if using handshake interface).
2. Set $\overline{SEN}$ = 0.
3. Assert chip selects, ($\overline{CS0}$ = 0 and CS1 = 1).
4. Set $\overline{WR}$ Low.
5. Clock in serial data with $\overline{RD}$ (falling edge).
6. Deactivate chip selects.
7. Wait until HSHK changes state or 5 ms before sending next byte or command.

Microcontroller Command Descriptions

In the following tables, * indicates the default setting.

NJU25019 Power-Up Default Settings

Operating Mode	Spatializer N-2-2 (2.1 channel output)
BBE Sound Enhancement	OFF
Front Filter	OFF
Subwoofer Crossover	80Hz
Auto Input Balance	ON
Noise Sequencer	OFF
Noise Sequencer Channel	Left
Surround Mode	ON
Surround Delay ON/OFF	OFF
Surround Time Delay	20ms
Center Channel Mode	ON in WideBand (when Pro Logic is selected changes to ON in NORMAL)
Level Trim	Master Volume
Trim Level	-6 dB
Balance/Tone Select	Balance
Balance/Tone Level	Centered
Subwoofer/Left Surround Swap	SDO1=L/R, SDO2=LS/C, SDO3=SW/RS
Serial Audio Data I/O	18 bits
Serial Audio Data Justification	I^2S
Output L/R Clock	Right when HIGH
Serial Clock for Audio Output	Serial data changes on falling edge
Input L/R Clock Polarity	Left data on HIGH
Serial Clock for Input Audio Data	Input data latches on rising edge
Master/Slave mode	Master
Serial data clock output for converters	32Fs (1/24 DSP clock, 768Fs)
Master clock output for converters	384Fs (1/2 DSP clock, 768Fs)

Configuration Command

After power is applied and a hardware reset is generated on the $\overline{RES}$ pin (pin 30), four bytes must be sent from the microprocessor, which define the hardware settings of the NJU25019 This data controls the digital audio interface format, the Clock Generator outputs, and the channel assignment for the output surround data. This command is one of two multi-byte commands—all the others are single byte and take effect immediately without interruption of the audio processing. The other commands contain a non- zero "op code" and all data bits in one byte.

When the DSP receives the first byte of the Configuration Command, which is all zeroes, the audio stops and the DSP waits for three more bytes. These hardware settings are intended to be set once, and not changed unless the chip is reset again.

Byte #1—Configuration Command op code, 00h.

Byte #2—Hardware Settings

SWP	Swap Subwoofer and Left Surround
0	6ch mode: L/R on SDO1, SW/C on SDO2, LS/RS on SDO3
1*	4ch mode: L/R on SDO1, LS/C on SDO2, SW/RS on SDO3* (allows 4ch Pro Logic Surround using only 2 stereo DACs)

BIO	Serial audio data I/O number of bits
0	16 bits
1*	18 bits*

FMT1, 0	Serial Audio Data Justification Format
0, 0	Right-justified
0, 1*	I^2S*
1, 0	Reserved
1, 1	Left-justified

Note: In I^2S Master mode, LRI becomes an output.

* indicates the default setting

Byte #3—Reserved, 19h

Byte #4—Clock Outputs

LRO	Output L/R Clock
0	Left data on SDOn when High, Right data on SDOn when Low
1*	Right data on SDOn when High, Left data on SDOn when Low*

SCKO	Serial Clock for Output Audio Data
0*	Serial data on SDOn changes on falling edge*
1	Serial data on SDOn changes on rising edge

LRI[1]	Input L/R Clock Polarity
0*	Left data on SDI when High, Right data on SDI when Low*
1	Right data on SDI when High, Left data on SDI when Low

1. In I²S Master mode, LRI becomes an output

SCKI[1]	Serial Clock for Input audio data
0*	Serial data on SDI latches on rising edge*
1	Serial data on SDI latches on falling edge

1. In I²S Master mode, SCKI becomes an output, and the function is identical to SCKO

MS	Master/Slave
0*	Master mode*
1	Slave mode

ADSCK	A/D-D/A Serial data Clock output
0*	32Fs* (1/24 DSP clock, 768Fs)
1	64Fs (1/12 DSP clock, 768Fs)

ADMCK	A/D-D/A Master Clock output
0*	384Fs* (1/2 DSP clock, 768Fs)
1	256Fs (1/3 DSP clock, 768Fs)

Noise Sequencer Command

A pink noise generator is required for Dolby Pro Logic to set the levels for the front, center, and surround speakers. When the noise sequencer is turned ON, the audio input is ignored, and the noise generator is output on the channel selected. The Noise Sequencer works on any of the selected Operating Modes. When the Noise-Sequencer is ON, the front High Pass Filters are bypassed.

NS	Noise Sequencer On/Off
0*	OFF*, normal audio output
1	ON, noise generator on selected channel

NCH1, NCH0	Noise Sequencer Channel
0, 0	Left
0, 1	Center
1, 0	Right
1, 1*	Surround* (both LS and RS)

Auto Input Balance/Crossover Filters Command

The NJU25019can automatically compensate for mismatch in level between the Left and Right stereo input. This is done by continuously comparing the ratio of Center Channel signal to the other signals and minimizing the Center from Left and Right. At the same time, this assures optimum Surround under varying conditions, such as slight shift in balance due to program changes in TV.

IBL	Auto Input Balance
0	OFF
1*	ON*

In addition to Dolby Pro Logic decoding, the NJU25019 provides an optional subwoofer output that is created by summing, scaling and Low Pass Filtering the Left, Center and Right channels. This single pole filter has a default cutoff at 80Hz. The subwoofer output is always active and the cutoff frequency may be changed by the Coefficient Download Command. If using an external crossover filter, the LPF may be bypassed and the full-bandwidth mix of L, C, and R appears at the output.

LPF	Low Pass Crossover Filter
0*	Full bandwidth, no filtering*
1	80Hz

When a subwoofer is used, smaller front speakers with limited low frequency response may be used. To prevent distortion caused by over driving small speakers with full bandwidth audio, a single-pole High Pass Crossover Filter on the front Left and Right channels is normally active. When ON, the High Pass Crossover Filter has a default -3dB cutoff frequency of 80Hz. Full bandwidth audio can be restored by turning off the filter, or the filter's crossover frequency can be changed using the Coefficient Download Command.

HPF	High Pass Crossover Filter[1]
0*	OFF, full bandwidth to Front Left and Right*
1	ON, 80Hz

1. High Pass Filters are bypassed (full bandwidth) when Noise Sequencer is ON.

Operating Mode Command

Sets the audio processing to be performed: Dolby Pro Logic, N-2-2, Simulated Stereo, or Surround Off (normal stereo).

OP1, OP0	Operating Mode
0, 0	Dolby Pro Logic (5.1ch, L,R,SW,C,LS,RS)
0, 1*	Spatializer N-2-2 (2.1ch, L,R,SW)*
1, 0	Simulated Stereo (mono-to-stereo synthesis)
1, 1	Surround OFF (Normal Stereo)

* indicates the default setting

Surround Mode Command

For systems limited to only the front Left, Center, and Right speakers, Dolby 3 Stereo can be selected which mixes the surround information into the front Left and Right channels. All the Dolby Surround information can be heard, except from the front speakers only. The Center Channel is output the same way in both Dolby 3 Stereo and Dolby Pro Logic modes: mixed equally into the front Left and Right channels.

SM	Surround Mode
0	Dolby 3 Stereo (surround redirected to front)
1*	Surround Active* (applies to Pro Logic mode)

For Spatializer N-2-2 mode, the surround channels delay is set to zero because the HRTF creates the equivalent effect of surround delay. For Dolby Pro Logic, the required delay range is from 15 to 30ms. There may be some cases where zero surround delay is desired. in which case the delay memory can be bypassed by setting the DLY bit. Since the delay memory is 16 bits wide, the output data is reduced to 16 bits when interfacing to 18-bit data input. If the surround time delay is bypassed while in Dolby Pro Logic mode, a front panel indicator may be required indicating non-standard operation.

DLY	Surround Delay
0	Normal (defaults to 20ms with Dolby Pro Logic)
1*	Bypass* (Spatializer N-2-2 mode)

Center Mode Command

The Center channel of Dolby Pro Logic is primarily intended for movie dialog and is filtered to remove low bass energy as well as high frequencies, leaving mostly voice bandwidth in the center speaker. The is the Normal setting for the Center channel in Dolby Pro Logic mode. However, when listening to music with Dolby Pro Logic, it may be desirable to reconfigure the center channel into full bandwidth, since musical instruments generally have wider bandwidth and are frequently mixed as a center image. The Center filtering can be defeated by activating the WideBand mode. A panel indicator may be required since this is not the normal Dolby Pro Logic operating mode.

Dolby Pro Logic operation requires a Phantom Center channel mode which is intended for systems without a center speaker. In this mode, the Center audio is mixed equally into the front Left and Right channels to create a phantom center image between the speakers. During N-2-2 operation, the center channel operates as a wideband phantom channel and other Center modes should not be allowed.

CM1, CM0	Center Mode[1]
0, 0	Center ON (Normal)
0, 1	Phantom
1, 0*	WideBand* (full bandwidth)
1, 1	Center OFF

1. Center default is WideBand in N-2-2 and only Center ON/OFF is possible. In Dolby Pro Logic mode, default is Center ON in Normal.

Level Trim Command

In Pro Logic mode, the Center and Surround Channels are required to have a level trim of +10dB to -10dB. The NJU25019 provides a range of 0 dB to -31 dB attenuation. To obtain +10dB gain, it is necessary to set the NJU25019 to nominal -10 dB and apply +10 dB gain in the audio path for that channel. In addition to Center and Surround, the Subwoofer and Master Volume may be attenuated by the same range. Master Volume may be used either as a volume control or headroom control.

The volume and trim control may be done either digitally in the NJU25019 or with analog techniques. In order to preserve the maximum signal-to-noise audio performance, it is better to use analog attenuators external to the DSP, since the signal and noise will be attenuated in the same ratio. Attenuation in the digital domain, although easily done, attenuates the signal only with the system noise level remaining constant. The signal-to-noise ratio increases with increasing attenuation. Nothing is lost in the NJU25019 that has over a 140 dB dynamic range. However, system signal-to-noise is limited by the resolution and S/N of the A/D and D/A converters in a digital audio system. After deducting operating headroom for input signal range and level trims, inadequate dynamic range remains unless high resolution data converters are employed. For optimum signal-to-noise performance, the clipping indicator can be used like a Vu meter to adjust the input attenuation for maximum signal without clipping.

The Subwoofer is always ON in any operating mode with Level Trim control. Level Trim for Center and Surround are active in the two surround modes, Pro Logic and N-2-2. In N-2-2, the Level Trims control both the Phantom Center and Virtual Surround in

the front channels (SDO1) together with the Dolby Pro Logic Center and Surround on the other outputs (SDO2 and SDO3).

CH1, CH0	Channel
0, 0	Center
0, 1	Surround
1, 0	Subwoofer
1, 1*	Master Volume (Headroom)*

TR4-TR0	Trim Level[1]
00000	0dB
00001	-1dB
•	•
11110	-30dB
11111	MUTE

1. The default Trim Level is -6dB.

* indicates the default setting

Surround Delay Time Command

Dolby Pro Logic requires the surround channels to be delayed from 15ms to 30ms. An internal 16 bit wide SRAM has 1.5K bytes for 1,536 audio samples. The delay memory can be bypassed using the DLY bit in the Surround mode Command.

DLY3-DLY0	Delay
1111	30 ms
1110	29 ms
•	•
0101*	20 ms*
•	•
0001	16 ms
0000	15 ms

Balance/BBE Parameters Command

The Front Left and Right channels may be balanced in any mode with this command. To shift the balance to the Left channel, the Right channel is attenuated up to -15dB in 1dB steps using the Level Command, explained below. To shift the balance toward the Right channel, the Left channel is attenuated up to 16dB.

Alternately, the Level Command data may be used to adjust the BBE parameters. There are two components to BBE, Lo Coutour and Process. Lo Contour controls the amount of phase compensated bass equalization on the Left and Right channels. Process controls the amount of phase compensated high frequency equalization. Initially, the default BBE settings are +3dB Lo Contour and +6dB Process. This curve produces about -3dB attenuation of the mid-band frequencies centered at 500Hz (see Figure 21).

The procedure is to first specify which of the three parameters is to be adjusted with this command, followed by the adjustment level in the Level Command. New levels can be set for the same parameter without repeating this command until a new parameter is to be set.

BB1, BB0	Balance/BBE Parameter
0, 0*	Balance Adjust*
0, 1	BBE Lo Contour
1, 0	BBE Process
1, 1	Reserved

Balance/BBE Level Command

The Balance Level is performed by specifying an attenuation for the opposite channel, maintaining 0dB on the louder side according to the table below.

BAL4-BAL0	Left	Right	Balance
01111	0dB	-15dB	Minimum Right
01110	0dB	-14dB	
•	•	•	•
00001	0dB	-1dB	
00000*	0dB	0dB	Center*
11111	-1dB	0dB	
•	•	•	•
10001	-15dB	0dB	
10000	-16dB	0dB	Minimum Left

It is possible to vary the BBE levels independently from 0dB to +15dB as shown in the family of curves in Figure 21 depending on which Parameter was previously selected. The phase response varies with gain according to Figure 22, starting with linear phase at 0dB. When BBE is turned Off, the frequency response of the NJU25019 is flat at 0dB. Increasing levels of BBE requires additional headroom using the Master Volume Level Trim Command. The clipping indicator may be used to detect when the headroom has been exceeded.

BAL4-BAL0	BBE Level
01111	+15dB
01110	+14dB
•	•
00001	+1dB
00000	0dB

Successive Level changes may be made to the same parameter without a new Balance/ BBE Control Command. The Balance/ BBE Level Command applies to the last function specified.

Sampling Frequency Command

In most cases, it is desirable to keep the 768Fs DSP clock synchronous with the converter clocks and the sample rate according to the following table.

Sample Rate	768Fs DSP Clock
32 kHz	24.576 MHz
44.1 kHz*	33.868 MHz*

* indicates the default setting

The firmware that runs in the NJU25019 is based on a 33.868 MHz clock. For systems based on a 44.1 kHz sample rate, the NJU25019 will operate as defined. When using a different sample rate, alternate data must be downloaded to the NJU25019 using the Coefficient Download command. The alternate data over writes the default data until either the Reset command or the device is powered-down, in which case the default settings are restored. When operating the NJU25019 with other than a 33.868 MHz clock, each time the device is powered-up the alternate data must be downloaded for proper operation.

Coefficient Download Command

Several default parameters in the NJU25019 can be changed by downloading a new set of coefficients: Sampling Frequency, Bass Low Pass and Treble High Pass Filter Cutoff Frequencies, Subwoofer Cutoff Frequency, and Front Left/Right High Pass Filter Cutoff Frequency. The Bass Low Pass Cutoff Filter Frequency is set at 100 Hz and the Treble High Pass Cutoff Frequency is set at 10 kHz. The download sequence and the exact data for each is available in a separate Application Note from MedianiX.

Microcontroller Command Tables

In the following tables, * indicates the default setting.

Configuration Command (4 bytes)

Byte 1—Download Command

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Byte #1
								Command

Byte 2—Download Data, Hardware Settings

7	6	5	4	3	2	1	0		
SWP	0	0	0	0	BIO	FMT1	FMT0	Byte #2 Data, Hardware settings	
						0	0	Right Justified	Audio Data
						0	1	I²S*	Interface Mode
						1	0	Reserved	
						1	1	Left Justified	
					0			16 bits	Audio Data Width
					1			18 bits*	
								Reserved	
0								Std. DAC configuration (L/R, SW/C, LS/RS)	
1								Alt. DAC configuration (L/R, LS/C, SW/RS)*	

Note: In I²S Master mode, SCK1 becomes an output, and the function is identical to SCKO. Also, in I²S Master mode, LRI becomes an output

Byte 3—Download Data—Reserved

7	6	5	4	3	2	1	0	
0	0	0	1	1	0	0	1	Byte #3 Data
								Reserved

Byte 4—Download Data, Clock Outputs

7	6	5	4	3	2	1	0			
LRO	SCKO	LRI	SCKI	0	MS	ADSCK	ADMCK	Byte #4 Data, Clock Outputs		
							0	384Fs*	A/D-D/A MCLK	
							1	256Fs		
						0		32Fs*	A/D-D/A SCLK	
						1		64Fs		
					0			Master*	Audio Data	
					1			Slave	Interface Mode	
				0				Reserved		
			0					↑	Data latches on rising edge*	
			1					↓	Data latches on falling edge	
		0						Left:high	Right:low*	Input
		1						Left:low	Right:high	L/R Clock
	0							↓	Data changes on falling edge*	
	1							↑	Data changes on rising edge	
0								Left:high	Right:low	Output
1								Left:low	Right:high*	L/R Clock

4

Noise Sequencer

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1
0	0	1	0	0	NS	NCH1	NCH0	Command
						0	0	Left
						0	1	Center
						1	0	Right
						1	1	Surround
					0			OFF*
					1			ON

Auto Input Balance/Crossover Filters

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1	
0	1	0	0	IBL	HPF	0	LPF0	Command	
							0	Full BW	Subwoofer
							1	80Hz*	
								Reserved	
					0			OFF*	Front L/R High-pass filter
					1			ON	
				0				OFF	Auto Input Balance
				1				ON*	

Operating Mode

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1
0	0	0	1	1	OP1	OP0	BBE	Command
							0	OFF*
							1	ON
					0	0		Dolby Pro Logic (5.1ch)
					0	1		Spatializer N-2-2 (2.1ch)*
					1	0		Spatializer Mono-to-Stereo
					1	1		Stereo (surround OFF)

Surround Mode

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1	
0	0	1	1	1	SM	OM	DLY	Command	
							0	ON*	Surround Delay
							1	OFF	
						0		OFF	(defaults to OFF with Pro Logic)
						1		ON*	Spatializer Surround Decorrelation
					0			Dolby 3 Stereo (3.1ch)	
					1			Dolby Pro Logic (5.1ch)*	

Center Mode

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1
0	0	1	1	0	CM1	CM0	0	Command
								Reserved
					0	0		Center ON (default with Pro Logic)
					0	1		Phantom
					1	0		WideBand* (full bandwith with Spatializer)
					1	1		Center OFF

Level Trim

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1
1	CH1	CH0	TR4	TR3	TR2	TR1	TR0	Command
			0	0	0	0	0	0dB* Level
			0	0	0	0	1	-1dB
			0	0	0	1	0	-2dB
			⋮	⋮	⋮	⋮	⋮	⋮
			1	1	1	1	0	-30dB
			1	1	1	1	1	MUTE
	0	0						Center
	0	1						Surround
	1	0						Subwoofer
	1	1						Master Volume (Headroom control)

Surround Delay

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1
0	1	0	1	DLY3	DLY2	DLY1	DLY0	Command
				1	1	1	1	30ms
				1	1	1	0	29ms
				⋮	⋮	⋮	⋮	⋮
				0	1	0	1	20ms*
				⋮	⋮	⋮	⋮	⋮
				0	0	0	1	16ms
				0	0	0	0	15ms

Balance/BBE Parameters

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1
0	0	0	0	1	0	BT1	BT0	Command
						0	0	Balance*
						0	1	Lo Contour
						1	0	Process
						1	1	Reserved
								Reserved

Balance/BBE Level

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1			BBE Process/
0	1	1	BAL4	BAL3	BAL2	BAL1	BAL0	Left	Right		Lo Contour
			0	1	1	1	1	0dB	-15dB	Min. Right	+15dB
			0	1	1	1	0	0dB	-14dB		+14dB
			⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮
			0	0	0	0	1	0dB	-1dB		+1dB
			0	0	0	0	0	0dB	0dB	Center*	0dB
			1	1	1	1	1	-1dB	0dB		
			⋮	⋮	⋮	⋮	⋮	⋮	⋮		
			1	0	0	0	1	-15dB	0dB		
			1	0	0	0	0	-16dB	0dB	Min. Left	

Coefficient Download

Byte 1—Command

7	6	5	4	3	2	1	0	Byte #1
0	0	0	1	0	0	0	MEM	Command
					0	0	0	RAM 0
					0	0	1	RAM 1

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Byte 2—Address Data Pointer

7	6	5	4	3	2	1	0	Byte #2
M7	M6	M5	M4	M3	M2	M1	M0	Address
								Data pointer

Byte 3—Data Length

7	6	5	4	3	2	1	0	Byte #3
L7	L6	L5	L4	L3	L2	L1	L0	Data Length
								Number of 24-bit coefficients, L

DataByte#	Coeff#	8/24bits
1	1	MSB's
2	1	Middle
3	1	LSB's
4	2	MSB's
5	2	Middle
6	2	LSB's
7	3	MSB's
8	3	Middle
9	3	LSB's
M	M	MSB's
M	M	Middle
M	M	LSB's
M	L	MSB's
M	L	Middle
3*L	L	LSB's

MEMO