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FAST Products	

FAST 74F620, 74F623 Transceivers

74F620 Octal Bus Transceiver, Inverting (3-State)
74F623 Octal Bus Transceiver, Non-Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F620	3.5ns	80mA
74F623	4.5ns	105mA

FEATURES

- **High impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 64mA and source 15mA**
- **-'F620 Inverting**
  -'F623 Non-Inverting

DESCRIPTION

The 74F620 is an octal bus transceiver featuring inverting 3-state bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 74F623 is a non-inverting version of the 74F620.These octal bus transceivers are designed for asynchro-

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F620N, N74F623N
20-Pin Plastic SOL[1]	N74F620D, N74F623D

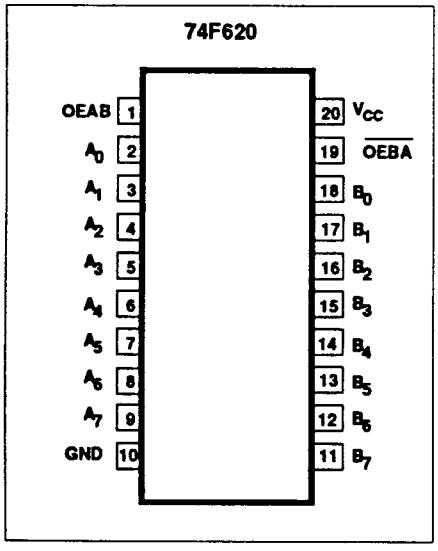
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal considerations for suface mounted device.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

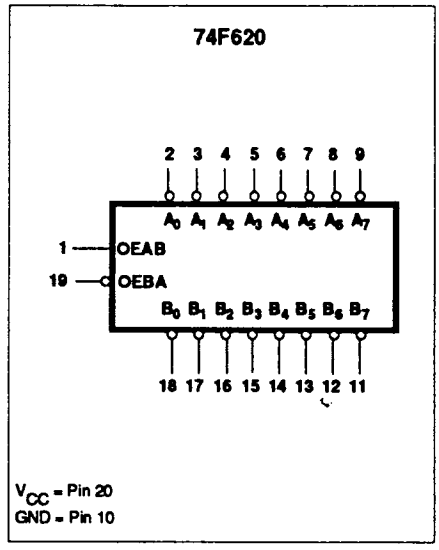
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	3.5/1.16	70μA/70μA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/0.033	20μA/20μA
A_0-A_7	Data outputs	150/40	3mA/24mA
B_0-B_7	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

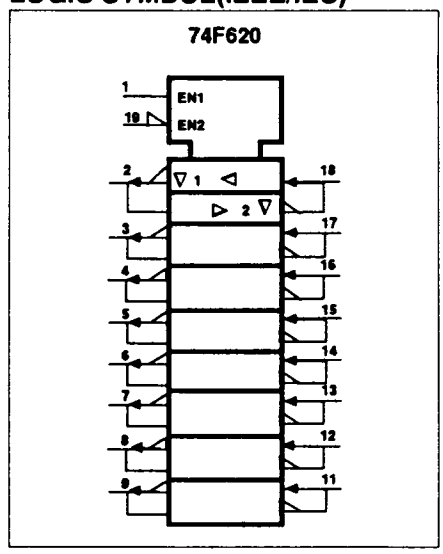
PIN CONFIGURATION



LOGIC SYMBOL



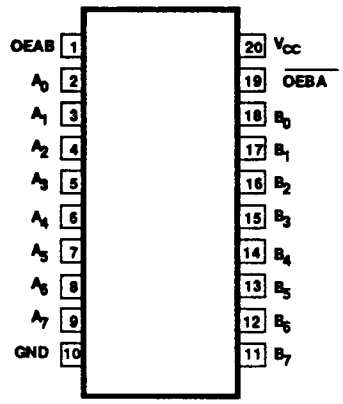
LOGIC SYMBOL(IEEE/IEC)



nous two-way communication between data busses. The control function implementation allows for maximum flexibilty in timing. These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the 'F620 and 'F623 the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance,both sets of bus lines (16 in all) will remain at their last states.

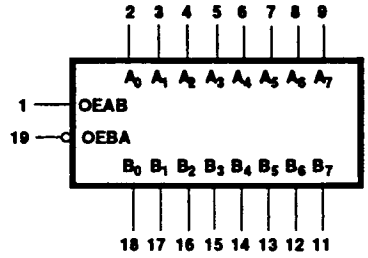
PIN CONFIGURATION

74F623



LOGIC SYMBOL

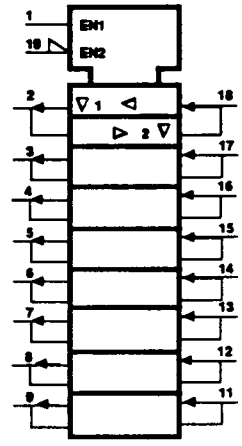
74F623



V_{CC} = Pin 20
GND = Pin 10

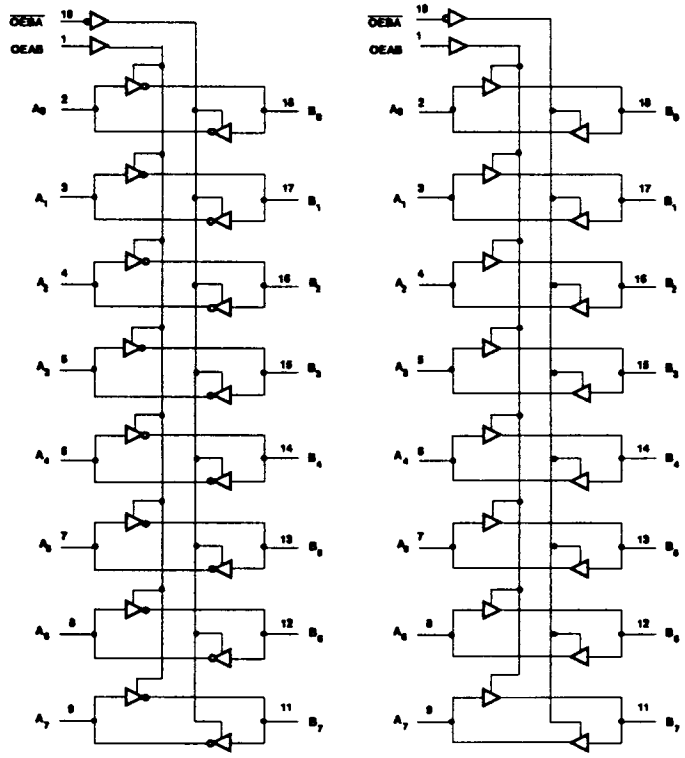
LOGIC SYMBOL(IEEE/IEC)

74F623



LOGIC DIAGRAM

74F620 74F623



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS		OPERATING MODES	
$\overline{OEBA}$	OEAB	'F620	'F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus $\overline{A}$ data to B bus	B data to A bus A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEBA}$, OEAB	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		Others	V_{CC} = 5.5V, V_I =5.5V					1	mA
I_{IH}	High-level input current	$\overline{OEBA}$, OEAB only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH} +I_{IH}	Off state output current, High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-70	µA
I_{OS}	Short circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	'F620 I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=GND			70	92	mA
		'F620 I_{CCL}		$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=4.5V			84	110	mA
		'F620 I_{CCZ}		OEAB=GND; $\overline{OEBA}$= A_0-A_7=4.5V			84	110	mA
		'F623 I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=4.5V			110	140	mA
		'F623 I_{CCL}		$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=GND			110	140	mA
		'F623 I_{CCZ}		OEAB=GND; $\overline{OEBA}$= A_0-A_7=4.5V			99	130	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

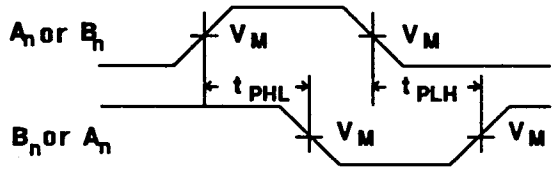
AC CHARACTERISTICS for 'F620

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	3.0 4.0	7.5 7.5	10.5 10.5	2.5 3.5	11.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	7.5 7.0	2.0 1.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	4.5 4.5	7.5 7.5	10.5 10.0	4.0 4.0	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.5 6.5	9.5 9.5	2.5 3.5	10.5 10.5	ns

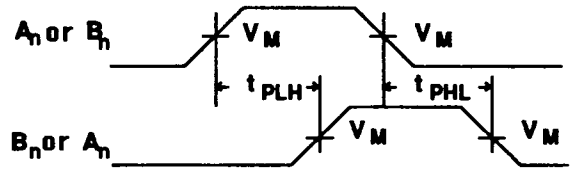
AC CHARACTERISTICS for 'F623

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.0 3.0	4.0 5.0	5.5 7.0	2.0 2.5	6.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.0 2.5	4.0 4.5	5.5 6.5	2.0 2.5	6.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	5.0 5.0	8.5 7.5	10.5 9.5	5.0 5.0	12.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.5 6.5	2.5 2.5	7.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	5.0 4.5	8.0 7.0	10.0 9.0	5.0 4.5	11.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.0 7.0	8.5 9.0	3.0 4.0	10.0 10.0	ns

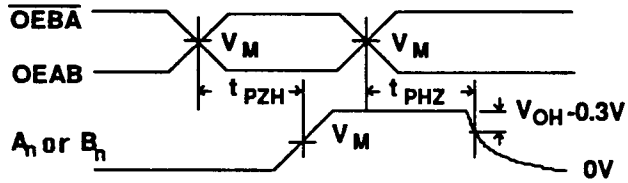
AC WAVEFORMS



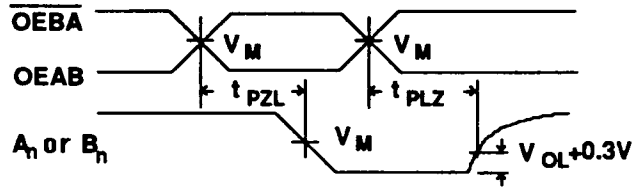
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



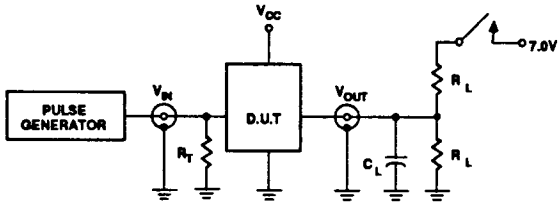
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

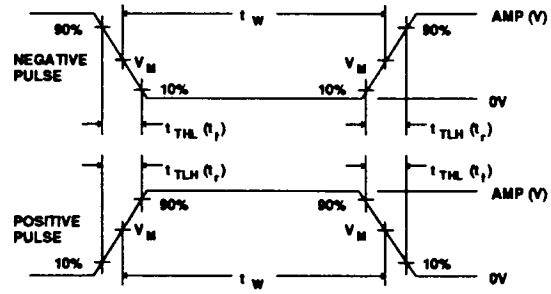
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns