Genesys Logic, Inc.

GL9711

PCI Express™ PIPE x1 PHY

Datasheet

Revision 1.10

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Revision History

Revision	Date	Description
0.95	7/11/2005	Preliminary release
0.96	7/27/2005	1. Modify Table3.1–Ball Out, p.11 2. Modify "PIPE Interface" and "Other Signals", Table3.4–Pin Descriptions, p.15~p.17 3. Modify Ch4.2 Registers Descriptions, p.19 4. Modify Ch6.10 Operation Mode and Multi-Functional Pins, p.28 5. Modify Table6.1-Pin Functions, p.28~p.30 6. Modify Table8.1~8.5, p.36~p.37
0.97	09/20/2005	Modify Package Dimension,Ch9 , p.40
0.98	11/15/2005	1. Add "Bottom View", Figures.3.1, p.10 2. Update Table3.4, p.15~p.18 3. Update Table3.5, p.18 4. Modify the default value of REG0 and REG1, Table4.1, p.19 5. Modify Ch4.2 Registers Descriptions for REG0 and REG1, p.20 6. Add Ch 4.3, p.22~p.25 7. Update Table 7.5 for power consumption, p.35 8. Change TXDx to RXDx, Figure 8.4, p.39 9. The minimum and maximum value of $T_{CYCLE,}$ Table8.2 and Table 8.5, p.40
1.00	12/15/2005	1. Update Table 7.8 for temperature ranges (p.37) 2. Update Table 8.1~8.4 for output delay of RX bus (p.39~p.40)
1.01	04/13/2006	1. Modify the description of OSC25MI and OSC25MO signals, Table 3.4, p.15 2. Swap the Pin Out of OSC25MI and OSC25MO in Table 3.1~Table 3.4. 3. Update Table 7.1 for deleting I_{DD1-X4}, I_{DD2-X4}, I_{DD3-X4}, I_{DD1-X2}, I_{DD2-X2}, and I_{DD3-X2} six items, p.34 4. Update Table 7.8 for deleting the $I_{SUPPLY-1.8}$ item and adding θ_{JA}, Ψ_{JT} and θ_{JC} three items, p.37
1.02	04/26/2006	Divide Table 7.8 into Table 7.8(Temperature Range) and Table 7.9(Thermal Characteristics), p.37
1.10	07/04/2006	1. Update Table 3.5 for the parameter of buffer I/O, p.18 2. Remove Table 7.2, p.34 3. Update Fig. 8.1, 8.2 and Table 8.1~8.5 for PIPE input and output timing characteristic, p.38~p.40

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CHAPTER 1 GENERAL DESCRIPTION

The GL9711 is a 1-lane PCI Express PHY Layer Controller, which is compliant with PCI Express Base Specification rev. 1.0a and Intel's PHY Interface for the PCI Express Architecture rev. 1.0. It integrates one SerDes and the Physical Coding Sublayer (PCS) which performs 8b/10b encoding and decoding, elastic buffer and receiver detection, data serialization and deserialization. The SerDes in the GL9711 supports an effective serial interface speed (2.5 Gb/s) of data bandwidth, intended for use in ultrahigh-speed bi-directional data transmission system. The GL9711 can also be externally configured for various parallel bus width which is flexible and suitable for implementation. It also supports four operational states for power management to minimize power consumption. For production and self-test purposes, the GL9711 provides BIST and an internal loopback capability.

The primary application of this chip is to provide very high-speed I/O data channels for point-to-point baseband data transmission over an on-chip termination resister of 50 Ohm +/- 10%.

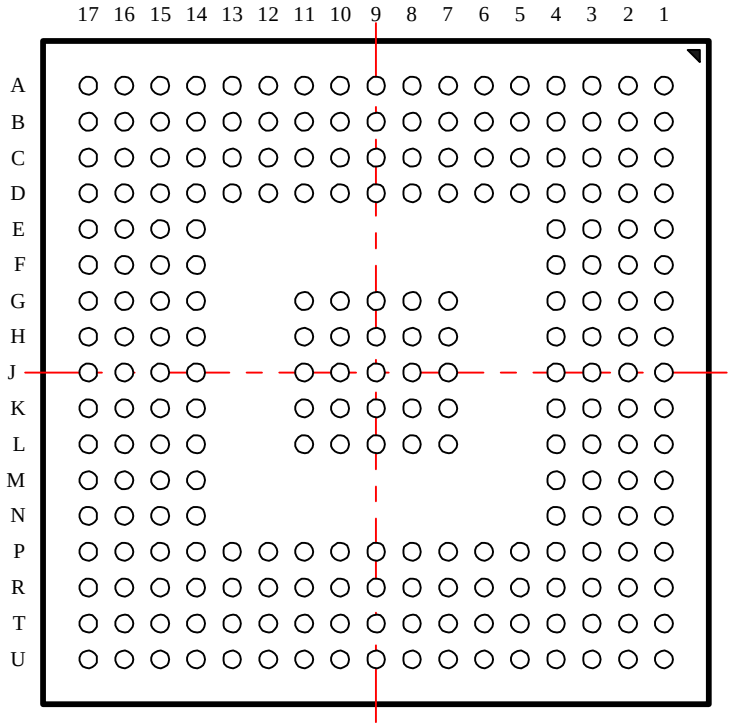
This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector pins, and transmit/receive pins. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel. It is then reconstructed into its original parallel format. The maximum data transfer rate in each direction is 256M bytes per second. It also offers various power saving modes to significantly reduce power consumption as well as scalability for a higher data rate in the future.

CHAPTER 2 FEATURES

- Complies with PCI Express Base Specification rev. 1.0a
- Complies with Intel's PHY Interface for PCI Express Architecture rev. 1.0
- Integrates 2.5 gigabit per second (Gpbs) Serializer/Deserializer
- Supports 8-bit or 10-bit parallel interface @250MHz
- Supports 16-bit parallel interface @125MHz
- Supports DDR configuration for 8-bit or 10-bit mode
- Beacon transmission and reception
- Receiver detection
- Transmission and detection of electrical idle
- Clock tolerance for 600 ppm in frequencies between bit rates at the two end of a Link
- On-chip 8-bit/10-bit encoding/decoding and comma alignment
- On-chip PLL provides clock synthesis
- 1.8-V power supply for core
- 2.5-V power supply for IO
- Above 2.0 kV ESD protection
- 0.18 µm process
- Available in LFBGA-233 package

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout



Bottom View

Figure 3.1 - 233 Pin LFBGA Pinout Diagram

3.2 Ball Out

Table 3.1 - Ball Out

	1	2	3	4	5	6	7	8	9
A	REFCLKP	NC	VDDTX	NC	VDDRX	NC	VDDTX	NC	VDDRX
B	REFCLKN	NC	VSSTX	NC	VSSRX	NC	VSSTX	NC	VSSRX
C	OSC25MO	NC	NC	VDD18	NC	NC	VSSTX	VDDPLL	NC
D	OSC25MI	VDD25	NC	VSS	VSS	NC	VDD18	RTERM	VSSPLL
E	NC	NC	NC	NC					
F	VSS	NC	NC	NC					
G	NC	VDD25	NC	NC			VSS	VSS	VSS
H	NC	NC	NC	NC			VSS	VSS	VSS
J	NC	VSS	NC	NC			VSS	VSS	VSS
K	VDD25	NC	NC	VDD12			VSS	VSS	VSS
L	VSS	VSS	NC	VDD18			VSS	VSS	VSS
M	VSS	NC	VDD18	NC					
N	NC	VSS	NC	NC					
P	VDD25	NC	NC	NC	NC	NC	NC	NC	VSS

R	NC	NC	NC	NC	NC	NC	VSS	NC	OPMODE0
T	NC	VDD25	NC	NC	VDD25	VDD18	NC	NC	NC
U	VSS	NC	VSS	NC	PHYSTS	NC	NC	NC	VDD25
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**

	10	**11**	**12**	**13**	**14**	**15**	**16**	**17**	
A	TXN	VDDTX	RXN	VDDRX	NC	VDDTX	NC	VDDRX	
B	TXP	VSSTX	RXP	VSSRX	NC	VSSTX	NC	VSSRX	
C	VDD18	NC	VDD18	NC	TXD9	VSSGR	TXD14	TXD15	
D	NC	NC	NC	TXD8	TXD11	TXD12	VDD25	NC	
E					TXD13	TXDK1	TXD10	RXDK1	
F					NC	NC	RXD8	VDD25	
G	VSS	VSS			NC	RXD9	RXD10	RXD12	
H	VSS	VSS			RXD13	RXD11	RXD15	VDD18	
J	VSS	VSS			VDD12	VSS	RXD14	VDD18	
K	VSS	VSS			TXD2	VDD25	TXDK0	NC	
L	VSS	VSS			TXCMP	TXD6	TXD1	TXD0	
M					RXSTS1	TXD4	TXD3	VSS	
N					RXD3	RXDK0	TXD7	TXD5	
P	PD1	RXVLD	NC	RXD7	RXD5	RXD1	VSS	RXSTS0	
R	SCC	TXDET/ LPBK	TXIDLE	VDD25	NC	RXD4	RXD0	VDD25	
T	TESTD	PD0	RXIDLE	NC	PCLK	VSS	RXD2	RXSTS2	
U	OPMODE1	TESTC	RST_N	RXPLR	VSS	NC	RXD6	VDD25	
	10	**11**	**12**	**13**	**14**	**15**	**16**	**17**	

3.3 Pin List

Table 3.2 - Numeric Pin List

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
A1	REFCLKP	C1	OSC25MO	E1	NC	G1	NC	J1	NC
A2	NC	C2	NC	E2	NC	G2	VDD25	J2	VSS
A3	VDDTX	C3	NC	E3	NC	G3	NC	J3	NC
A4	NC	C4	VDD18	E4	NC	G4	NC	J4	NC
A5	VDDRX	C5	NC	E5		G5		J5	
A6	NC	C6	NC	E6		G6		J6	
A7	VDDTX	C7	VSSTX	E7		G7	VSS	J7	VSS
A8	NC	C8	VDDPLL	E8		G8	VSS	J8	VSS
A9	VDDRX	C9	NC	E9		G9	VSS	J9	VSS
A10	TXN	C10	VDD18	E10		G10	VSS	J10	VSS
A11	VDDTX	C11	NC	E11		G11	VSS	J11	VSS
A12	RXN	C12	VDD18	E12		G12		J12	

A13	VDDRX	C13	NC	E13		G13		J13	
A14	NC	C14	TXD9	E14	TXD13	G14	NC	J14	VDD12
A15	VDDTX	C15	VSSGR	E15	TXDK1	G15	RXD9	J15	VSS
A16	NC	C16	TXD14	E16	TXD10	G16	RXD10	J16	RXD14
A17	VDDRX	C17	TXD15	E17	RXDK1	G17	RXD12	J17	VDD18
B1	REFCLKN	D1	OSC25MI	F1	VSS	H1	NC	K1	VDD25
B2	NC	D2	VDD25	F2	NC	H2	NC	K2	NC
B3	VSSTX	D3	NC	F3	NC	H3	NC	K3	NC
B4	NC	D4	VSS	F4	NC	H4	NC	K4	VDD12
B5	VSSRX	D5	VSS	F5		H5		K5	
B6	NC	D6	NC	F6		H6		K6	
B7	VSSTX	D7	VDD18	F7		H7	VSS	K7	VSS
B8	NC	D8	RTERM	F8		H8	VSS	K8	VSS
B9	VSSRX	D9	VSSPLL	F9		H9	VSS	K9	VSS
B10	TXP	D10	NC	F10		H10	VSS	K10	VSS
B11	VSSTX	D11	NC	F11		H11	VSS	K11	VSS
B12	RXP	D12	NC	F12		H12		K12	
B13	VSSRX	D13	TXD8	F13		H13		K13	
B14	NC	D14	TXD11	F14	NC	H14	RXD13	K14	TXD2
B15	VSSTX	D15	TXD12	F15	NC	H15	RXD11	K15	VDD25
B16	NC	D16	VDD25	F16	RXD8	H16	RXD15	K16	TXDK0
B17	VSSRX	D17	NC	F17	VDD25	H17	VDD18	K17	NC

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
L1	VSS	N1	NC	R1	NC	U1	VSS
L2	VSS	N2	VSS	R2	NC	U2	NC
L3	NC	N3	NC	R3	NC	U3	VSS
L4	VDD18	N4	NC	R4	NC	U4	NC
L5		N5		R5	NC	U5	PHYSTS
L6		N6		R6	NC	U6	NC
L7	VSS	N7		R7	VSS	U7	NC
L8	VSS	N8		R8	NC	U8	NC
L9	VSS	N9		R9	OPMODE0	U9	VDD25
L10	VSS	N10		R10	SCC	U10	OPMODE1
L11	VSS	N11		R11	TXDET/LPBK	U11	TESTC
L12		N12		R12	TXIDLE	U12	RST_N
L13		N13		R13	VDD25	U13	RXPLR
L14	TXCMP	N14	RXD3	R14	NC	U14	VSS

L15	TXD6	N15	RXDK0	R15	RXD4	U15	NC
L16	TXD1	N16	TXD7	R16	RXD0	U16	RXD6
L17	TXD0	N17	TXD5	R17	VDD25	U17	VDD25
M1	VSS	P1	VDD25	T1	NC	Blank	
M2	NC	P2	NC	T2	VDD25		
M3	VDD18	P3	NC	T3	NC		
M4	NC	P4	NC	T4	NC		
M5		P5	NC	T5	VDD25		
M6		P6	NC	T6	VDD18		
M7		P7	NC	T7	NC		
M8		P8	NC	T8	NC		
M9		P9	VSS	T9	NC		
M10		P10	PD1	T10	TESTD		
M11		P11	RXVLD	T11	PD0		
M12		P12	NC	T12	RXIDLE		
M13		P13	RXD7	T13	NC		
M14	RXSTS1	P14	RXD5	T14	PCLK		
M15	TXD4	P15	RXD1	T15	VSS		
M16	TXD3	P16	VSS	T16	RXD2		
M17	VSS	P17	RXSTS0	T17	RXSTS2		

Table 3.3 - Alphabetic Pin List

Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#
NC	C3	NC	G4	NC	F15	NC	A6	VSS	H7
NC	C5	NC	E2	TXCMP	L14	NC	A2	VSS	H8
NC	C6	NC	F3	NC	R3	NC	B14	VSS	H9
NC	C9	NC	D3	NC	G1	TXP	B10	VSS	H10
NC	C11	NC	E3	TXD8	D13	NC	B6	VSS	H11
NC	C13	NC	E4	TXD9	C14	NC	B2	VSS	J2
NC	D6	NC	F4	TXD10	E16	VDD12	J14	VSS	J7
NC	D10	NC	C2	TXD11	D14	VDD12	K4	VSS	J8
NC	D11	RXDK1	E17	TXD12	D15	VDD18	C4	VSS	J9
NC	D12	RXDK0	N15	TXD13	E14	VDD18	C10	VSS	J10
NC	K17	NC	T1	TXD14	C16	VDD18	C12	VSS	J11
OPMODE0	R9	NC	E1	TXD15	C17	VDD18	D7	VSS	J15
OPMODE1	U10	NC	T13	TXD0	L17	VDD18	H17	VSS	K7
OSC25MO	C1	RXIDLE	T12	TXD1	L16	VDD18	J17	VSS	K8
OSC25MI	D1	NC	T8	TXD2	K14	VDD18	L4	VSS	K9

PCLK	T14	NC	P8	TXD3	M16	VDD18	M3	VSS	K10
PD0	T11	NC	A16	TXD4	M15	VDD18	T6	VSS	K11
PD1	P10	RXN	A12	TXD5	N17	VDD25	D2	VSS	L1
PHYSTS	U5	NC	A8	TXD6	L15	VDD25	D16	VSS	L2
REFCLKN	B1	NC	A4	TXD7	N16	VDD25	F17	VSS	L7
REFCLKP	A1	NC	B16	NC	U4	VDD25	G2	VSS	L8
RST_N	U12	RXP	B12	NC	R6	VDD25	K1	VSS	L9
RTERM	D8	NC	B8	NC	T4	VDD25	K15	VSS	L10
RXD8	F16	NC	B4	NC	P6	VDD25	P1	VSS	L11
RXD9	G15	NC	U15	NC	U2	VDD25	R13	VSS	M1
RXD10	G16	RXPLR	U13	NC	R5	VDD25	R17	VSS	M17
RXD11	H15	NC	T9	NC	T3	VDD25	T2	VSS	N2
RXD12	G17	NC	R8	NC	R4	VDD25	T5	VSS	P9
RXD13	H14	NC	F14	NC	K2	VDD25	U9	VSS	P16
RXD14	J16	NC	G14	NC	K3	VDD25	U17	VSS	R7
RXD15	H16	NC	D17	NC	J1	VDDPLL	C8	VSS	T15
RXD0	R16	RXSTS0	P17	NC	J4	VDDRX	A17	VSS	U1
RXD1	P15	RXSTS1	M14	NC	H1	VDDRX	A13	VSS	U3
RXD2	T16	RXSTS2	T17	NC	J3	VDDRX	A9	VSS	U14
RXD3	N14	NC	P5	NC	H2	VDDRX	A5	VSSGR	C15
RXD4	R15	NC	R2	NC	H3	VDDTX	A15	VSSPLL	D9
RXD5	P14	NC	P4	TXDET/LPBK	R11	VDDTX	A11	VSSRX	B17
RXD6	U16	NC	H4	TXDK1	E15	VDDTX	A7	VSSRX	B13
RXD7	P13	NC	F2	TXDK0	K16	VDDTX	A3	VSSRX	B9
NC	N4	NC	G3	NC	P7	VSS	D4	VSSRX	B5
NC	P2	NC	P12	NC	L3	VSS	D5	VSSTX	B15
NC	P3	RXVLD	P11	NC	R14	VSS	F1	VSSTX	B11
NC	R1	NC	U7	TXIDLE	R12	VSS	G7	VSSTX	B7
NC	M4	NC	U6	NC	U8	VSS	G8	VSSTX	C7
NC	N1	SCC	R10	NC	T7	VSS	G9	VSSTX	B3
NC	N3	TESTC	U11	NC	A14	VSS	G10		
NC	M2	TESTD	T10	TXN	A10	VSS	G11		

3.4 Pin Descriptions

Table 3.4 - Pin Descriptions

PIPE Interface				
Pin Name	**I/O Standard**	**Pin#**	**Type**	**Description**
RST_N	LVCMOS2	U12	I	Global reset
PCLK	SSTL2_I	T14	O	Parallel interface clock All data movement across the parallel interface is synchronous to this clock. 1. For 8-bit mode: PCLK operates at 250 MHz and is applied to synchronize all TXD, RXD data bus and all commands. 2. For 16-bit mode: PCLK operates at 125 MHz and is applied to synchronize all TXD, RXD data bus and all commands. 3. For 10-bit mode(TBC): PCLK operates at 250 MHz and is applied to synchronize the TXD data bus and all commands.
RXSTS[2:0]	SSTL2_I	T17, M14, P17	O	1. For 8-bit and 16-bit modes: Encodes receiver status and error codes for the received data stream and receiver detection 000 Received data OK 001 1 SKP added 010 1 SKP removed 011 Receiver detected 100 8B/10B decode error 101 Elastic Buffer overflow 110 Elastic Buffer underflow 111 Receiver disparity error 2. For 10-bit modes: RXSTS[2]: RBC, synchronize the RXD data bus RXSTS[1]: RXPRSNT, report the result of receiver detection RXSTS[0]: RXD9, bit 9 of RXD data bus
RXIDLE	LVCMOS2	T12	O	Indicates receiver detection of an electrical idle This is an asynchronous signal.
PHYSTS	SSTL2_I	U5	O	Used to communicate completion of several PHY functions including power state transitions and receiver detection
RXVLD	LVCMOS2	P11	O	Indicates symbol lock and valid data on RXDx and RXDKx
TXCMP	SSTL2_I	L14	I	1. For 8-bit and 16-bit modes: Sets the running disparity to negative 2. For 10-bit mode: TXD9, bit 9 of TXD data bus
TXIDLE	LVCMOS2	R12	I	Forces Tx output to electrical idle

RXDK[1:0]	SSTL2_I	E17, N15	O	1. For 8-bit and 16-bit modes: K-code indication for the received symbols In 8-bit mode, RXDK = RXDK0 In 16-bit mode, RXDK = {RXDK1, RXDK0} 2. For 10-bit mode: RXDK[0]: RXD8, bit 8 of RXD data bus
RXD[15:0]	SSTL2_I	H16, J16, H14, G17, H15, G16, G15, F16, P13, U16, P14, R15, N14, T16, P15, R16	O	RXD[7:0]: Parallel data output bus for all 8-bit, 16-bit and 10-bit modes RXD[15:0]: Parallel data output bus for 16-bit mode only
TXDK[1:0]	SSTL2_I	E15, K16	I	1. For 8-bit and 16-bit modes: K-code indication for the transmitted symbols In 8-bit mode, TXDK = TXDK0 In 16-bit mode, TXDK = {TXDK1, TXDK0} 2. For 10-bit mode: TXDK[0]: TXD8, bit 8 of TXD data bus
TXD[15:0]	SSTL2_I	C17, C16, E14, D15, D14, E16, C14, D13, N16, L15, N17, M15, M16, K14, L16, L17	I	TXD[7:0]: Parallel data input bus for all 8-bit, 16-bit and 10-bit modes TXD[15:0]: Parallel data input bus for 16-bit mode only
TXDET/LPBK	LVCMOS2	R11	I	Receiver detection/Loopback
PD[1:0]	LVCMOS2	P10, T11	I	Sets the power states 00 P0, normal operation 01 P0s, low recovery time latency, power saving state 10 P1, longer recovery time(64us max) latency, lower power state 11 P2, lowest power state
RXPLR	LVCMOS2	U13	I	Inverts the polarity on the RXP/RXN

Power and Ground Signals			
Pin Name	**Pin#**	**Type**	**Description**
VDD25	D2, D16, F17, G2, K1, K15, P1, R13, R17, T2, T5, U9, U17	P	2.5V Power Supplies for general I/O
VDD18	C4, C10, C12, D7, H17, J17, L4, M3, T6	P	1.8V Power Supplies for core and bias voltage
VDD12	J14, K4	P	1.25V Reference Voltage for high speed I/O
VSS	D4, D5, F1, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J2, J7, J8, J9, J10, J11, J15, K7, K8, K9, K10, K11, L1, L2, L7, L8, L9, L10, L11, M1, M17, N2, P9, P16, R7, T15, U1, U3, U14	P	Digital ground
VDDPLL	C8	P	1.8V Power Supplies for internal PLL
VSSPLL	D9	P	Ground for internal PLL
VDDRX VSSRX	A17, A13, A9, A5 B17, B13, B9, B5	P	1.8V Power Supplies for receiver part
VDDTX VSSTX	A15, A11, A7, A3 B15, B11, B7, C7, B3	P	1.8V Power Supplies for transceiver part

VSSGR	C15	P	Ground for the guard ring of the SerDes block

Serial Signals			
Pin Name	**Pin#**	**Type**	**Description**
RXN	A12	I	Received serial input, complement
RXP	B12	I	Received serial input, true
RTERM	D8	I	Connects an external 5.1KΩ resistor to ground for calibrating the on-chip termination resistors
TXN	A10	O	Transmitted serial output, complement
TXP	B10	O	Transmitted serial output, true

Other Signals				
Pin Name	**I/O Standard**	**Pin#**	**Type**	**Description**
REFCLKP	Analogue	A1	I	Reference clock signal
REFCLKN	Analogue	B1	I	Reference clock signal
OSC25MO	Crystal	C1	O	Connect to 25MHz crystal when using crystal as the reference clock source
OSC25MI	Crystal/ Oscillator	D1	I	Connect to 25MHz crystal/oscillator when using crystal/oscillator as the reference clock source
TESTC/SMC	LVCMOS2	U11	I	Test clock/SMBus clock
TESTD/SMD	LVCMOS2	T10	I/O	Test data/SMBus data
SCC	LVCMOS2	R10	I	Configures clock input source When SCC=1, the chip clock sources from a pair of differential signals, REFCLKP and REFCLKN, with a nominal frequency of 100 MHz. When SCC=0, the chip clock sources from a crystal at 25MHz.
OPMODE[1:0]	LVCMOS2	U10, R9	I	Operational Mode of the GL9711 00 8-bit mode 01 16-bit mode 10 10-bit mode 11 Internal use only
NC	-	A2, A4, A6, A8, A14, A16, B2, B4, B6, B8, B14, B16, C2, C3, C5, C6, C9, C11, C13, D3, D6, D10, D11, D12, D17, E1, E2, E3, E4, F2, F3, F4, F14, F15, G1, G3, G4, G14, H1, H2, H3, H4, J1, J3, J4, K2, K3, K17, L3,	-	No connection

		M2, M4, N1, N3, N4, P2, P3, P4, P5, P6, P7, P8, P12, R1, R2, R3, R4, R5, R6, R8, R14, T1, T3, T4, T7, T8, T9, T13, U2, U4, U6, U7, U8, U15		

Note: ”NC” pins should be left open on circuit board.

Table 3.5 - Parameter of Buffer I/O

Buffer type	V_{IH} (Input High Voltage, V)			V_{IL} (Input Low Voltage, V)			V_{OH} (Output High Voltage, V)			V_{OL} (Output Low Voltage, V)		
	Min	Norm	Max	Min	Norm	Max	Min	Norm	Max	Min	Norm	Max
LVCMOS2	1.7	-	-	-	-	0.7	2.4	-	-	-	-	0.4
SSTL2	1.57	-	-	-	-	0.93	1.76	-	-	-	-	0.74

CHAPTER 4 REGISTERS

There are some registers built-in the GL9711 for test purpose. These registers can be accessed through a serial bus interface using pin TESTC and TESTD. Registers at Offset 05h ~ 0Bh are for internal test only. Please be careful to leave them as default values.

4.1 Registers Base Address

Table 4.1 - Base Address for Registers

Mnemonic	Offset	Description	Default
REVID	00h	Revision ID and Auto-calibration Result Register	8'bxxxx1xxx
XCVROPT	01h	Transceiver Option Register	8'hE9
LPBKTEST	02h	BIST and Beacon/Test Data Pattern Register, Part 1	8'h00
BCNPAT2	03h	Beacon/Test Data Pattern Register, Part 2	8'h03
BCNPAT3	04h	Beacon/Test Data Pattern Register, Part 3	8'hFF
-	05h	For internal test only	-
-	06h	For internal test only	-
-	07h	For internal test only	-
-	08h	For internal test only	-
-	09h	For internal test only	-
-	0Ah	For internal test only	-
-	0Bh	For internal test only	-
BT	0Ch	Buffer Test Register	8'h00
SLCDT	0Dh	Serial Loopback and Comma Detect Test Register	8'h00

Notation:

R/W	Read / Write
R/O	Read Only
W/O	Write Only
R/W1C	Read / Write "1" to Clear
R/W/C	Read / Write and hardware automatic Clear

4.2 Registers Descriptions

Offset 00h – REVID ……..…… Default value = 8'bxxxx1xxx

REV3	REV2	REV1	REV0	BY1	RCAL0	RCAL1	RCAL2
R	R	R	R	R	R	R	R

7-4 REV[3:0] Chip revision code
3 BY1 x1 package
2-0 RCAL[0:2] Calibration result of on-chip termination resistors

Offset 01h – XCVROPT ……..……. Default value = 8'hE9

SW1	SW0	DEM1	DEM0	BW0	BW1	RDEF	FEVAL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 SW[1:0] Swing control of transmitter output
Output Swing (Differential, peak-to-peak)
00 0.6V
01 0.8V
10 1.0V
11 1.2V

5-4 DEM[1:0] De-emphasis control of transmitter output
Amount of De-emphasis
00 No de-emphasis
01 -1.6dB
10 -3.5dB
11 -6.0dB

3-2 BW[0:1] Bandwidth control of clock recovery circuit
Relative Bandwidth
00 1
01 2
10 4
11 Reserved

1 RDEF Disable calibration of on-chip termination resistors and leave the resistors to their default value

0 FEVAL Force calibration of on-chip termination resistors
When **RDEF**=0, writing a one to this bit will make the resistors re-calibrated. This bit is auto-cleared and always read as zero.

Offset 02h – LPBKTEST ……..……. Default value = 8'h00

BIST0	BIST1	BIST2	--	BCN19	BCN18	BCN17	BCN16
R/W	R/W	R/W	--	R/W	R/W	R/W	R/W

7-5 BIST[0:2] Select of built-in test pattern

Bit	Pattern	
00x	BIST disabled	
100	0000000000	0000000000
010	1111111111	1111111111
110	0101010101	0101010101
101	0011111010	1010101010
	1100000101	0101010101
011	0011111010	1010**0***01010
	1100000101	0101**1***10101
111	PRBS pattern	

It should be noted that the expected pattern while BIST[0:2]=011 is the same as BIST[0:2]=101. But when coming out of the transmitter, the two bits with "*****" in BIST[0:2]=011 are different from BIST[0:2]=101. As a result, even when there is no bit error, there will be bit errors intentionally introduced to verify the BIST circuit is functional.

4 RESERVED -

3-0 BCN[19:16] Data pattern for beacon and **TXTEST**

Offset 03h – BCNPAT2 ……. Default value = 8'h03

BCN15	BCN14	BCN13	BCN12	BCN11	BCN10	BCN9	BCN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BCN[15:8] Data pattern for beacon and **TXTEST**

Offset 04h – BCNPAT3 ……. Default value = 8'hFF

BCN7	BCN6	BCN5	BCN4	BCN3	BCN2	BCN1	BCN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BCN[7:0] Data pattern for beacon and **TXTEST**

Offset 0Ch – BT ……..……..……. Default value = 8'h00

--	--	DDR	REN	TXTEST	PLPBK	SKPDEL	SKPADD
--	--	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -

5 DDR Enable DDR at PIPE interface and make PCLK = 125MHz @ 8/10-bit mode

4 REN Enable terminator for REFCLKP/N

3 TXTEST Enable transmitter test with data pattern BCN[19:0], which are programmed in REG02h, 03h and 04h

2 PLPBK Enable parallel loopback of PCS

1	**SKPDEL**	Enable SKP deleting test of SKP ordered sets
0	**SKPADD**	Enable SKP adding test of SKP ordered sets

Offset 0Dh – SLCDT ……...……...……. Default value = 8'h00

--	SLPBK	--	--	--	FENCD	--	--
--	R/W	--	--	--	R/W	--	--

7	**RESERVED**	-
6	**SLPBK**	Enable serial loopback
5-3	**RESERVED**	-
2	**FENCD**	Force comma detect
1-0	**RESERVED**	-

4.3 SMBus Protocal

GL9711 registers are programmed by System Management Bus (SMBus). Fig. 4.1 shows the SMBus topology. The V_{DD} power is 2.5V +/- 10% and the pull up resistor is 1KΩ. Both SMBCLK and SMBDAT lines are bi-directional, connected to 2.5V supply voltage through a pull-up resistor. The operating frequency is 10~100KHz and the SMBus address of GL9711 is 7'h2C.

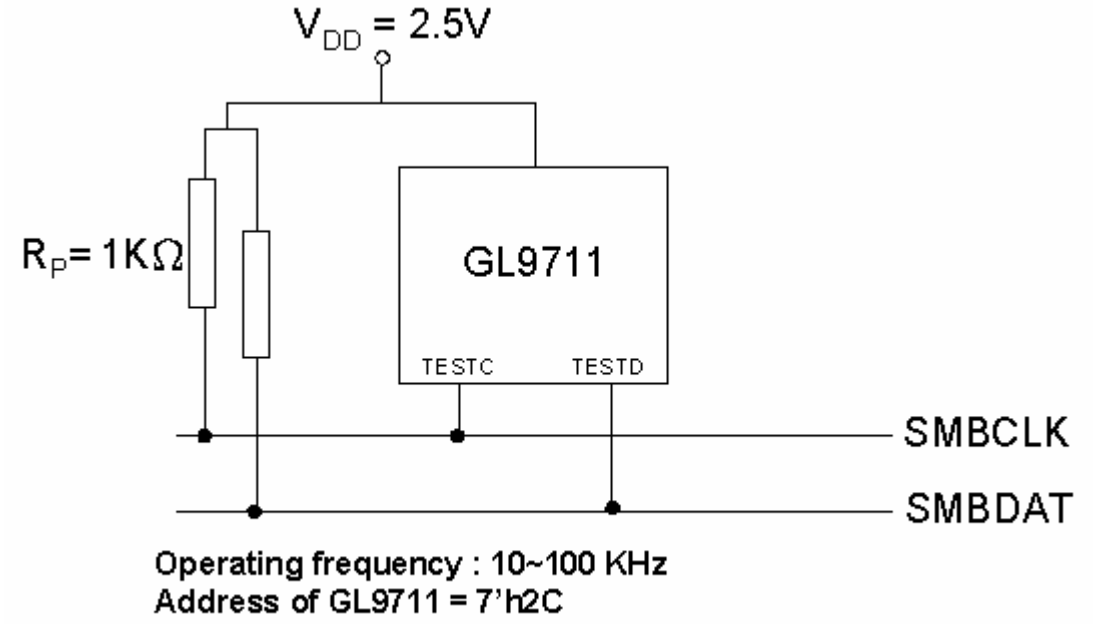


Figure 4.1 – SMBus Topology of GL9711

SMBus uses fixed voltage levels to define the logic “ZERO” and logic “ONE” on the bus respectively. The data on SMBDAT must be stable during the “HIGH” period of the clock. Data can change state only when SMBCLK is low. Fig. 4.2 illustrates the relationships.

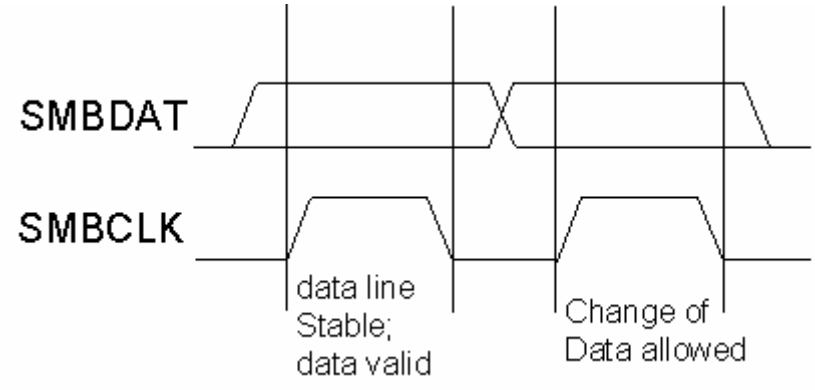


Figure 4.2 – Data Validity

Two unique bus situations define a message START and STOP condition.
1. A HIGH to Low transition of the SMBDAT line while SMBCLK is HIGH indicates a message START condition.
2. A LOW to HIGH transition of the SMBDAT line while SMBCLK is HIGH defines a message STOP condition.

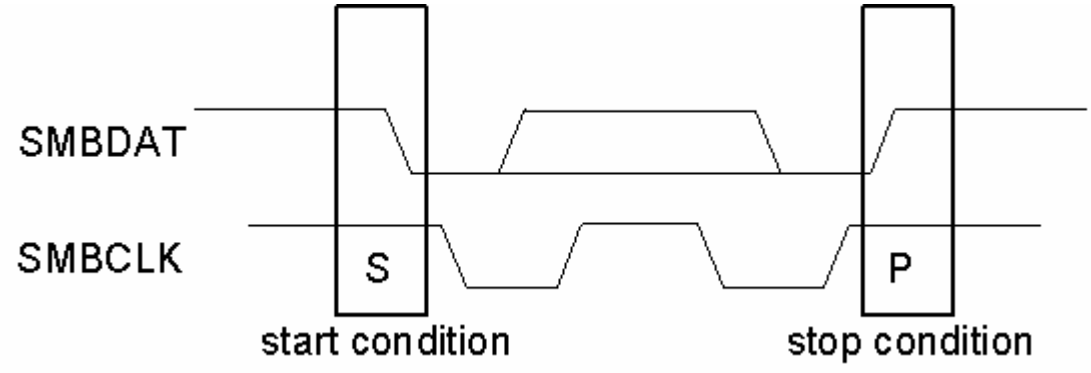


Figure 4.3 – START and STOP Condition

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an acknowledge bit. Bytes are transferred with the most significant bit (MSB) first. Fig. 4.4 illustrates the positioning of acknowledge (ACK) and not acknowledge (NACK) pulses relative to other data.

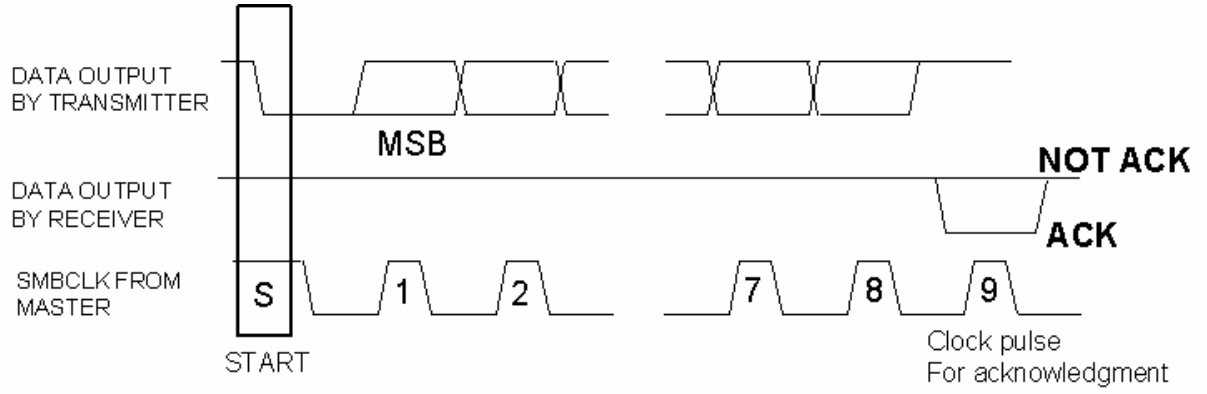


Figure 4.4 – ACK and NACK Signaling of SMBus

Below is a key to the protocol diagrams.

S	Start Condition
Sr	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
x	Shown under a field indicates that that field is required to have the value of ‘x’
A	Acknowledge (this bit position may be ‘0’ for an ACK or ‘1’ for a NACK)
P	Stop Condition
☐	Master-to-GL9711
■	GL9711-to-Master

Figure 4.5 – SMBus Packet Protocol Diagram Element Key

The first byte of a Write Byte access is the command code. The next one byte is the data to be written. In this example the master asserts GL9711's address followed by the write bit. GL9711 acknowledges and the master delivers the command code. GL9711 again acknowledges before the master sends the data byte. GL9711 acknowledges the data byte, and the entire transaction is finished with a STOP condition.

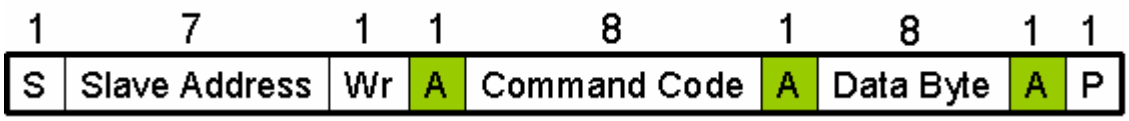


Figure 4.6 – Write Byte Protocol

Reading data is slightly more complicated than writing data. First the host must write a command to GL9711. Then it must follow that command with a repeated START condition to denote a read from GL9711's address. GL9711 then returns one byte of data.
Note that there is no STOP condition before the repeated START condition, and that a NACK signified the end of the read transfer.

Figure 4.7 – Read Byte Protocol

GL9711 requires a minimum time (16us) to reach the steady state after power on. So the master must start programming at least 16us later after power on.

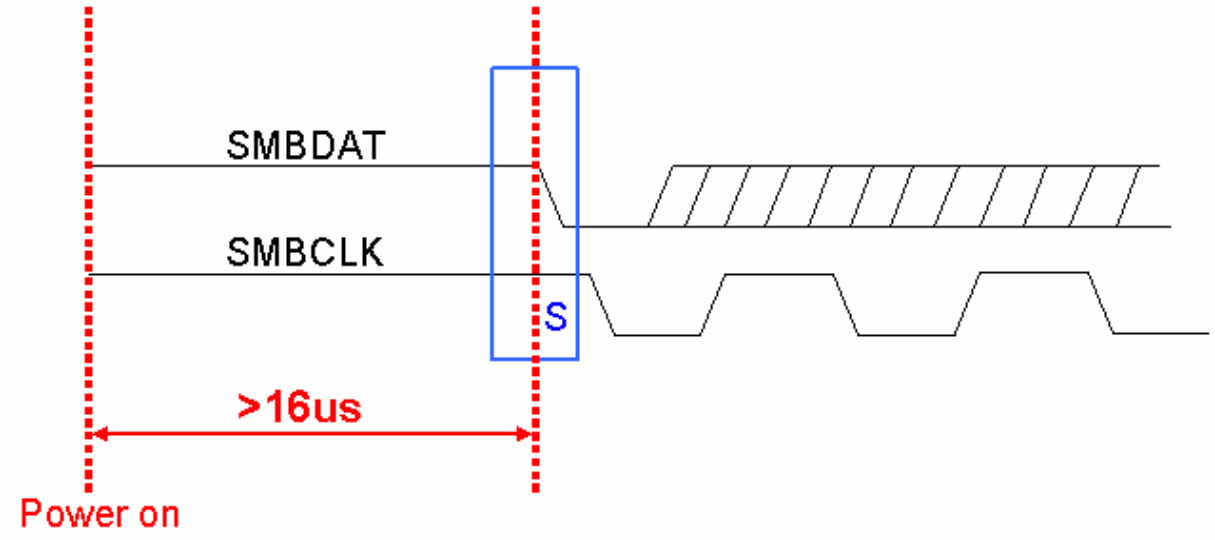


Figure 4.8 – The Minimum Wait Time from Power on to Programming Registers

CHAPTER 5 BLOCK DIAGRAM

5.1 Simplified Diagram

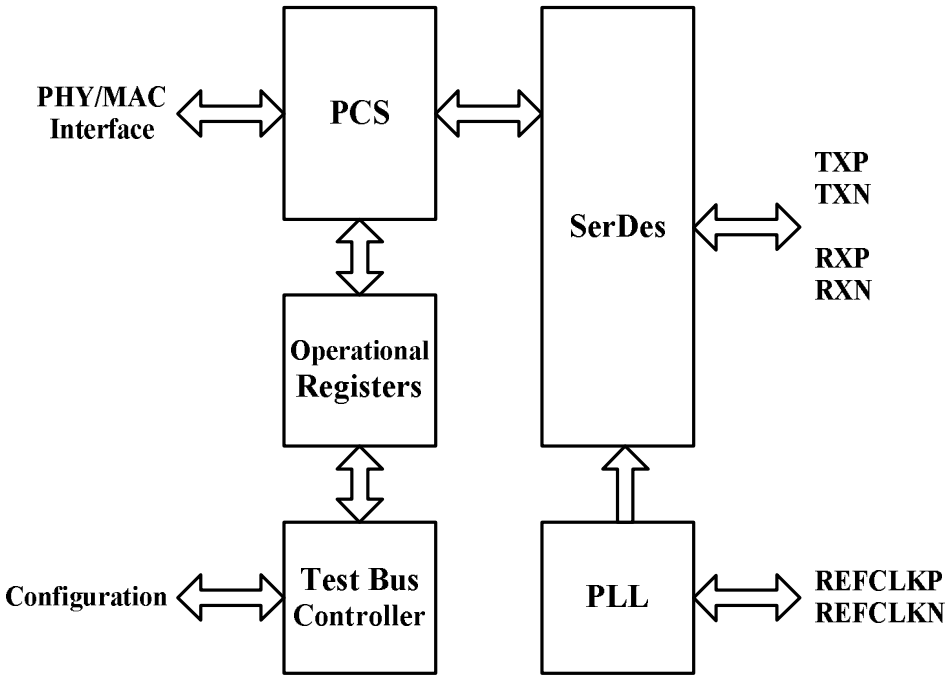


Figure 5.1 - Simplified Diagram

5.2 Transmitter Data Path Per Lane

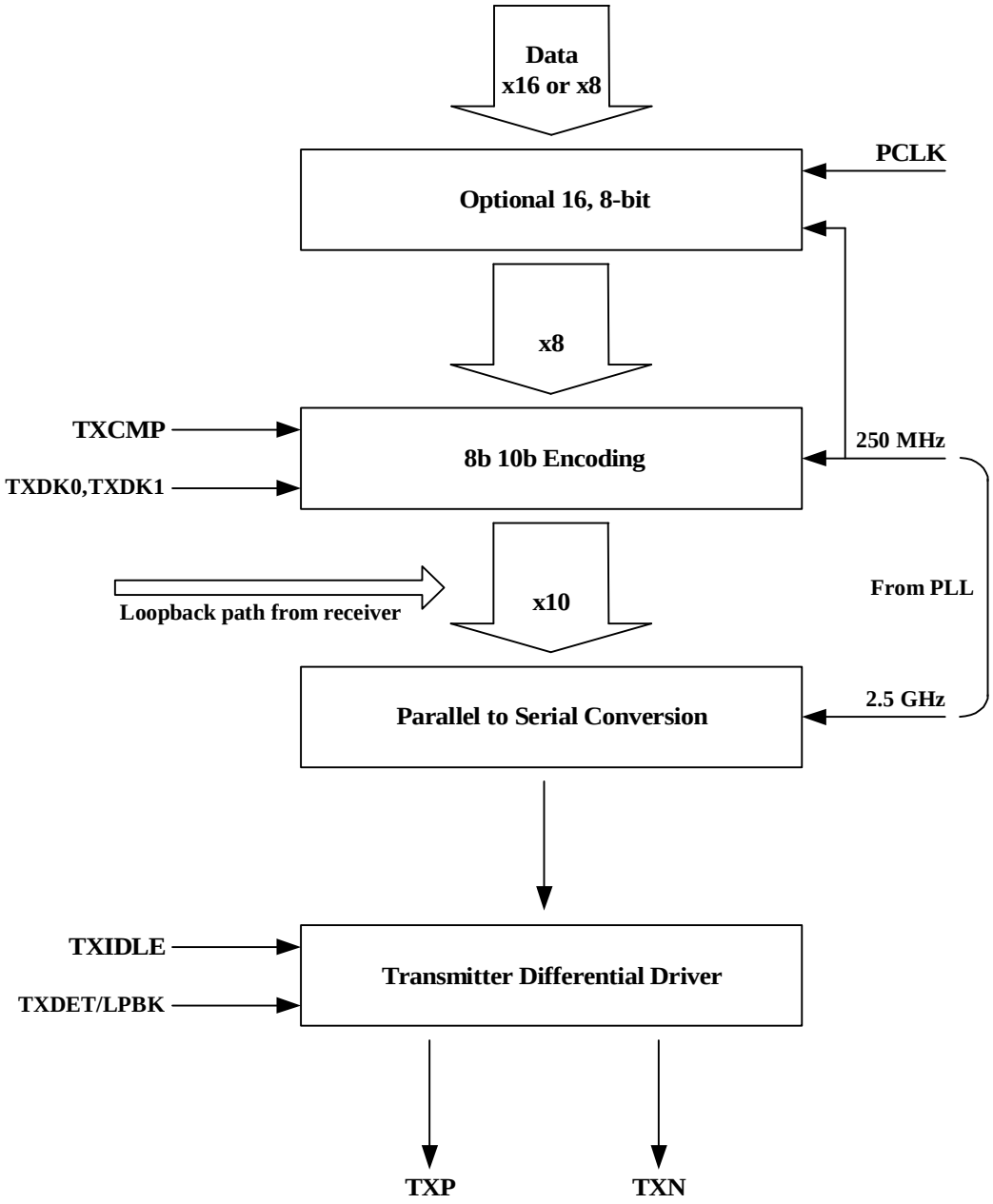


Figure 5.2 - Transmitter Data Path per Lane

5.3 Receiver Data Path Per Lane

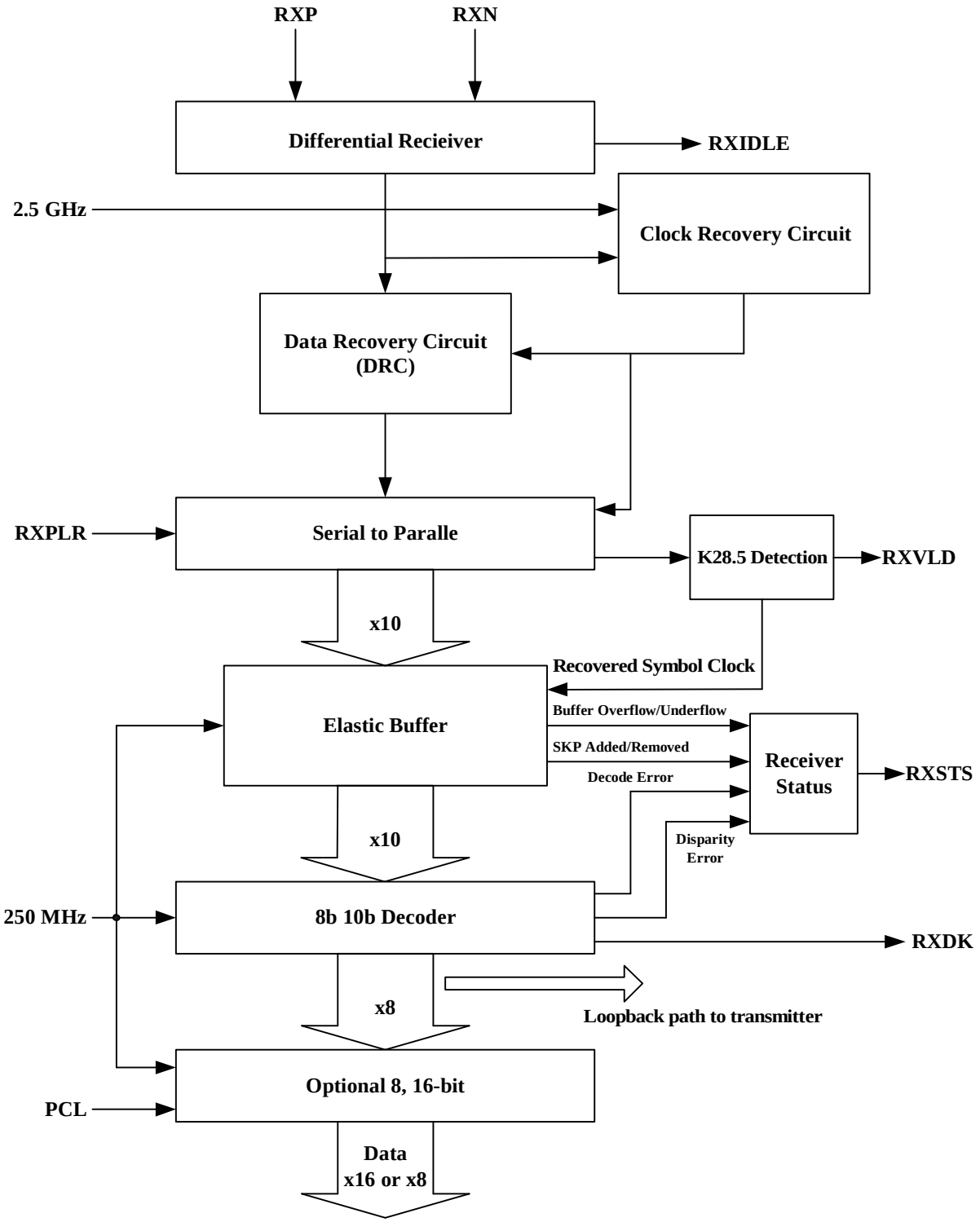


Figure 5.3 - Receiver Data Path per Lane

CHAPTER 6 FUNCTION DESCRIPTION

6.1 Clock and Reset

The clock source of the GL9711 comes externally from either the 100 MHz differential clock pair or the 25MHz crystal, which is selectable by pin SCC. The GL9711 uses the clock source with its PLL to generate the 2.5 GHz bit rate for transmitting and receiving.

The GL9711 also drives a clock output for the synchronization of MAC interface. Since the MAC interface can be configured to 8-bit, 16-bit and 10-bit mode, the clock, PCLK, runs at 250 MHz for 8-bit mode and 125 MHz for 16-bit mode. The MAC should use the rising edge of the clock to send and receive parallel data.

To initialize the GL9711, the MAC should assert the reset of the GL9711 to low. While the reset is asserted, the MAC should also make TXDET/LPBK deasserted, TXIDLE asserted, TXCMP deasserted, RXPLR deasserted and PD[1:0] = P1. When the GL9711 senses its reset asserted, it will drive its PHYSTS high immediately. After the reset deasserted, the GL9711 requires typically 16.7us for internal PLL stable and then transitions its PHYSTS to low. When MAC deasserts the reset, it should monitor the state of PHYSTS to make sure the GL9711 is ready for normal operation.

6.2 Receiver Detection

The receiver detection can only be performed while the GL9711 is in P1 state. To instruct the GL9711 to enter a receiver detection sequence, the MAC asserts TXDET/LPBK and hold it asserted until the GL9711 asserts PHYSTS for response. While finishing the receiver detection, the GL9711 will assert PHYSTS and present a appropriate value to RXSTS[2:0] to signal a detection completion. When the MAC detects PHYSTS asserted, it knows the detection result from RXSTS[2:0] and can deassert TXDET/LPBK.

6.3 Beacon Transmitting and Detection

Beacon transmitting is required for the GL9711 in P2 state to wake up the receiver in the other side of the link. When the GL9711 is in P2 state, the MAC can deassert TXIDLE to instruct the GL9711 to repeatedly transmit a beacon.

For the beacon receiving side, if the GL9711 receives a beacon, it will transition RXIDLE to low to indicate an exit from electrical idle. When the GL9711 is in P2 state and MAC senses the RXIDLE transitioned from high to low, it knows a beacon has been detected.

6.4 Receiver Status Report

- **Add and Remove a SKP**
  The GL9711 implements an elastic buffer to compensate the clock rate difference between the recovery clock and its transmit clock. While receiving a SKP ordered-set, compliant to PCI Express Base specification REV. 1.0a, the GL9711 can insert or remove one SKP symbol in the SKP ordered-set to avoid the buffer overrun or underrun. Whenever adding or removing a SKP symbol, the GL9711 will signal PHYSTS and corresponding RXSTS[2:0] to MAC.

SKP Ordered-Set Received	RXSTS Code
Add a SKP	001b
Remove a SKP	010b

- **Receiver Detected**

Detected Result	RXSTS code
Receiver not present	000b
Receiver present	011b

- **8B/10B Decode Error**
  When the GL9711 decodes the received 10-bit symbol and detects an error code which does not correspond to any valid data, it will replace the code with an EDB symbol, assert PHYSTS and encode RXSTS[2:0] with the values of decode error status, 3'b100.

- **Elastic Buffer Overrun and Underrun**
  When the overrun or underrun of the elastic buffer occurs, the GL9711 will assert PHYSTS and encode RXSTS[2:0] with the values of decode error status.

Elastic Buffer	RXSTS Code
Overrun	101b
Underrun	110b

  In the case of elastic buffer overrun, the GL9711 drops the symbol. For the elastic buffer underrun, the GL9711 inserts the EDB symbol. The PHYSTS and RXSTS[2:0] are presented on the MAC interface during the clock cycle where GL9711 drops or inserts the symbol.

- **Disparity Errors**
  To report a disparity error detected, the GL9711 asserts PHYSTS and encodes RXSTS[2:0] with the values of decode error status, 3'b111.

6.5 Loopback

The GL9711 supports a Loopback mode to re-transmit its received data. When the MAC sets the GL9711 in P0 state and asserts TXDET/LPBK, the GL9711 enters a Loopback. In Loopback, the GL9711 transmits data from it received data instead of MAC interface. Meanwhile, it presents the received data on the MAC interface as normal operation.

When set into Loopback mode and acting as a Loopback slave according to the PCI Express Base Specification Rev. 1.0a, the GL9711 received data from the Loopback master. If the master intends to end the Loopback, it sends an electrical idle ordered-set to the GL9711. When the MAC detects the electrical idle ordered-set, it de-asserts TXDET/LPBK and asserts TXIDLE to instruct the GL9711 to stop Loopback. The MAC should take care the GL9711 has retransmit at least three bytes of the electrical idle before it makes the GL9711's transmitter into electrical idle.

6.6 Polarity Inversion

The GL9711 supports lane polarity inversion. While pin RXPLR asserted, the GL9711 inverts its received data on the MAC interface.

6.7 Setting Negative Disparity

To set the running disparity to negative, the MAC asserts TXCMP for one PCLK cycle that matches with the data that is to be transmitted where running disparity is negative.

6.8 Behavior Summary

PD[1:0]	TXDET/LPBK	TXIDLEx	Behavior
P0	0	0	GL9711 is transmitting data from MAC interface normally.
	0	1	GL9711 is not transmitting and is in electrical idle.
	1	0	GL9711 enters Loopback mode.
	1	1	Illegal
P0S	X	0	Illegal
	X	1	GL9711 is not transmitting and is in electrical idle.
P1	X	0	Illegal
	0	1	GL9711 is idle.
	1	1	GL9711 performs a receiver detection.
P2	X	0	GL9711 transmits a beacon.
	X	1	GL9711 is idle.

6.9 Power Saving Support

The GL9711 supports four power states including P0, P0s, P1 and P2 and can be controlled to perform Active State Power Management on a PCI Express link. P0 is the normal operational state where data and control packets can be transmitted and received. When directed from P0 to a lower power state, the GL9711 can immediately take appropriate power saving actions. The power saving scheme of the GL9711 for various power down states is listed in the table below.

PD[1:0]	Transmitter	Receiver	PLL	PCLK Output
P0	On	On	On	On
P0s	High-impedance Electrical Idle	On	On	On
P1	High-impedance Electrical Idle	Off but exit from Electrical Idle is detectable	On	On
P2	High-impedance Electrical Idle (Capable of transmitting a Beacon)	Off but exit from Electrical Idle is detectable	Off	Off

6.10 Operation Mode and Multi-Functional Pins

There are four modes for GL9711 operation which is selected by pin OPMODE[1:0].

Mode	[1]	[0]	Description
1	0	0	8 bit mode
2	0	1	16 bit mode
3	1	0	10 bit mode
4	1	1	Internal use only

Mode 1: The GL9711 is configured into 8-bit parallel bus.
The parallel bus is synchronous with PCLK at 250 MHz.

Mode 2: The GL9711 acts as a 1-lane PHY with a 16-bit parallel interface at 125 MHz.

Mode 3: The GL9711 is configured as a SerDes with 10-bit parallel bus.

Mode 4: For internal use only

Table 6.1 - Pin Functions

Pin Number	Mode 1	Mode 2	Mode 3
T14	PCLK(O)	PCLK(O)	TBC(O)
C17		TXD15(I)	
C16		TXD14(I)	
E14		TXD13(I)	
D15		TXD12(I)	
D14		TXD11(I)	
E16		TXD10(I)	
C14		TXD9(I)	
D13		TXD8(I)	
N16	TXD7(I)	TXD7(I)	TXD7(I)
L15	TXD6(I)	TXD6(I)	TXD6(I)
N17	TXD5(I)	TXD5(I)	TXD5(I)
M15	TXD4(I)	TXD4(I)	TXD4(I)
M16	TXD3(I)	TXD3(I)	TXD3(I)
K14	TXD2(I)	TXD2(I)	TXD2(I)
L16	TXD1(I)	TXD1(I)	TXD1(I)
L17	TXD0(I)	TXD0(I)	TXD0(I)
E15		TXDK1(I)	
K16	TXDK(I)	TXDK0(I)	TXD8(I)
R12	TXIDLE(I)	TXIDLE(I)	TXIDLE(I)
L14	TXCMP(I)	TXCMP(I)	TXD9(I)
U13	RXPLR(I)	RXPLR(I)	RXPLR(I)
H16		RXD15(O)	
J16		RXD14(O)	
H14		RXD13(O)	
G17		RXD12(O)	
H15		RXD11(O)	

G16		RXD10(O)	
G15		RXD9(O)	
F16		RXD8(O)	
P13	RXD7(O)	RXD7(O)	RXD7(O)
U16	RXD6(O)	RXD6(O)	RXD6(O)
P14	RXD5(O)	RXD5(O)	RXD5(O)
R15	RXD4(O)	RXD4(O)	RXD4(O)
N14	RXD3(O)	RXD3(O)	RXD3(O)
T16	RXD2(O)	RXD2(O)	RXD2(O)
P15	RXD1(O)	RXD1(O)	RXD1(O)
R16	RXD0(O)	RXD0(O)	RXD0(O)
E17		RXDK1(O)	
N15	RXDK(O)	RXDK0(O)	RXD8(O)
P11	RXVLD(O)	RXVLD(O)	RXVLD(O)
T17	RXSTS2(O)	RXSTS2(O)	RBC(O)
M14	RXSTS1(O)	RXSTS1(O)	RXPRSNT(O)
P17	RXSTS0(O)	RXSTS0(O)	RXD9(O)
U5	PHYSTS(O)	PHYSTS(O)	PHYSTS(O)
T12	RXIDLE(O)	RXIDLE(O)	RXIDLE(O)

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 DC Voltage Specifications

Table 7.1 - DC Voltage Specifications

Symbol	Parameter	Min	Typ	Max	Unit
VDD25	PHY Interface Voltage	2.375	2.5	2.625	V
VDD18	Core Voltage	1.71	1.8	1.89	V
VDD12	Reference Voltage for PHY Inerface	1.1875	1.25	1.3125	V
VDDTX	Voltage for Transmitters	1.71	1.8	1.89	V
VDDRX	Voltage for Receivers	1.71	1.8	1.89	V
VDDPLL	Voltage for PLL	1.71	1.8	1.89	V

7.2 Transmit and Receive Latency Time

Table 7.2 - Transmit and Receive Latency Time

Symbol	Parameter	Min	Typ	Max	Unit
T_{TX-LAT}	Transmit Latency, time for data moving from MAC interface (PCLK rising edge) to TX serial lines (the first bit of 10-bit symbol)	25	-	30	ns
T_{RX-LAT}	Receive Latency, time for data moving from RX serial lines (the first bit of 10-bit symbol) to MAC interface (PCLK rising edge)	48	-	54	ns

7.3 Transition Time of Power State

Table 7.3 – Transition Time of Power State

Symbol	Parameter	Min	Typ	Max	Unit
T_{P0S-P0}	Time for PHY to return to P0, after having been in P0s. Time is measured when PD[1:0] are set to P0 until the PHY asserts PHYSTS	52	-	74	ns
T_{P1-P0}	Time for PHY to return to P0, after having been in P1. Time is measured when PD[1:0] are set to P0 until the PHY asserts PHYSTS	52	-	74	ns
T_{P2-P1}	Time for PHY to return to P1, after having been in P2. Time is measured when PD[1:0] are set to P1 until the PHY asserts PHYSTS	16	-	17	µs
T_{P0-P0S}	Time for PHY to return to P0s, after having been in P0. Time is measured when PD[1:0] are set to P0s until the PHY asserts PHYSTS	52	-	74	ns
T_{P0-P1}	Time for PHY to return to P1, after having been in P0. Time is measured when PD[1:0] are set to P1 until the PHY asserts PHYSTS	52	-	74	ns
T_{P0-P2}	Time for PHY to return to P2, after having been in P0. Time is measured when PD[1:0] are set to P2 until the PHY asserts PHYSTS	16	-	17	µs

7.4 Power Consumption

l Power Consumption

Table 7.4 - Power Consumption of Each Power State in Different Operation Mode

Current at 2.5V (mA)	Current at Analogue 1.8V (mA)	Current at Digital 1.8V (mA)	Operation Condition	Power State	Operation Mode	Power Consumption (mW)
59	90	57	All on	P0	16-bit @125MHz PCLK	412.1
12	71	49	PLL on TX idle RX on	P0s	16-bit @125MHz PCLK	246
12	64	38	PLL on TX idle RX idle	P1	16-bit @125MHz PCLK	213.6
6	36	6	PLL off TX idle RX idle	P2	16-bit @3.13MHz PCLK	90.6

7.5 Differential Transmitter and Receiver Serial Output

l Transmitter Serial Output

Table 7.5 – Transmitter Serial Output

Symbol	Parameter	Min	Typ	Max	Unit
UI	Unit interval	399.88	400	400.12	ps
$V_{TX\text{-}DIFFp\text{-}p}$	Differential peak to peak output voltage	0.8	-	1.2	UI
$V_{TX\text{-}DE\text{-}RATIO}$	De-emphasized differential output voltage (Ratio)	-3.0	-3.5	-4.0	dB
$T_{TX\text{-}EYE}$	Minimum TX eye width	0.7	-	-	UI
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.15	UI
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	D+/D- TX output rise/fall time	0.125	-	-	UI
$V_{TX\text{-}CM\text{-}ACp}$	RMS AC peak common mode output voltage	-	-	20	mA
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0	-	100	mA
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0	-	25	mA
$V_{TX\text{-}IDLE\text{-}DIFFp}$	Electrical idle differential peak output	0	-	20	mA

	voltage				
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	-	-	600	mA
$V_{TX-DC-CM}$	The TX DC common mode voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX short circuit current limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	50	-	-	UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	-	-	20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential return loss	12	-	-	dB
RL_{TX-CM}	Common mode return loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	Ω
C_{TX}	AC coupling capacitor	75	-	200	nF
Tcrosslink	Crosslink random timeout	0	-	1	ms

l Receiver Serial Output

Table 7.6 – Receiver Serial Output

Symbol	Parameter	Min	Typ	Max	Unit
UI	Unit interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential input peak to peak voltage	0.175	-	1.2	V
T_{RX-EYE}	Minimum receiver eye width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC peak common mode input voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential return loss	15	-	-	dB
RL_{RX-CM}	Common mode return loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	Ω
Z_{RX-DC}	DC input impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	-	-	10	ms

7.6 Recommended Operating Conditions

Table 7.7 – Temperature Range

Symbol	Parameter	Min	Typ	Max	Unit
$T_{JUNCTOIN}$	Junction operating temperature range	0	-	125	℃
T_A	Operating ambient temperature range	0	-	75	℃
T_{STG}	Storage temperature range	-40	-	150	℃

Table 7.8 – Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA} (0 m/s)	Thermal resistance from junction to ambient PS: "(x m/s)" means the air flow velocity (JEDEC JESD51-6 moving air, maximum reflow temperature for SMT is 255℃~260℃)	-	33.2	-	℃/W
θ_{JA} (1 m/s)		-	28.7	-	℃/W
θ_{JA} (2 m/s)		-	27.5	-	℃/W
Ψ_{JT}	Thermal characterization parameter from junction-to-top center (JEDEC JESD51-2 still air, maximum reflow temperature for SMT is 255℃~260℃)	-	0.39	-	℃/W
θ_{JC}	Thermal resistance from junction to case (JEDEC JESD51-2 still air, maximum reflow temperature for SMT is 255℃~260℃)	-	12.3	-	℃/W

CHAPTER 8 PIPE TIMING CHARACTERISTICS

8.1 Input Setup, Hold Time and Output Timing

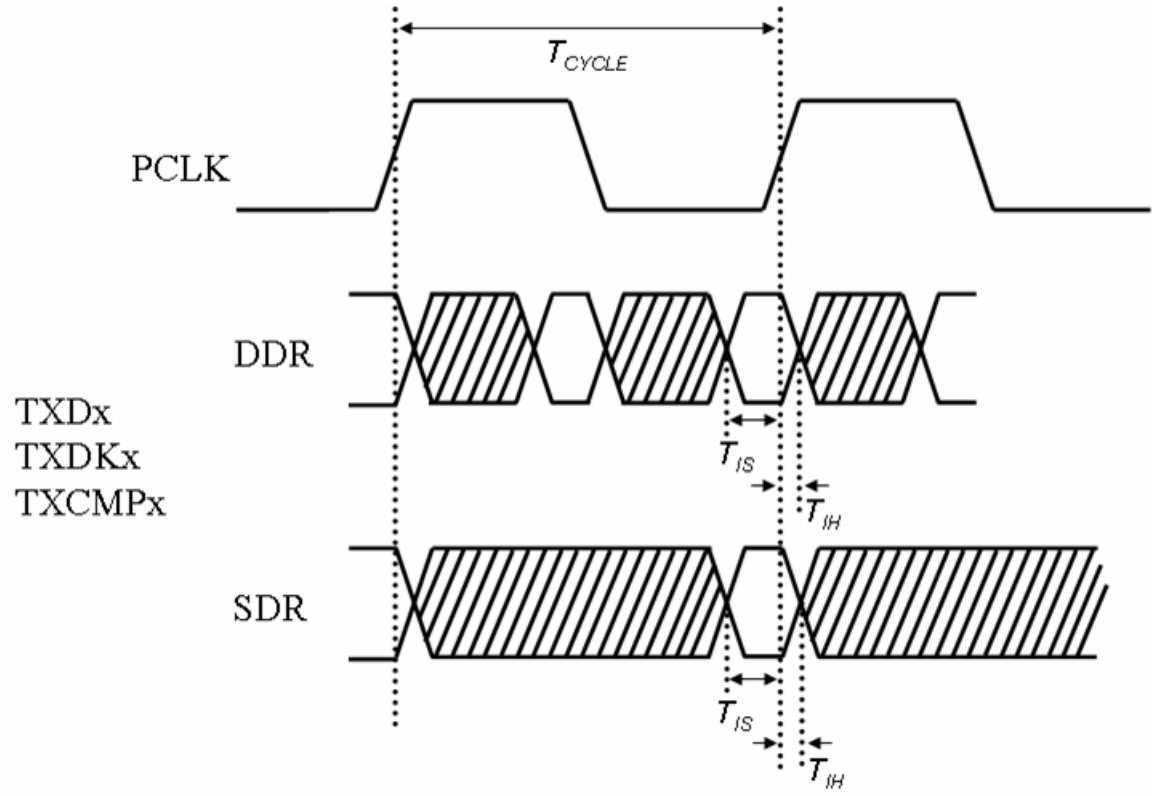


Figure 8.1 – Definition of Input Setup and Hold Time

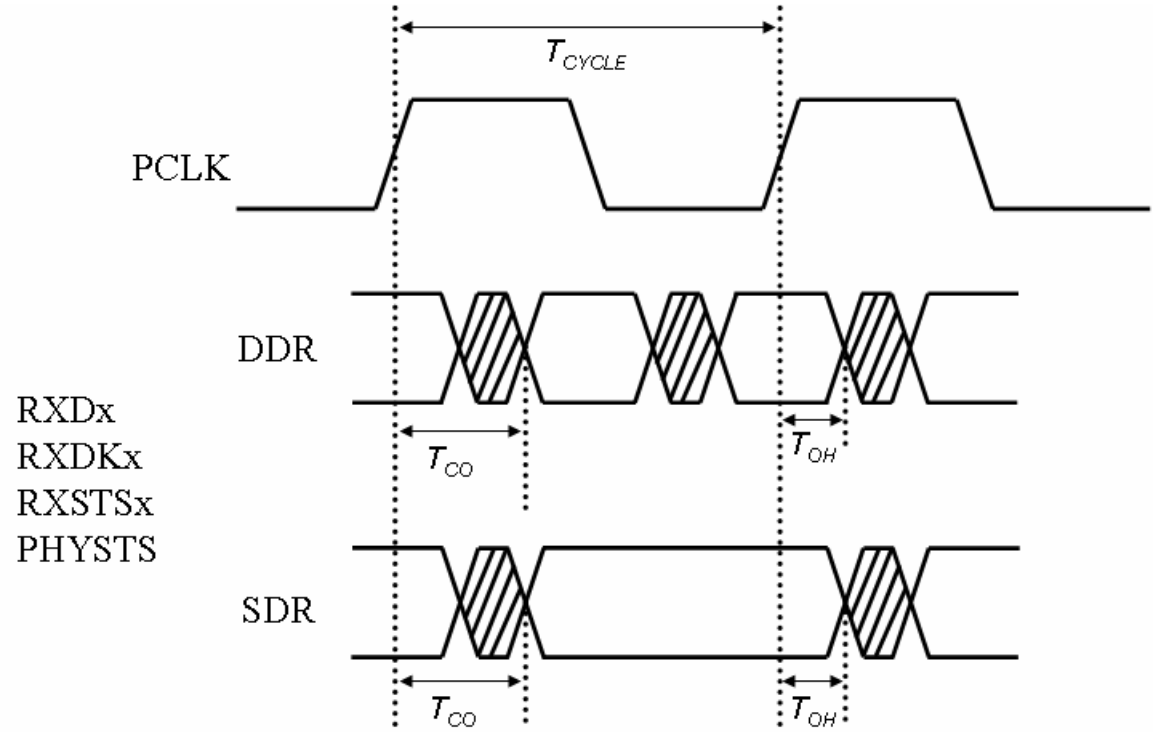


Figure 8.2 – Definition of Output Timing

Table 8.1 – Input Setup, Hold Time and Output Timing for 8-bit SDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	3.99	4	4.01	ns
Duty-$_H$	Duty cycle for PCLK high	35	-	50	%
T_{IS}	Input setup time	-	-	1	ns
T_{IH}	Input hold time	1	-	-	ns
T_{CO}	Clock to output delay	-	2.7	3.2	ns
T_{OH}	Output hold time	1	2.1	-	ns

Table 8.2 – Input Setup, Hold Time and Output Timing for 8-bit DDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	7.98	8	8.02	ns
T_{IS}	Input setup time	-	-	1.4	ns
T_{IH}	Input hold time	0.5	-	-	ns
T_{CO}	Clock to output delay	-	1.5	1.6	ns
T_{OH}	Output hold time	0.8	1	-	ns

Table 8.3 – Input Setup, Hold Time and Output Timing for 16-bit Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	7.98	8	8.02	ns
Duty-$_H$	Duty cycle for PCLK high	48	-	50	%
T_{IS}	Input setup time	-	-	1.4	ns
T_{IH}	Input hold time	0.5	-	-	ns
T_{CO}	Clock to output delay	-	5.3	5.6	ns
T_{OH}	Output hold time	4.3	4.7	-	ns

Table 8.4 – Input Setup, Hold Time and Output Timing for 10-bit SDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	3.99	4	4.01	ns
Duty-$_H$	Duty cycle for PCLK high	35	-	50	%
T_{IS}	Input setup time	-	-	1	ns
T_{IH}	Input hold time	1	-	-	ns
T_{CO}	Clock to output delay	-	4	4.2	ns
T_{OH}	Output hold time	3.4	3.7	-	ns

Table 8.5 – Input Setup, Hold Time and Output Timing for 10-bit DDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	7.98	8	8.02	ns
T_{IS}	Input setup time	-	-	1.4	ns
T_{IH}	Input hold time	0.5	-	-	ns
T_{CO}	Clock to output delay	-	4.1	4.3	ns
T_{OH}	Output hold time	3.5	3.7	-	ns

8.2 Reference Timing Information

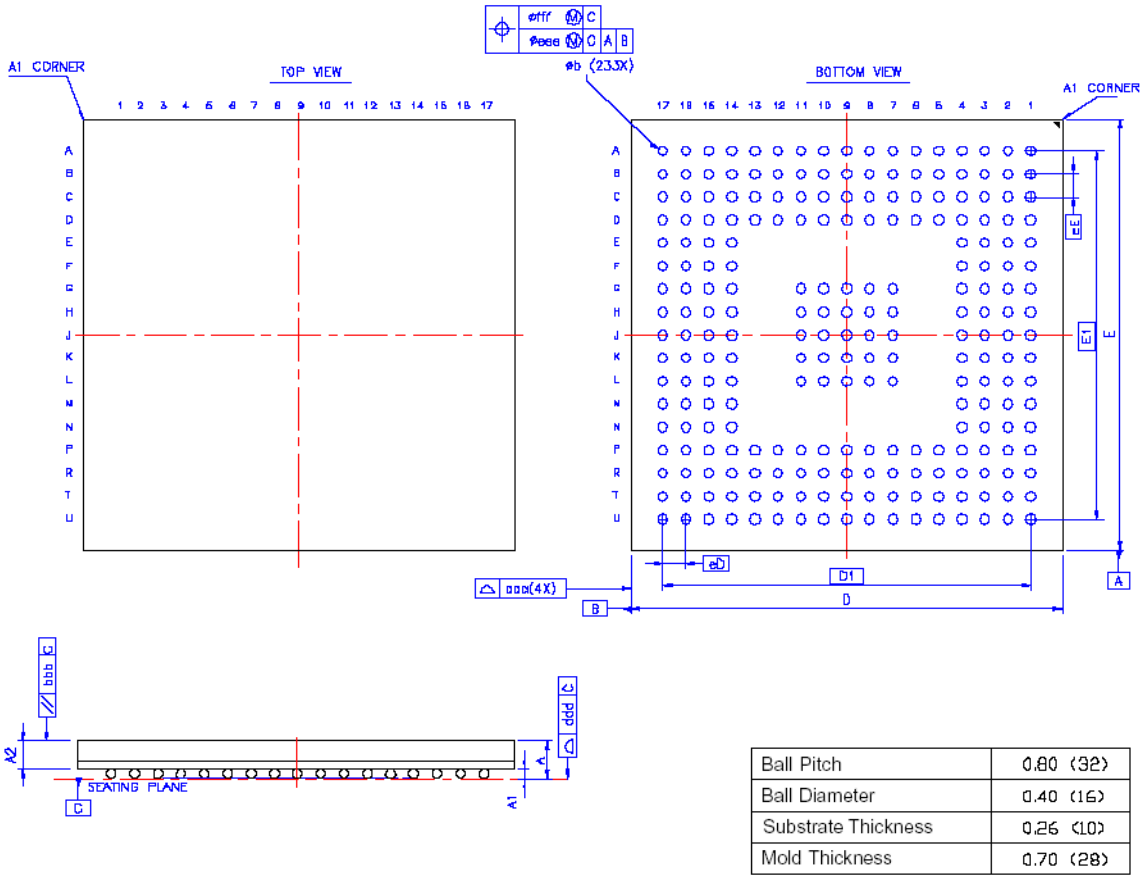
Table 8.6 – Reference Timing Information

Symbol	Parameter	Min	Typ	Max	Unit
T_{RECDET}	Time for receiver detection	-	10	-	us
$T_{PHYSTS-RESET}$	Timing from de-asserting RST_N to the falling edge of PHYSTS	-	16.7	-	us
T_{RESET}	Reset Assertion Time to GL9711	10	-	-	us

CHAPTER 9 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.40 (55)
A1	0.27 (11)		0.37 (15)
A2	0.96 (38) REF		
b	0.37 (15)		0.47 (19)
D	14.95 (589)	15.00 (591)	15.05 (593)
E	14.95 (589)	15.00 (591)	15.05 (593)
eD	0.80 (32) BSC		
D1	12.80 (504) BSC		
eE	0.80 (32) BSC		
E1	12.80 (504) BSC		
aaa	0.15 (6)		
bbb	0.20 (8)		
ddd	0.12 (5)		
eee	0.15 (6)		
fff	0.08 (3)		

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.



Ball Pitch	0.80 (32)
Ball Diameter	0.40 (16)
Substrate Thickness	0.26 (10)
Mold Thickness	0.70 (28)

Figure 9.1 - GL9711 233 Pin LFBGA Package

CHAPTER 10 ORDERING INFORMATION

Table 10.1 - Ordering Information

Part Number	Package	Green	Version	Status
GL9711-TgGXX	233-pin LFBGA	Green Package	XX	Engineering Sample

