

FDC6327C

Dual N & P-Channel 2.5V Specified PowerTrench™ MOSFET

General Description

These N & P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

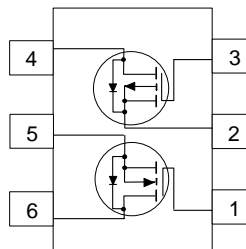
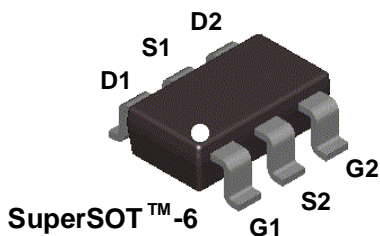
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

Applications

- DC/DC converter
- Load switch
- Motor driving

Features

- N-Channel 2.7A, 20V. $R_{DS(on)} = 0.08\Omega @ V_{GS} = 4.5V$
 $R_{DS(on)} = 0.12\Omega @ V_{GS} = 2.5V$
- P-Channel -1.6A, -20V. $R_{DS(on)} = 0.17\Omega @ V_{GS} = -4.5V$
 $R_{DS(on)} = 0.25\Omega @ V_{GS} = -2.5V$
- Fast switching speed.
- Low gate charge.
- High performance trench technology for extremely low $R_{DS(on)}$.
- SuperSOT™-6 package: small footprint (72% smaller than SO-8); low profile (1mm thick).



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 8	± 8	V
I_D	Drain Current - Continuous (Note 1a)	2.7	-1.9	A
	- Pulsed	8	-8	
P_D	Power Dissipation (Note 1a) (Note 1b) (Note 1c)	0.96		W
		0.9		
		0.7		
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.327	FDC6327C	7"	8mm	3000

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Off Characteristics

V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	N-Ch P-Ch	20 -20			V
$\frac{\Delta V_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C $I_D = -250\ \mu\text{A}$, Referenced to 25°C	N-Ch P-Ch		12 -19		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	N-Ch P-Ch			1 -1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	N-Ch P-Ch	0.4 -0.4	0.9 -0.9	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C $I_D = -250\ \mu\text{A}$, Referenced to 25°C	N-Ch P-Ch		-2.1 2.3		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.7\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 2.7\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 2.5\text{ V}, I_D = 2.2\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -1.6\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -1.6\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -2.5\text{ V}, I_D = -1.3\text{ A}$	N-Ch N-Ch N-Ch P-Ch P-Ch P-Ch		0.069 0.094 0.093 0.141 0.203 0.205	0.08 0.13 0.12 0.17 0.27 0.25	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	N-Ch P-Ch	8 -8			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 2.7\text{ A}$ $V_{DS} = -5\text{ V}, I_D = -1.9\text{ A}$	N-Ch P-Ch		7.7 4.5		S

Dynamic Characteristics

C_{iss}	Input Capacitance	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-Ch P-Ch		325 315		pF
C_{oss}	Output Capacitance	P-Channel	N-Ch P-Ch		75 65		pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-Ch P-Ch		35 24		pF

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Switching Characteristics (Note 2)

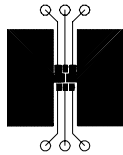
$t_{d(on)}$	Turn-On Delay Time	N-Channel $V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	N-Ch P-Ch		5 7	15 14	ns
t_r	Turn-On Rise Time		N-Ch P-Ch		9 14	18 25	ns
$t_{d(off)}$	Turn-Off Delay Time	P-Channel $V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	N-Ch P-Ch		12 14	22 25	ns
t_f	Turn-Off Fall Time		N-Ch P-Ch		3 3	9 9	ns
Q_g	Total Gate Charge	N-Channel $V_{DS} = 10\text{ V}, I_D = 2.7\text{ A}, V_{GS} = 4.5\text{ V}$	N-Ch P-Ch		3.25 2.85	4.5 4.0	nC
Q_{gs}	Gate-Source Charge		N-Ch P-Ch		0.65 0.68		nC
Q_{gd}	Gate-Drain Charge	P-Channel $V_{DS} = -10\text{ V}, I_D = -1.9\text{ A}, V_{GS} = -4.5\text{ V}$	N-Ch P-Ch		0.90 0.65		nC

Drain-Source Diode Characteristics and Maximum Ratings

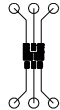
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch P-Ch			0.8 -0.8	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.8\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -0.8\text{ A}$ (Note 2)	N-Ch P-Ch		0.76 -0.79	1.2 -1.2	V

Notes:

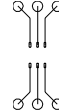
- 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally.



a) 130°C/W when mounted on a 0.125 in^2 pad of 2 oz. copper.



b) 140°C/W when mounted on a 0.005 in^2 pad of 2 oz. copper.



c) 180°C/W when mounted on a 0.0015 in^2 pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

- 2: Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics: N-Channel

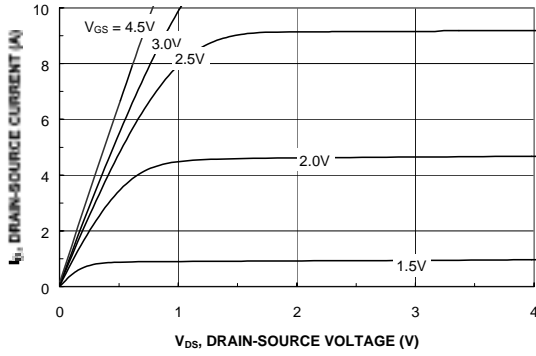


Figure 1. On-Region Characteristics.

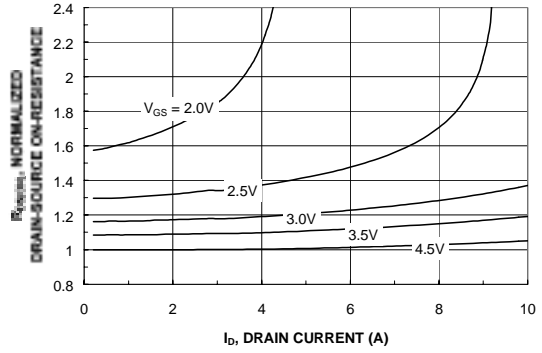


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

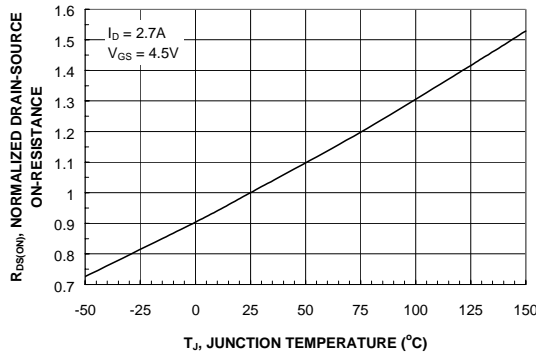


Figure 3. On-Resistance Variation with Temperature.

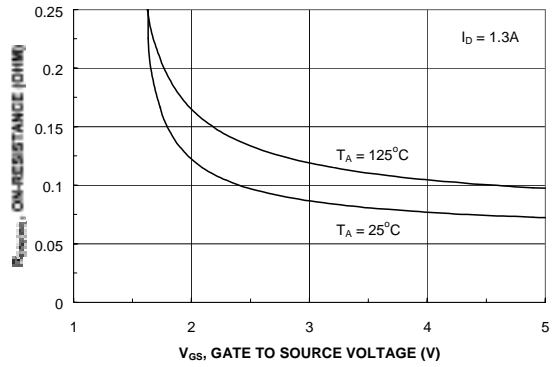


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

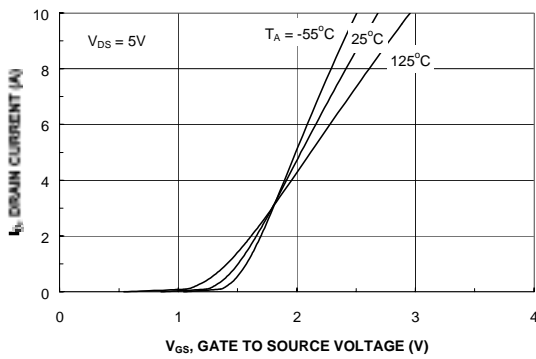


Figure 5. Transfer Characteristics.

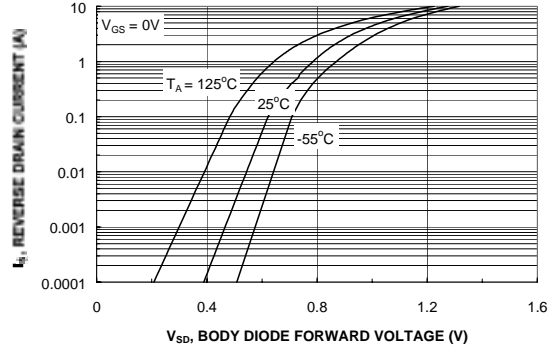


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-Channel (continued)

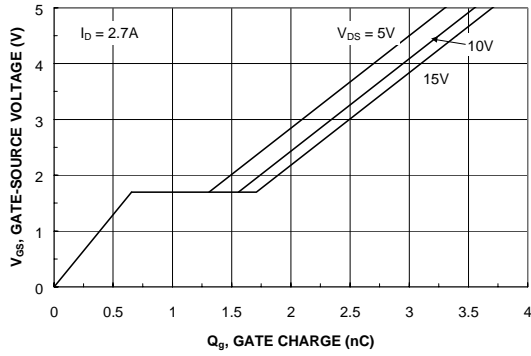


Figure 7. Gate-Charge Characteristics.

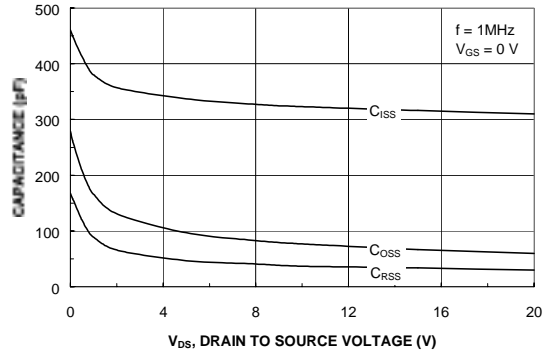


Figure 8. Capacitance Characteristics.

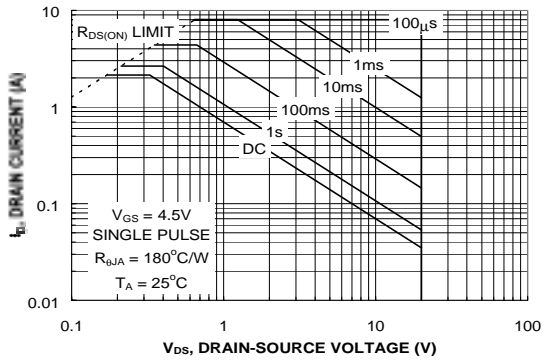


Figure 9. Maximum Safe Operating Area.

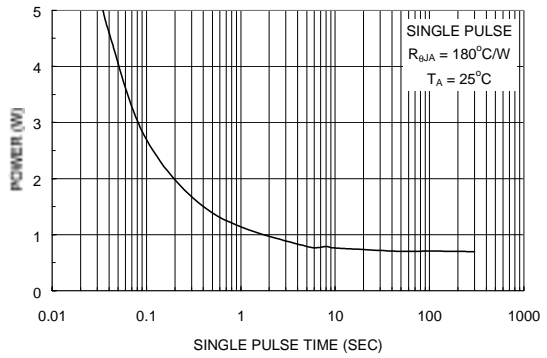


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel

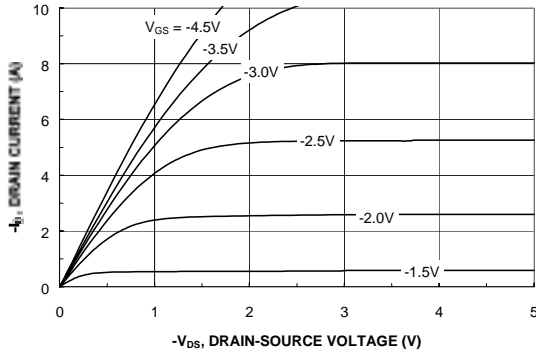


Figure 11. On-Region Characteristics.

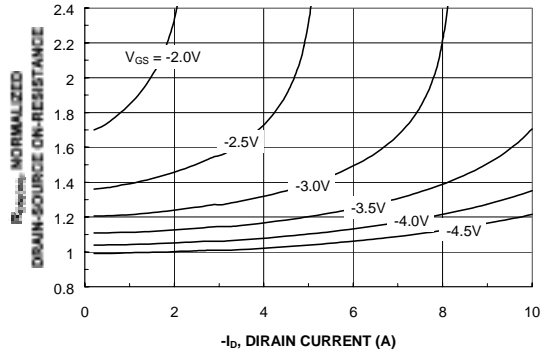


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

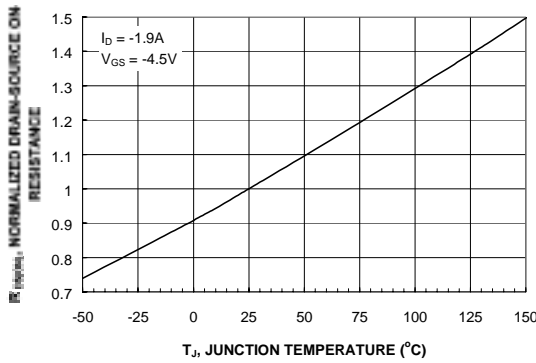


Figure 13. On-Resistance Variation with Temperature.

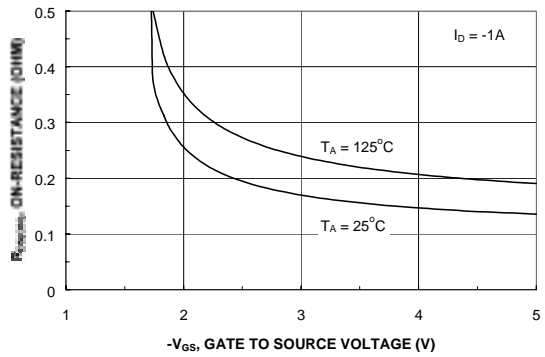


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

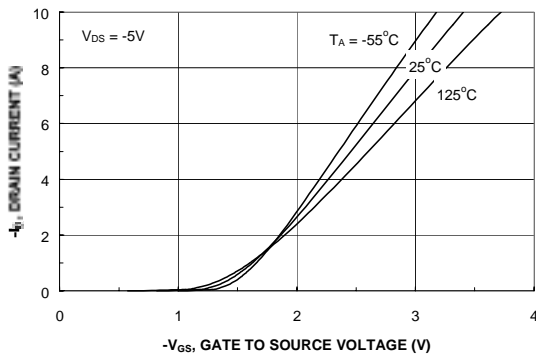


Figure 15. Transfer Characteristics.

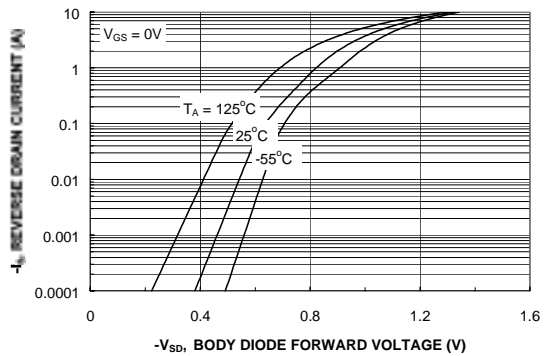


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: P-Channel (continued)

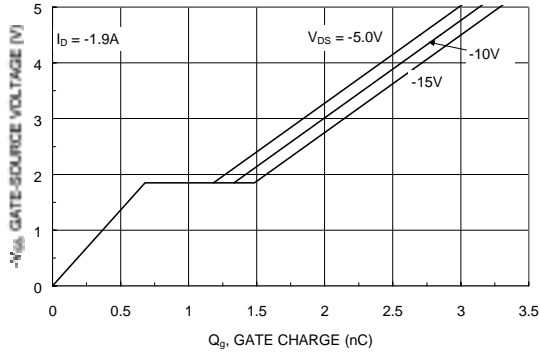


Figure 17. Gate-Charge Characteristics.

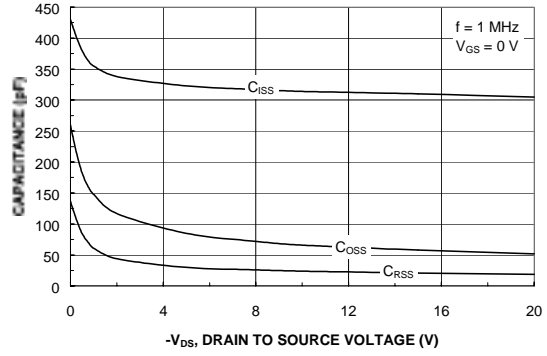


Figure 18. Capacitance Characteristics.

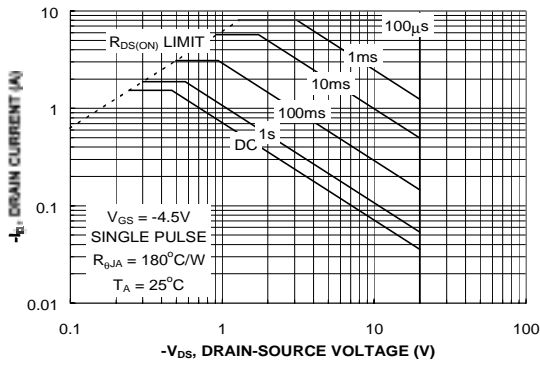


Figure 19. Maximum Safe Operating Area.

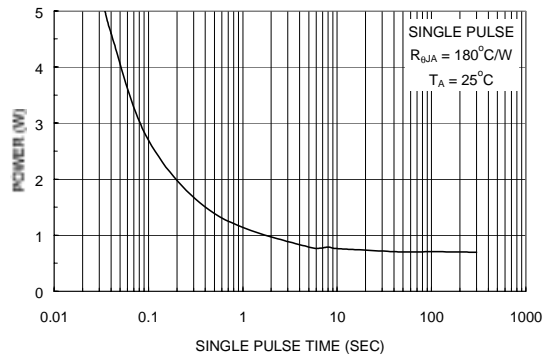


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Characteristics: N & P-Channel (continued)

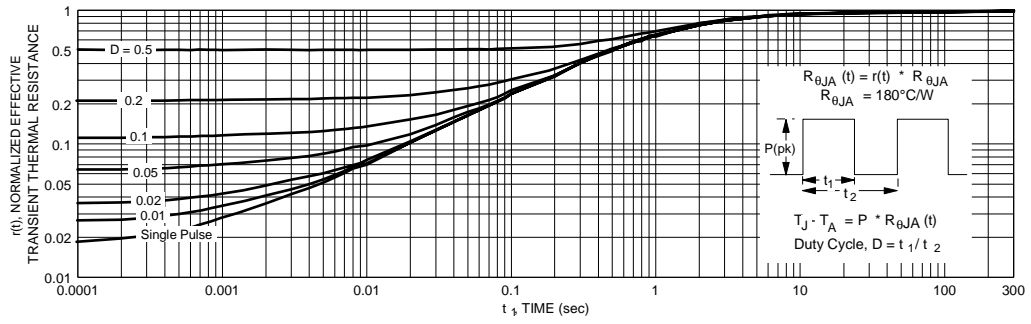
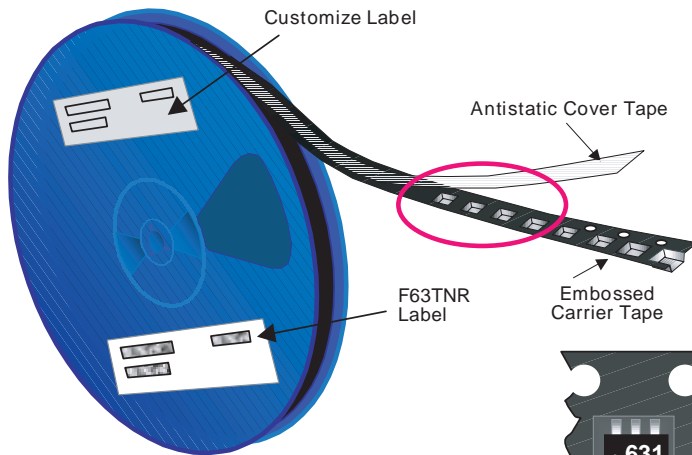


Figure 21. Transient Thermal Response Curve.

SuperSOT™-6 Tape and Reel Data and Package Dimensions



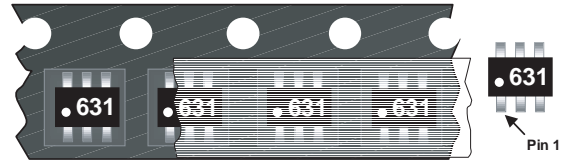
SSOT-6 Packaging Configuration: Figure 1.0



Packaging Description:

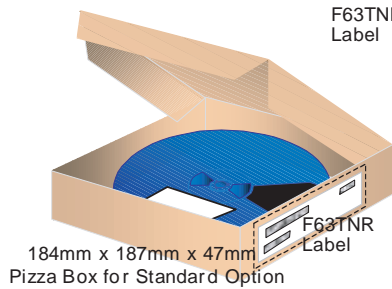
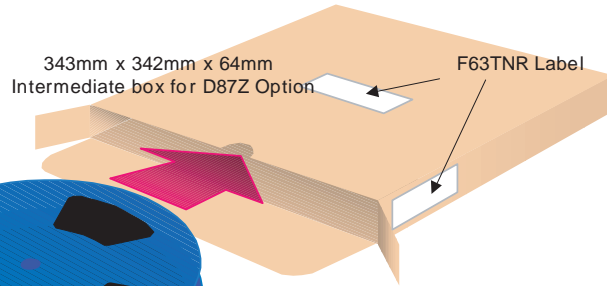
SSOT-6 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 177cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 10,000 units per 13" or 330cm diameter reel. This and some other options are described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a pizza box (illustrated in figure 1.0) made of recyclable corrugated brown paper with a Fairchild logo printing. One pizza box contains three reels maximum. And these pizza boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



SSOT-6 Unit Orientation

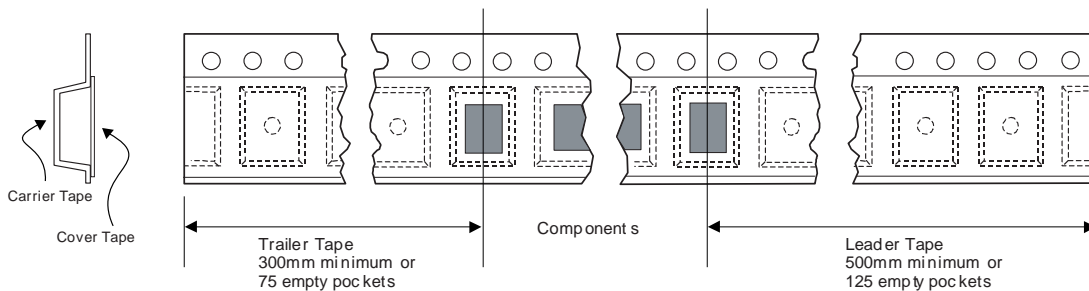
SSOT-6 Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	184x187x47	343x343x64
Max qty per Box	9,000	30,000
Weight per unit (gm)	0.0158	0.0158
Weight per Reel (kg)	0.1440	0.4700
Note/Comments		



F63TNR Label sample

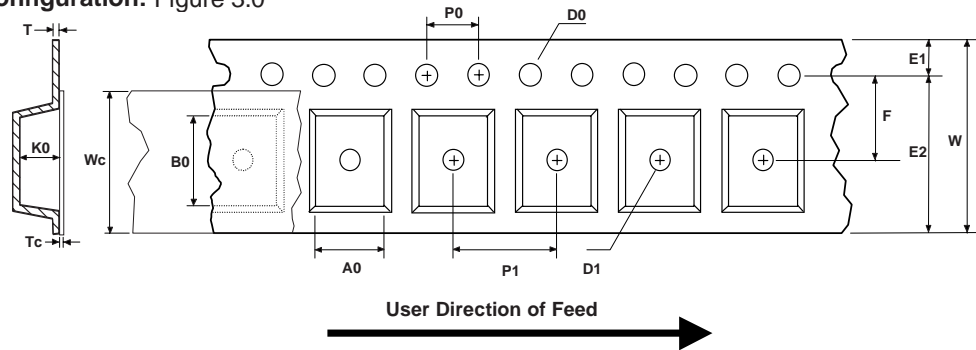


SSOT-6 Tape Leader and Trailer Configuration: Figure 2.0



SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

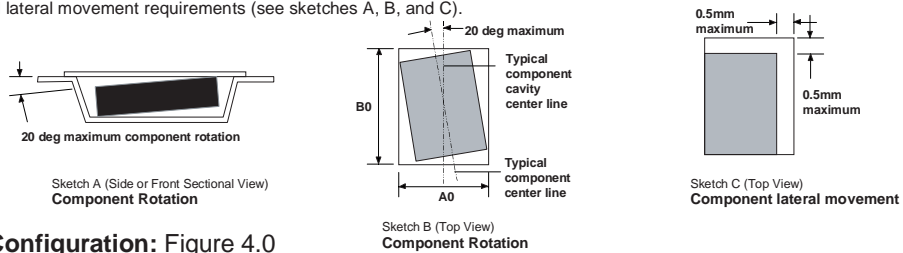
SSOT-6 Embossed Carrier Tape Configuration: Figure 3.0



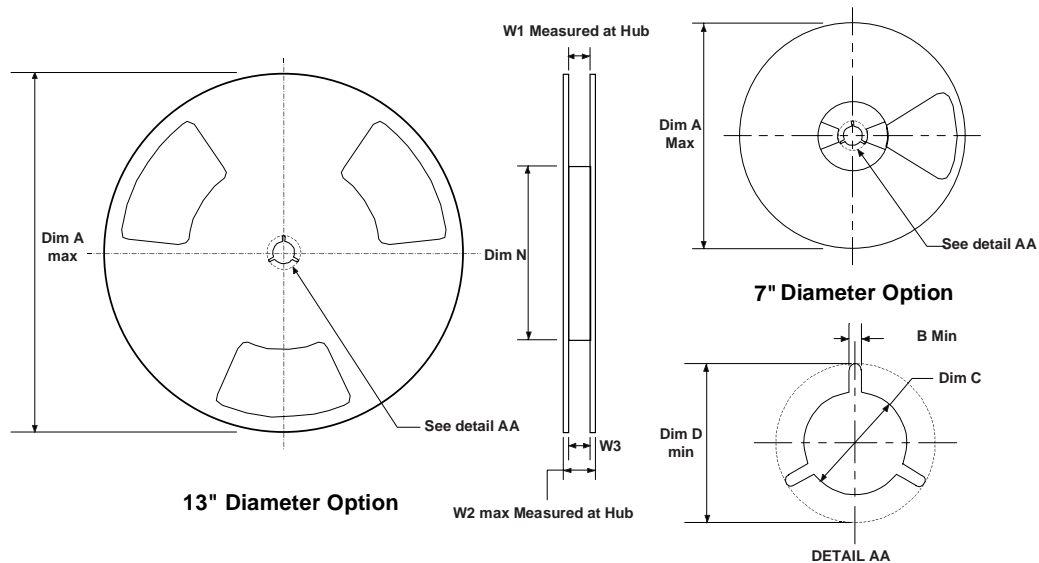
Dimensions are in millimeter

Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SSOT-6 (8mm)	3.23 +/-0.10	3.18 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



SSOT-6 Reel Configuration: Figure 4.0

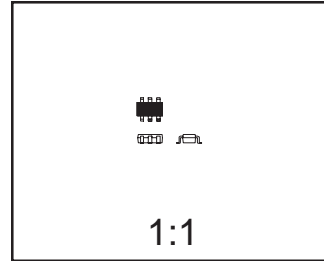
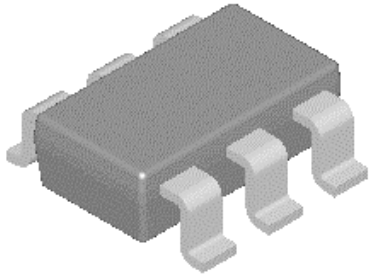


Dimensions are in inches and millimeters

Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

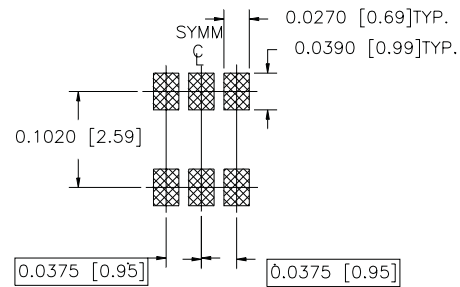
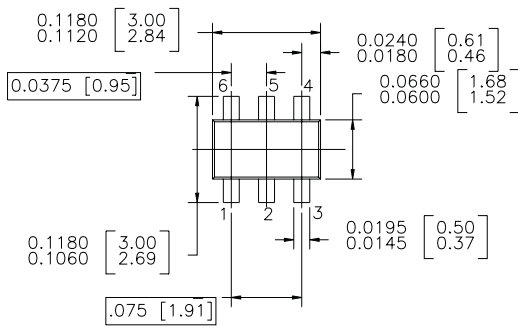
SuperSOT -6 (FS PKG Code 31, 33)



Scale 1:1 on letter size paper

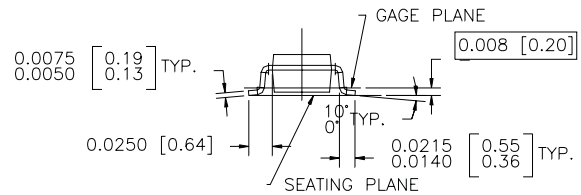
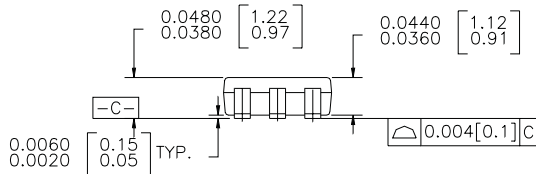
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0158



LAND PATTERN RECOMMENDATION

CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS



SUPER SOT 6 LEADS

NOTES : UNLESS OTHERWISE SPECIFIED

1.0 STANDARD LEAD FINISH : 150 MICRINCHES 93.81 MICROMETERS)
MINIMUM TIN / LEAD (SOLDER) ON COPPER.

2.0 NO JEDEC REGISTRATION AS OF JULY 1996

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FASTr™	QFET™	VCX™
Bottomless™	GlobalOptoisolator™	QS™	
CoolFET™	GTO™	QT Optoelectronics™	
CROSSVOLT™	HiSeC™	Quiet Series™	
DOME™	ISOPANAR™	SuperSOT™-3	
E ² CMOS™	MICROWIRE™	SuperSOT™-6	
EnSigna™	OPTOLOGIC™	SuperSOT™-8	
FACT™	OPTOPLANAR™	SyncFET™	
FACT Quiet Series™	POP™	TinyLogic™	
FAST®	PowerTrench®	UHC™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.