

SONY**CXK541020J** -20/25**262144-words x 4-bits High Speed CMOS Static RAM****Description**

The CXK541020J is a high speed CMOS static RAM organized as 262144-words by 4 bits.

It operates at 20ns/25ns access time from 5V single power supply.

The CXK541020J is suitable for use in high speed applications.

Features

- Fast access time: (Access time)
CXK541020J-20 20ns (Max.)
CXK541020J-25 25ns (Max.)
- Low power consumption (operation)
CXK541020J-20 880mW (Max.)
CXK541020J-25 825mW (Max.)
- Single +5V supply: $5V \pm 10\%$
- Fully static memory ... No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible all inputs and outputs
- Package
CXK541020J 400mil 28pin SOJ Package

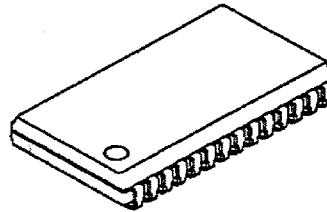
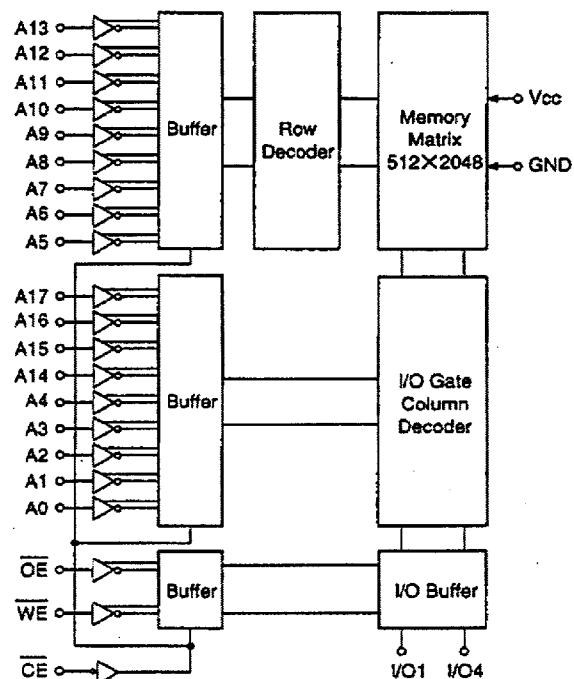
Function

262144-words x 4-bits static RAM

Structure

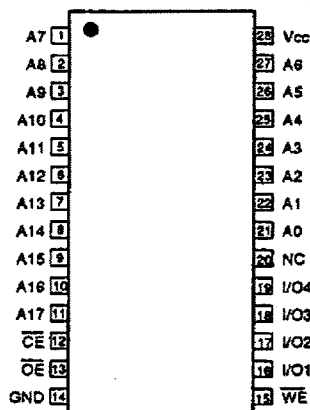
- Silicon gate CMOS IC

28 pin SOJ (Plastic)

**Block Diagram**

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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A17	Address input
I/O1 to I/O4	Data input output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5* to Vcc + 0.5	V
Input and output voltage	V _{IO}	-0.5* to Vcc + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-45 to +125	°C
Soldering temperature · time	T _{solder}	235 · 10	°C · s

* Vcc, V_{IN}, V_{IO} = -3.0V Min. for pulse width less than 5ns.

Truth Table

CE	OE	WE	Mode	I/O pin	Vcc current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC}
L	L	H	Read	Data out	I _{CC}
L	X	L	Write	Data in	I _{CC}

X: "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	Vcc + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL} = -3.0V Min. for pulse width less than 5ns.

Electrical Characteristics

• DC characteristics

(V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions			Min.	Typ.*1	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}			-2	—	2	μA
Output leakage current	I _{LO}	CE = V _{IH} or OE = V _{IH} or WE = V _{IL} V _{VO} = GND to V _{CC}			-2	—	2	μA
Average operating current	I _{CC}	Min. cycle duty = 100% *2 I _{OUT} = 0mA	Write	20	—	—	160	mA
				25	—	—	150	
			Read	20	—	—	110	
				25	—	—	100	
Standby current	I _{SB1}	CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V			—	—	2	mA
	I _{SB2}	CE = V _{IH} , V _{IN} = V _{IH} or V _{IL} , Min. cycle	20	—	—	35	mA	
			25	—	—	30		
Output high voltage	V _{OH}	I _{OH} = -4.0mA			2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA			—	—	0.4	V

*1 V_{CC} = 5V, T_a = 25°C

*2 Address is increased with binary count.

I/O Capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{VO} = 0V	—	—	7	pF

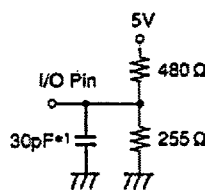
(Note) This parameter is sampled and is not 100% tested.

AC Characteristics

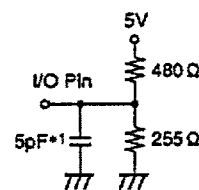
• AC test conditions (V_{CC} = 5V±10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 3ns
Input fall time	t _f = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output load (1)



Output load (2)*2



*1 This parameter includes scope and jig capacitances.

*2 For t_{LZ}, t_{OLZ}, t_{HZ}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1.

• Read cycle ($\overline{WE} = "H"$).

Item	Symbol	-20		-25		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	20	—	25	—	ns
Address access time	t_{AA}	—	20	—	25	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	20	—	25	ns
Output enable to output valid	t_{OE}	—	10	—	12	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}^*	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}^*	2	—	2	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}^*	—	9	—	10	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}^*	—	9	—	10	ns
Chip enable to power up time	t_{PU}	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	20	—	25	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

This parameter is sampled and is not 100% tested.

• Write cycle

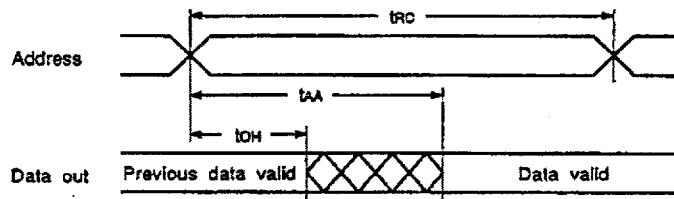
Item	Symbol	-20		-25		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	20	—	25	—	ns
Address valid to end of write	t_{AW}	15	—	20	—	ns
Chip enable to end of write	t_{CW}	15	—	20	—	ns
Data to write time overlap	t_{DW}	10	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	20	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	ns
Output active from end of write	t_{OW}^*	5	—	5	—	ns
Write to output in high Z	t_{WHZ}^*	—	9	—	10	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

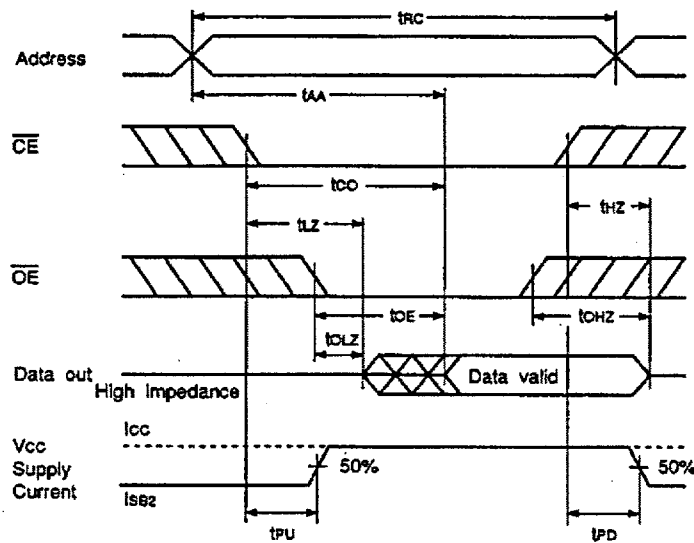
This parameter is sampled and is not 100% tested.

Timing Waveform

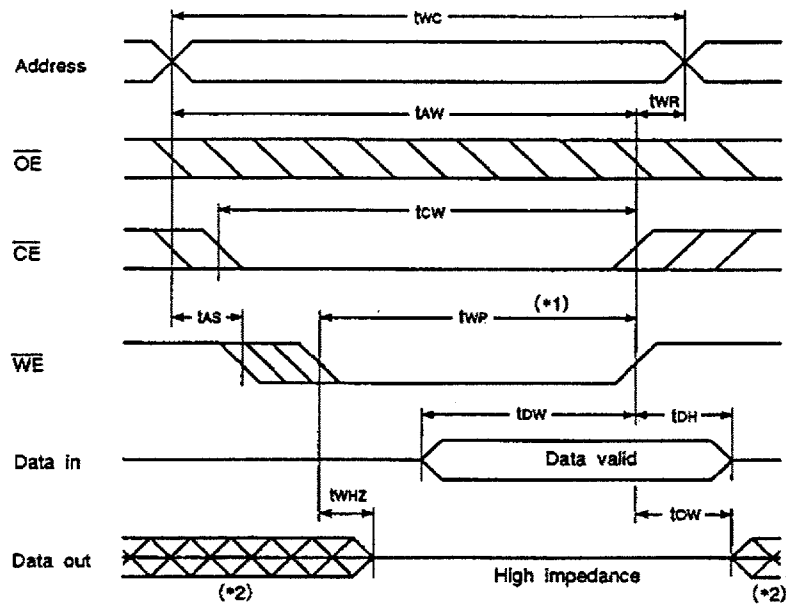
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



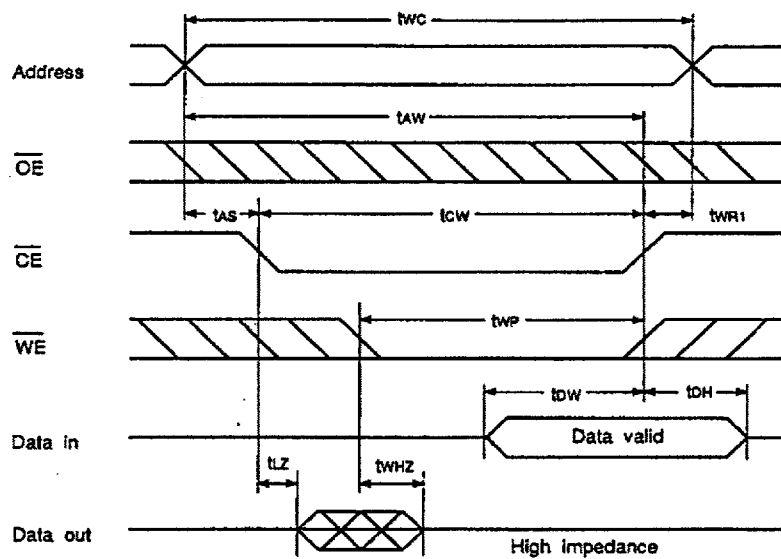
- Read cycle (2) : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



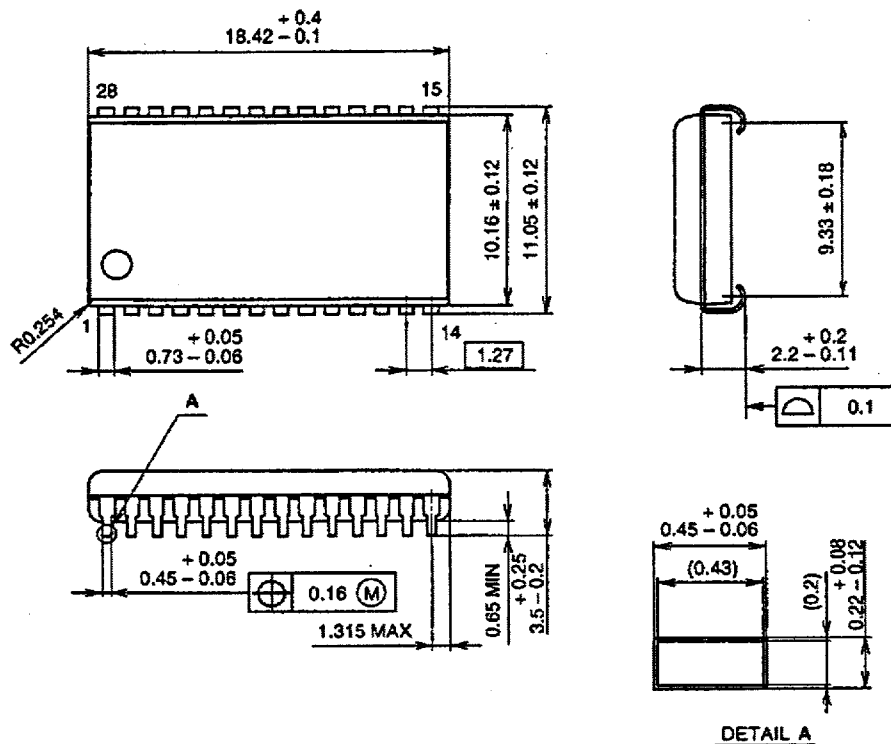
*1 Write is executed when both $\overline{CE}$ and $\overline{WE}$ are at low simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

Package Outline

Unit : mm

28PIN SOJ (PLASTIC) 400mil



PACKAGE STRUCTURE

SONY CODE	SOJ-28P-02
EIAJ CODE	*SOJ028-P-0400-A
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER
PACKAGE WEIGHT	1.1g