Features

- **High Sensitivity and High SNR Performance Linear CCD**
- **Resolution:**
  - **2048 Pixels with 14 µm Square Pixels**
  - **6144 or 8192 Pixels with 7 µm Square Pixels**
- **100% Aperture, Built-in Antiblooming, No Lag**
- **CameraLink Data Format (Medium Configuration)**
- **High Data Rate:**
  - **2048 Pixels: 120 Mpixels/s**
  - **6144 and 8192 Pixels: 160 Mpixels/s**
- **Flexible and Easy to Operate Via Serial Control Lines (CameraLink)**
  - **Integration Time**
  - **Gain: 0dB to 30 dB by Steps of 0.04dB**
  - **Output Format: 8 or 10 Bits Data**
  - **Offset (for Contrast Expansion)**
  - **Trigger Mode: Free Run or External Trigger Modes**
- **Multi-camera Synchronization**
- **Single Power Supply: 12 to 24V DC Provided on Hirose-6 Connector**
- **Compact Mechanical Design:**
  - **2048: 56 x 60 x 54 mm (W, H, L)**
  - **6144 and 8192: 82 x 60 x 54 mm (W, H, L)**
- **High Reliability – CE and FCC Compliant**
- **Available Lens Adapter (Lens Not Supplied):**
  - **F Mount or T2 Mount for 2048 and 6144 Pixels**
  - **M72 x 0.75 for 8192 Pixels**

Description

This camera has been designed with three concepts in mind: compactness, accuracy and versatility.

- Atmel manages the entire process, from the sensor to the camera. The result is a camera able to work in 8 or 10 bits, with dedicated electronics offering an excellent signal to noise ratio.
- The programmable settings let the user work in different illumination conditions: integration time, gain and offset.

Applications

The high speed, high resolution, performance and reliability of this camera make it well suited for the most demanding industrial applications.

- OCR and barcode reading: postal and parcel sorting, document scanning
- Inspection and metrology: PCB, CD, DVD, display, semiconductor and electronics
- Web inspection: ceramic, printing, currency, textile, wood, paper

CameraLink™ Linescan Camera 120 MHz

AViiVA™ M4 CL

Preliminary

Rev. 5330A–IMAGE–05/03

Typical Performances

Table 1. 2k Pixel Cameras Typical Performances

Parameter	Value			Unit
Sensor Characteristics at Maximum Pixel Rate				
Resolution	2048			pixels
Pixel size (square)	14			µm
Max Line rate	52			kHz
Peak data rate	4 x 30			MHz
Antiblooming	x 100			–
Radiometric Performances at Maximum Pixel Rate				
Output format	8 or 10			bit
Spectral range	250 – 1100			nm
Linearity	2			%
PRNU	±6			%
Sensitivity output matching	10			%
Offset output matching(1)	10			LSB
Gain range (steps of 0.035 dB)	Gmin 0	Gnom 18	Gmax 30	 dB
Peak response(1)(2) SEE	7 38.5	53 4.84	210 1.22	LSB/(nJ/cm^2) nJ/cm^2
SNR at 25°C	58	42	30	dB
NEE	50 TBC(3)	–	–	pJ/cm^2
Dark signal at 25°C(1)	260	2100	8500	LSB/s
DSNU at 25°C(1)	200	1600	6500	LSB/s
Mechanical and Electrical Interface				
Size (w x h x l)	56 x 60 x 54			mm
Lens mount	No optical mount or F mount or T2 mount			–
Sensor alignment	Δx,y = ±50 Δz = 0 – 60 $\Delta\theta$x,y = ±0.2 Δtilt$_z$ = 0 – 35			µm µm ° µm
Power supply	DC, single 12 to 24			V
Power dissipation	< 10			W
Operating temperature	0 to 55 (non-condensing)			°C
Storage temperature	-40 to 85 (non-condensing)			°C

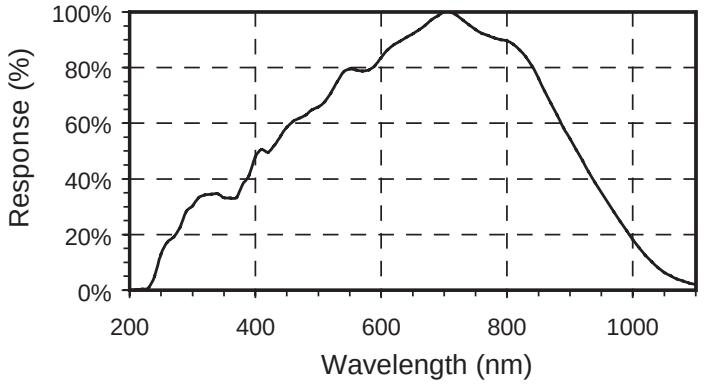
Notes: 1. LSB are given for 8 bit of resolution
2. nJ/cm² 4 front face temperature
3. In this specification TBD stands for To Be Defined, TBC for To Be Confirmed

Table 2. 6k and 8k Pixel Cameras Typical Performances

Parameter	Value			Unit
Sensor Characteristics at Maximum Pixel Rate	**6K**	**8K**		
Resolution	6144	8192		pixels
Pixel size (square)	7	7		µm
Max Line rate	18.5	14		kHz
Peak data rate	4 x 40			MHz
Antiblooming	x 100			–
Radiometric Performances at Maximum Pixel Rate				
Output format	8 or 10			bit
Spectral range	250 – 1100			nm
Linearity	2			%
PRNU	±6			%
Sensitivity output matching	10			%
Offset output matching(1)	10			LSB
Gain range (steps of 0.035 dB)	Gmin 0	Gnom 18	Gmax 30	 dB
Peak response(1)(2) SEE	4 60	34 7.6	135 1.9	LSB/(nJ/cm^2) nJ/cm^2
SNR at 25°C	58	42	30	dB
NEE	75 TBC(4)	–	–	pJ/cm^2
Dark signal at 25°C(1)	450	3500	14000	LSB/s
DSNU RMS at 25°C(1)	350	2700	11000	LSB/s
Mechanical and Electrical Interface				
Size (w x h x l)	82 x 60 x 54			mm
Lens mount	M72 x 0.75			–
Sensor alignment	Δx,y = ±50 Δz = 0 – 60 $\Delta\theta$x,y = ±0.2 Δtilt$_z$ = 0 – 35			µm µm ° µm
Power supply	DC, single 12 to 24V			V
Power dissipation	< 10			W
Operating temperature(3)	0 to 55 (non-condensing)			°C
Storage temperature	-40 to 85 (non-condensing)			°C

Notes:
1. LSB are given for 8 bit of resolution
2. nJ/cm² measured on the sensor
3. Front face temperature
4. In this specification TBD stands for To Be Defined, TBC for To Be Confirmed

Figure 1. Spectral Response

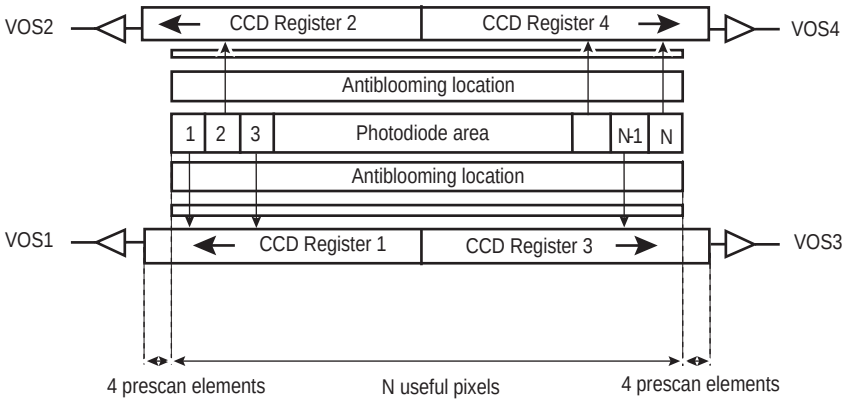


Description

CCD

The CCD uses 4 taps.

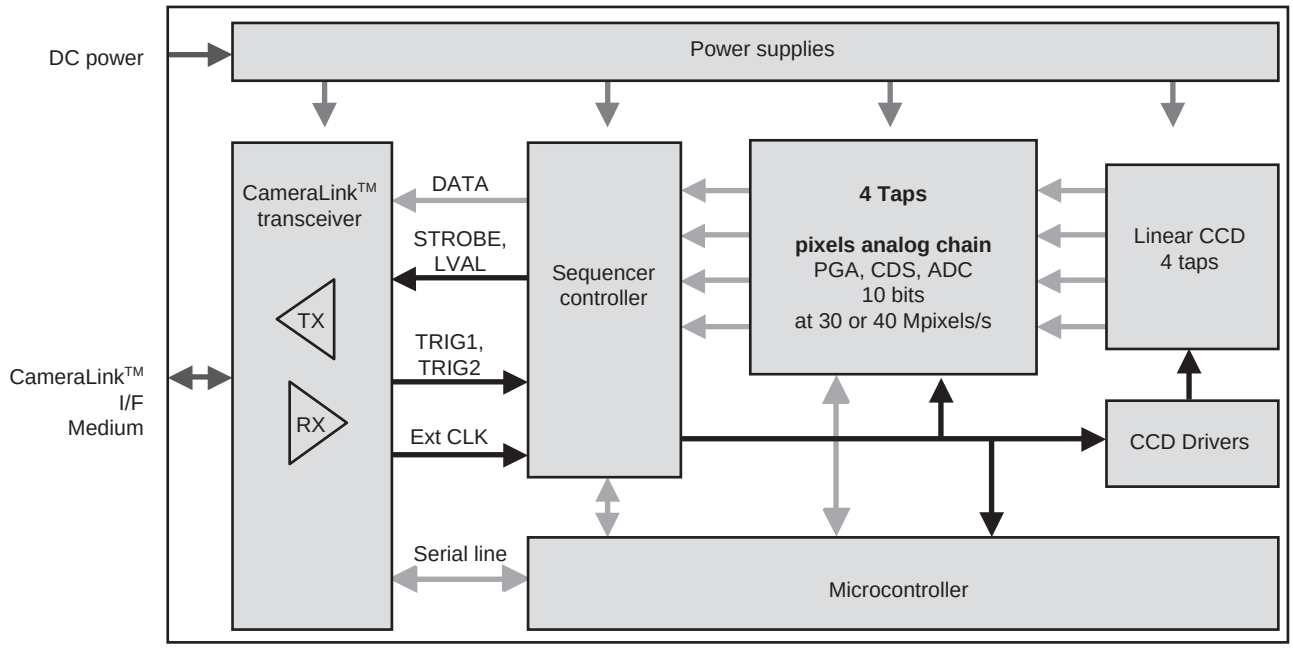
Figure 2. CCD Architecture



Note: The prescan pixels are not output from the camera.

Camera

Figure 3. Camera Synoptic



The AViiVA M4 cameras are based on four taps linear CCDs. Therefore, four analog chains process pixels of the linear sensor. The analog chains perform the CCD output processing. It encompasses the correlated double sampling (CDS), the dark level correction (dark pixel clamping), the gain (PGA) and offset correction and finally the analog to digital conversion on 10 bits (8- or 10-bit output).

Note: PGA stands for programmable gain array

- A single DC power voltage from 12 to 24 V supplies the camera.
- The functional interface (data and control) is provided by the CameraLink™ interface.
- The camera uses the medium configuration of CameraLink™ standard.
- Note: FVAL=0
- The camera can be used with an external trigger. The camera uses TRIG1 and TRIG2 signals in the different external trigger modes, (refer to “Camera configuration is set by the serial interface. Please refer to “Serial Communication” on page 13 for the detailed protocol of the serial line.” on page 7). The camera can be clocked externally, allowing system synchronization and/or multi-camera synchronization.

The camera configuration and settings are performed via a serial line. This interface is used for:

- Gain, offset setting
- Dynamic range, data rate setting
- Trigger mode setting: free running or external trigger modes
- Integration time setting: in free running and external trigger mode

Standard Conformity

The cameras have been tested in the following conditions:

- Shielded power supply cable.
- Two CameraLink data transfer cables ref. 14B26-SZLB-500-OLC (3M).

We recommend the use of the same configuration to ensure compliance with the following standards.

CE Conformity

AViiVA M4 Cameras comply with the requirements of the EMC (European) directive 89/336/CEE (EN 50081-2, EN 61000-6-2).

FCC Conformity

AViiVA M4 Cameras comply with Part 15 of FCC rules.

Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Camera Commands and Controls

Camera configuration is set by the serial interface. Please refer to “Serial Communication” on page 13 for the detailed protocol of the serial line.

Table 3. Camera Settings

	Functionalities	**Range/Values/Remarks**
Common gain	Camera gain adjustment	2 to 35 dB
Channel 1 gain	Fine gain adjustment for balance	
Channel 2 gain	Fine gain adjustment for balance	
Channel 3 gain	Fine gain adjustment for balance	
Channel 4 gain	Fine gain adjustment for balance	
Channel 1 offset	Channel offset adjustment	
Channel 2 offset	Channel offset adjustment	
Channel 3 offset	Channel offset adjustment	
Channel 4 offset	Channel offset adjustment	
Contrast expansion Channel 1		256 steps
Contrast expansion Channel 2		256 steps
Contrast expansion Channel 3		256 steps
Contrast expansion Channel 4		256 steps

Table 4. Camera Configuration

	Functionalities	**Range/Values/Remarks**
Output mode (TBC)	2, or 4 outputs	
Automatic offset compensation	Allows automatic digital offset compensation	
Master clock	30 MHz	
Clock source selection	Internal or external Rising or falling edge selection	
Integration time	1 to 32000 steps	Each step = 1.00 µs
Trigger mode	Free run	Integration time set by serial line
	External trigger mode	
	One signal integration time control	Integration time and readout time controlled by one or two external signals
	Two signals integration time control	
Output data rate	Master clock period Master clock period/2 Master clock period/4	Data valid is used
Data size output	8 or 10 bits	
Output signal	Pattern	
	Raw video	

Table 5. Configuration Settings

	Functionalities	Range/Values/Remarks
Storage/Restoration	One factory settings and four customer settings	The maximum number of write cycles allowed by the EEPROM is 100,000

Table 6. Camera Readout

	Functionalities	Range/Values/Remarks
Camera status	Camera gives information on an external clock or trigger presence	
Factory ID readout	Allows ID and serial number readout	
Customer ID readout/storage	Allows customer ID readout	

Timing

Synchronization Mode

Four different modes may be used under user control.

- The TRIG1 and TRIG2 signals may be used to trigger an external event and control the integration time.
- The Master clock is either external or internal.
- Times are given in seconds or in number of master clock periods (MCP). M.C.P is 33 nsecs when master clock frequency is 30 MHz

Free Run Mode

Integration time is set by the serial line.

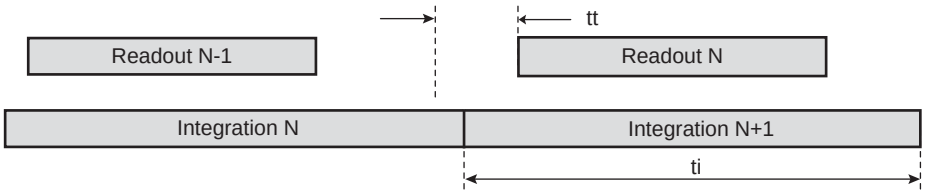
The integration and readout periods start automatically and immediately after the previous period. The readout time depends on the pixel number and pixel rate.

Table 7. Timing Specification

Label	Description	Min	Typ	Max
ti	Integration time duration	(1)	–	32 ms
tt	Integration period to readout delay at master clock H	–	21 MCP	–
tt	Integration period to readout delay at master clock H/2	–	44 MCP	–
tt	Integration period to readout delay at master clock H/4	–	90 MCP	–

Note: 1. The Integration time is set by the serial line and should be higher than the readout time + tt (otherwise it is adjusted to the readout time + tt).

Figure 4. Timing Diagram



Trigger Mode

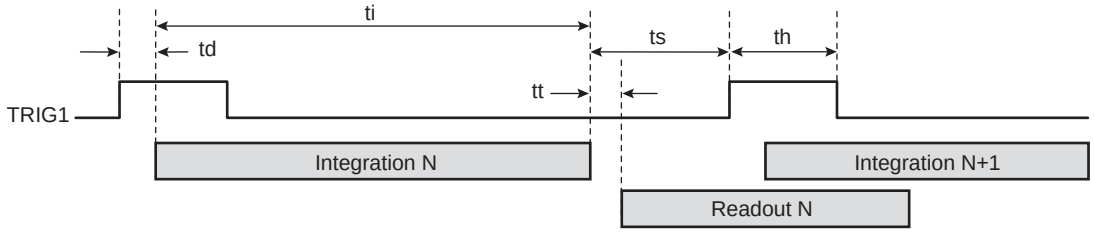
The integration period starts immediately after the rising edge of TRIG1 input signal. The integration time is set by the serial line. This integration period is immediately followed by a readout period. The readout time depends on the pixel number and the pixel rate.

A 270 ns jitter may occur between the rising edge of TRIG1 and the beginning of real integration time.

Table 8. Timing Specification: Selected output data rate = master clock

Label	Description	Min	Typ	Max
ti	Integration time duration	1,9 µs	–	32 ms
td	TRIG1 rising to integration period delay	–	21 MCP	–
tt	Integration period stop to readout delay	–	See Table 7	–
ts	Integration period to TRIG1 rising set-up time	80 MCP	–	–
th	TRIG1 hold time (pulse high duration)	8 MCP	–	–

Figure 5. Timing Diagram



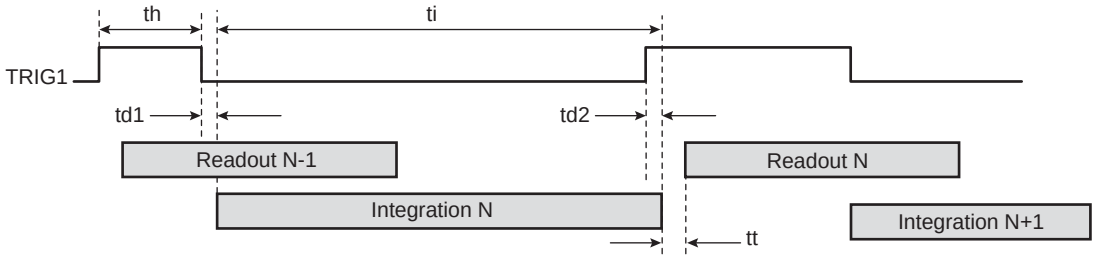
ITC Mode (One Signal)

In the Integration Time Control (ITC) mode, the integration period starts immediately after the falling edge of TRIG1 input signal and stops immediately after the rising edge of TRIG1 input signal. It is immediately followed by a readout period. The readout time depends on the pixel number and pixel rate.

Table 9. Timing Specification: Selected output data rate period = Master Clock

Label	Description	Min	Typ	Max
ti	Integration time duration	1,9 µs	–	–
td1	TRIG1 falling to starting integration period delay	–	21 MCP	–
td2	TRIG1 rising to ending integration period delay	–	39 MCP	–
tt	Integration period to readout delay	–	See Table 7	–
th	TRIG1 hold time (pulse high duration)	8 MCP	–	–

Figure 6. Timing Diagram



ITC Mode (Two Signals)

The TRIG2 rising edge starts the integration period.

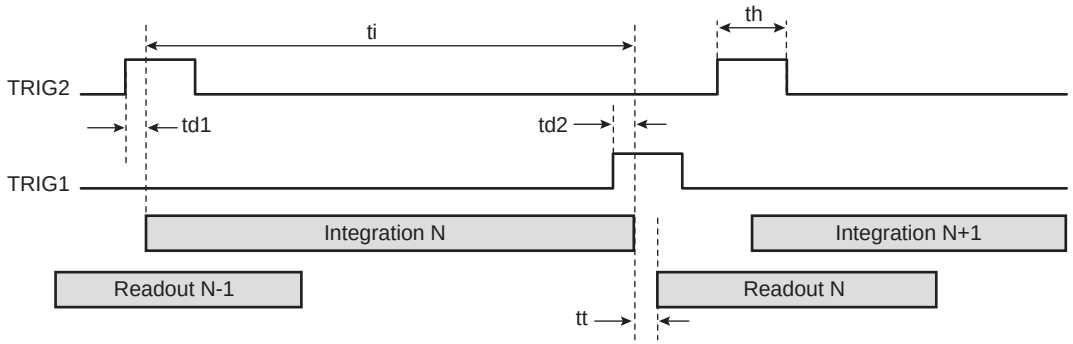
The TRIG1 rising edge stops the integration period.

This period is immediately followed by a readout period.

Table 10. Timing Specification : Selected Output Data Rate = Master Clock

Label	Description	Min	Typ	Max
ti	Integration time duration	1,9 µs	–	–
td1	TRIG2 rising to starting integration period delay	–	21 MCP	–
td2	TRIG1 rising to ending integration period delay	–	39 MCP	–
tt	Integration period to readout delay	–	See Table 7	–
th	TRIG1 and TRIG2 hold time (pulse high duration)	8 MCP	–	–

Figure 7. Timing Diagram

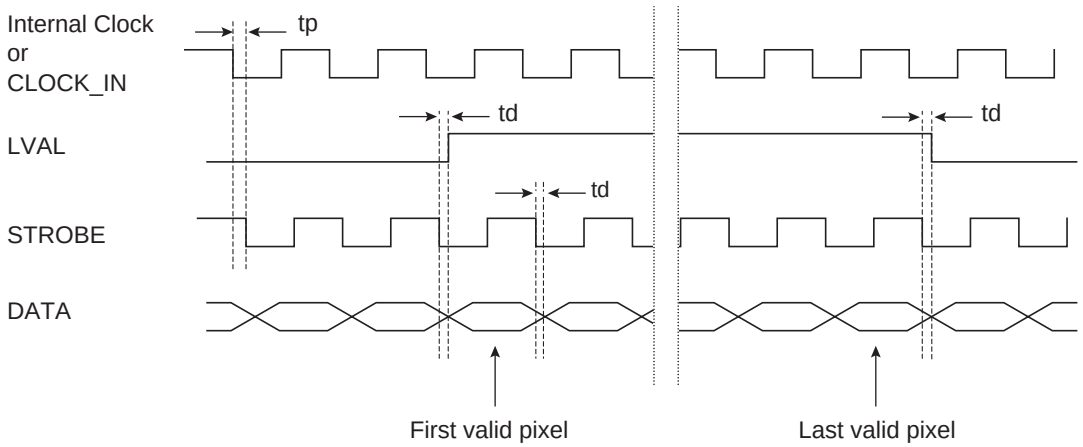


Output Data Timing

Table 11. Timing Specification

Label	Description	Min	Typ	Max
tp	Input to output clock propagation delay	–	5 µs	–
td	STROBE to synchronize signal delay	–	1.8 µs	–

Figure 8. Timing Diagram



Note: DVAL, as defined in the CameraLink standard is active at high level

Electrical Interface

Power Supply

It is recommended to insert a 1A fuse between the power supply and the camera. The voltage ripple of the power supply should be below ±50 mVp-p at BW = 50MHz for full camera performance.

Table 12. Power Supply

Signal Name	I/O	Type	Description
PWR	P	–	DC power input: +12 to +24V
GND	P	–	Electrical and mechanical ground

Note: I = input, O = output, IO = bi-directional signal, P = power/ground, NC = not connected

Command and Control

The CameraLink interface provides four LVDS signals dedicated to camera control (CC1 to CC4). On the AViiVA, three of them are used to synchronize the camera on external events.

1. FVAL, as defined in the CameraLink standard, is not used. FVAL is permanently tied to 0 (low) level.
2. CC3 is not used

Table 13. Signal Definitions

Signal Name	I/O[2]	Type	Description
TRIG1	I	RS644	CC1 – Synchronization input[1]
TRIG2	I	RS644	CC2 – Start Integration period in dual synchro mode[1]
CLOCK_IN	I	RS644	CC4 – External clock for (multi-) camera synchronization[1]

Notes: 1. Refer to “Synchronization Mode” on page 8.
2. I = input, O = output, IO = bi-directional signal, P = power/ground, NC = not connected

Video Data

Data and enable signals are provided on the CameraLink interfaces.

1. FVAL, as defined in the CameraLink standard, is not used. FVAL is permanently tied to 0 (low) level.
2. DVAL, as defined in the CameraLink standard, when used is active at high level.

Table 14. Video Data

Signal Name	I/O[2]	Type	Description
OUT1-D[9-0]	O	RS644	Out 1 pixel data, OUT1-0 = LSB, OUT1-9 = MSB[1]
OUT2-D[9-0]	O	RS644	Out 2 pixel data, OUT2-0 = LSB, OUT2-9 = MSB[1]
OUT3-D[9-0]	O	RS644	Out 3 pixel data, OUT3-0 = LSB, OUT3-9 = MSB[1]
OUT4-D[9-0]	O	RS644	Out 4 pixel data, OUT4-0 = LSB, OUT4-9 = MSB[1]
STROBE	O	RS644	Output data clock, data valid on the rising edge[1]
LVAL	O	RS644	Line valid or line enable, active high signal[1]
DVAL	O	RS644	Data valid, active high signal

Notes: 1. Refer to “Output Data Timing” on page 11
2. I = input, O = output, IO = bi-directional signal, P = power/ground, NC = not connected

Serial Communication

The CameraLink interface provides two LVDS signal pairs for the communication between the camera and the frame grabber. This is an asynchronous serial communication based on the RS-232 protocol.

The configuration of the serial line is:

- Full duplex/without handshaking
- 9600 bauds, 8-bit data, no parity, 1 stop bit.

Table 15. Signal Definition

Signal Name	I/O	Type	Description
SerTFG	O	RS644	Differential pair for serial communication to the frame grabber
SerTC	I	RS644	Differential pair for serial communication from the frame grabber

The camera will be delivered with:

- Software dedicated to camera control.
- .dll and .h files to allow camera control in a customer development software.

Connector Description

All connectors are on the rear panel. Better results are obtained by using shielded cables (foil and braid).

CameraLink Connector

Standard CameraLink cables should be used to ensure the full electrical compatibility.

Camera connector type: 2 x MDR-26 (female) ref. 10226-2210VE

Cable connector type: Standard CameraLink cable should be used (ex. 3M™ – 14B26-SZLB-x00-OLC)

Table 16. CameraLink Connector

Signal	Pin	Signal	Pin
GND	1	GND	14
X0-	2	X0+	15
X1-	3	X1+	16
X2-	4	X2+	17
Xclk-	5	Xclk+	18
X3-	6	X3+	19
SerTC+	7	SerTC-	20
SerTFG-	8	SerTFG+	21
CC1-	9	CC1+	22
CC2+	10	CC2-	23
CC3-	11	CC3+	24
CC4+	12	CC4-	25
GND	13	GND	26

Bit Assignment

This bit assignment is compliant with CameraLink specifications in the **Medium Configuration with two cables** (see AIA CameraLink documentation).

Power Supply

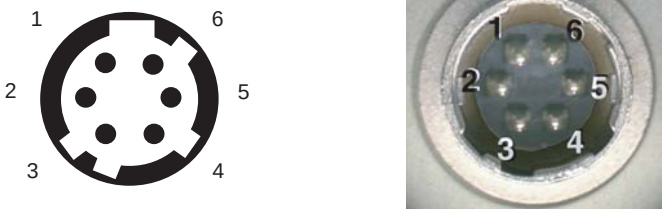
Camera connector type: Hirose HR10A-7R-6PB (male)

Cable connector type: Hirose HR10A-7P-6S (female), one connector is delivered with each camera.

Table 17. Power Connector J01

Signal	Pin	Signal	Pin
PWR	1	GND	4
PWR	2	GND	5
PWR	3	GND	6

Figure 9. Receptacle Viewed from the Rear of the Camera



Ordering Codes

Table 18. Cameras

Item	Part Number
AVIIVA M4 CameraLink 2048 pixels 14 µm	AT71XM4CL2014-BA0
AVIIVA M4 CameraLink 6144 pixels 7 µm	AT71XM4CL6007-BA0
AVIIVA M4 CameraLink 8192 pixels 7 µm	AT71XM4CL8007-BA0

Note: The cameras are delivered with a power supply connector.

Table 19. Optical Mount

Item	Part Number
F Mount for Aviiva M4 2k or 6k	AT71-AVIIVAX4-F
T2 Mount for Aviiva M4 2k or 6k	AT71-AVIIVAX4-T2
M72 x 0.75 Mount for Aviiva M4 8k	AT71-AVIIVAX4-M72

Note: The cameras are delivered without an optical mount.

Table 20. BG38 Filters

Item	Part Number
Kit BG38 for 2k and 6k	AT71ABG38AVIVX4-6K
Kit BG38 for 8k	AT71ABG38AVIVX4-8K

Note: Filters are held by an optical mount

Table 21. Accessories

Item	Part Number
2 CameraLink cables (5 meters long)	AT71KAVIIVA-X4-CL
Optional heatsink	Please contact factory

Mechanical Characteristics

Weight

The camera typical weight (without lens) is 500g (TBC).

Dimensions

Figure 10. 2k

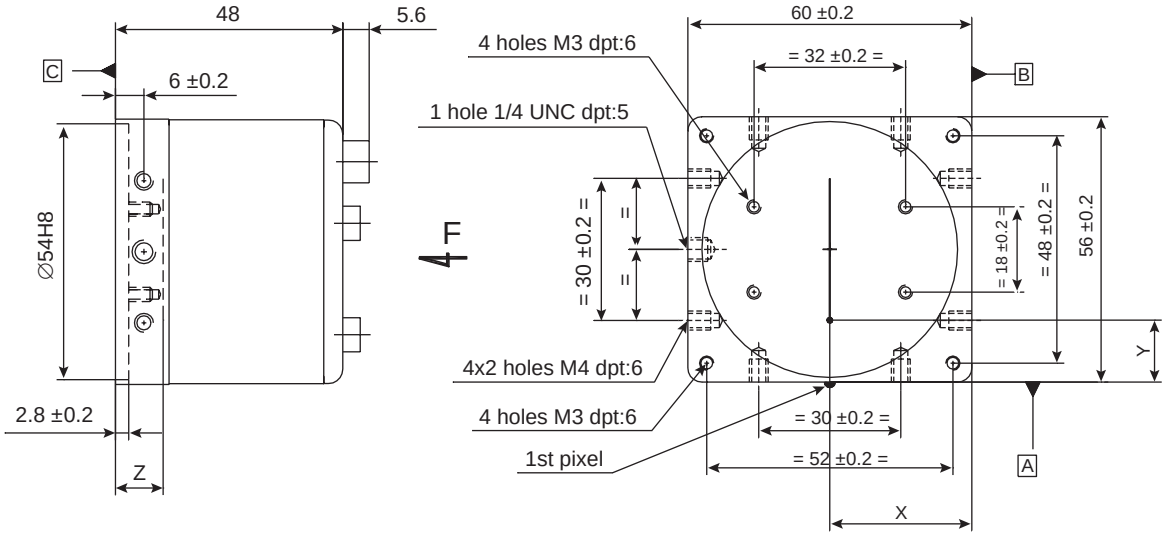


Figure 11. 6k and 8k

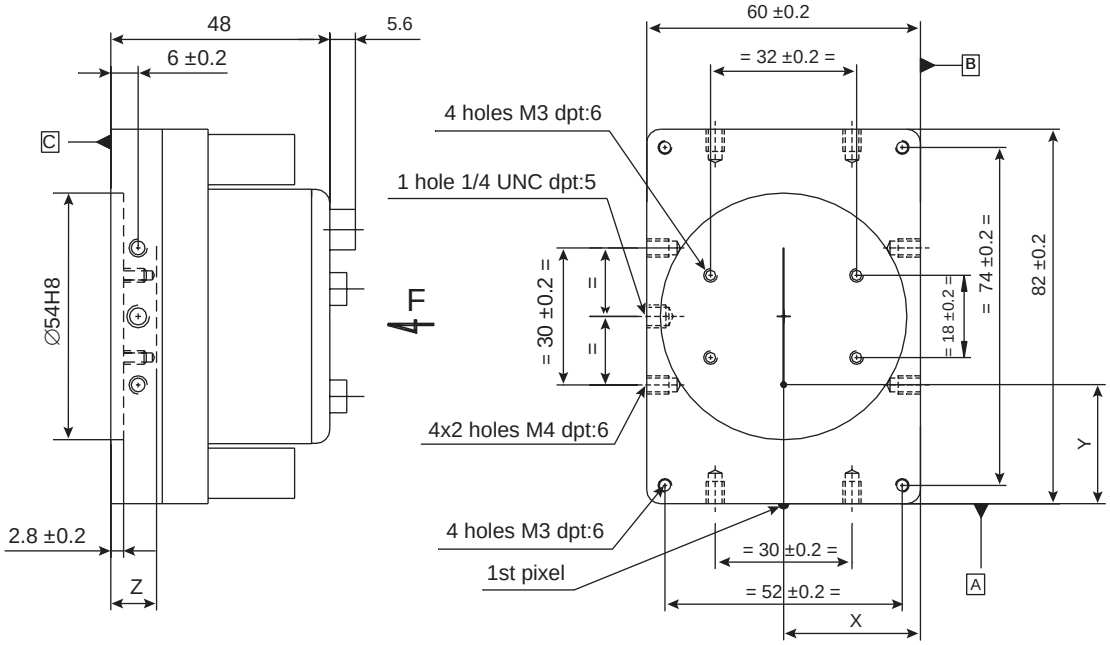
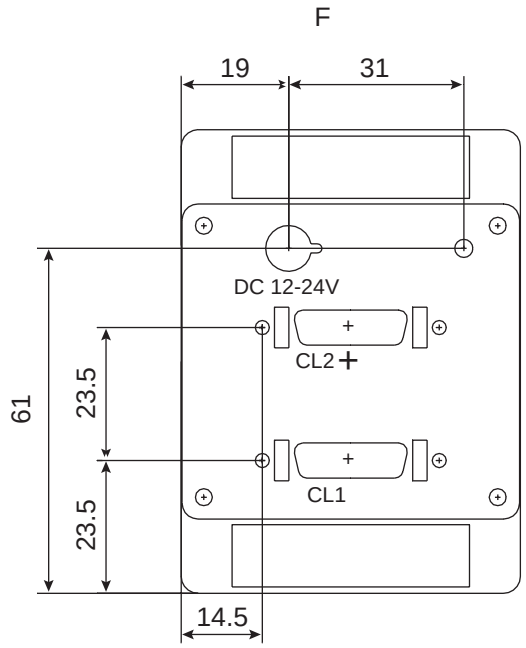


Figure 12. Rear Face



Note: The 2k rear face doesn't have the two heat sinks.

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