National Semiconductor

July 1994

54VHC/74VHC00•54VHCT/74VHCT00 Quad 2-Input NAND Gate

General Description

The VHC/VHCT00 is an advanced high-speed CMOS 2-Input NAND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

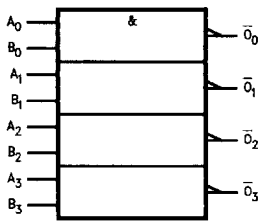
- High speed:
  VHC t_{PD} = 3.7 ns (typ.) at V_{CC} = 5V
  VHCT t_{PD} = 5.0 ns (typ.) at V_{CC} = 5V
- High noise immunity:
  VHC $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
  VHCT V_{IH} = 2.0V, V_{IL} = 0.8V
- Operating voltage:
  VHC V_{CC} (opr) = 2.0V ~ 5.5V
  VHCT V_{CC} (opr) = 4.5V–5.5V
- Power down protection:
  VHC inputs only
  VHCT inputs and outputs
- Low noise:
  VHC V_{OLP} = 0.3V (typ)
  VHCT V_{OLP} = 0.4V (typ)
- Low power dissipation:
  I_{CC} = 2 μA (max) at T_A = 25°C
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Pin and function compatible with 74HC/HCT00

NOTE:

ADD EXTERNAL PULL UP RESISTOR TO VHCT OUTPUTS TO DRIVE CMOS INPUTS
MILITARY SPECIFICATIONS ARE PRELIMINARY

Logic Symbol

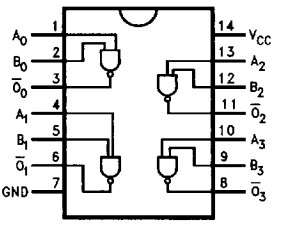
IEEE/IEC



TL/F/11504–1

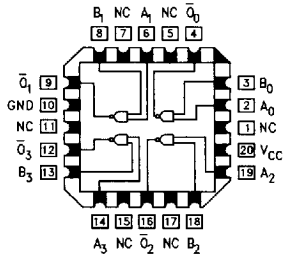
Connection Diagrams

Pin Assignment for DIP, Flatpak, SSOP, TSSOP and SOIC



TL/F/11504–2

Pin Assignment for LCC



TL/F/11504–3

Pin Names	Description
An, Bn	Inputs
On	Outputs

Truth Table

A	B	O
L	L	H
L	H	H
H	L	H
H	H	L

RRD B20M114/Printed in U S A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	
VHC	−0.5V to V_{CC} + 0.5V
VHCT*	−0.5V to 7.0V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	
VHC	±20 mA
VHCT	−20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

*V_{OUT} > V_{CC} only if output is in H state

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
VHC	2.0V to +5.5V
VHCT	4.5V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	
54VHC/VHCT	−55°C to +125°C
74VHC/VHCT	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V (VHC Only)	0 ns/V ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ns/V ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC T_A = 25°C			54VHC T_A = −55°C to +125°C		74VHC T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0–5.5			0.50 0.3 V_{CC}		0.50 0.3 V_{CC}		0.50 0.3 V_{CC}	V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0 4.5	2.58 3.94			3.70		2.48 3.80		V		I_{OH} = −4 mA I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0 4.5			0.36 0.36		0.50 0.50		0.44 0.44	V		I_{OL} = 4 mA I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		160.0		20.0	μA	V_{IN} = V_{CC} or GND	

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Typ	74VHC $T_A = 25°C$ Limit	54VHC $T_A = -55°C$ to $+125°C$ Limit	74VHC $T_A = -40°C$ to $+85°C$ Limit	Units	Conditions
*V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.3	0.8			V	$C_L = 50$ pF
*V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.3	−0.8			V	$C_L = 50$ pF
*V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0		3.5			V	$C_L = 50$ pF
*V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		1.5			V	$C_L = 50$ pF

*Parameter guaranteed by design

DC Characteristics for 'VHCT Family Devices

Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$ Min	Typ	Max	54VHCT $T_A = -55°C$ to $+125°C$ Min	Max	74VHCT $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions	
V_{IH}	High Level Input Voltage	4.5 5.5	2.0 2.0					2.0 2.0		V		
V_{IL}	Low Level Input Voltage	4.5 5.5			0.8 0.8				0.8 0.8	V		
V_{OH}	High Level Output Voltage	4.5	3.15	3.65				3.15		V	$V_{IN} = V_{IH}$	$I_{OH} = -50\ \mu A$
		4.5	2.5					2.4		V		$I_{OH} = -8$ mA
V_{OL}	Low Level Output Voltage	4.5		0.0	0.1				0.1	V	$V_{IN} = V_{IH}$	$I_{OL} = 50\ \mu A$
		4.5			0.36				0.44	V		$I_{OL} = 8$ mA
I_{IN}	Input Leakage Current	0–5.5			±0.1				±1.0	μA	$V_{IN} = 5.5V$ or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0				20.0	μA	$V_{IN} = V_{CC}$ or GND	
I_{CCT}	Maximum I_{CC}/ Input	5.5			1.35				1.50	mA	$V_{IN} = 3.4V$ Other Inputs = V_{CC} or GND	
I_{OPD}	Output Leakage Current (Power Down State)	0.0			0.5				5.0	μA	$V_{OUT} = 5.5V$	

DC Characteristics for 'VHCT Family Devices

Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$ Typ	74VHCT $T_A = 25°C$ Limit	54VHCT $T_A = -55°C$ to $+125°C$ Limit	74VHCT $T_A = -40°C$ to $+85°C$ Limit	Units	Conditions
*V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.4	0.8			V	C_L = 50 pF
*V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		−0.4	−0.8			V	C_L = 50 pF
*V_{IHD}	Minimum High Level Dynamic Input Voltage			2.0			V	C_L = 50 pF
*V_{ILD}	Maximum Low Level Dynamic Input Voltage			0.8			V	C_L = 50 pF

*Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Min	Typ	Max	54VHC $T_A = -55°C$ to $+125°C$ Min	Max	74VHC $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions
t_{PLH}, t_{PHL}	Propagation Delay	3.3 ±0.3		5.5	7.9			1.0	9.5	ns	C_L = 15 pF
				8.0	11.4			1.0	13.0		C_L = 50 pF
		5.0 ±0.5		3.7	5.5			1.0	6.5	ns	C_L = 15 pF
				5.2	7.5			1.0	8.5		C_L = 50 pF
C_{IN}	Input Capacitance			4	10				10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			19						pF	(Note 1)

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/4 (per gate).

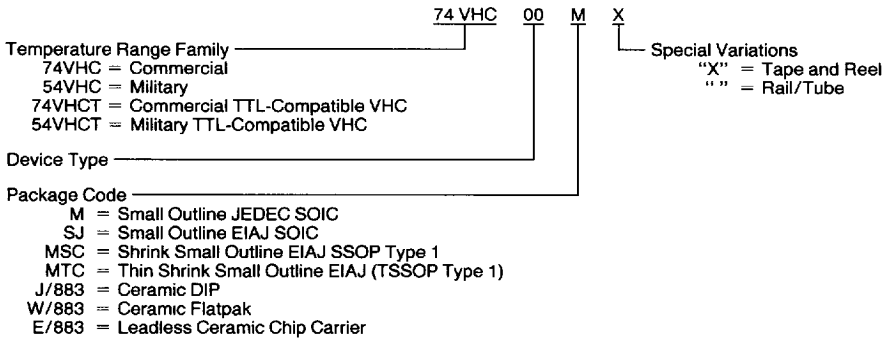
AC Electrical Characteristics for 'VHCT Family Devices

Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$ Min	Typ	Max	54VHCT $T_A = -55°C$ to $+125°C$ Min	Max	74VHCT $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions
t_{PLH}, t_{PHL}	Propagation Delay	5.0 ±0.5		5.0	6.9			1.0	8.0	ns	C_L = 15 pF
				5.5	7.9			1.0	9.0		C_L = 50 pF
C_{IN}	Input Capacitance			4	10				10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			17						pF	(Note 1)

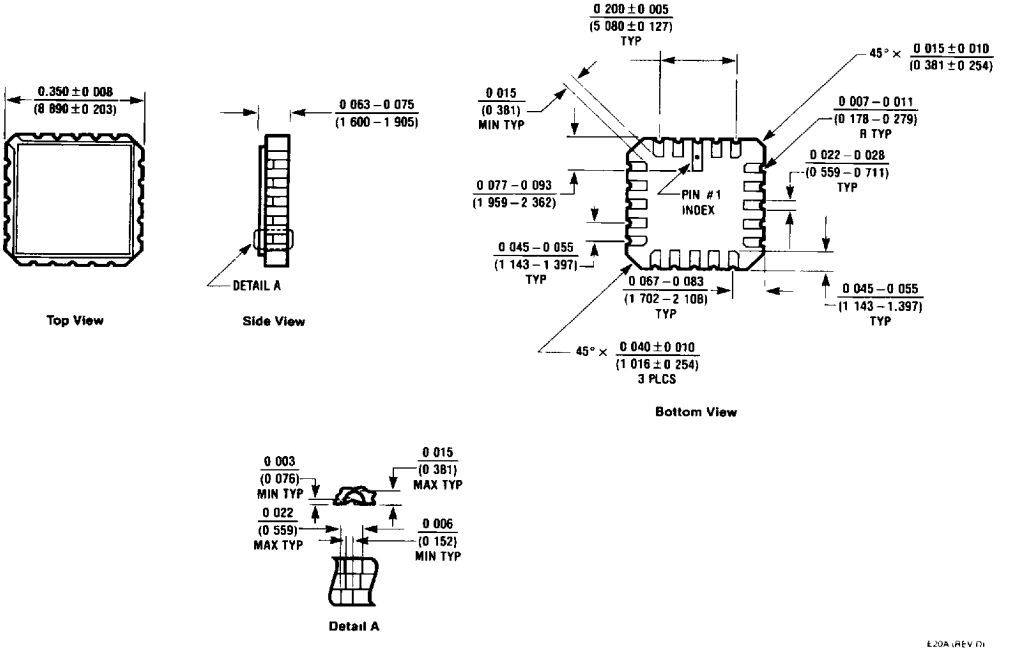
Note 1: C_{PD} is defined as the value of the internal equivalent capacitance, which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/4 (per gate)

Ordering Information

The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:



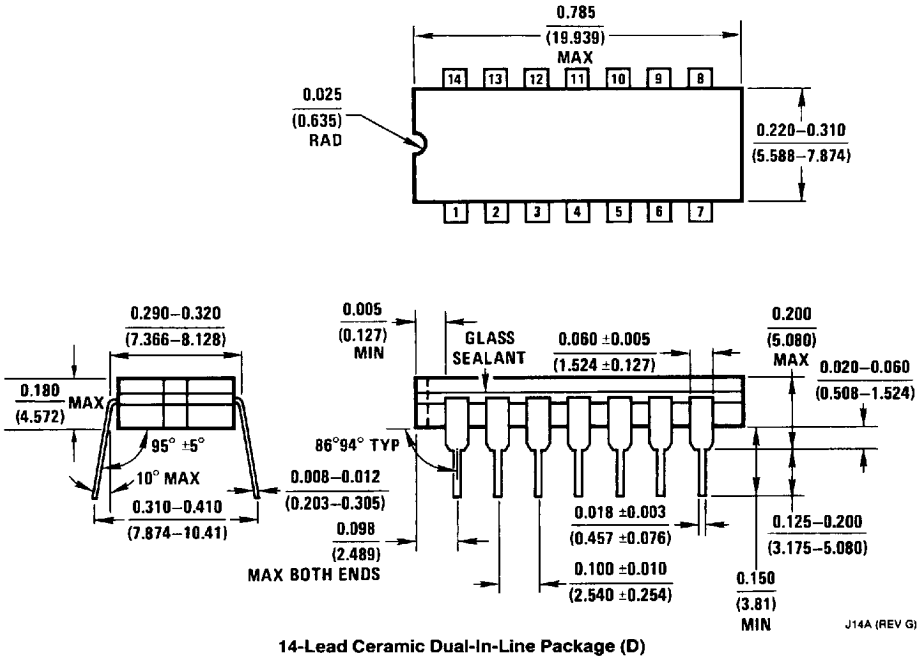
Physical Dimensions inches (millimeters)



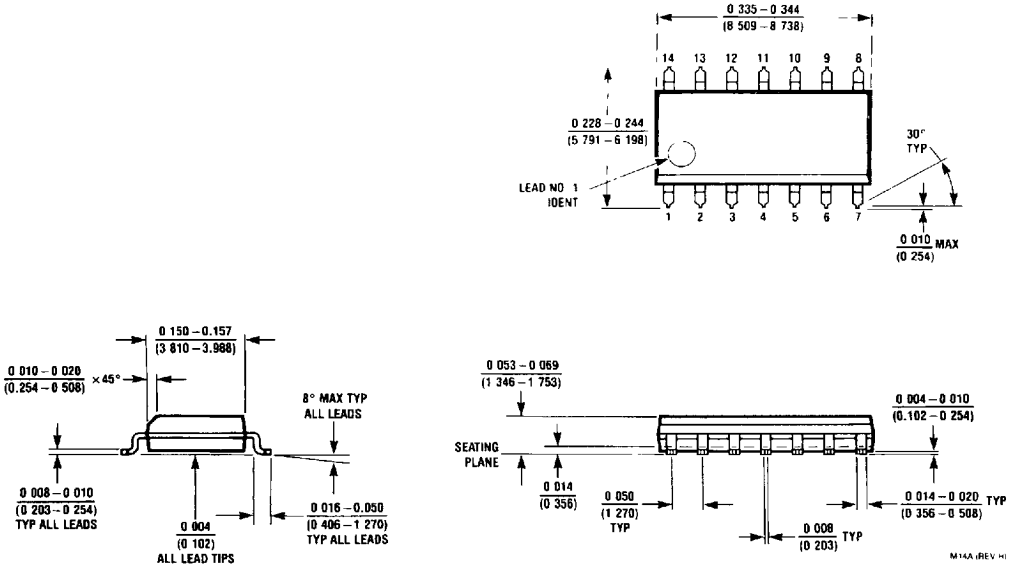
E20A (REV D)

20-Lead Ceramic Leadless Chip Carrier, Type C (L)
Order Number 54VHC00E/883 or 54VHCT00E/883
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)

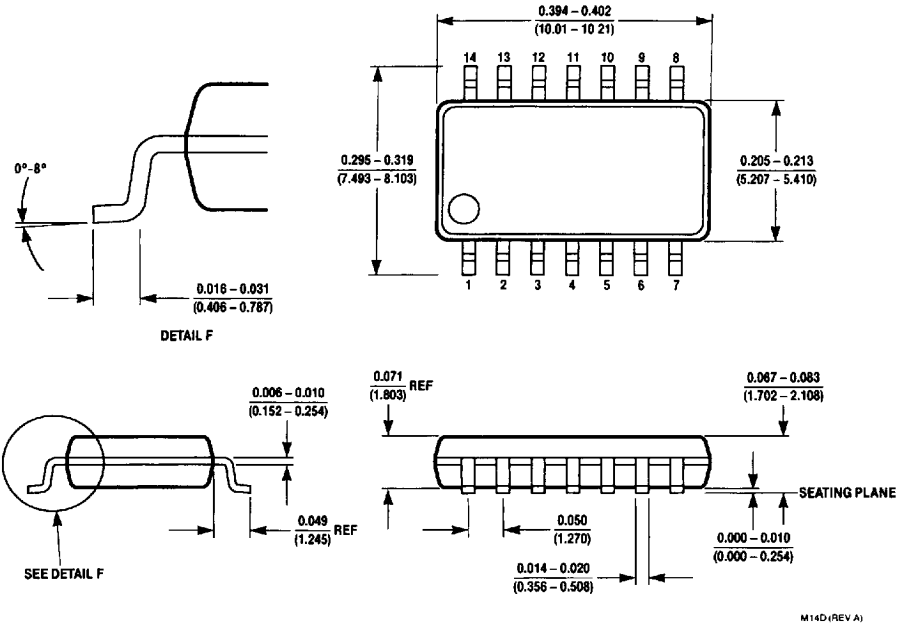


14-Lead Ceramic Dual-In-Line Package (D)
Order Number 54VHC00J/883 or 54VHCT00J/883
NS Package Number J14A

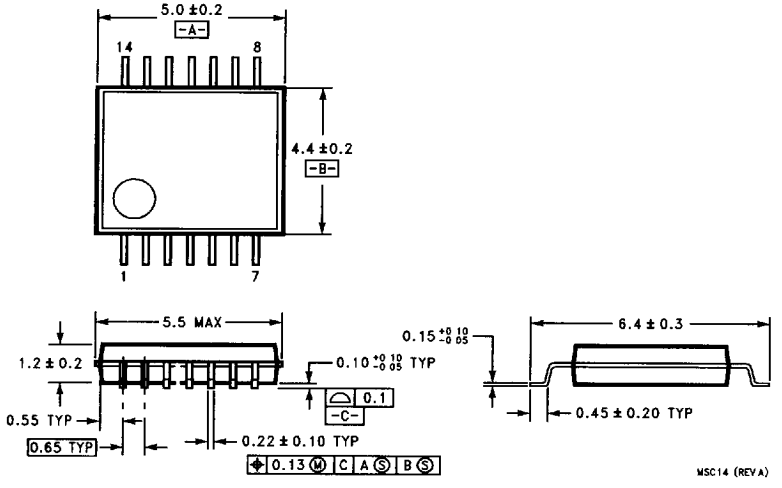


14-Lead Small Outline Integrated Circuit—JEDEC (M)
Order Number 74VHC00M, 74VHC00MX, 74VHCT00M or 74VHCT00MX
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)

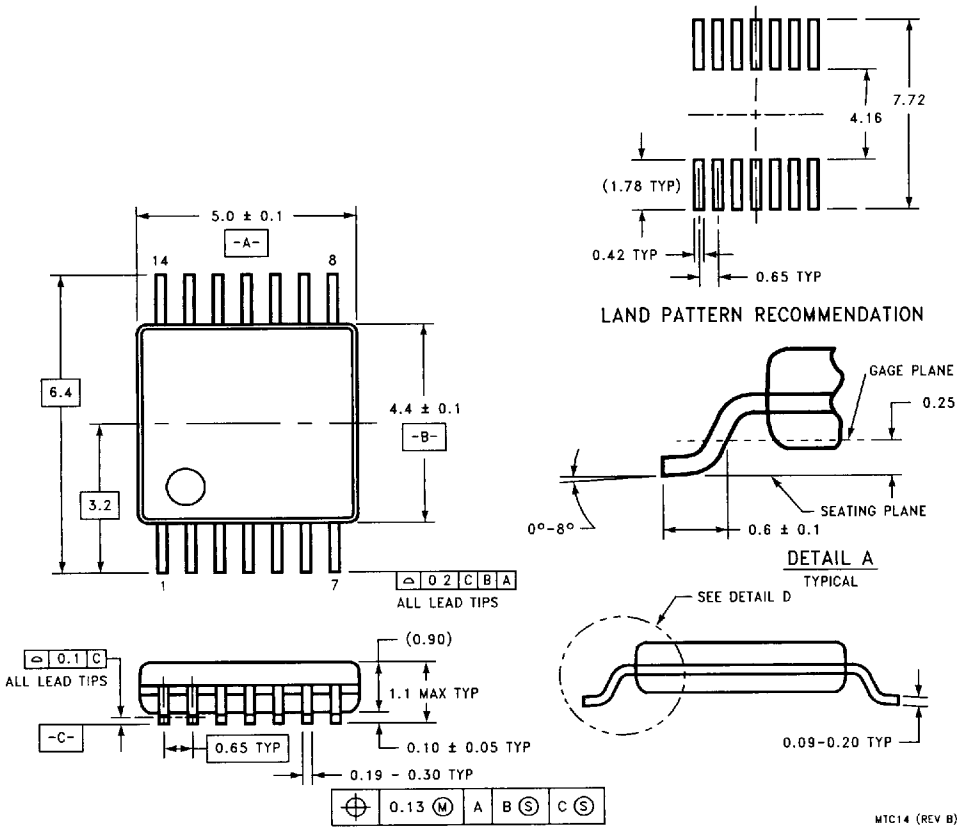


14-Lead Plastic EIAJ SOIC (SJ)
Order Number 74VHC00SJ, 74VHC00SJX, 74VHCT00SJ or 74VHCT00SJX
NS Package Number M14D



14-Lead Plastic EIAJ SSOP Type I (MSC)
Order Number 74VHC00MSCX or 74VHCT00MSCX
NS Package Number MSC14

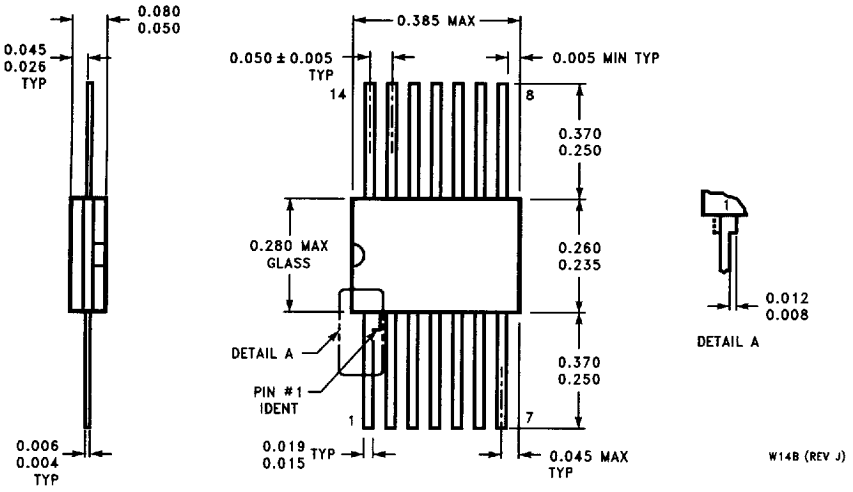
Physical Dimensions inches (millimeters) (Continued)



14-Lead Plastic EIAJ TSSOP Type 1 (MTC)
Order Number 74VHC00MTC, 74VHC00MTCX, 74VHCT00MTC or 74VHCT00MTCX
NS Package Number MTC14

Physical Dimensions inches (millimeters) (Continued)

Lit. # 118000-002



14-Lead Cerpack (F)
Order Number 54VHC00W/883 or 54VHCT00W/883
NS Package Number W14B

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