PowerNP™ NPe405H Embedded Processor Data Sheet

Features

- IBM PowerPC™ 405 32-bit RISC processor core operating up to 266 MHz
- PC-100 Synchronous DRAM (SDRAM) interface operating up to 133 MHz
  - 32-bit interface for non-ECC applications
  - 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
- External Peripheral Bus
  - Flash ROM/Boot ROM interface
  - Direct support for 8-, or 16-, or 32-bit SRAM and external peripherals
  - Up to 8 banks
  - External Mastering supported
- DMA support for external peripherals, internal UARTs and memory
  - Scatter-gather chaining supported
  - Four channels
- PCI Revision 2.2 Compliant Interface (32-bit, up to 66 MHz)
  - Asynchronous PCI Bus interface
  - Internal PCI Bus Arbiter which can be disabled for use with an external arbiter
- Up to4 Ethernet 10/100 Mbps (full-duplex) units with a choice of MII, RMII, or SMII interfaces.
- HDLC interface with 32 channels through 2 ports
- HDLC interface with 8 channels through 8 ports
- Programmable Interrupt Controllers supports interrupts from a variety of sources
  - Seven external and 49 internal
  - Edge triggered or level-sensitive
  - Positive or negative active
  - Non-critical or critical interrupt to processor core
  - Programmable critical interrupt priority ordering
  - Programmable critical interrupt vector for faster vector processing
- Programmable Timers
- Two serial ports (16550 compatible UART)
- One IIC (I^2C) interface
- General Purpose I/O (GPIO) available
- Supports JTAG for board level testing
- Internal Processor Local Bus (PLB) runs at SDRAM interface frequency
- Supports PowerPC processor boot from PCI memory
- User accessible performance counters

Description

Designed specifically to address embedded applications, the NPe405H provides a high-performance, low-power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and intrinsically lower power dissipation requirements.

This chip contains a high-performance RISC processor core, SDRAM controller, PCI bus interface, Ethernet interfaces, HDLC interfaces, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: IBM CMOS 6SF 0.25 µm (0.18 µm L_{eff})

Package: 580-ball (35mm) enhanced plastic ball grid array (E-PBGA)

Power (estimated): Typical 1.4W, Maximum 2.3W

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Ordering, PVR, and JTAG Information

Product Name	Order Part Number[1]	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
NPe405H		200 MHz	35 mm, 580 E-PBGA		0x414100C0	0x????????
NPe405H		200 MHz	35 mm, 580 E-PBGA		0x414100C0	0x????????
NPe405H		266 MHz	35 mm, 580 E-PBGA		0x414100C0	0x????????
NPe405H		266 MHz	35 mm, 580 E-PBGA		0x414100C0	0x????????

Note 1: Z at the end of the Order Part Number indicates a tape and reel shipping package. Otherwise, the chips are shipped in a tray.

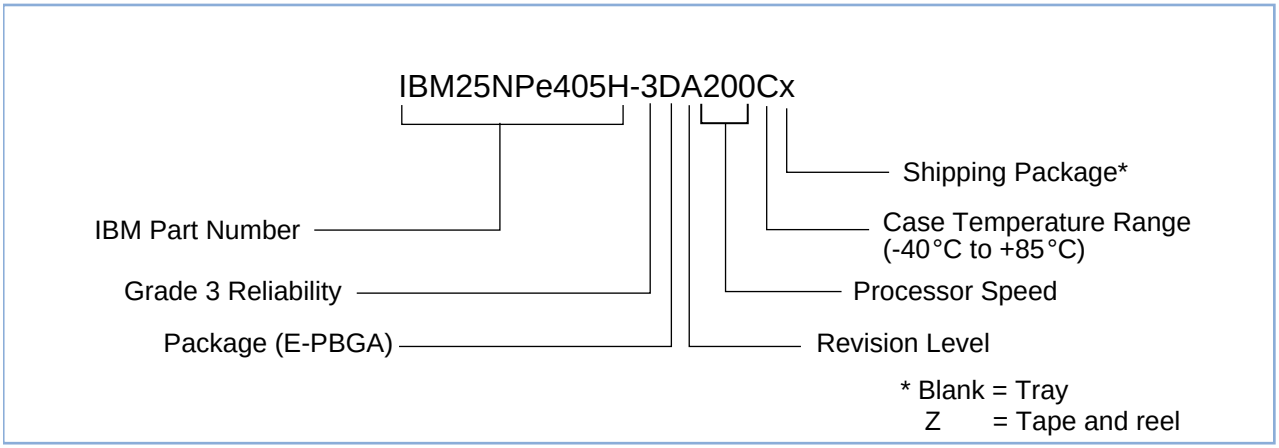
This section provides the part numbering nomenclature for the NPe405H. For availability, contact your local IBM sales office.

The part number contains a part modifier. This modifier provides for identification of future enhancements (for example, higher performance).

Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) is software accessible and contains additional information about the revision level of the part. Refer to the NPe405H User's Manual for details on the register content.

IBM Part Number Key



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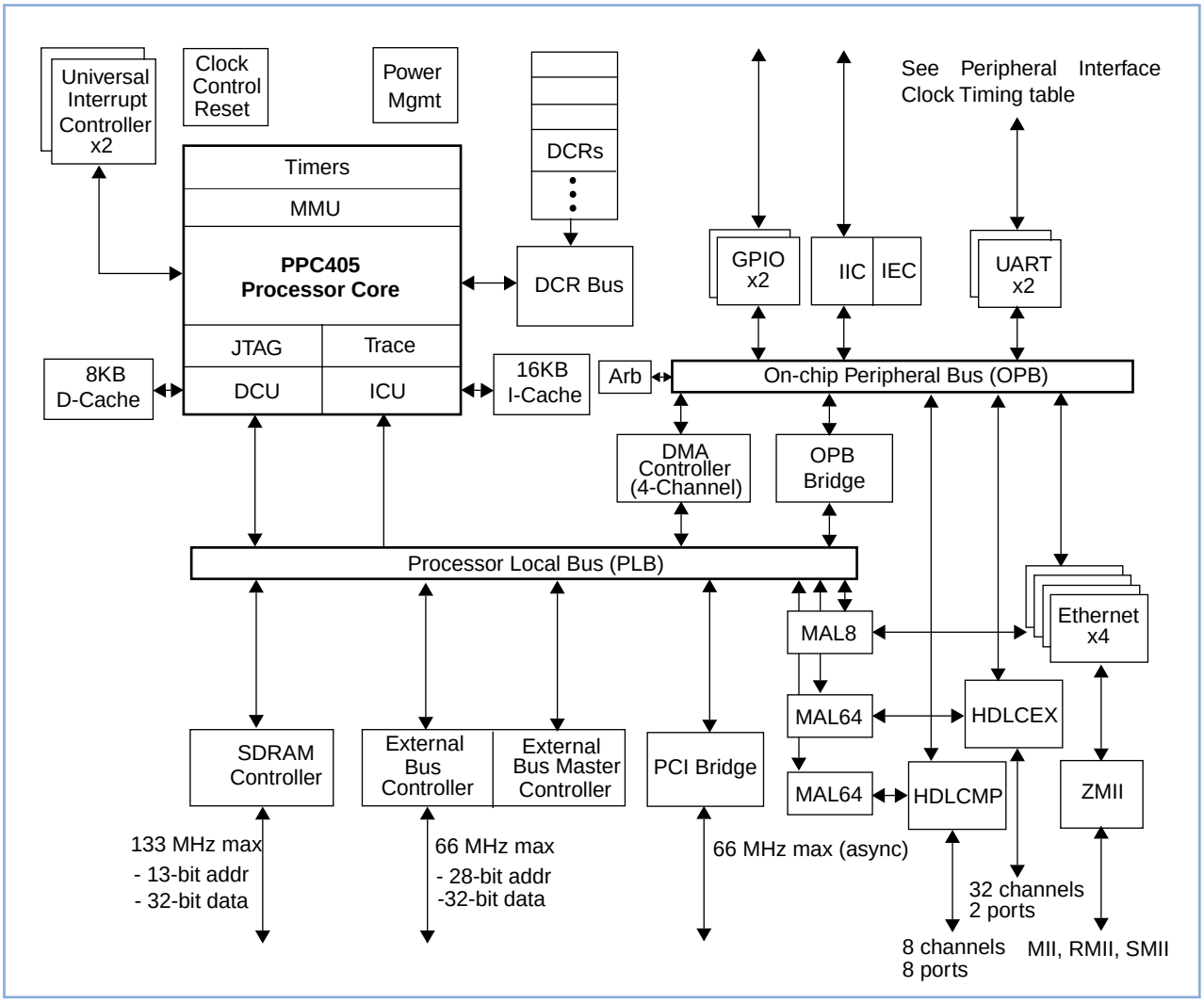
NPe405H Embedded Controller Functional Block Diagram



The NPe405H is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated to create an application-specific ASIC product. This approach provides a consistent way to generate complex ASICs using IBM CoreConnect™ Bus Architecture.

Note: IBM CoreConnect busses provide:

- 64-bit PLB interfaces up to 133MHz
- 32-bit OPB interfaces up to 66MHz

Address Map Support

The NPe405H incorporates two simple and separate address maps. The first is a fixed processor address map that serves the PowerPC family of processors. This address map defines the possible contents of various address regions which the processor can access. The second address map is for Device Configuration Registers (DCR). This address map is accessed by software running on the NPe405H processor through the use of **mtdcr** and **mfdcr** commands.

SysMem Memory Address Map 4GB System Memory

Function	Sub Function	Start Address	End Address	Size
Local Memory/Peripherals[1]		00000000	7FFFFFFF	2GB
PCI	Total	80000000	EF5FFFFF	1.74GB
	PCI Memory	80000000	E7FFFFFF	1.63GB
	PCI I/O	E8000000	E800FFFF	64KB
	Reserved	E8010000	E87FFFFF	
	PCI I/O	E8800000	EBFFFFFF	56MB
	Reserved	EC000000	EEBFFFFF	
	PCI Configuration Registers	EEC00000	EEC00007	8B
	Reserved	EEC00008	EECFFFFF	
	PCI Interrupt Acknowledge	EED00000	EEDFFFFF	1MB
	Reserved	EEE00000	EF3FFFFF	
	PCI local Configuration Registers	EF400000	EF40003F	64B
	Reserved	EF400040	EF5FFFFF	
Internal Peripherals	Total	EF600000	EFFFFFFF	10MB
	UART0	EF600300	EF600307	8B
	Reserved	EF600308	EF6003FF	
	UART1	EF600400	EF600407	8B
	Reserved	EF600408	EF6004FF	
	IIC0	EF600500	EF60051F	32B
	Reserved	EF600520	EF6005FF	
	OPB Arbiter	EF600600	EF60063F	64B
	Reserved	EF600640	EF6006FF	
	SGPIO Controller Registers	EF600700	EF60077F	128B
	CGPIO Controller Registers	EF600780	EF6007FF	128B
	Ethernet 0 Controller Registers	EF600800	EF6008FF	256B
	Ethernet 1 Controller Registers	EF600900	EF6009FF	256B
	Ethernet 2 Controller Registers	EF600A00	EF600AFF	256B
	Ethernet 3 Controller Registers	EF600B00	EF600BFF	256B
	Reserved	EF600C00	EF600C0F	.
	ZMII	EF600C10	EF600C1F	16B
	Reserved	EF600C20	EF60FFFF	
	HDLCEX	EF610000	EF61FFFF	64KB
	HDLCMP	EF620000	EF62FFFF	64KB
	Reserved	EF630000	EFFFFFFF	
Expansion ROM[2]		F0000000	FFDFFFFF	254MB
Boot ROM[2, 3]		FFE00000	FFFFFFFF	2MB

Notes:

1. The Local Memory/Peripheral area of the memory map can be configured for SDRAM, ROM or Peripherals.
2. The Boot ROM and Expansion ROM area of the memory map are intended for use by ROM or Flash-type devices. While locating volatile SDRAM and SRAM in this region is supported by the controller it is not recommended that these regions be used for this purpose.
3. When the optional boot from PCI Memory is selected, the PCI Boot ROM address space begins at FFFE 0000 (size is 128KB).

DCR Address Map 4KB Device Configuration Register

Function	Base Address Strap/Parameter	Start Address(0:9)	End Address(0:9)	Size
DCR Address Space[1]		000	3FF	1KW (4KB)[1]
Reserved		000	00F	16W
Memory Controller Registers		010	011	2W
External Bus Controller Registers		012	013	2W
Reserved		014	07F	108W
PLB Registers		080	08F	16W
Performance Counters		090	091	2W
Reserved		092	09F	14W
OPB Bridge Out Registers		0A0	0A7	8W
Reserved		0A8	0AF	8W
Clock, Control and Reset		0B0	0B7	8W
Power Management		0B8	0BF	8W
Interrupt Controller 0		0C0	0CF	16W
Interrupt Controller 1		0D0	0DF	16W
Reserved		0E0	0EF	16W
Miscellaneous		0F0	0FF	16W
DMA Controller Registers		100	13F	64W
Reserved		140	17F	64W
MAL8 Registers (Ethernet)		180	1FF	128W
MAL64 Registers (HDLCEX)		200	27F	128W
MAL64 Registers (HDLCMP)		280	2FF	128W
Reserved		300	3FF	256W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

PLB to PCI Interface

The PLB to PCI interface core provides a mechanism for connecting PCI devices to the local PowerPC processor and local memory. This interface is compliant with version 2.2 of the PCI Specification.

Features include:

- Internal PCI bus arbiter for up to six external devices at PCI bus speeds up to 66 MHz. Internal arbiter use is optional and can be disabled for systems which employ an external arbiter.
- PLB 3.0 Compliant
- PLB bus frequency up to 133 MHz
- 64-bit PLB Master
- 32-bit PLB Slave
- PCI bus frequency up to 66 MHz
  - Asynchronous operation from 1/8 PLB frequency to 66 MHz maximum
- 32-bit PCI Address/Data Bus
- Power Management:
  - PCI Bus Power Management v1.1 compliant
- Supports 1:1, 2:1, 3:1, 4:1 clock ratios from PLB to PCI
- Buffering between PLB and PCI:
  - PCI Target 64-byte write post buffer
  - PCI Target 96-byte read prefetch buffer
  - PLB Slave 8-byte write post buffer
  - PLB Slave 64-byte read prefetch buffer
- Error tracking/status
- Supports PCI Target side configuration
- Supports processor access to all PCI address spaces:
  - Single-byte PCI I/O reads and writes
  - PCI memory single-beat and prefetch-burst reads and single-beat writes
  - Single-byte PCI configuration reads and writes (type 0 and type 1)
  - PCI interrupt acknowledge
  - PCI special cycle
- Supports PCI target access to all PLB address spaces
- Supports PowerPC processor boot from PCI memory

SDRAM Memory Controller

The NPe405H Memory Controller core provides a low latency access path to SDRAM memory. A variety of system memory configurations are supported. The memory controller supports up to four logical banks. Up to 256 MB per bank are supported, up to a maximum of 1 GB. Memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 addressing for SDRAM (2- and 4-bank)
- Memory bus operates at same frequency as PLB
- 32-bit memory interface support
- Programmable address compare for each bank of memory
  - 4 GB of address space
- Industry standard 168-pin DIMMS are supported (some configurations)
- Up to 133 MHz Memory, includes PC133 support
- 4 MB to 256 MB per bank
- Programmable address mapping and timing
- Auto refresh
- Page Mode Accesses with up to 4 open pages
- Sync DRAM configuration via mode set command
- Power Management (self-refresh)
- Error Checking and Correction (ECC) support
  - Standard SEC/DED coverage
  - Aligned nibble error detect
  - Address error logging
  - Mixed ECC/non-ECC banks
  - Bypass mode

External Peripheral Bus Controller (EBC)

- Up to eight ROM, EPROM, SRAM, Flash, and Slave Peripheral I/O banks supported
- Up to 66 MHz operation
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus width support
- Latch data on Ready, Synchronous or Asynchronous

- Programmable 2K clock time-out counter with disable for Ready
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- Peripheral Device pacing with external “Ready”
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for own access and control

DMA Controller

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 32-bit addressing
- Address increment or decrement
- Internal 32-byte data buffering capability
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

UART

- Two 8-pin UART interfaces provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16550 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with 16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC Bus Interface

- Compliant with Phillips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

IIC EEPROM Controller

Supports setting of default initial conditions from serial EEPROM during system reset.

HDLCEX Interface

- Multichannel HDLC controller core
- Two full-duplex Pulse Code Modulation (PCM) Highway ports at speeds up to 8 Mbps
- 32 transmit and 32 receive channels

- Supports HDLC protocol as well as a Transparent mode
- One channel per port, autonomous management of the I-Frame and S-Frame of the Normal Response mode (NRM) protocol
- Software emulation of NRM mode

HDLCMP Interface

- HDLC controller core providing eight full-duplex serial ports
- Up to 2Mbps data rate
- Supports HDLC protocol as well as a Transparent mode
- Software emulation of NRM mode

General Purpose IO (GPIO) Controller

- Two GPIO functions
  - System GPIO (SGPIO)
  - Communications GPIO (CGPIO)
- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses
- Most GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose. Both GPIO functions have 32 I/Os.
- Each GPIO output is separately programmable to emulate an open-drain driver (drives to zero, three-stated if output bit is 1)

Universal Interrupt Controller (UIC)

Two cascaded Universal Interrupt Controllers (UICs) provides the control, status, and communications necessary between the various sources of interrupts and the local PowerPC processor.

Features include:

- Supports 7 external and 49 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to PPC405 processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

10/100 Mbps Ethernet MAC

- Four units capable of full- or half-duplex operation at up to 100 Mbps
- ZMII Bridge to external Ethernet PHYs that support
  - Reduced Media Independent Interface (RMII) or Serial Media Independent Interface (SMII) for multiple PHY applications
  - Media Independent Interface (MII) for single PHY applications
- Dedicated DMA channel

JTAG

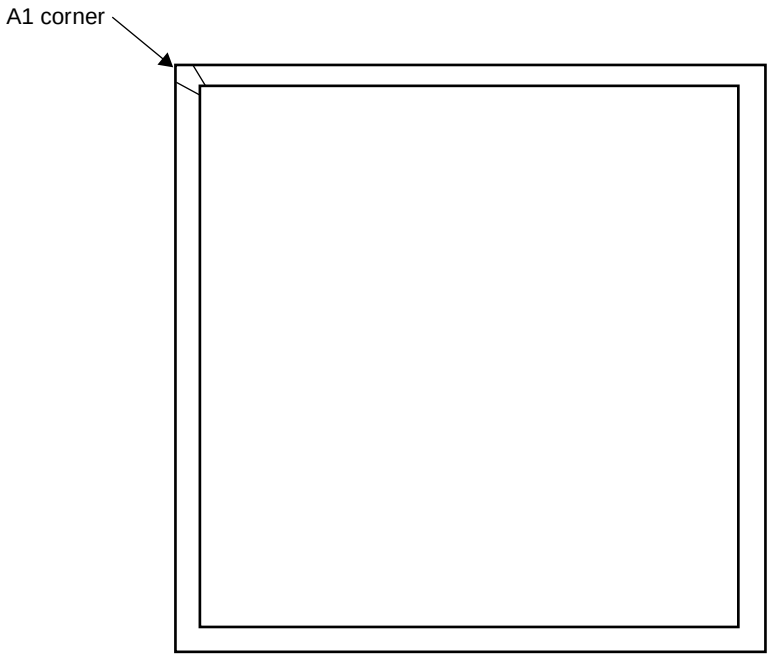
- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

Performance Counters

A series of software accessible PLB transaction event counters that can be used to analyze PLB performance.

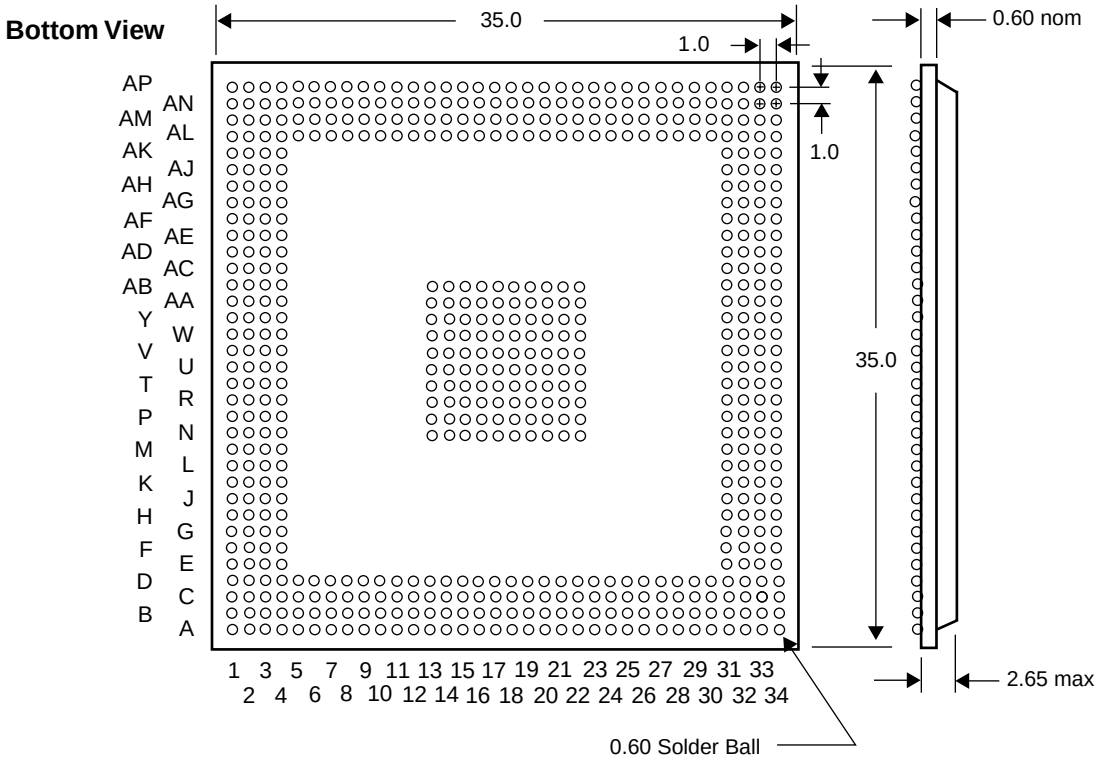
35mm, 580-Ball E-PBGA Package

Top View



Note: All dimensions are in mm.

Bottom View



Pin Lists

The following table lists all the external signals in alphabetical order and shows the ball number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. The page number listed gives the page in “Signal Functional Description” on page 37 where the signals in the indicated interface group begin.

Signals Listed Alphabetically (Part 1 of 12)

Signal Name	Ball	Interface Group	Page
AV_{DD}		Power	45
BA0 BA1		SDRAM	40
$\overline{\text{BankSel0}}$ $\overline{\text{BankSel1}}$ $\overline{\text{BankSel2}}$ $\overline{\text{BankSel3}}$		SDRAM	40
[$\overline{\text{BE0}}$]PCIC0 [$\overline{\text{BE1}}$]PCIC1 [$\overline{\text{BE2}}$]PCIC2 [$\overline{\text{BE3}}$]PCIC3		PCI	37
BusReq		External Master Peripheral	43
$\overline{\text{CAS}}$		SDRAM	40

Signals Listed Alphabetically (Part 2 of 12)

Signal Name	Ball	Interface Group	Page
CGPIO0[HDLCMPTxClk4][PHY1RxD0][PHY1Rx2D0] CGPIO1[HDLCMPTxData4][PHY1RxD1][PHY1Rx2D1] CGPIO2[HDLCMPTxEn4][PHY1RxD2][PHY1Rx3D0] CGPIO3[HDLCMPRxClk4][PHY1RxD3][PHY1Rx3D1] CGPIO4[HDLCMPRxData4][EMC1TxD0][EMC1Tx2D0] CGPIO5[HDLCMPTxClk5][EMC1TxD1][EMC1Tx2D1] CGPIO6[HDLCMPTxData5][EMC1TxD2][EMC1Tx3D0] CGPIO7[HDLCMPTxEn5][EMC1TxD3][EMC1Tx3D1] CGPIO8[HDLCMPRxClk5][PHY1RxErr][PHY1Rx2Er] CGPIO9[HDLCMPRxData5][PHY1CrS3DV][PHY1RxDV] CGPIO10[HDLCMPTxClk6][PHY1CrS][PHY1CrS2DV] CGPIO11[HDLCMPTxData6][EMC1TxErr][EMC1Tx3En] CGPIO12[HDLCMPTxEn6][EMC1TxEn][EMC1Tx2En] CGPIO13[HDLCMPRxClk6][PHY1RxClk] CGPIO14[HDLCMPRxData6][PHY1Col][PHY1Rx3Er] CGPIO15[HDLCMPTxClk7] CGPIO16[HDLCMPTxData7] CGPIO17[HDLCMPTxEn7][PHY1TxClk] CGPIO18[HDLCMPRxClk7] CGPIO19[HDLCMPRxData7] CGPIO20[HDLCMPTxEn0][$\overline{\text{UART1\_CTS}}$] CGPIO21[HDLCMPTxEn1][$\overline{\text{UART1\_DSR}}$] CGPIO22[HDLCMPTxEn2][$\overline{\text{UART1\_DCD}}$] CGPIO23[HDLCMPTxEn3][$\overline{\text{UART1\_RI}}$] CGPIO24[HDLCEXTxEnA][$\overline{\text{UART1\_RTS}}$] CGPIO25[HDLCEXTxEnB][$\overline{\text{UART1\_DTR}}$] CGPIO26[$\overline{\text{UART0\_CTS}}$] CGPIO27[$\overline{\text{UART0\_DSR}}$] CGPIO28[$\overline{\text{UART0\_DCD}}$] CGPIO29[$\overline{\text{UART0\_RI}}$] CGPIO30[$\overline{\text{UART0\_RTS}}$] CGPIO31[$\overline{\text{UART0\_DTR}}$]		System	45
ClkEn0 ClkEn1		SDRAM	40
[$\overline{\text{DMAAck0}}$]SGPIO13 [$\overline{\text{DMAAck1}}$]SGPIO14 [$\overline{\text{DMAAck2}}$]SGPIO15 [$\overline{\text{DMAAck3}}$]SGPIO16		External Slave Peripheral	41
[$\overline{\text{DMAReq0}}$]SGPIO9 [$\overline{\text{DMAReq1}}$]SGPIO10 [$\overline{\text{DMAReq2}}$]SGPIO11 [$\overline{\text{DMAReq3}}$]SGPIO12		External Slave Peripheral	41
DQM0 DQM1 DQM2 DQM3		SDRAM	40
DQMCB		SDRAM	40

Signals Listed Alphabetically (Part 3 of 12)

Signal Name	Ball	Interface Group	Page
ECC0 ECC1 ECC2 ECC3 ECC4 ECC5 ECC6 ECC7		SDRAM	40
EMC0MDClk EMC0MDIO		Ethernet	38
[EMC0Sync]EMC0TxEn[EMC0Tx0En]		Ethernet	38
EMC0TxD0[EMC0Tx0D0][EMC0Tx0D] EMC0TxD1[EMC0Tx0D1][EMC0Tx1D] EMC0TxD2[EMC0Tx1D0][EMC0Tx2D] EMC0TxD3[EMC0Tx1D1][EMC0Tx3D]		Ethernet	38
EMC0TxEn[EMC0Tx0En][EMC0Sync]		Ethernet	38
EMC0TxErr[EMC0Tx1En]		Ethernet	38
[EMC0Tx0En]EMC0TxEn[EMC0Sync] [EMC0Tx1En]EMC0TxErr		Ethernet	38
EMC1TxEn][EMC1Tx2En]CGPIO12[HDLCMPTxEn6] [EMC1TxErr][EMC1Tx3En]CGPIO11[HDLCMPTxData6] [EMC1Tx2En][EMC1TxEn]CGPIO12[HDLCMPTxEn6] [EMC1Tx3En][EMC1TxErr]CGPIO11[HDLCMPTxData6]		Ethernet	38
[EMC1TxD0][EMC1Tx2D0]CGPIO4[HDLCMPRxData4] [EMC1TxD1][EMC1Tx2D1]CGPIO5[HDLCMPTxClk5] [EMC1TxD2][EMC1Tx3D0]CGPIO6[HDLCMPTxData5] [EMC1TxD3][EMC1Tx3D1]CGPIO7[HDLCMPTxEn5]		Ethernet	38
[$\overline{\text{EOT0}}$][$\overline{\text{TC0}}$]SGPIO24 [$\overline{\text{EOT1}}$][$\overline{\text{TC1}}$]SGPIO25 [$\overline{\text{EOT2}}$][$\overline{\text{TC2}}$]SGPIO26 [$\overline{\text{EOT3}}$][$\overline{\text{TC3}}$]SGPIO27		External Slave Peripheral	41
$\overline{\text{ExtAck}}$ $\overline{\text{ExtReq}}$ $\overline{\text{ExtReset}}$		External Master Peripheral	43
GND	xxx N13-N22 P13-P22 R13-R22 T13-T22 U13-U22 V13-V22 W13-W22 Y13-Y22 AA13-AA22 AB13-AB22 xxx	Power **Note:** Balls N13-N22, P13-P22, R13-R22, T13-T22, U13-U22, V13-V22, W13-W22, Y13-Y22, AA13-AA22, and AB13-AB22 are also thermal balls.	45
[$\overline{\text{Gnt}}$]$\overline{\text{PCIReq0}}$		PCI	37
$\overline{\text{Halt}}$		System	45

Signals Listed Alphabetically (Part 4 of 12)

Signal Name	Ball	Interface Group	Page
HDLCEXRxDataA HDLCEXRxDataB		HDLC 32-Channel	38
HDLCEXRxClk		HDLC 32-Channel	38
HDLCEXRxFS		HDLC 32-Channel	38
HDLCEXTxDataA HDLCEXTxDataB		HDLC 32-Channel	38
HDLCEXTxClk		HDLC 32-Channel	38
[HDLCEXTxEnA]CGPIO24[$\overline{\text{UART1\_RTS}}$] [HDLCEXTxEnB]CGPIO25[$\overline{\text{UART1\_DTR}}$]		HDLC 32-Channel	38
HDLCMPRxClk0 HDLCMPRxClk1 HDLCMPRxClk2 HDLCMPRxClk3 [HDLCMPRxClk4]CGPIO3[PHY1RxD3][PHY1Rx3D1] [HDLCMPRxClk5]CGPIO8[PHY1RxErr][PHY1Rx2Er] [HDLCMPRxClk6]CGPIO13[PHY1RxClk] [HDLCMPRxClk7]CGPIO18]		HDLC 8-Port	38
HDLCMPRxData0 HDLCMPRxData1 HDLCMPRxData2 HDLCMPRxData3 [HDLCMPRxData4]CGPIO4[EMC1TxD0][EMC1Tx2D0] [HDLCMPRxData5]CGPIO9[PHY1CrS3DV][PHY1RxDV] [HDLCMPRxData6]CGPIO14[PHY1Col][PHY1Rx3Er] [HDLCMPRxData7]CGPIO19		HDLC 8-Port	38
HDLCMPTxClk0 HDLCMPTxClk1 HDLCMPTxClk2 HDLCMPTxClk3 [HDLCMPTxClk4]CGPIO0[PHY1RxD0][PHY1Rx2D0] [HDLCMPTxClk5]CGPIO5[EMC1TxD1][EMC1Tx2D1] [HDLCMPTxClk6]CGPIO10[PHY1CrS][PHY1CrS2DV] [HDLCMPTxClk7]CGPIO15		HDLC 8-Port	38
HDLCMPTxData0 HDLCMPTxData1 HDLCMPTxData2 HDLCMPTxData3 [HDLCMPTxData4]CGPIO1[PHY1RxD1][PHY1Rx2D1] [HDLCMPTxData5]CGPIO6[EMC1TxD2][EMC1Tx3D0] [HDLCMPTxData6]CGPIO11[EMC1TxErr][EMC1Tx3En] [HDLCMPTxData7]CGPIO16		HDLC 8-Port	38
[HDLCMPTxEn0]CGPIO20[$\overline{\text{UART1\_CTS}}$] [HDLCMPTxEn1[CGPIO21[$\overline{\text{UART1\_DSR}}$] [HDLCMPTxEn2]CGPIO22[$\overline{\text{UART1\_DCD}}$] [HDLCMPTxEn3]CGPIO23[$\overline{\text{UART1\_RI}}$] [HDLCMPTxEn4]CGPIO2[PHYRx3D0] [HDLCMPTxEn5]CGPIO7[EMC0Tx3D1] [HDLCMPTxEn6]CGPIO12[EMC0Tx2En] [HDLCMPTxEn7]CGPIO17		HDLC 8-Port	38

Signals Listed Alphabetically (Part 5 of 12)

Signal Name	Ball	Interface Group	Page
HoldAck HoldPri HoldReq		External Master Peripheral	43
IICSCL[IECSCL] IICSDA[IECSDA]		Internal Peripheral	43
[IRQ0]SGPIO17 [IRQ1]SGPIO18 [IRQ2]SGPIO19 [IRQ3]SGPIO20 [IRQ4]SGPIO21 [IRQ5]SGPIO22 [IRQ6]SGPIO23		Interrupts	44
MemAddr0 MemAddr1 MemAddr2 MemAddr3 MemAddr4 MemAddr5 MemAddr6 MemAddr7 MemAddr8 MemAddr9 MemAddr10 MemAddr11 MemAddr12		SDRAM	40
MemClkOut0 MemClkOut1		SDRAM	40

Signals Listed Alphabetically (Part 6 of 12)

Signal Name	Ball	Interface Group	Page
MemData0 MemData1 MemData2 MemData3 MemData4 MemData5 MemData6 MemData7 MemData8 MemData9 MemData10 MemData11 MemData12 MemData13 MemData14 MemData15 MemData16 MemData17 MemData18 MemData19 MemData20 MemData21 MemData22 MemData23 MemData24 MemData25 MemData26 MemData27 MemData28 MemData29 MemData30 MemData31		SDRAM **Notes:** 1. MemData00 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb)	40
OV_{DD}		Power	45

Signals Listed Alphabetically (Part 7 of 12)

Signal Name	Ball	Interface Group	Page
PCIAD0 PCIAD1 PCIAD2 PCIAD3 PCIAD4 PCIAD6 PCIAD7 PCIAD8 PCIAD9 PCIAD10 PCIAD11 PCIAD12 PCIAD13 PCIAD14 PCIAD15 PCIAD16 PCIAD17 PCIAD18 PCIAD19 PCIAD20 PCIAD21 PCIAD22 PCIAD23 PCIAD24 PCIAD25 PCIAD26 PCIAD27 PCIAD28 PCIAD29 PCIAD30 PCIAD31		PCI	37
PCIC0[$\overline{BE0}$] PCIC1[$\overline{BE1}$] PCIC2[$\overline{BE2}$] PCIC3[$\overline{BE3}$]		PCI	37
PCIClk		PCI	37
$\overline{PCIDevSel}$		PCI	37
$\overline{PCIFrame}$		PCI	37
$\overline{PCIGnt0}$[$\overline{Req}$] $\overline{PCIGnt1}$ $\overline{PCIGnt2}$ $\overline{PCIGnt3}$ $\overline{PCIGnt4}$ $\overline{PCIGnt5}$		PCI	37
$\overline{PCIIDSel}$		PCI	37
$\overline{PCIINT}$[$\overline{PerWE}$]		PCI	37
$\overline{PCIIRDY}$		PCI	37
PCIParity		PCI	37
$\overline{PCIPErr}$		PCI	37

Signals Listed Alphabetically (Part 8 of 12)

Signal Name	Ball	Interface Group	Page
PCIReq0[Gnt] PCIReq1 PCIReq2 PCIReq3 PCIReq4 PCIReq5		PCI	37
PCIReset		PCI	37
PCISErr		PCI	37
PCIStop		PCI	37
PCITRDY		PCI	37
PerAddr4 PerAddr5 PerAddr6 PerAddr7 PerAddr8 PerAddr9 PerAddr10 PerAddr11 PerAddr12 PerAddr13 PerAddr14 PerAddr15 PerAddr16 PerAddr17 PerAddr18 PerAddr19 PerAddr20 PerAddr21 PerAddr22 PerAddr23 PerAddr24 PerAddr25 PerAddr26 PerAddr27 PerAddr28 PerAddr29 PerAddr30 PerAddr31		External Slave Peripheral	41
PerBLast		External Slave Peripheral	41
PerClk		External Slave Peripheral	41
PerCS0 [PerCS1]SGPIO28 [PerCS2]SGPIO29 [PerCS3]SGPIO30 [PerCS4]SGPIO12[DMAReq3] [PerCS5]SGPIO16[DMAAck3] [PerCS6]SGPIO23[IRQ6] [PerCS7]SGPIO27[EOT3][TC3]		External Slave Peripheral	41

Signals Listed Alphabetically (Part 9 of 12)

Signal Name	Ball	Interface Group	Page
PerData0 PerData1 PerData2 PerData3 PerData4 PerData5 PerData6 PerData7 PerData8 PerData9 PerData10 PerData11 PerData12 PerData13 PerData14 PerData15 PerData16 PerData17 PerData18 PerData19 PerData20 PerData21 PerData22 PerData23 PerData24 PerData25 PerData26 PerData27 PerData28 PerData29 PerData30 PerData31		External Slave Peripheral **Note:** PerData00 is the most significant bit (msb) on this bus.	41
PerErr		External Slave Peripheral	43
$\overline{\text{PerOE}}$		External Slave Peripheral	41
PerPar0 PerPar1 PerPar2 PerPar3		External Slave Peripheral	41
PerR/$\overline{\text{W}}$		External Slave Peripheral	41
PerReady		External Slave Peripheral	41
$\overline{\text{PerWBE0}}$ $\overline{\text{PerWBE1}}$ $\overline{\text{PerWBE2}}$ $\overline{\text{PerWBE3}}$		External Slave Peripheral	41
[$\overline{\text{PerWE}}$]$\overline{\text{PCIINT}}$		External Slave Peripheral	37
PHY0Col[PHY0Rx1Er]		Ethernet	38
PHY0CrS[PHY0CrS0DV]		Ethernet	38
[PHY0CrS0DV]PHY0CrS [PHY0CrS1DV]PHY0RxDV		Ethernet	38
[PHY0RefClk]PHY0TxClk		Ethernet	38
PHY0RxClk		Ethernet	38

Signals Listed Alphabetically (Part 10 of 12)

Signal Name	Ball	Interface Group	Page
PHY0RxDV[PHY0CrS1DV]		Ethernet	38
PHY0RxD0[PHY0Rx0D0][PHY0Rx0D] PHY0RxD1[PHY0Rx0D1][PHY0Rx1D] PHY0RxD2[PHY0Rx1D0][PHY0Rx2D] PHY0RxD3[PHY0Rx1D1][PHY0Rx3D]		Ethernet	38
PHY0RxErr[PHY0Rx0Er]		Ethernet	38
[PHY0Rx0Er]PHY0RxErr [PHY0Rx1Er]PHY0Col		Ethernet	38
PHY0TxClk[PHY0RefClk]		Ethernet	38
[PHY1Col][PHY1Rx3Er]CGPIO14[HDLCMPRxData6]		Ethernet	38
[PHY1CrS][PHY1CrS2DV]CGPIO10[HDLCMPTxClk6]		Ethernet	38
[PHY1CrS2DV][PHY1CrS]CGPIO10[HDLCMPTxClk6] [PHY1CrS3DV][PHY1RxDV]CGPIO9[HDLCMPRxData5]		Ethernet	38
[PHY1RxClk]CGPIO13[HDLCMPRxClk6]		Ethernet	38
[PHY1RxDV][PHY1CrS3DV]CGPIO9[HDLCMPRxData5]		Ethernet	38
[PHY1RxD0][PHY1Rx2D0]CGPIO0[HDLCMPTxClk4] [PHY1RxD1][PHY1Rx2D1]CGPIO1[HDLCMPTxData4] [PHY1RxD2][PHY1Rx3D0]CGPIO2[HDLCMPTxEn4] [PHY1RxD3][PHY1Rx3D1]CGPIO3[HDLCMPRxClk4]		Ethernet	38
[PHY1RxErr][PHY1Rx2Er]CGPIO8[HDLCMPRxClk5]		Ethernet	38
[PHY1Rx2Er][PHY1RxErr]CGPIO8[HDLCMPRxClk5] [PHY1Rx3Er][PHY1Col]CGPIO14[HDLCMPRxData6]		Ethernet	38
[PHY1TxClk]CGPIO17[HDLCMPTxEn7]		Ethernet	38
$\overline{\text{RAS}}$		SDRAM	40
[$\overline{\text{Req}}$]$\overline{\text{PCIGnt0}}$		PCI	37
Reserved		Other	45
SGPIO0 SGPIO1[TS1E] SGPIO2[TS2E] SGPIO3[TS1O] SGPIO4[TS2O] SGPIO5[TS3] SGPIO6[TS4] SGPIO7[TS5] SGPIO8[TS6]		System	45
SGPIO9[$\overline{\text{DMAReq0}}$] SGPIO10[$\overline{\text{DMAReq1}}$] SGPIO11[$\overline{\text{DMAReq2}}$] SGPIO12[$\overline{\text{DMAReq3}}$][$\overline{\text{PerCS4}}$]		System	45
SGPIO13[$\overline{\text{DMAAck0}}$] SGPIO14[$\overline{\text{DMAAck1}}$] SGPIO15[$\overline{\text{DMAAck2}}$] SGPIO16[$\overline{\text{DMAAck3}}$][$\overline{\text{PerCS5}}$]		System	45

Signals Listed Alphabetically (Part 11 of 12)

Signal Name	Ball	Interface Group	Page
SGPIO17[IRQ0 SGPIO18[IRQ1] SGPIO19[IRQ2] SGPIO20[IRQ3] SGPIO21[IRQ4] SGPIO22[IRQ5] SGPIO23[IRQ6][$\overline{\text{PerCS6}}$]		System	45
SGPIO24[$\overline{\text{EOT0}}$][$\overline{\text{TC0}}$] SGPIO25[$\overline{\text{EOT1}}$][$\overline{\text{TC1}}$] SGPIO26[$\overline{\text{EOT2}}$][$\overline{\text{TC2}}$] SGPIO27[$\overline{\text{EOT3}}$][$\overline{\text{TC3}}$][$\overline{\text{PerCS7}}$]		System	45
SGPIO28[$\overline{\text{PerCS1}}$] SGPIO29[$\overline{\text{PerCS2}}$] SGPIO30[$\overline{\text{PerCS3}}$]		System	45
SGPIO31[TrcClk]		System	45
SysClk		System	45
SysErr		System	45
$\overline{\text{SysReset}}$		System	45
TCK		JTAG	44
[$\overline{\text{TC0}}$][$\overline{\text{EOT0}}$]SGPIO24 [$\overline{\text{TC1}}$][$\overline{\text{EOT1}}$]SGPIO25 [$\overline{\text{TC2}}$][$\overline{\text{EOT2}}$]SGPIO26 [$\overline{\text{TC3}}$][$\overline{\text{EOT3}}$]SGPIO27		External Slave Peripheral	41
TDI		JTAG	44
TDO		JTAG	44
TestEn		System	45
TmrClk		System	45
TMS		JTAG	44
TrcClk		Trace	45
$\overline{\text{TRST}}$		JTAG	44
[TS1E]SGPIO1 [TS2E]SGPIO2 [TS1O]SGPIO3 [TS2O]SGPIO4 [TS3]SGPIO5 [TS4]SGPIO6 [TS5]SGPIO7 [TS6]SGPIO8		Trace	45
[$\overline{\text{UART0\_CTS}}$]CGPIO26 [$\overline{\text{UART0\_DCD}}$]CGPIO28 [$\overline{\text{UART0\_DSR}}$]CGPIO27 [$\overline{\text{UART0\_DTR}}$]CGPIO31 [$\overline{\text{UART0\_RI}}$]CGPIO29 [$\overline{\text{UART0\_RTS}}$]CGPIO30 UART0_Rx UART0_Tx		Internal Peripheral	43

Signals Listed Alphabetically (Part 12 of 12)

Signal Name	Ball	Interface Group	Page
[$\overline{\text{UART1\_CTS}}$]CGPIO20[HDLCMPTxEn0] [$\overline{\text{UART1\_DCD}}$]CGPIO22[HDLCMPTxEn2] [$\overline{\text{UART1\_DSR}}$]CGPIO21[HDLCMPTxEn1] [$\overline{\text{UART1\_DTR}}$]CGPIO25[HDLCMPTxEnB] [$\overline{\text{UART1\_RI}}$]CGPIO23[HDLCMPTxEn3] [$\overline{\text{UART1\_RTS}}$]CGPIO24[HDLCMPTxEnA] UART1_Rx UART1_Tx		Internal Peripheral	43
UARTSerClk		Internal Peripheral	43
V_{DD}		Power	45
$\overline{\text{WE}}$		SDRAM	40

Signals Listed by Ball Assignment (Part 1 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01		B01		C01		D01	
A02		B02		C02		D02	
A03		B03		C03		D03	
A04		B04		C04		D04	
A05		B05		C05		D05	
A06		B06		C06		D06	
A07		B07		C07		D07	
A08		B08		C08		D08	
A09		B09		C09		D09	
A10		B10		C10		D10	
A11		A11		C11		D11	
A12		B12		C12		D12	
A13		B13		C13		D13	
A14		B14		C14		D14	
A15		B15		C15		D15	
A16		B16		C16		D16	
A17		B17		C17		D17	
A18		B18		C18		D18	
A19		B19		C19		D19	
A20		B20		C20		D20	
A21		B21		C21		D21	
A22		B22		C22		D22	
A23		B23		C23		D23	
A24		B24		C24		D24	
A25		B25		C25		D25	
A26		B26		C26		D26	
A27		B27		C27		D27	
A28		B28		C28		D28	
A29		B29		C29		D29	
A30		B30		C30		D30	
A31		B31		C31		D31	
A32		B32		C32		D32	
A33		B33		C33		D33	
A34		B34		C34		D34	

Signals Listed by Ball Assignment (Part 2 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01		F01		G01		H01	
E02		F02		G02		H02	
E03		F03		G03		H03	
E04		F04		G04		H04	
E05	No ball	F05	No ball	G05	No ball	H05	No ball
E06	No ball	F06	No ball	G06	No ball	H06	No ball
E07	No ball	F07	No ball	G07	No ball	H07	No ball
E08	No ball	F08	No ball	G08	No ball	H08	No ball
E09	No ball	F09	No ball	G09	No ball	H09	No ball
E10	No ball	F10	No ball	G10	No ball	H10	No ball
E11	No ball	A11	No ball	G11	No ball	H11	No ball
E12	No ball	F12	No ball	G12	No ball	H12	No ball
E13	No ball	F13	No ball	G13	No ball	H13	No ball
E14	No ball	F14	No ball	G14	No ball	H14	No ball
E15	No ball	F15	No ball	G15	No ball	H15	No ball
E16	No ball	F16	No ball	G16	No ball	H16	No ball
E17	No ball	F17	No ball	G17	No ball	H17	No ball
E18	No ball	F18	No ball	G18	No ball	H18	No ball
E19	No ball	F19	No ball	G19	No ball	H19	No ball
E20	No ball	F20	No ball	G20	No ball	H20	No ball
E21	No ball	F21	No ball	G21	No ball	H21	No ball
E22	No ball	F22	No ball	G22	No ball	H22	No ball
E23	No ball	F23	No ball	G23	No ball	H23	No ball
E24	No ball	F24	No ball	G24	No ball	H24	No ball
E25	No ball	F25	No ball	G25	No ball	H25	No ball
E26	No ball	F26	No ball	G26	No ball	H26	No ball
E27	No ball	F27	No ball	G27	No ball	H27	No ball
E28	No ball	F28	No ball	G28	No ball	H28	No ball
E29	No ball	F29	No ball	G29	No ball	H29	No ball
E30	No ball	F30	No ball	G30	No ball	H30	No ball
E31		F31		G31		H31	
E32		F32		G32		H32	
E33		F33		G33		H33	
E34		F34		G34		H34	

Signals Listed by Ball Assignment (Part 3 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01		K01		L01		M01	
J02		K02		L02		M02	
J03		K03		L03		M03	
J04		K04		L04		M04	
J05	No ball	K05	No ball	L05	No ball	M05	No ball
J06	No ball	K06	No ball	L06	No ball	M06	No ball
J07	No ball	K07	No ball	L07	No ball	M07	No ball
J08	No ball	K08	No ball	L08	No ball	M08	No ball
J09	No ball	K09	No ball	L09	No ball	M09	No ball
J10	No ball	K10	No ball	L10	No ball	M10	No ball
J11	No ball	K11	No ball	L11	No ball	M11	No ball
J12	No ball	K12	No ball	L12	No ball	M12	No ball
J13	No ball	K13	No ball	L13	No ball	M13	No ball
J14	No ball	K14	No ball	L14	No ball	M14	No ball
J15	No ball	K15	No ball	L15	No ball	M15	No ball
J16	No ball	K16	No ball	L16	No ball	M16	No ball
J17	No ball	K17	No ball	L17	No ball	M17	No ball
J18	No ball	K18	No ball	L18	No ball	M18	No ball
J19	No ball	K19	No ball	L19	No ball	M19	No ball
J20	No ball	K20	No ball	L20	No ball	M20	No ball
J21	No ball	K21	No ball	L21	No ball	M21	No ball
J22	No ball	K22	No ball	L22	No ball	M22	No ball
J23	No ball	K23	No ball	L23	No ball	M23	No ball
J24	No ball	K24	No ball	L24	No ball	M24	No ball
J25	No ball	K25	No ball	L25	No ball	M25	No ball
J26	No ball	K26	No ball	L26	No ball	M26	No ball
J27	No ball	K27	No ball	L27	No ball	M27	No ball
J28	No ball	K28	No ball	L28	No ball	M28	No ball
J29	No ball	K29	No ball	L29	No ball	M29	No ball
J30	No ball	K30	No ball	L30	No ball	M30	No ball
J31		K31		L31		M31	
J32		K32		L32		M32	
J33		K33		L33		M33	
J34		K34		L34		M34	

Signals Listed by Ball Assignment (Part 4 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01		P01		R01		T01	
N02		P02		R02		T02	
N03		P03		R03		T03	
N04		P04		R04		T04	
N05	No ball	P05	No ball	R05	No ball	T05	No ball
N06	No ball	P06	No ball	R06	No ball	T06	No ball
N07	No ball	P07	No ball	R07	No ball	T07	No ball
N08	No ball	P08	No ball	R08	No ball	T08	No ball
N09	No ball	P09	No ball	R09	No ball	T09	No ball
N10	No ball	P10	No ball	R10	No ball	T10	No ball
N11	No ball	P11	No ball	R11	No ball	T11	No ball
N12	No ball	P12	No ball	R12	No ball	T12	No ball
N13	GND	P13	GND	R13	GND	T13	GND
N14	GND	P14	GND	R14	GND	T14	GND
N15	GND	P15	GND	R15	GND	T15	GND
N16	GND	P16	GND	R16	GND	T16	GND
N17	GND	P17	GND	R17	GND	T17	GND
N18	GND	P18	GND	R18	GND	T18	GND
N19	GND	P19	GND	R19	GND	T19	GND
N20	GND	P20	GND	R20	GND	T20	GND
N21	GND	P21	GND	R21	GND	T21	GND
N22	GND	P22	GND	R22	GND	T22	GND
N23	No ball	P23	No ball	R23	No ball	T23	No ball
N24	No ball	P24	No ball	R24	No ball	T24	No ball
N25	No ball	P25	No ball	R25	No ball	T25	No ball
N26	No ball	P26	No ball	R26	No ball	T26	No ball
N27	No ball	P27	No ball	R27	No ball	T27	No ball
N28	No ball	P28	No ball	R28	No ball	T28	No ball
N29	No ball	P29	No ball	R29	No ball	T29	No ball
N30	No ball	P30	No ball	R30	No ball	T30	No ball
N31		P31		R31		T31	
N32		P32		R32		T32	
N33		P33		R33		T33	
N34		P34		R34		T34	

Signals Listed by Ball Assignment (Part 5 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01		V01		W01		Y01	
U02		V02		W02		Y02	
U03		V03		W03		Y03	
U04		V04		W04		Y04	
U05	No ball	V05	No ball	W05	No ball	Y05	No ball
U06	No ball	V06	No ball	W06	No ball	Y06	No ball
U07	No ball	V07	No ball	W07	No ball	Y07	No ball
U08	No ball	V08	No ball	W08	No ball	Y08	No ball
U09	No ball	V09	No ball	W09	No ball	Y09	No ball
U10	No ball	V10	No ball	W10	No ball	Y10	No ball
U11	No ball	V11	No ball	W11	No ball	Y11	No ball
U12	No ball	V12	No ball	W12	No ball	Y12	No ball
U13	GND	V13	GND	W13	GND	Y13	GND
U14	GND	V14	GND	W14	GND	Y14	GND
U15	GND	V15	GND	W15	GND	Y15	GND
U16	GND	V16	GND	W16	GND	Y16	GND
U17	GND	V17	GND	W17	GND	Y17	GND
U18	GND	V18	GND	W18	GND	Y18	GND
U19	GND	V19	GND	W19	GND	Y19	GND
U20	GND	V20	GND	W20	GND	Y20	GND
U21	GND	V21	GND	W21	GND	Y21	GND
U22	GND	V22	GND	W22	GND	Y22	GND
U23	No ball	V23	No ball	W23	No ball	Y23	No ball
U24	No ball	V24	No ball	W24	No ball	Y24	No ball
U25	No ball	V25	No ball	W25	No ball	Y25	No ball
U26	No ball	V26	No ball	W26	No ball	Y26	No ball
U27	No ball	V27	No ball	W27	No ball	Y27	No ball
U28	No ball	V28	No ball	W28	No ball	Y28	No ball
U29	No ball	V29	No ball	W29	No ball	Y29	No ball
U30	No ball	V30	No ball	W30	No ball	Y30	No ball
U31		V31		W31		Y31	
U32		V32		W32		Y32	
U33		V33		W33		Y33	
U34		V34		W34		Y34	

Signals Listed by Ball Assignment (Part 6 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01		AB01		AC01		AD01	
AA02		AB02		AC02		AD02	
AA03		AB03		AC03		AD03	
AA04		AB04		AC04		AD04	
AA05	No ball	AB05	No ball	AC05	No ball	AD05	No ball
AA06	No ball	AB06	No ball	AC06	No ball	AD06	No ball
AA07	No ball	AB07	No ball	AC07	No ball	AD07	No ball
AA08	No ball	AB08	No ball	AC08	No ball	AD08	No ball
AA09	No ball	AB09	No ball	AC09	No ball	AD09	No ball
AA10	No ball	AB10	No ball	AC10	No ball	AD10	No ball
AA11	No ball	AB11	No ball	AC11	No ball	AD11	No ball
AA12	No ball	AB12	No ball	AC12	No ball	AD12	No ball
AA13	GND	AB13	GND	AC13	No ball	AD13	No ball
AA14	GND	AB14	GND	AC14	No ball	AD14	No ball
AA15	GND	AB15	GND	AC15	No ball	AD15	No ball
AA16	GND	AB16	GND	AC16	No ball	AD16	No ball
AA17	GND	AB17	GND	AC17	No ball	AD17	No ball
AA18	GND	AB18	GND	AC18	No ball	AD18	No ball
AA19	GND	AB19	GND	AC19	No ball	AD19	No ball
AA20	GND	AB20	GND	AC20	No ball	AD20	No ball
AA21	GND	AB21	GND	AC21	No ball	AD21	No ball
AA22	GND	AB22	GND	AC22	No ball	AD22	No ball
AA23	No ball	AB23	No ball	AC23	No ball	AD23	No ball
AA24	No ball	AB24	No ball	AC24	No ball	AD24	No ball
AA25	No ball	AB25	No ball	AC25	No ball	AD25	No ball
AA26	No ball	AB26	No ball	AC26	No ball	AD26	No ball
AA27	No ball	AB27	No ball	AC27	No ball	AD27	No ball
AA28	No ball	AB28	No ball	AC28	No ball	AD28	No ball
AA29	No ball	AB29	No ball	AC29	No ball	AD29	No ball
AA30	No ball	AB30	No ball	AC30	No ball	AD30	No ball
AA31		AB31		AC31		AD31	
AA32		AB32		AC32		AD32	
AA33		AB33		AC33		AD33	
AA34		AB34		AC34		AD34	

Signals Listed by Ball Assignment (Part 7 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AE01		AF01		AG01		AH01	
AE02		AF02		AG02		AH02	
AE03		AF03		AG03		AH03	
AE04		AF04		AG04		AH04	
AE05	No ball	AF05	No ball	AG05	No ball	AH05	No ball
AE06	No ball	AF06	No ball	AG06	No ball	AH06	No ball
AE07	No ball	AF07	No ball	AG07	No ball	AH07	No ball
AE08	No ball	AF08	No ball	AG08	No ball	AH08	No ball
AE09	No ball	AF09	No ball	AG09	No ball	AH09	No ball
AE10	No ball	AF10	No ball	AG10	No ball	AH10	No ball
AE11	No ball	AF11	No ball	AG11	No ball	AH11	No ball
AE12	No ball	AF12	No ball	AG12	No ball	AH12	No ball
AE13	No ball	AF13	No ball	AG13	No ball	AH13	No ball
AE14	No ball	AF14	No ball	AG14	No ball	AH14	No ball
AE15	No ball	AF15	No ball	AG15	No ball	AH15	No ball
AE16	No ball	AF16	No ball	AG16	No ball	AH16	No ball
AE17	No ball	AF17	No ball	AG17	No ball	AH17	No ball
AE18	No ball	AF18	No ball	AG18	No ball	AH18	No ball
AE19	No ball	AF19	No ball	AG19	No ball	AH19	No ball
AE20	No ball	AF20	No ball	AG20	No ball	AH20	No ball
AE21	No ball	AF21	No ball	AG21	No ball	AH21	No ball
AE22	No ball	AF22	No ball	AG22	No ball	AH22	No ball
AE23	No ball	AF23	No ball	AG23	No ball	AH23	No ball
AE24	No ball	AF24	No ball	AG24	No ball	AH24	No ball
AE25	No ball	AF25	No ball	AG25	No ball	AH25	No ball
AE26	No ball	AF26	No ball	AG26	No ball	AH26	No ball
AE27	No ball	AF27	No ball	AG27	No ball	AH27	No ball
AE28	No ball	AF28	No ball	AG28	No ball	AH28	No ball
AE29	No ball	AF29	No ball	AG29	No ball	AH29	No ball
AE30	No ball	AF30	No ball	AG30	No ball	AH30	No ball
AE31		AF31		AG31		AH31	
AE32		AF32		AG32		AH32	
AE33		AF33		AG33		AH33	
AE34		AF34		AG34		AH34	

Signals Listed by Ball Assignment (Part 8 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AJ01		AK01		AL01		AM01	
AJ02		AK02		AL02		AM02	
AJ03		AK03		AL03		AM03	
AJ04		AK04		AL04		AM04	
AJ05	No ball	AK05	No ball	AL05		AM05	
AJ06	No ball	AK06	No ball	AL06		AM06	
AJ07	No ball	AK07	No ball	AL07		AM07	
AJ08	No ball	AK08	No ball	AL08		AM08	
AJ09	No ball	AK09	No ball	AL09		AM09	
AJ10	No ball	AK10	No ball	AL10		AM10	
AJ11	No ball	AK11	No ball	AL11		AM11	
AJ12	No ball	AK12	No ball	AL12		AM12	
AJ13	No ball	AK13	No ball	AL13		AM13	
AJ14	No ball	AK14	No ball	AL14		AM14	
AJ15	No ball	AK15	No ball	AL15		AM15	
AJ16	No ball	AK16	No ball	AL16		AM16	
AJ17	No ball	AK17	No ball	AL17		AM17	
AJ18	No ball	AK18	No ball	AL18		AM18	
AJ19	No ball	AK19	No ball	AL19		AM19	
AJ20	No ball	AK20	No ball	AL20		AM20	
AJ21	No ball	AK21	No ball	AL21		AM21	
AJ22	No ball	AK22	No ball	AL22		AM22	
AJ23	No ball	AK23	No ball	AL23		AM23	
AJ24	No ball	AK24	No ball	AL24		AM24	
AJ25	No ball	AK25	No ball	AL25		AM25	
AJ26	No ball	AK26	No ball	AL26		AM26	
AJ27	No ball	AK27	No ball	AL27		AM27	
AJ28	No ball	AK28	No ball	AL28		AM28	
AJ29	No ball	AK29	No ball	AL29		AM29	
AJ30	No ball	AK30	No ball	AL30		AM30	
AJ31		AK31		AL31		AM31	
AJ32		AK32		AL32		AM32	
AJ33		AK33		AL33		AM33	
AJ34		AK34		AL34		AM34	

Signals Listed by Ball Assignment (Part 9 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AN01		AP01					
AN02		AP02					
AN03		AP03					
AN04		AP04					
AN05		AP05					
AN06		AP06					
AN07		AP07					
AN08		AP08					
AN09		AP09					
AN10		AP10					
AN11		AP11					
AN12		AP12					
AN13		AP13					
AN14		AP14					
AN15		AP15					
AN16		AP16					
AN17		AP17					
AN18		AP18					
AN19		AP19					
AN20		AP20					
AN21		AP21					
AN22		AP22					
AN23		AP23					
AN24		AP24					
AN25		AP25					
AN26		AP26					
AN27		AP27					
AN28		AP28					
AN29		AP29					
AN30		AP30					
AN31		AP31					
AN32		AP32					
AN33		AP33					
AN34		AP34					

Signal List

The table following table provides a summary of the number of package pins associated with each functional interface group.

Pin Summary

Group	No. of Pins
Nonmultiplexed Signals	259
Multiplexed Signals	79
Total Signal Pins	**338**
AV_{DD}	
OV_{DD}	
V_{DD}	
Gnd	
Thermal (and Gnd)	100
Reserved	0
Total Pins	**580**

In the table “Signal Functional Description” on page 37, each external signal is listed along with a short description of the signal function. The signals are grouped together according to their function. Some signals are multiplexed on the same package pin (ball) so that the pin can be used for different functions. In most cases, the signal name is shown in this table without any multiplexed signal names that may be associated with it. In cases where multiplexed signals are in the same functional group, the names appear as a default signal followed by secondary signals in square brackets (for example, PCIC0:3[$\overline{\text{BE0:3}}$]). Active-low signals such as $\overline{\text{BE0:3}}$ are marked with an overline. Any signal that is not the primary (default) signal on a multiplexed pin is shown in square backets.

The active signal on a multiplexed pin is controlled by programming. It is expected that in any single application, a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

In addition to multiplexing, many pins are also multi-purpose. For example, EMC0TxErr[EMC0Tx1En] functions as an error output when the Ethernet interface operates in MII mode, or as a transmit enable output when operating in RMII mode.

Another multi-purpose use occurs when the EBC peripheral controller address pins are used as outputs by the NPe405H to broadcast an address to external slave devices when the NPe405H has control of the external bus. However, when an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the NPe405H. In this example, the pins are also bidirectional, serving as both inputs and outputs.

The following table lists all of the I/O signals provided by the NPe405H. Please refer to “Signals Listed Alphabetically” on page 15 for the pin number to which each signal is assigned.

Signal Functional Description (Part 1 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)

Signal Name	Description	I/O	Type	Notes
PCI Interface				
PCIAD0:31	PCI Address/Data bus. Multiplexed address and data bus	I/O	5V tolerant 3.3V PCI	4
PCIC0:3[$\overline{\text{BE0:3}}$]	PCI bus command or Byte Enable	I/O	5V tolerant 3.3V PCI	4
PCIParity	PCI Parity. Parity is even across PCIAD0:31 and PCIC0:3[$\overline{\text{BE0:3}}$]. PCIParity is valid one cycle after either an address or data phase. The PCI device that drove PCIAD0:31 is responsible for driving PCIParity on the next PCI bus clock.	I/O	5V tolerant 3.3V PCI	4
$\overline{\text{PCIFrame}}$	Driven by the current PCI bus master to indicate beginning and duration of a PCI access.	I/O	5V tolerant 3.3V PCI	4
$\overline{\text{PCIIRDY}}$	Driven by the current PCI bus master. Assertion of $\overline{\text{PCIIRDY}}$ indicates that the PCI initiator is ready to transfer data.	I/O	5V tolerant 3.3V PCI	4
$\overline{\text{PCITRDY}}$	The target of the current PCI transaction drives $\overline{\text{PCITRDY}}$. Assertion of $\overline{\text{PCITRDY}}$ indicates that the PCI target is ready to transfer data.	I/O	5V tolerant 3.3V PCI	4
$\overline{\text{PCIStop}}$	The target of the current PCI transaction can assert $\overline{\text{PCIStop}}$ to indicate to the requesting PCI master that it wants to end the current transaction.	I/O	5V tolerant 3.3V PCI	4
$\overline{\text{PCIDevSel}}$	Driven by the target of the current PCI transaction. A PCI target asserts $\overline{\text{PCIDevSel}}$ when it has decoded an address and command encoding and claims the transaction.	I/O	5V tolerant 3.3V PCI	4
PCIIDSel	Used during configuration cycles to select the PCI slave interface for configuration	I	5V tolerant 3.3V PCI	5
$\overline{\text{PCISErr}}$	Used for reporting address parity errors or catastrophic failures detected by a PCI target.	I/O	5V tolerant 3.3V PCI	4
$\overline{\text{PCIPErr}}$	Used for reporting data parity errors on PCI transactions. $\overline{\text{PCIPErr}}$ is driven active by the device receiving PCIAD0:31, PCIC0:3[$\overline{\text{BE0:3}}$], and PCIParity, two PCI clocks following the data in which bad parity is detected.	I/O	5V tolerant 3.3V PCI	4
PCIClk	Used as the asynchronous PCI clock when in asynch mode. It is unused when the PCI interface is operated synchronously with the PLB bus.	I	5V tolerant 3.3V PCI	5
$\overline{\text{PCIReset}}$	PCI specific reset	O	5V tolerant 3.3V PCI	
$\overline{\text{PCIINT}}$	PCI Interrupt. Open-drain output (two states; 0 or open circuit).	O	5V tolerant 3.3V PCI	
$\overline{\text{PCIReq0}}$[$\overline{\text{Gnt}}$]	$\overline{\text{Req0}}$ when internal arbiter is used, or $\overline{\text{Gnt}}$ when external arbiter is used.	I	5V tolerant 3.3V PCI	4
$\overline{\text{PCIReq1:5}}$	Used as $\overline{\text{PCIReq1:5}}$ input when internal arbiter is used	I	5V tolerant 3.3V PCI	4
$\overline{\text{PCIGnt0}}$[$\overline{\text{Req}}$]	$\overline{\text{Gnt0}}$ when internal arbiter is used, or $\overline{\text{Req}}$ when external arbiter is used	O	5V tolerant 3.3V PCI	

Signal Functional Description (Part 2 of 9)

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)

Signal Name	Description	I/O	Type	Notes
$\overline{\text{PCIGnt1:5}}$	$\overline{\text{PCIGnt1:5}}$ output when internal arbiter is used.	O	5V tolerant 3.3V PCI	
HDLCEX Interface				
HDLCEXTxClk	Transmit Clock	I	3.3V LVTTL	
HDLCEXTxFS	Transmit Frame Synchronization	I	3.3V LVTTL	
HDLCEXTxDataA	Transmit Data port A	O	3.3V LVTTL	
HDLCEXTxDataB	Transmit Data port B	O	3.3V LVTTL	
HDLCEXRxClk	Receive Clock	I	3.3V LVTTL	
HDLCEXRxFS	Receive Frame Synchronization	I	3.3V LVTTL	
HDLCEXRxDataA	Receive Data port A	I	3.3V LVTTL	
HDLCEXRxDataB	Receive Data port B	I	3.3V LVTTL	
[HDLCEXTxEnA]	Transmit Enable port A	O	5V tolerant 3.3V LVTTL	
[HDLCEXTxEnB]	Transmit Enable port B	O	5V tolerant 3.3V LVTTL	
HDLCMP Interface				
HDLCMPTxClk0:3	Transmit Clock signal that controls the transmit bit rate	O	3.3V LVTTL	
[HDLCMPTxClk4:7]	Transmit Clock signal that controls the transmit bit rate	O	5V tolerant 3.3V LVTTL	
HDLCMPTxData0:3	Transmit Data signal	O	3.3V LVTTL	
[HDLCMPTxData4:7]	Transmit Data signal	O	5V tolerant 3.3V LVTTL	
[HDLCMPTxEn0:7]	Transmit Data Enable signal that controls when the external buffer is tri-stated	O	5V tolerant 3.3V LVTTL	
HDLCMPRxClk0:3	Receive Clock signal that controls the receive bit rate	I	3.3V LVTTL	
[HDLCMPRxClk4:7]	Receive Clock signal that controls the receive bit rate	I	5V tolerant 3.3V LVTTL	
HDLCMPRxData0:3	Receive Data signal	I	3.3V LVTTL	
[HDLCMPRxData4:7]	Receive Data signal	I	5V tolerant 3.3V LVTTL	
Ethernet Interface				
EMC0MDClk	Management Data Clock. The MDClk is sourced to the PHY. Management information is transferred synchronously with respect to this clock (MII, RMII, and SMII).	O	5V tolerant 3.3V LVTTL	
EMC0MDIO	Management Data Input/Output is a bidirectional signal between the Ethernet controller and the PHY. It is used to transfer control and status information (MII, RMII, and SMII).	I/O	5V tolerant 3.3V LVTTL	1, 4

Signal Functional Description (Part 3 of 9)

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)

Signal Name	Description	I/O	Type	Notes
EMC0TxD0[EMC0Tx0D0][EMC0Tx0D] EMC0TxD1[EMC0Tx0D1][EMC0Tx1D] EMC0TxD2[EMC0Tx1D0][EMC0Tx2D] EMC0TxD3[EMC0Tx1D1][EMC0Tx3D]	Transmit Data. A nibble wide data bus towards the net. The data is synchronous with PHY0TxClk (MII 0[RMII 0 and 1][SMII 0, 1, 2, and 3]).	O	3.3V LVTTL	
[EMC1TxD0][EMC1Tx2D0] [EMC1TxD1][EMC1Tx2D1] [EMC1TxD2][EMC1Tx3D0] [EMC1TxD3][EMC1Tx3D1]	RMII Transmit Data (MII 1[RMII 0 and 1]).	O	5V tolerant 3.3V LVTTL	
EMC0TxEn[EMC0Tx0En][EMC0Sync]	Transmit Enable. This signal is driven by EMAC2 to the PHY. Data is valid during the active state of this signal. Deassertion of this signal indicates end of frame transmission. This signal is synchronous with PHYTxClk (MII 0[RMII 0]). or SMII Sync.	O	3.3V LVTTL	
EMC0TxErr[EMC0Tx1En]	Transmit Error. This signal is generated by the Ethernet controller, is connected to the PHY and is synchronous with the PHY0TxClk. It informs the PHY that an error was detected (MII 0). or Transmit Enable [RMII 1].	O	5V tolerant 3.3V LVTTL	
[EMC1TxEn][EMC1Tx2En]	Transmit Enable ([MII 1][RMII 2]).	O	5V tolerant 3.3V LVTTL	
[EMC1TxErr][EMC1Tx3En]	Transmit Error. This signal is generated by the Ethernet controller, is connected to the PHY and is synchronous with the PHY1TxClk. It informs the PHY that an error was detected ([MII 1]). or Transmit Enable [RMII 3].	O	5V tolerant 3.3V LVTTL	
PHY0Col[PHY0Rx1Er]l	Collision [receive error] signal from the PHY. This is an asynchronous signal (MII 0). or Receive Error ([RMII 1]).	I	5V tolerant 3.3V LVTTL	
PHY0CrS[PHY0CrS0DV]	Carrier Sense signal from the PHY. This is an asynchronous signal (MII 0). or Carrier sense data valid ([RMII 0]).	I	5V tolerant 3.3V LVTTL	1, 5
PHY0RxClk	Receiver medium clock. This signal is generated by the PHY (MII 0).	I	5V tolerant 3.3V LVTTL	1, 4
PHY0RxD0[PHY0Rx0D0][PHY0Rx0D] PHY0RxD1[PHY0Rx0D1][PHY0Rx1D] PHY0RxD2[PHY0Rx1D0][PHY0Rx2D] PHY0RxD3[PHY0Rx1D1][PHY0Rx3D]	Received Data. This is a nibble wide bus from the PHY. The data is synchronous with PHY0RxClk (MII 0[RMII 0 and 1][SMII 0, 1, 2, and 3]).	I	5V tolerant 3.3V LVTTL	1, 4
[PHY1RxD0][PHY1Rx2D0] [PHY1RxD1][PHY1Rx2D1] [PHY1RxD2][PHY1Rx3D0] [PHY1RxD3][PHY1Rx3D1]	Receive Data (MII 1[RMII 0 and 1]).	I	5V tolerant 3.3V LVTTL	

Signal Functional Description (Part 4 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)

Signal Name	Description	I/O	Type	Notes
PHY0RxDV[PHY0CrS1DV]	Receive Data Valid. Data on the Data Bus is valid when this signal is activated. Deassertion of this signal indicates end of the frame reception (MII 0). or Carrier sense data valid ([RMII 1])	I	5V tolerant 3.3V LVTTL	1, 5
PHY0RxErr[PHY0Rx0Er]	Receive Error. This signal comes from the PHY and is synchronous with PHY0RxClk (MII 0 [RMII 0]).	I	5V tolerant 3.3V LVTTL	1, 5
PHY0TxClk[PHY0RefClk]	Transmit medium clock. This signal is generated the PHY ([MII 0]). or Reference Clock [RMII and SMII].	I	5V tolerant 3V LVTTL	1, 4
[PHY1Col][PHY1Rx3Er]	Collision [receive error] signal from the PHY. This is an asynchronous signal ([MII 1]). or Receive Error. This signal comes from the PHY and is synchronous with PHY1RxClk ([RMII 3]).	I	5V tolerant 3.3V LVTTL	1, 5
[PHY1CrS][PHY1CrS2DV]	Carrier Sense signal from the PHY. This is an asynchronous signal ([MII 1]). or Carrier Sense Data Valid ([RMII 2]).	I	5V tolerant 3.3V LVTTL	
[PHY1RxClk]	Receiver medium clock. This signal is generated by the PHY ([MII 1]).	I	5V tolerant 3.3V LVTTL	1, 4
[PHY1RxDV][PHY1CrS3DV]	Receive Data Valid ([MII 0]). or Carrier Sense Data Valid ([RMII 3]).	i	5V tolerant 3.3V LVTTL	
[PHY1RxErr][PHY1Rx2Er]	Receive Error. This signal comes from the PHY and is synchronous with PHY1RxClk ([MII 1][RMII 2]).	I	5V tolerant 3.3V LVTTL	
[PHY1TxClk]	Transmit medium clock. This signal is generated the PHY ([MII 1]).	I	5V tolerant 3.3V LVTTL	1, 4
SDRAM Interface				
MemData0:31	Memory Data bus **Notes:** 1. MemData0 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb).	I/O	3.3V LVTTL	4
MemAddr12:0	Memory Address bus. **Notes:** 1. MemAddr12 is the most significant bit (msb). 2. MemAddr0 is the least significant bit (lsb).	O	3.3V LVTTL	

Signal Functional Description (Part 5 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)

Signal Name	Description	I/O	Type	Notes
BA1:0	Bank Address supporting up to 4 internal banks	O	3.3V LVTTL	
$\overline{\text{RAS}}$	Row Address Strobe.	O	3.3V LVTTL	
$\overline{\text{CAS}}$	Column Address Strobe.	O	3.3V LVTTL	
DQM0:3	DQM for byte lanes 0 (MemData0:7), 1 (MemData8:15), 2 (MemData16:23), and 3 (MemData24:31)	O	3.3V LVTTL	
DQMCB	DQM for ECC check bits.	O	3.3V LVTTL	
ECC0:7	ECC check bits 0:7.	I/O	3.3V LVTTL	4
$\overline{\text{BankSel0:3}}$	Select up to four external SDRAM banks.	O	3.3V LVTTL	
$\overline{\text{WE}}$	Write Enable.	O	3.3V LVTTL	
ClkEn0:1	SDRAM Clock Enable.	O	3.3V LVTTL	
MemClkOut0:1	Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attachment without requiring this signal to be repowered by a PLL or zero-delay buffer.	O	3.3V LVTTL	
External Slave Peripheral Interface				
PerData0:31	Peripheral data bus used by NPe405H when not in external master mode, otherwise used by external master. **Note:** PerData00 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
PerAddr4:31	Peripheral Address bus used by NPe405H when not in external master mode, otherwise used by external master.	I/O	5V tolerant 3.3V LVTTL	1
PerPar0:3	Peripheral byte parity signals.	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerWBE0:3}}$	As outputs, these pins can act as byte-enables which are valid for an entire cycle or as write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions. As outputs, pins are used by either peripheral controller or DMA controller depending upon the type of transfer involved. Used as inputs when external bus master owns the external interface.	I/O	5V tolerant 3.3V LVTTL	1, 2
$\overline{\text{PerWE}}$	Peripheral Write Enable. Low when any of the four $\overline{\text{PerWBE}}$ signals are low.	I/O	5V tolerant 3.3V LVTTL	
[$\overline{\text{PerCS0:7}}$]	Peripheral Chip Selects	O	5V tolerant 3.3V LVTTL	2
$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the NPe405H is the bus master, it enables the selected SDRAMs to drive the bus.	O	5V tolerant 3.3V LVTTL	2

Signal Functional Description (Part 6 of 9)

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)

Signal Name	Description	I/O	Type	Notes
PerR/$\overline{W}$	Used by the NPe405H when not in external master mode, as an output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise it used by the external master as an input to indicate the direction of transfer.	I/O	5V tolerant 3.3V LVTTL	1
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerBLast}}$	Used by the NPe405H when not in external master mode, otherwise used by external master. Indicates the last transfer of a memory access.	I/O	5V tolerant 3.3V LVTTL	1, 4
PerClk	Peripheral Clock to be used by an external master and by synchronous peripheral slaves.	O	5V tolerant 3.3V LVTTL	
PerErr	Used as an input to record external master and slave peripheral errors.	I	5V tolerant 3.3V LVTTL	1, 5
[$\overline{\text{DMAReq0:3}}$]	Used by slave peripherals to indicate they are prepared to transfer data.	I	5V tolerant 3.3V LVTTL	1, 5
[$\overline{\text{DMAAck0:3}}$]	Used by the NPe405H to indicate that data transfers have occurred.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{EOT0:3}}$][$\overline{\text{TC0:3}}$]	End Of Transfer[Terminal Count].	I/O	5V tolerant 3.3V LVTTL	1, 5

Signal Functional Description (Part 7 of 9)

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)

Signal Name	Description	I/O	Type	Notes
External Master Peripheral Interface				
$\overline{\text{ExtReset}}$	Peripheral Reset. Used by an external master and synchronous peripheral slaves.	O	5V tolerant 3.3V LVTTL	
HoldReq	Hold Request. Used by an external master to request ownership of the peripheral bus.	I	5V tolerant 3.3V LVTTL	1, 5
HoldAck	Hold Acknowledge. Used by the NPe405H to transfer ownership of peripheral bus to an external master.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{ExtReq}}$	External Request. Used by an external master to indicate it is prepared to transfer data.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{ExtAck}}$	Exteranl Acknowledgement. Used by the NPe405H to indicate that a data transfer occurred.	O	5V tolerant 3.3V LVTTL	
HoldPri	Hold Primary. Used by an external master to indicate the priority of a given transfer (0 = high, 1 = low).	I	5V tolerant 3.3V LVTTL	1, 4
BusReq	Bus Request. Used when the NPe405H needs to regain control of peripheral interface from an external Master.	O	5V tolerant 3.3V LVTTL	
Internal Peripheral Interface				
UARTSerClk	Serial Clock used to provide an alternative clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either or both UART0 and UART1.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Rx	UART0 Receive data.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Tx	UART0 Transmit data.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART0\_DCD}}$]	UART0 Data Carrier Detect.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART0\_DSR}}$]	UART0 Data Set Ready.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART0\_CTS}}$]	UART0 Clear To Send.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART0\_DTR}}$]	UART0 Data Terminal Ready.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART0\_RTS}}$]	UART0 Request To Send.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART0\_RI}}$]	UART0 Ring Indicator.	I	5V tolerant 3.3V LVTTL r	1, 4

Signal Functional Description (Part 8 of 9)

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)

Signal Name	Description	I/O	Type	Notes
UART1_Rx	UART1 Receive data.	I	5V tolerant 3.3V LVTTL	1, 4
UART1_Tx	UART1 Transmit data.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART1\_DCD}}$]	UART1 Data Carrier Detect.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART1\_DSR}}$]	UART1 Data Set Ready.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART1\_CTS}}$]	UART1 Clear To Send.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART1\_DTR}}$]	UART1 Data Terminal Ready.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART1\_RTS}}$]	UART1 Request To Send.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART1\_RI}}$]	UART1 Ring Indicator.	I	5V tolerant 3.3V LVTTL	1, 4
IICSCL[IECSCL]	IIC [Initilization PROM] Serial Clock.	I/O	5V tolerant 3.3V LVTTL	1, 2
IICSDA[IECSDA]	IIC [Initilization PROM] Serial Data.	I/O	5V tolerant 3.3V LVTTL	1, 2
Interrupts Interface				
[IRQ0:6]	Interrupt Requests.	I	5V tolerant 3.3V LVTTL	1, 5
JTAG Interface				
TDI	Test Data In.	I	5V tolerant 3.3V LVTTL	1, 4
TMS	Test Mode Select.	I	5V tolerant 3.3V LVTTL	1, 4
TDO	Test Data Out.	O	5V tolerant 3.3V LVTTL	
TCK	Test Clock.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{TRST}}$	Test Reset.	I	5V tolerant 3.3V LVTTL	2, 5

Signal Functional Description (Part 9 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	Main System Clock input.	I	3.3V Analog Wire w/ESD	
$\overline{\text{SysReset}}$	Main System Reset.	I/O	5V tolerant 3.3V LVTTL	1, 2
SysErr	Set to 1 when a Machine Check is generated.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL	1, 4
CGPIO0:31	Communicatons General Purpose I/O.	I/O	5V tolerant 3.3V LVTTL	
SGPIO0:31	System General Purpose I/O.	I/O	5V tolerant 3.3V LVTTL	
TestEn	Test Enable. Used only for manufacturing tests. Pull down for normal operation.	I	3.3V LVTTL Rcvr w/ PD	3
TmrClk	This input must toggle at a rate of less than one half the CPU core frequency (less than 100MHz in most cases). In most cases this input toggles much slower (in the 1MHz to 10MHz range).	I	5V tolerant 3.3V LVTTL	1, 4
Trace Interface				
[TS1E] [TS2E]	Even Trace execution status.To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
[TS1O] [TS2O]	Odd Trace execution status. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
[TS3:6]	Trace Status. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
[TrcClk]	Trace interface clock. A toggling signal that is always half of the CPU core frequency. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	1
Power Pins				
GND	Ground **Note:** J09-J14, K09-K14, L09-L14, M09-M14, N09-N14, and P09-P14 are also thermal balls.	I	Hardwire	
V_{DD}	Logic voltage—2.5V	I	Hardwire	
OV_{DD}	Output driver voltage—3.3V	I	Hardwire	
AV_{DD}	Filtered PLL voltage—2.5V	I	3.3V DC Wire w/ESD	
Other Pins				
Reserved	Do not connect signals, voltage, or ground to these pins.	n/a	n/a	

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Characteristic	Symbol	Value	Unit
Supply Voltage (Internal Logic)	V_{DD}	0 to 2.7	V
Supply Voltage (I/O Interface)	OV_{DD}	0 to 3.6	V
PLL Supply Voltage	AV_{DD}	0 to 2.7	V
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to 3.6	V
Input Voltage (5.0V LVTTL receivers)	V_{IN}	0 to 5.5	V
Storage Temperature Range	T_{STG}	-55 to 150	°C
Case temperature under bias	T_C	-40 to +120	°C

Package Thermal Specifications

The NPe405H is designed to operate within a case temperature range of -40˚C to 120˚C. Thermal resistance values for the E-PBGA packages in a convection environment are as follows:

Package—Thermal Resistance	Symbol	Airflow ft/min (m/sec)			Unit
		0 (0)	100 (0.51)	200 (1.02)	
35mm, 580-balls—Junction-to-Case	θ_{JC}				°C/W
35mm, 580-balls—Case-to-Ambient[1]	θ_{CA}				°C/W

Notes:

1. For a chip mounted on a JEDEC 2S2P card without a heat sink.
2. For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
   a. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
   b. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
   c. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.

Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Notes:

1. PCI drivers meet PCI specifications.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	2.3	2.5	2.7	V	1
I/O Supply Voltage	OV_{DD}	3.0	3.3	3.6	V	1
PLL Supply Voltage	AV_{DD}	2.3	2.5	2.7	V	
Input Logic High (3.3V LVTTL receivers)	V_{IH}	2.0		OV_{DD}	V	
Input Logic High (5.0V LVTTL receivers)	V_{IH}	2.0		5.5	V	
Input Logic Low	V_{IL}	0		0.8	V	
Output Logic High	V_{OH}	2.4		OV_{DD}	V	
Output Logic Low	V_{OL}	0		0.4	V	
Input Leakage Current (No pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for Pull-Down	I_{IL2}	0 (LPDL)		400 (MPUL)	µA	
Input Leakage Current for Pull-Up	I_{IL3}	–250 (LPDL)		0 (MPUL)	µA	
Input Max Allowable Overshoot (3.3V LVTTL receivers)	V_{IMAO3}			OV_{DD} + 0.6	V	
Input Max Allowable Overshoot (5.0V LVTTL receivers)	V_{IMAO5}			5.5	V	
Input Max Allowable Undershoot (3.3V or 5.0V receivers)	V_{IMAU}	– 0.6			V	
Output Max Allowable Overshoot (3.3V or 5.0V receivers)	V_{OMAO}			OV_{DD} + 0.3	V	
Output Max Allowable Undershoot (3.3V and 5.0V receivers)	V_{OMAU3}	– 0.6			V	
Case Temperature	T_C	– 40		85	°C	

Capacitance

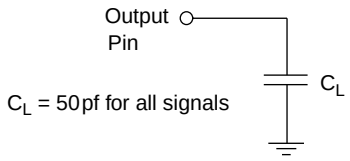
Parameter	Symbol	Maximum	Unit	Notes
Input Capacitance Group 1 (3.3V LVTTL //O)	C_{IN1}	2.5	pF	
Input Capacitance Group 2 (5V tolerant LVTTL I/O)	C_{IN2}	3.5	pF	
Input Capacitance Group 3 (PCI I/O)	C_{IN3}	5.0	pF	
Input Capacitance Group 1 (RX only pins)	C_{IN4}	0.75	pF	

DC Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Active Operating Current (V_{DD})	I_{DD}		390	600	mA
Active Operating Current (OV_{DD})	I_{ODD}		35	100	mA
PLL Voltage (AV_{DD})	V_{PLL}	2.3	2.5	2.7	V
PLL V_{DD} Input current	I_{PLL}		16	23	mA

Test Conditions

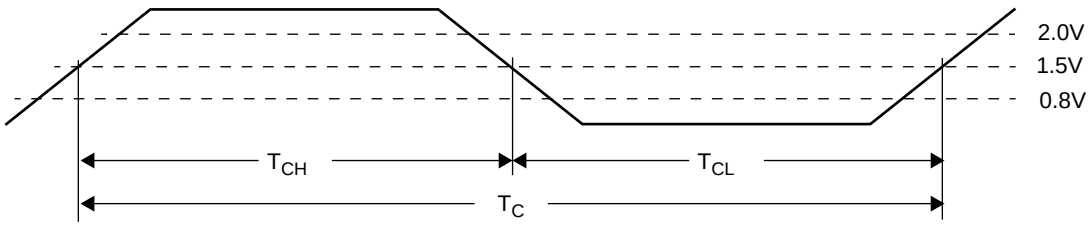
Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized at V_{DD} = 3.14V and T_J = 100˚C with the 50pF test load (C_L) shown in the figure at right.



SysClk and MemClk Timing

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	SysClk clock input frequency	25	66.6	MHz
T_C	SysClk clock period	15	40	ns
T_{CS}	Clock edge stability		0.15	ns
T_{CH}	Clock input high time	40% of nominal period	60% of nominal period	ns
T_{CL}	Clock input low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate > 2V/ns				
MemClk Output				
F_C	MemClk clock output frequency–200MHz		100	MHz
T_C	MemClk clock period–200MHz	10		ns
F_C	MemClk clock output frequency–266MHz		133	MHz
T_C	MemClk clock period–266MHz	7.5		ns
T_{CH}	Clock output high time	35% of nominal period	65% of nominal period	ns
T_{CL}	Clock output low time	35% of nominal period	65% of nominal period	ns

Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the NPe405H. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the NPe405H the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the NPe405H with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board NPe405H peripherals impose more stringent requirements (see Note 1).
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClk since it also tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates. If an external serial clock is used the baud rate is unaffected by the modulation
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.
4. The PCI clock specification for 66 MHz allows a maximum frequency deviation of –1% at a modulation between 30 kHz and 33 kHz. PCI asynchronous mode is unaffected.

Caution: It is up to the system designer to ensure that any SSCG used with the NPe405H meets the above requirements and does not adversely affect other aspects of the system.

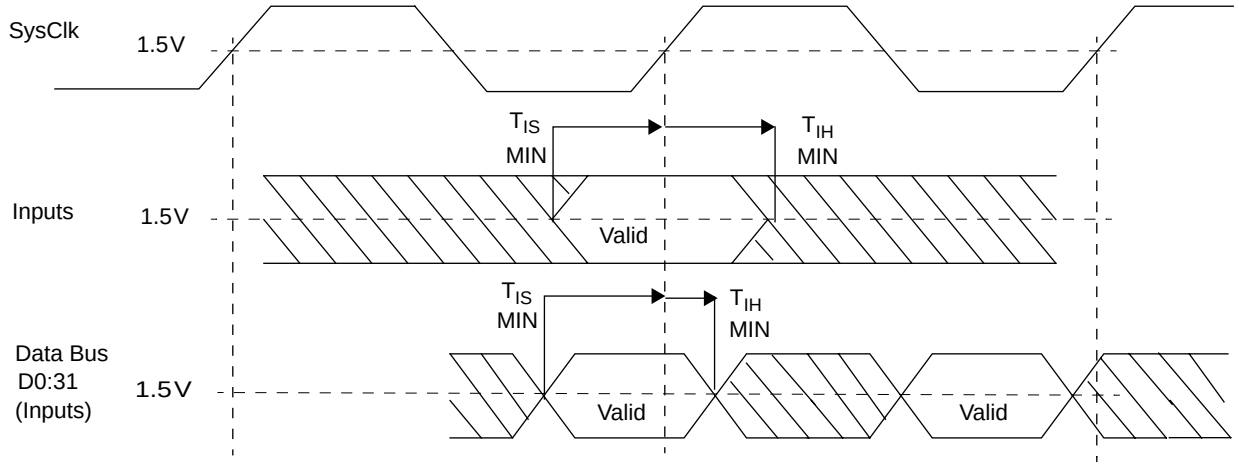
Peripheral Interface Clock Timings

Parameter	Min	Max	Units
PCIClk input frequency (asynchronous mode)	Note 2	66	MHz
PCIClk period (asynchronous mode)	15	Note 2	ns
PCI Clock frequency (synchronous mode)	25	33	MHz
PCI Clock period (synchronous mode - Note 3)	30	40	ns
PCIClk input high time	40% of nominal period	60% of nominal period	ns
PCIClk input low time	40% of nominal period	60% of nominal period	ns
EMC0MDClk output frequency	–	2.5	MHz
EMC0MDClk period	400	–	ns
EMC0MDClk output high time	160	–	ns
EMC0MDClk output low time	160	–	ns
PHY0TxClk input frequency	2.5	25	MHz
PHY0TxClk period	40	400	ns
PHY0TxClk input high time	35% of nominal period	–	ns
PHY0TxClk input low time	35% of nominal period	–	ns
PHY0RxClk input frequency	2.5	25	MHz
PHY0RxClk period	40	400	ns
PHY0RxClk input high time	35% of nominal period	–	ns
PHY0RxClk input low time	35% of nominal period	–	ns
PerClk output frequency–200MHz (for external master or synchronous slaves)	–	50	MHz
PerClk period–200MHz	20	–	ns
PerClk output frequency–266MHz (for external master or synchronous slaves)	–	66	
PerClk period–266MHz	15	–	
PerClk output high time	50% of nominal period	66% of nominal period	ns
PerClk output low time	33% of nominal period	50% of nominal period	ns
UARTSerClk input frequency (Note 1)	–	$1000/(2T_{OPB}+2ns)$	MHz
UARTSerClk period	$2T_{OPB}+2$	–	ns
UARTSerClk input high time	$T_{OPB}+1$	–	ns
UARTSerClk input low time	$T_{OPB}+1$	–	ns
TmrClk input frequency–200MHz	–	50	MHz
TmrClk period–200MHz	20	–	ns
TmrClk input frequency–266MHz	–	66	
TmrClk period–266MHz	15	–	
TmrClk input high time	40% of nominal period	60% of nominal period	ns
TmrClk input low time	40% of nominal period	60% of nominal period	ns

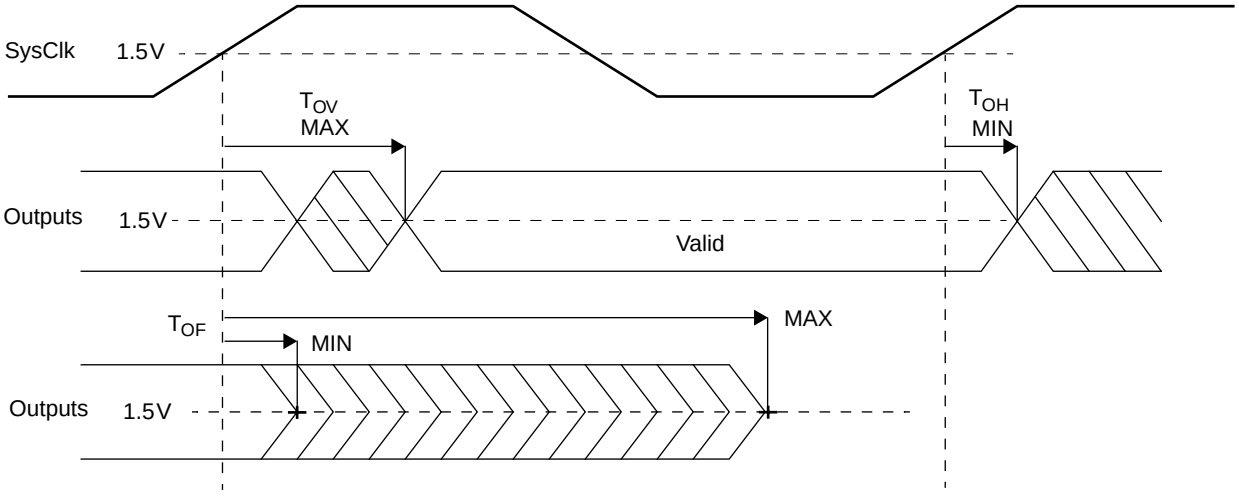
Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at 1/2 the frequency of the PLB clock. The maximum OPB clock frequency is 50 MHz for 200MHz parts and 66MHz.for 266MHz parts.
2. In asynchronous PCI mode the minimum PCIClk frequency is 1/8 the PLB Clock. Refer to the NPe405H User's Manual for more information.
3. In synchronous PCI mode the PCI clock is derived from SysClk and the PCIClk input pin is unused.

Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



I/O Specifications—200MHz (Part 1 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
PCI Interface								
PCIAD0:31					12.3	15.5	PCIClk	6
PCIC0:3[$\overline{BE3:0}$]					12.3	15.5	PCIClk	6
PCIClk			n/a	n/a	n/a	n/a		async
$\overline{PCIDevSel}$					12.3	15.5	PCIClk	6
$\overline{PCIFrame}$					12.3	15.5	PCIClk	6
$\overline{PCIGnt0}$[Req] PCIGnt1:5	n/a	n/a			12.3	15.5	PCIClk	6
PCIIDSel					n/a	n/a	PCIClk	6
$\overline{PCIINT}$[PerWE]	n/a	n/a			12.3	15.5	PCIClk	async
$\overline{PCIIRDY}$					12.3	15.5	PCIClk	6
PCIParity					12.3	15.5	PCIClk	6
$\overline{PCIPErr}$					12.3	15.5	PCIClk	6
$\overline{PCIReq0}$[Gnt] PCIReq1:5			n/a	n/a	n/a	n/a	PCIClk	6
$\overline{PCIReset}$	n/a	n/a	n/a	n/a	12.3	15.5	PCIClk	
$\overline{PCISErr}$	n/a	n/a	n/a	n/a	12.3	15.5	PCIClk	
$\overline{PCIStop}$					12.3	15.5	PCIClk	6
$\overline{PCITRDY}$					12.3	15.5	PCIClk	6
Ethernet Interface								
EMC0MDClk	n/a	n/a	7.4	1.5	12	8		1, async
EMC0MDIO	n/a	n/a	8.8	1.2	12	8	EMC0MDClk	1
EMC0TxD0:3 [EMC0Tx0:1D0:1 [EMC0Tx0:3D]	n/a	n/a	10.5 [7.3] [5.0]	3.0 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxEn [EMC0Tx0En] [EMC0Sync]	n/a	n/a	11.8 [7.2] [5.6]	2.9 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxErr [EMC0Tx1En]	n/a	n/a	11.8[7.4]	2.9[2.4]	12	8	PHYTX	1
[EMC1TxD0:3] [EMC1Tx2:3D0:1]					12	8		
[EMC1TxEn] [EMC1Tx2En]					12	8		
[EMC1TxErr] [EMC1Tx3En]					12	8		

I/O Specifications—200MHz (Part 2 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
PHY0Col[PHY0Rx1Er]l	async[0.2]	async[1.7]	n/a	n/a	n/a	n/a		1
PHY0CrS[PHY0CrS0DV]	async[0.1]	async[1.9]	n/a	n/a	n/a	n/a		1
PHY0RxClk	n/a	n/a	n/a	n/a	n/a	n/a		1, async
PHY0RxD0:3 [PHY0Rx0:1D0:1] [PHY0Rx0:3D]	1.5 [0.8] [0.9]	1.7 [1.7] [0.3]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxDV [PHY0CRS1DV]	1.3[0.7]	1.7[1.7]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxErr[PHY0Rx0Er]	1.3[0.7]	1.8[1.9]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0TxClk[PHY0RefClk]	n/a	n/a	n/a	n/a	n/a	n/a		1, async
[PHY1RxD0:3] [PHY1Rx2:3D0:1]					n/a	n/a		
[PHY1Col] [PHY1Rx3Er]					n/a	n/a		
[PHY1CrS] [PHY1CrS2DV]					n/a	n/a		
[PHY1RxClk]					n/a	n/a		
[PHY1RxDV] [PHY1CrS3DV]					n/a	n/a		
[PHY1RxErr] [PHY1Rx2Er]					n/a	n/a		
[PHY1TxClk]					n/a	n/a		
HDLCEX Interface								
HDLCEXRxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXRxDataA:B	23.8	2.1	n/a	n/a	n/a	n/a		
HDLCEXRxFS	24.2	1.1	n/a	n/a	n/a	n/a		
HDLCEXTxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXTxDataA:B	n/a	n/a	10.5	3.3	12	8		
HDLCEXTxFS	20.3	1.0	n/a	n/a	n/a	n/a		
HDLCEXTxEnA [CGPIO24][$\overline{\text{UART1\_RTS}}$]	n/a	n/a	11.3	3.5	12	8		
HDLCEXTxEnB [CGPIO25][$\overline{\text{UART1\_DTR}}$]	n/a	n/a	11.8	3.8	12	8		
HDLCMP Interface								
HDLCMPTxClk0:3					n/a	n/a		
[HDLCMPTxClk4:7]					n/a	n/a		
HDLCMPTxData0:3					12	8		

I/O Specifications—200MHz (Part 3 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
[HDLCMPTxData4:7]					12	8		
[HDLCMPTxEn0:7]					12	8		
HDLCMPRxClk0:3					n/a	n/a		
[HDLCMPRxClk4:7]					n/a	n/a		
HDLCMPRxData0:3					n/a	n/a		
[HDLCMPRxData4:7]					n/a	n/a		
Internal Peripheral Interface								
IICSCL	async	async	async	async	17	11		
IICSDA	async	async	async	async	17	11		
[$\overline{\text{UART0\_CTS}}$]CGPIO26	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_DCD}}$]CGPIO28	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_DSR}}$]CGPIO27	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_DTR}}$]CGPIO31	n/a	n/a	async	async	12	8		
[$\overline{\text{UART0\_RI}}$][CGPIO29]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_RTS}}$]CGPIO30	n/a	n/a	async	async	12	8		
UART0_Rx	async	async	n/a	n/a	n/a	n/a		
UART0_Tx	n/a	n/a	async	async	12	8		
[$\overline{\text{UART1\_CTS}}$]CGPIO20	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_DCD}}$]CGPIO22	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_DSR}}$]CGPIO21	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_DTR}}$]CGPIO25	n/a	n/a	async	async	12	8		
[$\overline{\text{UART1\_RI}}$]CGPIO23	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_RTS}}$]CGPIO24	n/a	n/a	async	async	12	8		
UART1_Rx	async	async	n/a	n/a	n/a	n/a		
UART1_Tx	n/a	n/a	async	async	12	8		
UARTSerClk	async	async	n/a	n/a	n/a	n/a		
Interrupts Interface								
[IRQ0:6]SGPIO17:23	async	async	n/a	n/a	n/a	n/a		
JTAG Interface								
TCK	async	async	n/a	n/a	n/a	n/a		
TDI	async	async	n/a	n/a	n/a	n/a		
TDO	n/a	n/a	async	async	12	8		
TMS	async	async	n/a	n/a	n/a	n/a		
$\overline{\text{TRST}}$	async	async	n/a	n/a	n/a	n/a		

I/O Specifications—200MHz (Part 4 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
System Interface								
SGPIO0					12	8		
[TrcClk]SGPIO31	n/a	n/a	11.2	1.2	12	8		
[TS1E]SGPIO1	n/a	n/a	7.0	1.2	12	8		
[TS2E]SGPIO2	n/a	n/a	7.0	1.2	12	8		
[TS1O]SGPIO3	n/a	n/a	6.5	1.0	12	8		
[TS2O]SGPIO4	n/a	n/a	6.4	1.0	12	8		
[TS3]SGPIO5	n/a	n/a	6.4	1.0	12	8		
[TS4]SGPIO6	n/a	n/a	6.4	1.0	12	8		
[TS5]SGPIO7	n/a	n/a	6.6	1.0	12	8		
[TS6]SGPIO8	n/a	n/a	6.4	1.0	12	8		
$\overline{\text{Halt}}$	async	async	n/a	n/a	n/a	n/a		
SysClk	n/a	n/a	n/a	n/a	n/a	n/a		
SysErr	n/a	n/a	5.3	1.7	12	8		
$\overline{\text{SysReset}}$	n/a	n/a	n/a	n/a	12	8		
TestEn	dc	dc	n/a	n/a	n/a	n/a		
TmrClk	n/a	n/a	async	async	n/a	n/a		
SDRAM Interface								
BA1:0	n/a	n/a	7.2	1.5	19	12	SysClk	2, 3
$\overline{\text{BankSel3:0}}$	n/a	n/a	5.8	1.0	19	12	SysClk	3
$\overline{\text{CAS}}$	n/a	n/a	7.0	1.4	19	12	SysClk	2, 3
ClkEn0:1	n/a	n/a	4.9	1.0	40	25	SysClk	3
DQM3:0	n/a	n/a	5.9	1.0	19	12	SysClk	3
DQMCB	n/a	n/a	5.9	1.0	19	12	SysClk	3
ECC7:0	2.0	0.3	5.7	1.0	19	12	SysClk	3
MemAddr12:0	n/a	n/a	7.2	1.4	19	12	SysClk	2, 3
MemClkOut0:1	n/a	n/a	0.4	-1.2	19	12	SysClk	3, 4
MemData31:0	2.0	0.3	5.6	1.0	19	12	SysClk	3
$\overline{\text{RAS}}$	n/a	n/a	7.4	1.6	19	12	SysClk	2, 3
$\overline{\text{WE}}$	n/a	n/a	7.1	1.4	19	12	SysClk	2, 3

I/O Specifications—200MHz (Part 5 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
External Slave Peripheral Interface								
$\overline{\text{DMAReq0:3}}$[SGPIO9:12]	4.8	0.0	7.0	1.1	n/a	n/a	PerClk	
$\overline{\text{DMAAck0:3}}$[SGPIO13:16]	n/a	n/a	7.5	1.1	12	8	PerClk	
$\overline{\text{EOT0:3}}$[$\overline{\text{TC0:3}}$] [SGPIO24:27]	4.3	-0.1	8.5	1.2	12	8	PerClk	
PerAddr4:31	n/a	n/a	8.5	0.9	17	11	PerClk	
$\overline{\text{PerBLast}}$	n/a	n/a	7.4	1.4	12	8	PerClk	
$\overline{\text{PerCS0:7}}$	n/a	n/a	7.2	1.3	12	8	PerClk	
PerData0:31	4.8	1.0	9.3	1.0	17	11	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	7.6	1.4	12	8	PerClk	
PerPar0:3	3.1	0.0	8.3	0.9	17	11	PerClk	
PerR/$\overline{\text{W}}$	n/a	n/a	7.5	1.4	12	8	PerClk	
PerReady	7.5	-0.5	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:3}}$	n/a	n/a	7.5	1.3	12	8	PerClk	
PerClk	n/a	n/a	0.5	-0.9	17	11	PLB Clk	5
PerErr	4.0	-0.6	n/a	n/a	n/a	n/a	PerClk	
External Master Peripheral Interface								
BusReq	n/a	n/a	8	0	12	8	PerClk	
$\overline{\text{ExtAck}}$	n/a	n/a	7	0	12	8	PerClk	
$\overline{\text{ExtReq}}$	5	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{ExtReset}}$	n/a	n/a	8	0	19	12	PerClk	
HoldAck	n/a	n/a	8	0	12	8	PerClk	
HoldPri	4	1	n/a	n/a	n/a	n/a	PerClk	
HoldReq	5	1	n/a	n/a	n/a	n/a	PerClk	

I/O Specifications—266MHz (Part 1 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
PCI Interface								
PCIAD0:31					12.3	15.5	PCIClk	6
PCIC0:3[$\overline{BE3:0}$]					12.3	15.5	PCIClk	6
PCIClk			n/a	n/a	n/a	n/a		async
$\overline{PCIDevSel}$					12.3	15.5	PCIClk	6
$\overline{PCIFrame}$					12.3	15.5	PCIClk	6
$\overline{PCIGnt0}$[Req] PCIGnt1:5	n/a	n/a			12.3	15.5	PCIClk	6
PCIIDSel					n/a	n/a	PCIClk	6
$\overline{PCIINT}$[PerWE]	n/a	n/a			12.3	15.5	PCIClk	async
$\overline{PCIIRDY}$					12.3	15.5	PCIClk	6
PCIParity					12.3	15.5	PCIClk	6
$\overline{PCIPErr}$					12.3	15.5	PCIClk	6
$\overline{PCIReq0}$[Gnt] PCIReq1:5			n/a	n/a	n/a	n/a	PCIClk	6
$\overline{PCIReset}$	n/a	n/a	n/a	n/a	12.3	15.5	PCIClk	
$\overline{PCISErr}$	n/a	n/a	n/a	n/a	12.3	15.5	PCIClk	
$\overline{PCIStop}$					12.3	15.5	PCIClk	6
$\overline{PCITRDY}$					12.3	15.5	PCIClk	6
Ethernet Interface								
EMC0MDClk	n/a	n/a	7.4	1.5	12	8		1, async
EMC0MDIO	n/a	n/a	6.7	1.2	12	8	EMC0MDClk	1
EMC0TxD0:3 [EMC0Tx0:1D0:1 [EMC0Tx0:3D]	n/a	n/a	7.7 [5.6] [4.6]	3.0 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxEn [EMC0Tx0En] [EMC0Sync]	n/a	n/a	9.4 [5.5] [4.2]	2.9 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxErr [EMC0Tx1En]	n/a	n/a	9.4[5.7]	2.9[2.4]	12	8	PHYTX	1
[EMC1TxD0:3] [EMC1Tx2:3D0:1]					12	8		
[EMC1TxEn] [EMC1Tx2En]					12	8		
[EMC1TxErr] [EMC1Tx3En]					12	8		

I/O Specifications—266MHz (Part 2 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
PHY0Col[PHY0Rx1Er]l	async[0.1]	async[1.4]	n/a	n/a	n/a	n/a		1
PHY0CrS[PHY0CrS0DV]	async[0.1]	async[1.5]	n/a	n/a	n/a	n/a		1
PHY0RxClk	n/a	n/a	n/a	n/a	n/a	n/a		1, async
PHY0RxD0:3 [PHY0Rx0:1D0:1] [PHY0Rx0:3D]	1.5 [0.8] [0.8]	1.4 [1.3] [0.2]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxDV [PHY0CRS1DV]	1.3[0.7]	1.3[1.3]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxErr[PHY0Rx0Er]	1.3[0.7]	1.4[1.5]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0TxClk[PHY0RefClk]	n/a	n/a	n/a	n/a	n/a	n/a		1, async
[PHY1RxD0:3] [PHY1Rx2:3D0:1]					n/a	n/a		
[PHY1Col] [PHY1Rx3Er]					n/a	n/a		
[PHY1CrS] [PHY1CrS2DV]					n/a	n/a		
[PHY1RxClk]					n/a	n/a		
[PHY1RxDV] [PHY1CrS3DV]					n/a	n/a		
[PHY1RxErr] [PHY1Rx2Er]					n/a	n/a		
[PHY1TxClk]					n/a	n/a		
HDLCEX Interface								
HDLCEXRxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXRxDataA:B	23.8	1.5	n/a	n/a	n/a	n/a		
HDLCEXRxFS	24.2	0.8	n/a	n/a	n/a	n/a		
HDLCEXTxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXTxDataA:B	n/a	n/a	7.6	3.3	12	8		
HDLCEXTxFS	24.2	0.8	n/a	n/a	n/a	n/a		
HDLCEXTxEnA [CGPIO24][$\overline{\text{UART1\_RTS}}$]	n/a	n/a	8.5	3.5	12	8		
HDLCEXTxEnB [CGPIO25][$\overline{\text{UART1\_DTR}}$]	n/a	n/a	8.9/	3.8	12	8		
HDLCMP Interface								
HDLCMPTxClk0:3					n/a	n/a		
[HDLCMPTxClk4:7]					n/a	n/a		
HDLCMPTxData0:3					12	8		

I/O Specifications—266MHz (Part 3 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
[HDLCMPTxData4:7]					12	8		
[HDLCMPTxEn0:7]					12	8		
HDLCMPRxClk0:3					n/a	n/a		
[HDLCMPRxClk4:7]					n/a	n/a		
HDLCMPRxData0:3					n/a	n/a		
[HDLCMPRxData4:7]					n/a	n/a		
Internal Peripheral Interface								
IICSCL	async	async	async	async	17	11		
IICSDA	async	async	async	async	17	11		
[$\overline{\text{UART0\_CTS}}$]CGPIO26	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_DCD}}$]CGPIO28	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_DSR}}$]CGPIO27	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_DTR}}$]CGPIO31	n/a	n/a	async	async	12	8		
[$\overline{\text{UART0\_RI}}$][CGPIO29]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_RTS}}$]CGPIO30	n/a	n/a	async	async	12	8		
UART0_Rx	async	async	n/a	n/a	n/a	n/a		
UART0_Tx	n/a	n/a	async	async	12	8		
[$\overline{\text{UART1\_CTS}}$]CGPIO20	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_DCD}}$]CGPIO22	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_DSR}}$]CGPIO21	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_DTR}}$]CGPIO25	n/a	n/a	async	async	12	8		
[$\overline{\text{UART1\_RI}}$]CGPIO23	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_RTS}}$]CGPIO24	n/a	n/a	async	async	12	8		
UART1_Rx	async	async	n/a	n/a	n/a	n/a		
UART1_Tx	n/a	n/a	async	async	12	8		
UARTSerClk	async	async	n/a	n/a	n/a	n/a		
Interrupts Interface								
[IRQ0:6]SGPIO17:23	async	async	n/a	n/a	n/a	n/a		
JTAG Interface								
TCK	async	async	n/a	n/a	n/a	n/a		
TDI	async	async	n/a	n/a	n/a	n/a		
TDO	n/a	n/a	async	async	12	8		
TMS	async	async	n/a	n/a	n/a	n/a		
$\overline{\text{TRST}}$	async	async	n/a	n/a	n/a	n/a		

I/O Specifications—266MHz (Part 4 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
System Interface								
SGPIO0					12	8		
[TrcClk]SGPIO31	n/a	n/a	8.7	1.2	12	8		
[TS1E]SGPIO1	n/a	n/a	5.8	1.2	12	8		
[TS2E]SGPIO2	n/a	n/a	5.7	1.2	12	8		
[TS1O]SGPIO3	n/a	n/a	5.3	1.0	12	8		
[TS2O]SGPIO4	n/a	n/a	5.3	1.0	12	8		
[TS3]SGPIO5	n/a	n/a	5.3	1.0	12	8		
[TS4]SGPIO6	n/a	n/a	5.3	1.0	12	8		
[TS5]SGPIO7	n/a	n/a	5.4	1.0	12	8		
[TS6]SGPIO8	n/a	n/a	5.3	1.0	12	8		
$\overline{\text{Halt}}$	async	async	n/a	n/a	n/a	n/a		
SysClk	n/a	n/a	n/a	n/a	n/a	n/a		
SysErr	n/a	n/a	5.3	1.7	12	8		
$\overline{\text{SysReset}}$	n/a	n/a	n/a	n/a	12	8		
TestEn	dc	dc	n/a	n/a	n/a	n/a		
TmrClk	n/a	n/a	async	async	n/a	n/a		
SDRAM Interface								
BA1:0	n/a	n/a	5.5	1.5	19	12	SysClk	1, 2
$\overline{\text{BankSe3:0}}$	n/a	n/a	4.6	1.0	19	12	SysClk	2
$\overline{\text{CAS}}$	n/a	n/a	5.3	1.4	19	12	SysClk	1, 2
ClkEn0:1	n/a	n/a	3.9	1.0	40	25	SysClk	2
DQM3:0	n/a	n/a	4.7	1.0	19	12	SysClk	2
DQMCB	n/a	n/a	4.7	1.0	19	12	SysClk	2
ECC7:0	1.8	0.3	4.5	1.0	19	12	SysClk	2
MemAddr12:0	n/a	n/a	5.5	1.4	19	12	SysClk	1, 2
MemClkOut0:1	n/a	n/a	0.4	-1.2	19	12	SysClk	2, 3
MemData31:0	1.8	0.3	4.4	1.0	19	12	SysClk	2
$\overline{\text{RAS}}$	n/a	n/a	5.7	1.6	19	12	SysClk	1, 2
$\overline{\text{WE}}$	n/a	n/a	5.4	1.4	19	12	SysClk	1, 2

I/O Specifications—266MHz (Part 5 of 5)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
6. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
External Slave Peripheral Interface								
$\overline{\text{DMAReq0:3}}$[SGPIO9:12]	4.1	0.0	5.5	1.1	n/a	n/a	PerClk	
$\overline{\text{DMAAck0:3}}$[SGPIO13:16]	n/a	n/a	5.8	1.1	12	8	PerClk	
$\overline{\text{EOT0:3}}$[$\overline{\text{TC0:3}}$] [SGPIO24:27]	3.7	-0.1	6.7	1.2	12	8	PerClk	
PerAddr4:31	n/a	n/a	6.5	0.9	17	11	PerClk	
$\overline{\text{PerBLast}}$	n/a	n/a	5.6	1.4	12	8	PerClk	
$\overline{\text{PerCS0:3}}$	n/a	n/a	5.5	1.3	12	8	PerClk	
PerData0:31	3.9	1.0	7.1	1.0	17	11	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	5.7	1.4	12	8	PerClk	
PerPar0:3	2.7	0.0	6.4	0.9	17	11	PerClk	
PerR/$\overline{\text{W}}$	n/a	n/a	5.7	1.4	12	8	PerClk	
PerReady	6.2	-0.5	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:3}}$	n/a	n/a	5.7	1.3	12	8	PerClk	
PerClk	n/a	n/a	0.5	-0.9	17	11	PLB Clk	4
PerErr	3.5	-0.6	n/a	n/a	n/a	n/a	PerClk	
External Master Peripheral Interface								
BusReq	n/a	n/a			12	8	PerClk	
$\overline{\text{ExtAck}}$	n/a	n/a			12	8	PerClk	
$\overline{\text{ExtReq}}$			n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{ExtReset}}$	n/a	n/a			19	12	PerClk	
HoldAck	n/a	n/a			12	8	PerClk	
HoldPri			n/a	n/a	n/a	n/a	PerClk	
HoldReq			n/a	n/a	n/a	n/a	PerClk	

Initialization

The following describes the method by which initial chip settings are established when a system reset occurs.

EEPROM

The default initial conditions can be read from a serial EEPROM.

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