

622 Mbit/s ATM and Packet Over SONET Physical Layer Device

FEATURES

GENERAL

- ATM and Packet over SONET/SDH (POS) OC-12c (622 Mbit/s) PHY
- Provides on-chip clock and data recovery and clock synthesis
- Exceeds Bellcore-GR-253 jitter requirements
- Inserts and extracts ATM cells or POS packets into/from SONET SPE
- Filters and captures Automatic Protection Switch bytes (K1,K2) and detects APS byte failure
- Detects signal degrade and signal failure thresholds crossing alarms
- Captures and debounces synchronization status byte (S1)
- Extracts and Inserts the 16 or 64-byte section trace (J0) and path trace (J1) messages
- Extracts and inserts section/line data communication channels (DCC)
- Provides circuitry to meet holdover, wander and long term stability
- Provides a generic 8-bit

microprocessor interface for device control and register access

- Provides standard IEEE 1149.1 JTAG test port for boundary scan

ATM

- Implements the ATM Forum User Network Interface Specification
- Performs cell payload scrambling and descrambling
- Provides a UTOPIA Level 2 and an 8-bit 100MHz UTOPIA Level 3 compliant system interface
- Provides synchronous 4 cell transmit and receive FIFO buffers

PACKET OVER SONET/SDH

- Supports direct packet mapping into SONET/SDH such as PPP, HDLC and Frame Relay
- Implements the PPP over SONET/SDH specification according to RFC 1619 and 1662 of the IETF
- Performs flag sequence detection and insertion
- Performs CRC-CCITT and CRC-32 FCS generation and validation

- Performs byte stuffing and destuffing
- Checks for minimum and maximum packet lengths
- Checks for packet abort sequence
- Performs X⁴³⁺¹ payload scrambling
- Provides a SATURN POS-PHY Level 2 and an 8-bit 100MHz POS-PHY Level 3 system interface
- Provides synchronous 256 byte transmit and receive FIFO buffers

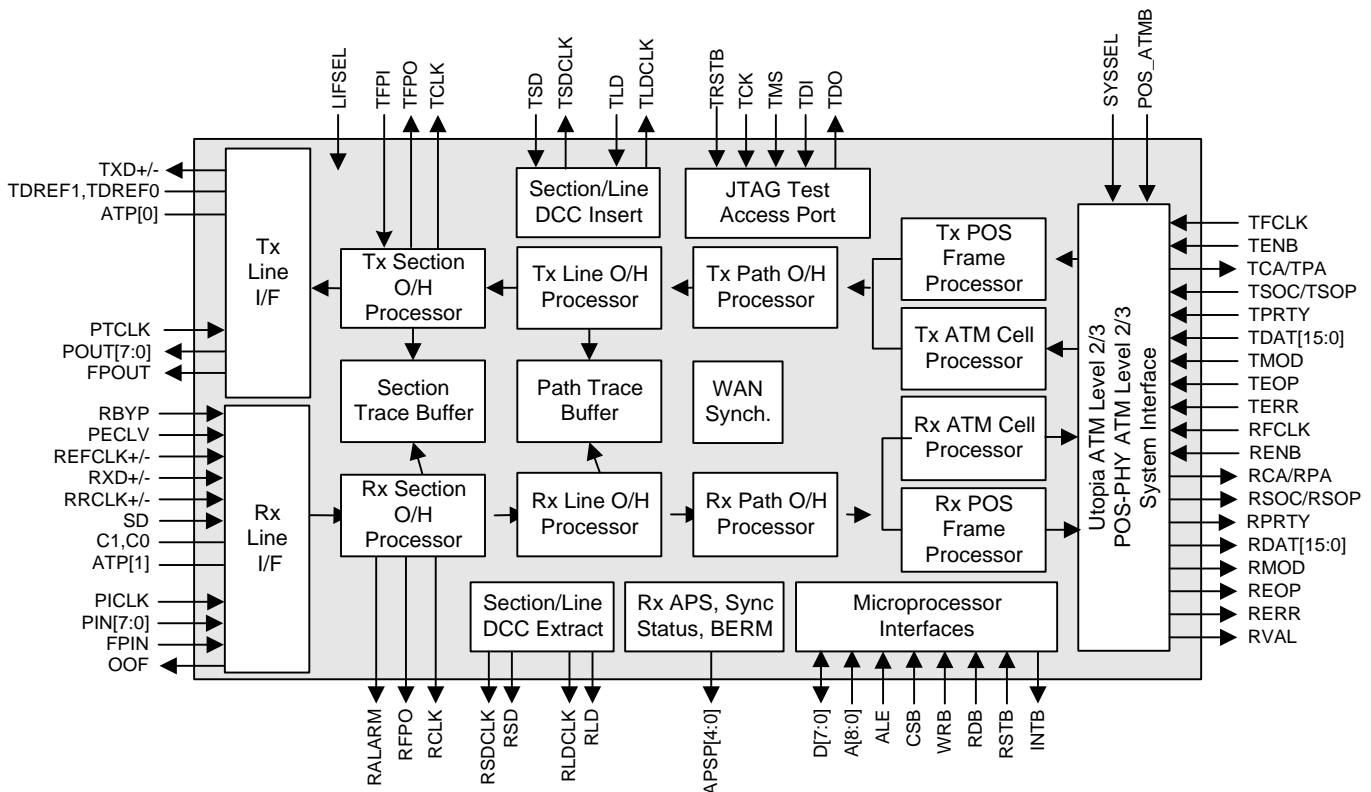
PACKAGING

- Implemented in low power 3.3 Volt CMOS technology
- Packaged in a 304 SBGA
- Industrial temperature range (-40°C to +85°C)

APPLICATIONS

- WAN and Edge ATM switches
- Multiprotocol switches
- Layer 3 switches
- Routers, Packet switches and Hubs

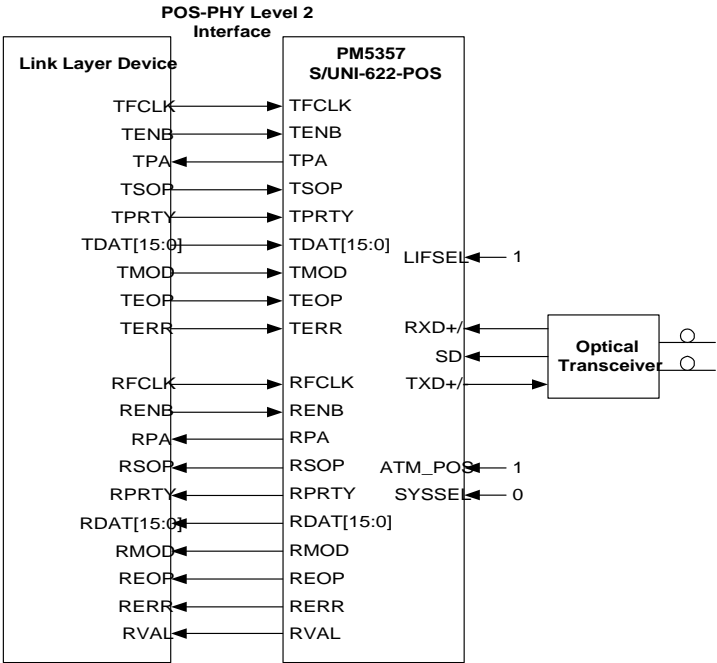
BLOCK DIAGRAM



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TYPICAL APPLICATIONS

POS-PHY LEVEL 2 APPLICATION



POS-PHY LEVEL 3 APPLICATION

