



## PI6C2520

### Low-Noise Phase-Locked Loop Clock Driver with 20 Clock Outputs

#### Product Features

- Low-Noise Phase-Locked Loop Clock Distribution.
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction. The clock outputs track the Clock Input modulation.
- Maximum clock frequency of 125 MHz.
- Zero Input-to-Output delay.
- Low jitter: Cycle-to-Cycle jitter  $\pm 100$ ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction.
- Operates at 3.3V V<sub>CC</sub>.
- Output-to-Output skew less than 200ps.
- Package: Plastic 56-pin TSSOP (A).

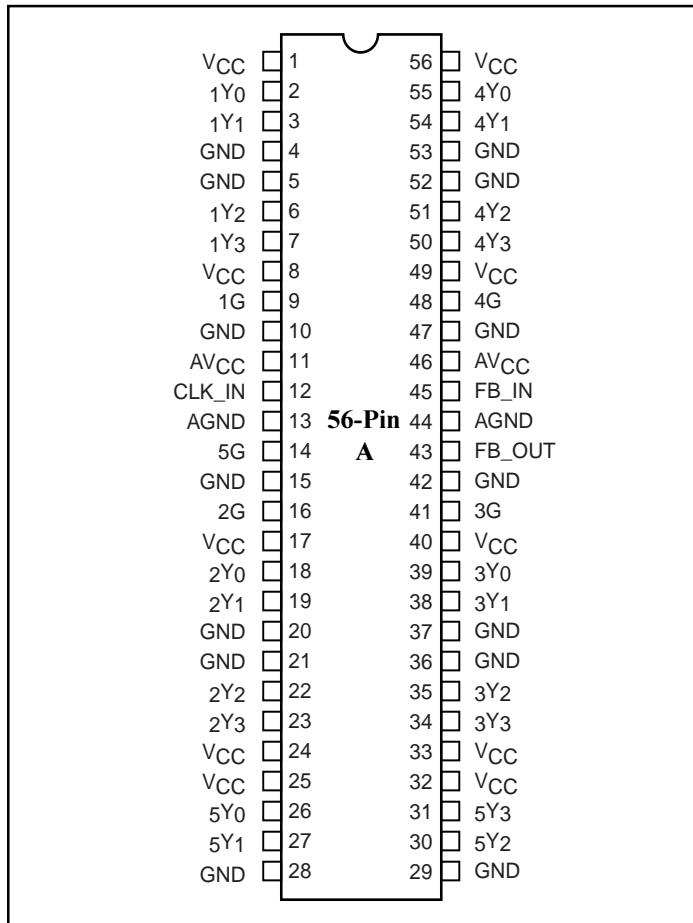
#### Product Description

The PI6C2520 is a low-skew, low-jitter, phase-locked loop (PLL) clock driver, distributing low-noise clock signals for Networking Applications. By connecting the feedback FB\_OUT output to the feedback FB\_IN input, the propagation delay from the CLK\_IN input to any clock output will be nearly zero. This zero-delay feature allows the CLK\_IN input clock to be distributed, providing 5 banks of 4 clocks and an extra clock for feedback.

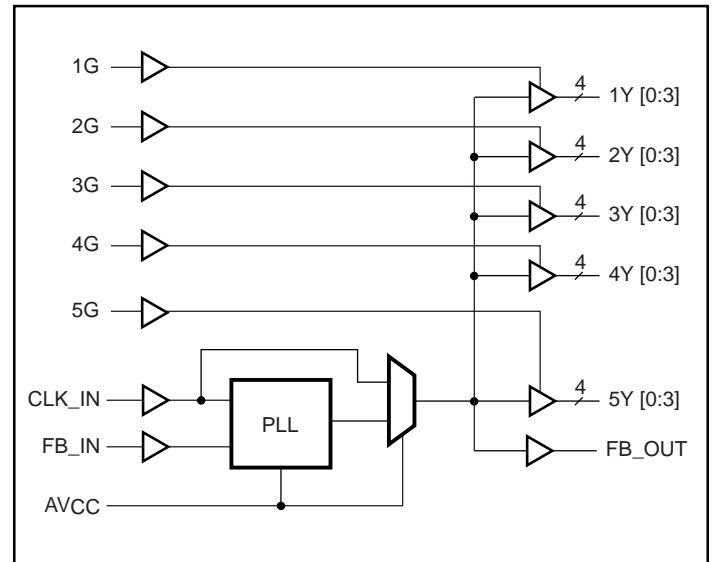
For test purposes, the PLL can be bypassed by strapping AV<sub>CC</sub> to ground. The PI6C2520, which allows a Spread Spectrum clock input, operates at 3.3V V<sub>CC</sub> and provides integrated series-damping resistors that make it ideal for driving point-to-point loads. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at the input clock.

Each bank of outputs can be enabled or disabled via the 1G, 2G, 3G, 4G, and 5G control inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK\_IN. When the G inputs are low, the outputs are disabled to the logic low state.

#### Product Pin Configuration



#### Block Diagram



## Pin Functions

Pin Name	Pin Number	Type	Description
CLK_IN	12	I	Clock input. CLK allows spread spectrum.
FB_IN	45	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
1G	9	I	Output bank enable. When 1G is LOW, outputs 1Y[0:3] are disabled to a logic low state. When 1G is HIGH, all outputs 1Y[0:3] are enabled.
2G	16	I	Output bank enable. When 2G is LOW, outputs 2Y[0:3] are disabled to a logic low state. When 2G is HIGH, all outputs 2Y[0:3] are enabled.
3G	41	I	Output bank enable. When 3G is LOW, outputs 3Y[0:3] are disabled to a logic low state. When 3G is HIGH, all outputs 3Y[0:3] are enabled.
4G	48	I	Output bank enable. When 4G is LOW, outputs 4Y[0:3] are disabled to a logic low state. When 4G is HIGH, all outputs 4Y[0:3] are enabled.
5G	14	I	Output bank enable. When 5G is LOW, outputs 5Y[0:3] are disabled to a logic low state. When 5G is HIGH, all outputs 5Y[0:3] are enabled.
FB_OUT	43	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs 1Yx, 2Yx, 3Yx, 4Yx, and 5Yx.
1Y[0:3]	2,3,6,7	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
2Y[0:3]	18,19,22,23	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
3Y[0:3]	39,38,35,34	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
4Y[0:3]	55,54,51,50	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
5Y[0:3]	26,27,30,31	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
AVCC	11,46	Power	Analog power supply. AVCC can be also used to bypass the PLL for test purposes. When AVCC is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	13,44	Ground	Analog ground. AGND provides the ground reference for the analog circuitry
VCC	1,8,17,24,25,32,33,40,49,56	Power	Power supply
GND	4,5,10,15,20,21,28,29,36,37,42,47,52,53	Ground	Ground

**Absolute Maximum Ratings** (Over Operating Free-Air Temperature, unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5V to 4.6V
Input voltage range, $V_I$ <sup>(1)</sup> .....	-0.5V to 6.5V
Voltage range applied to any output in the high or low state, $V_O$ <sup>(1,2)</sup> .....	-0.5V to $V_{CC}+0.5V$
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50mA
Continuous current through each $V_{CC}$ or GND .....	±100mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) <sup>(3)</sup> .....	0.85W
Storage Temperature Range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

**Notes:**

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6V maximum.
3. Maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

**Recommended Operating Conditions**<sup>(4)</sup>

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Supply voltage	3	3.6	V
$V_{IH}$	High-level input voltage	2		
$V_{IL}$	Low-level input voltage		0.8	
$V_I$	Input Voltage	0	$V_{CC}$	
$I_{OH}$	High-level output current		-12	mA
$I_{OL}$	Low-level output current		12	
$T_A$	Operating free-air temperature	0	70	°C

**Notes:**

4. Unused inputs must be held high or low to prevent them from floating.

**Function Table**

xG	CLK_IN	xY [0:3]	FB_OUT
L	L	L	L
L	H	L	H
H	L	L	L
H	H	H	H

**Note:**

x is from 1 to 5

**Electrical Characteristics** (Over Recommended Operating Free-air Temperature Range, unless otherwise noted)

Symbol	Test Condition	V <sub>CC</sub>	Min.	Typ. <sup>(1)</sup>	Max.	Units
V <sub>IK</sub> , Input clamp voltage	Input current at -18mA	3V		-0.79	-1.2	V
V <sub>OH</sub>	I <sub>OH</sub> = -100μA	Min. to Max.	V <sub>CC</sub> -0.2	2.99		
	I <sub>OH</sub> = -12mA	3V	2.1	2.66		
	I <sub>OH</sub> = -6mA		2.4	2.83		
V <sub>OL</sub>	I <sub>OL</sub> = 100μA	Min. to Max.		0.01	0.2	
	I <sub>OL</sub> = 12mA	3V		0.3	0.8	
	I <sub>OL</sub> = 6mA			0.15	0.55	
I <sub>I</sub> , Input current	Clock input voltage = V <sub>CC</sub> or GND	3.6V			±5	μA
I <sub>CC</sub> , Analog supply current	Clock input voltage = V <sub>CC</sub> or GND				20	
C <sub>i</sub>	Input voltage = V <sub>CC</sub> or GND	3.3V		4	3.5	pF
C <sub>O</sub>	Output voltage = V <sub>CC</sub> or GND			6		
ΔI <sub>CC</sub>	One input @ V <sub>CC</sub> -0.6V, other inputs @ V <sub>CC</sub> or GND	3.3V to 3.6V		4.0	500	μA

**Notes:**

- For Min. or Max. conditions, use the appropriate value specified under recommended operating conditions.

**Timing Requirements** (Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature).

Symbol	Parameter	Min.	Max.	Units	Note
F <sub>CLK</sub>	Clock Frequency	25	125	MHz	1
D <sub>CYI</sub>	Input clock duty cycle	40	60	%	
t <sub>Stabilization</sub>	Stabilization Time after power up		1	ms	

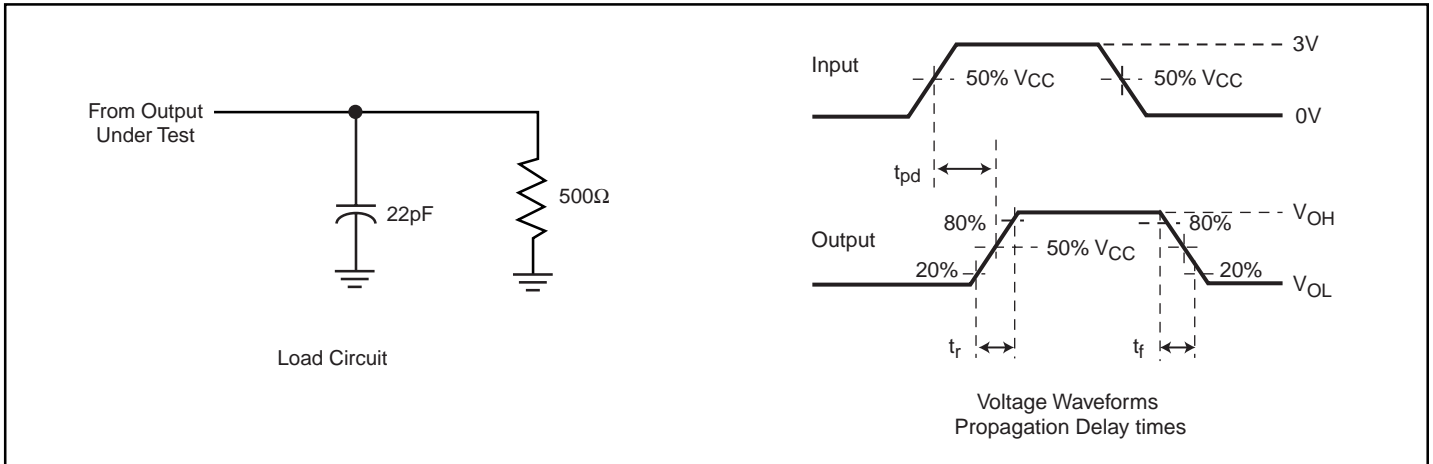
**Switching Characteristics** (Over Recommended Ranges of Supply Voltage & Operating Free-Air Temperature, C<sub>L</sub> = 22pF)<sup>(1,3)</sup>

Parameter	From (Input)	To (Output)	V <sub>CC</sub> = 3.3V ± 0.3V			Units
			Min.	Typ.	Max.	
t <sub>phase error</sub>	CLK_IN↑ = 100MHz	FB_IN↑		170		ps
t <sub>sk(O)</sub> <sup>(2)</sup>	Any Y or FBOUT	Any Y or FB_OUT			200	
Jitter <sub>(pk-pk)</sub>	F(CLK_IN > 66MHz)		-100		100	
Duty cycle	F(CLK_IN ≤ 66MHz)		45		55	%
	F(CLK_IN > 66MHz)		45		55	
t <sub>r</sub>	Measured from 20% to 80%		0.7		2.8	ns
t <sub>f</sub>			1.2		2.8	

**Notes:**

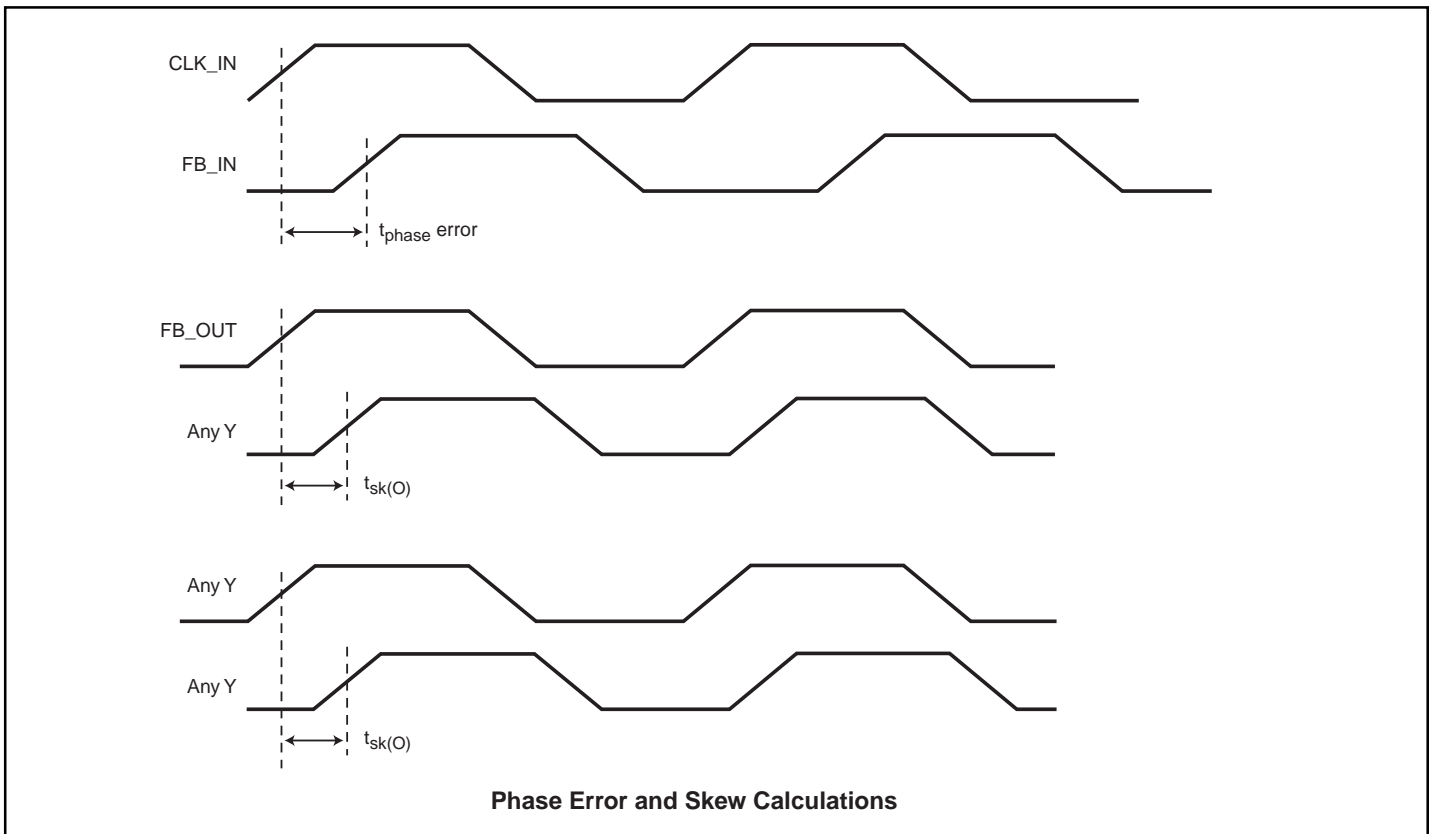
- These parameters are not production tested.
- The t<sub>sk(o)</sub> specification is only valid for equal loading of all outputs.
- The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

## Parameter Measurement Information

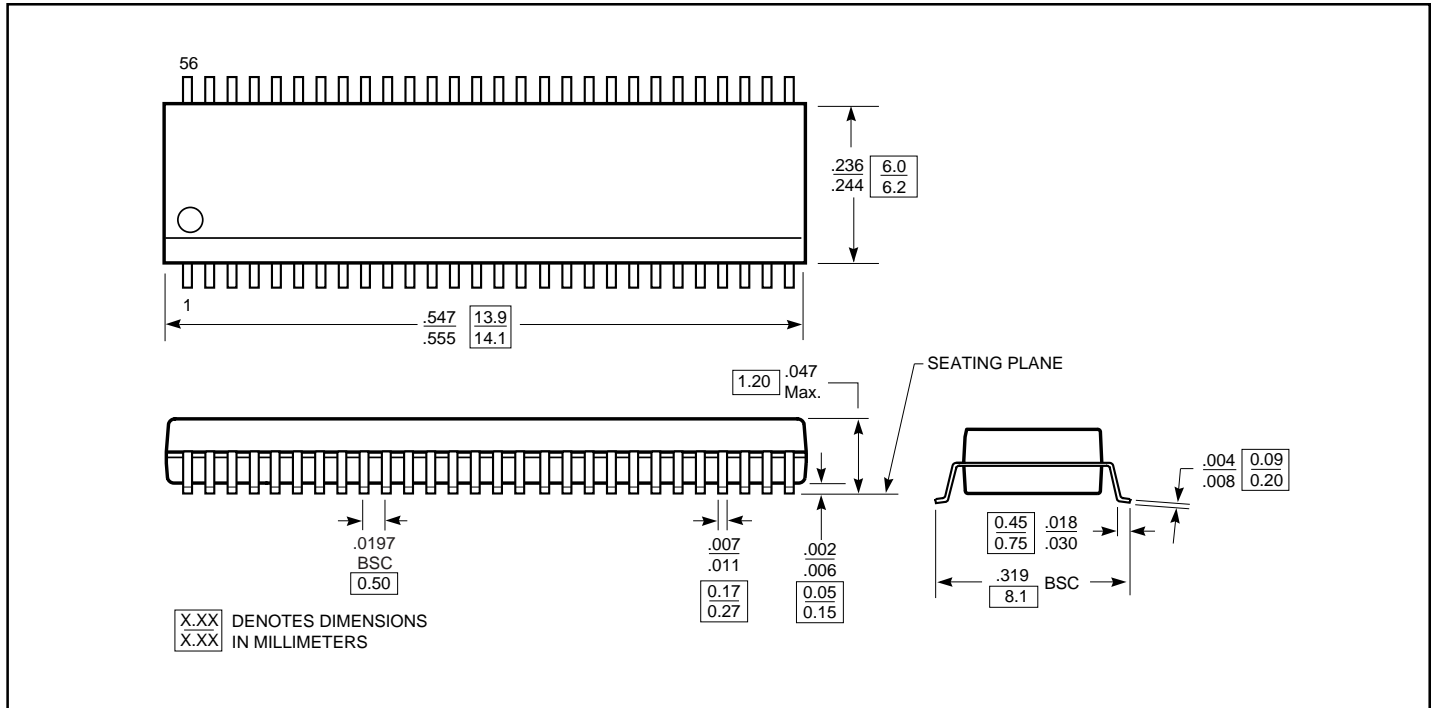


### Notes:

1.  $C_L$  includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:  $CLK\_IN \leq 100MHz$ ,  $Z_O = 50\text{ ohms}$ ,  $t_r \leq 1.2ns$ ,  $t_f \leq 1.2ns$ .
3. The outputs are measured one at a time with one transition per measurement.



### 56-pin Thin Shrink Small-Outline Package (A)



### Ordering Information

Part Number	Ordering P/N	Package
PI6C2520	PI6C2520A	56-Pin TSSOP