RAMBUS® DRAM

MT6V16M16 - 512K x 16 x 32 banks
MT6V16M18 - 512K x 18 x 32 banks

For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/datasheets/datasheet.html

FEATURES

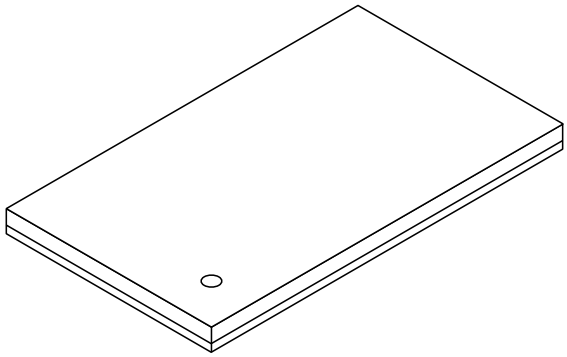
- High-speed 300 MHz, 356 MHz, and 400 MHz clocks with 2x data rates
- 1.6 GB/s peak I/O bandwidth
- Rambus® signaling level (RSL) using differential 300 MHz, 356 MHz, and 400 MHz transmit and receive clocks
- Packet-oriented Rambus protocol transmitted in 8-bit-long packets
- Separate control (8-bit) and data (18-bit) buses for increased data bandwidth capability
- Control bus with separate row (3-bit) and column (5-bit) buses for easier command scheduling
- Programmable output delay timing for roundtrip delay of one to five cycles
- Support for up to four simultaneous transactions (within bank restrictions)
- Write buffer to reduce READ latency
- Three precharge mechanisms for controller flexibility
- Programmable power states for flexibility in power consumption versus data access time
- Power-down Self-Refresh and Active Refresh
- Organization: 2KB pages and 32 banks, x16 or x18
- FBGA package
- Interleaved Data Mode (IDM) on the MT6V16M18 for system level error correction
- 32ms, 16,384 cycle refresh
- 2.5V power supply with 1.8V CMOS supply for I/Os

OPTIONS — NUMBER

- Configurations
  - 16 Meg x 16 — 16M16
  - 16 Meg x 18 — 16M18
- Package
  - FBGA (84-pin, 2-row depopulated pinout) — F2
- Timing (Cycle Time)
  - 300 MHz Clock Rate, Access Time = 53ns — -3M
  - 356 MHz Clock Rate, Access Time = 50ns — -3B
  - 356 MHz Clock Rate, Access Time = 45ns — -3C
  - 400 MHz Clock Rate, Access Time = 45ns — -4C
  - 400 MHz Clock Rate, Access Time = 40ns — -4D

Part Number Example:
MT6V16M16F2-3B

84-PIN FBGA
(TOP VIEW)



RDRAM® PART NUMBERS

PART NUMBER	ORGANIZATION[1]	CLK FREQ. (MHz)	ACCESS TIME (ns)
MT6V16M16F2-3M	512K x 16 x 32	300	53
MT6V16M16F2-3B	512K x 16 x 32	356	50
MT6V16M16F2-3C	512K x 16 x 32	356	45
MT6V16M16F2-4C	512K x 16 x 32	400	45
MT6V16M16F2-4D	512K x 16 x 32	400	40
MT6V16M18F2-3M	512K x 18 x 32	300	53
MT6V16M18F2-3B	512K x 18 x 32	356	50
MT6V16M18F2-3C	512K x 18 x 32	356	45
MT6V16M18F2-4C	512K x 18 x 32	400	45
MT6V16M18F2-4D	512K x 18 x 32	400	40

NOTE: 1. The "x32" designation indicates that this RDRAM core is comprised of 32 banks which use a "split" bank architecture.

GENERAL DESCRIPTION

The MT6V16M16 RDRAM® is a general-purpose, high-performance, packet-oriented, dynamic random-access memory containing 268,435,456, bits. The MT6V16M16 is internally configured as 32 banks of 64K x 128; each of the 64K x 128 banks is organized as 512 rows by 128 columns by 128 bits. The 128 bits are serially multiplexed onto the RDRAM's I/O pins as eight 16-bit words.

The MT6V16M18 RDRAM is a general-purpose, high-performance, packet-oriented, dynamic random-access memory containing 301,989,888 bits. The MT6V16M18 is internally configured as 32 banks of 64K x 144; each of the 64K x 144 banks is organized as 512 rows by 128 columns by 144 bits. The 144 bits are serially multiplexed onto the RDRAM's I/O pins as eight 18-bit words.

The MT6V16M16/MT6V16M18 use Rambus signaling level (RSL) technology to achieve 300 MHz, 356 MHz or 400 MHz clock speeds using differential clocks. Control and I/O data is transferred on both rising and falling edges of the clock. This allows data transfers at 1.25ns per two bytes (10ns per 16 bytes) during peak operation.

All DRAM commands are communicated to the MT6V16M16/MT6V16M18 through a 3-bit row or 5-bit column bus in packets which are 8 bits in length. These packets are then decoded on the RDRAM into the operation and address requiring access.

Initialization and mode configuration for the MT6V16M16/MT6V16M18 are accessed through the slow-speed CMOS serial I/O interface.

The architecture of RDRAMs allows high sustained bandwidth memory transactions for multiple, simultaneous, semi-random addresses. The RDRAM's 32 banks can support up to four simultaneous transactions (within bank restrictions).

System-oriented features include power management, byte masking, and x18 organization. The two data bits in the x18 organization are general and can be used for additional storage and bandwidth, or for error correction. Additionally, the MT6V16M18 includes interleaved data mode (IDM) which may be used to enable higher error correction algorithms at system level.

DEVICE PINOUT

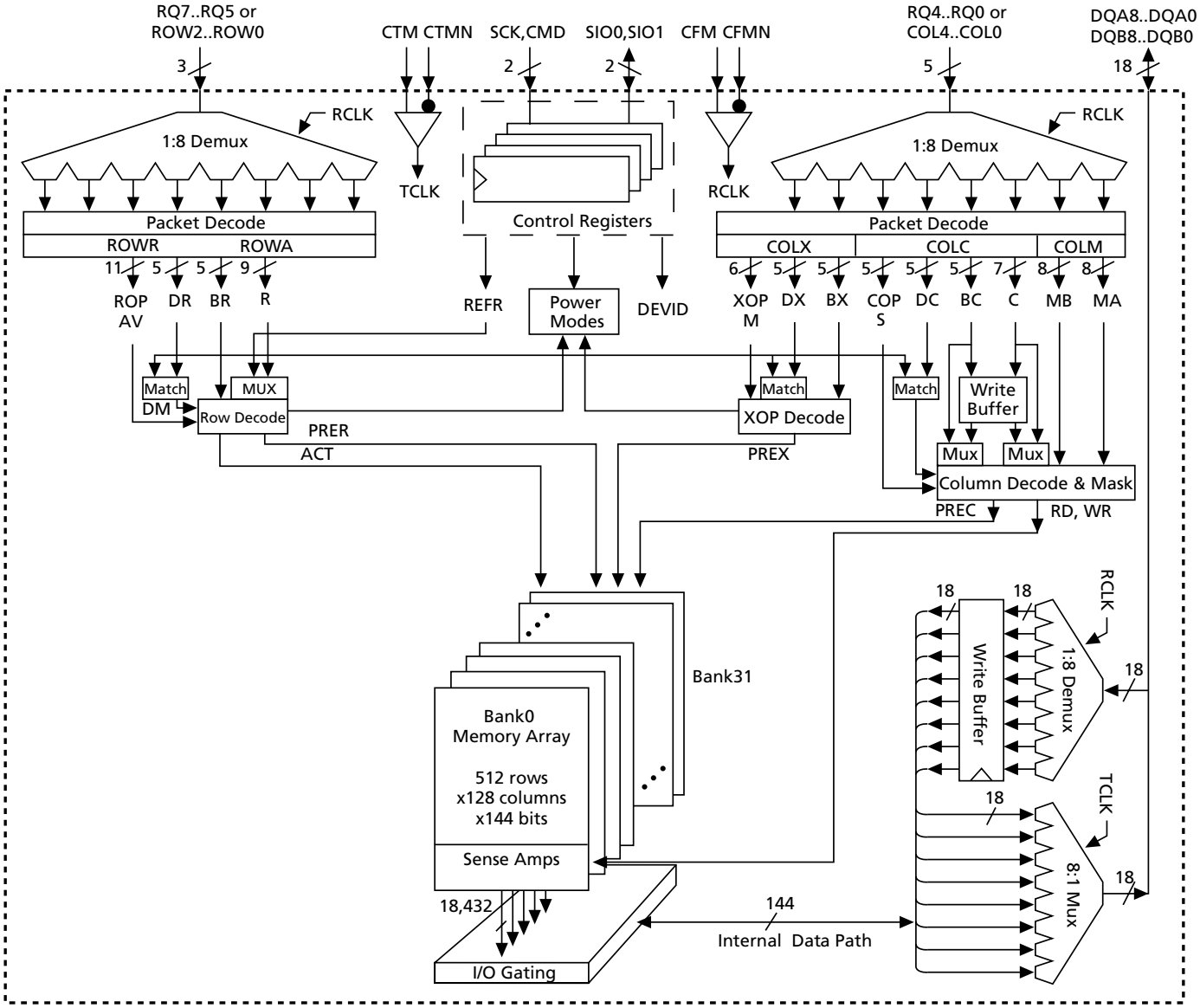
The pinout tables below show the pin assignments of the center-bonded RDRAM package from the top side of the package (the view looking down on the package as it is mounted on the circuit board). The MT6V16M16 and MT6V16M18 devices are available in an FBGA package with a ball pitch of 0.8mm.

FBGA PACKAGE
F2 PINOUT
(TOP VIEW)

10	V_{DD}	GND		V_{DD}	GND	V_{DD}					V_{DD}	V_{DD}	V_{DD}		GND	V_{DD}
9																
8	V_{DD}	CMD	V_{DD}	GND	GNDa	GNDa	V_{DD}	V_{DD}	GND	GND	V_{DD}	V_{DD}	GND	GND	V_{CMOS}	V_{DD}
7	DQA8	DQA7	DQA5	DQA3	DQA1	CTMN	CTM	RQ7	RQ5	RQ3	RQ1	DQB1	DQB3	DQB5	DQB7	DQB8
6																
5																
4	GND	DQA6	DQA4	DQA2	DQA0	CFM	CFMN	RQ6	RQ4	RQ2	RQ0	DQB0	DQB2	DQB4	DQB6	GND
3	GND	SCK	V_{CMOS}	GND	V_{DD}	GND	V_{DDa}	V_{REF}	GND	V_{DD}	GND	GND	V_{DD}	SIO0	SIO1	GND
2																
1	V_{DD}	GND		GND	V_{DD}	GND					GND	GND	GND		GND	V_{DD}
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**	**K**	**L**	**M**	**N**	**P**	**R**	**S**

NOTE: For the MT6V16M16 device, DQA8 and DQB8 are no connects.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The drawing is for the MT6V16M18 device. The MT6V16M16 device has a 128-bit internal bus width (instead of 144) and DQA8/DQB8 are not used.
2. Function Block Diagrams illustrate simplified device operation.

DEVICE MARKING

Due to the size of the package, Micron's standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used (see Figure 1). The abbreviated device marks are cross referenced to the Micron part numbers in Table 1.

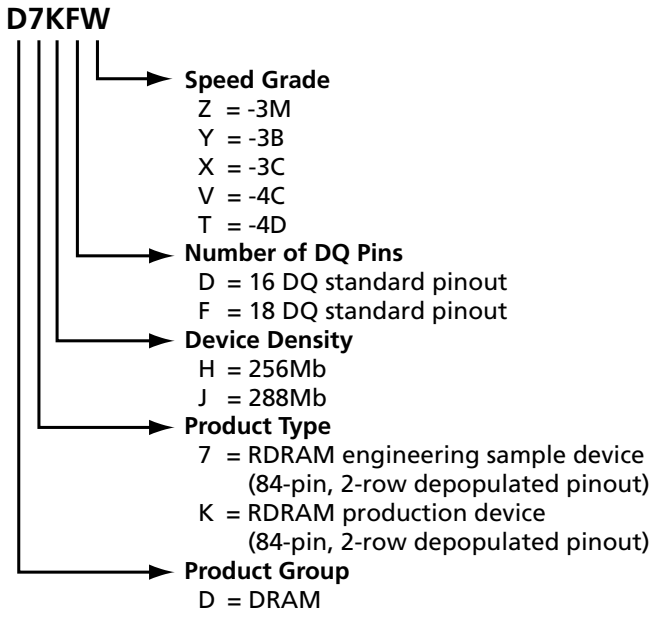


Figure 1
Abbreviated Device Mark

Table 1
Cross Reference for Abbreviated Device Marks

PART NUMBER	CLK FREQ. (MHz)	ACCESS TIME (ns)	SAMPLE MARKING	PRODUCTION MARKING
MT6V16M16F2-3M	300	53	D7HDZ	DKHDZ
MT6V16M16F2-3B	356	50	D7HDY	DKHDY
MT6V16M16F2-3C	356	45	D7HDX	DKHDX
MT6V16M16F2-4C	400	45	D7HDV	DKHDV
MT6V16M16F2-4D	400	40	D7HDT	DKHDT
MT6V16M18F2-3M	300	53	D7JFZ	DKJFZ
MT6V16M18F2-3B	356	50	D7JFY	DKJFY
MT6V16M18F2-3C	356	45	D7JFX	DKJFX
MT6V16M18F2-4C	400	45	D7JFV	DKJFV
MT6V16M18F2-4D	400	40	D7JFT	DKJFT

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