



# HCPL0600, HCPL0601, HCPL0611, HCPL0637, HCPL0638, HCPL0639 High Speed-10 MBit/s Logic Gate Optocouplers

Single Channel: HCPL0600, HCPL0601, HCPL0611  
Dual Channel: HCPL0637, HCPL0638, HCPL0639

## Features

- Compact SO8 package
- Very high speed-10 MBit/s
- Superior CMR
- Logic gate output
- Storable output (single channel devices)
- Wired OR-open collector
- U.L. recognized (File # E90700)
- VDE approval pending

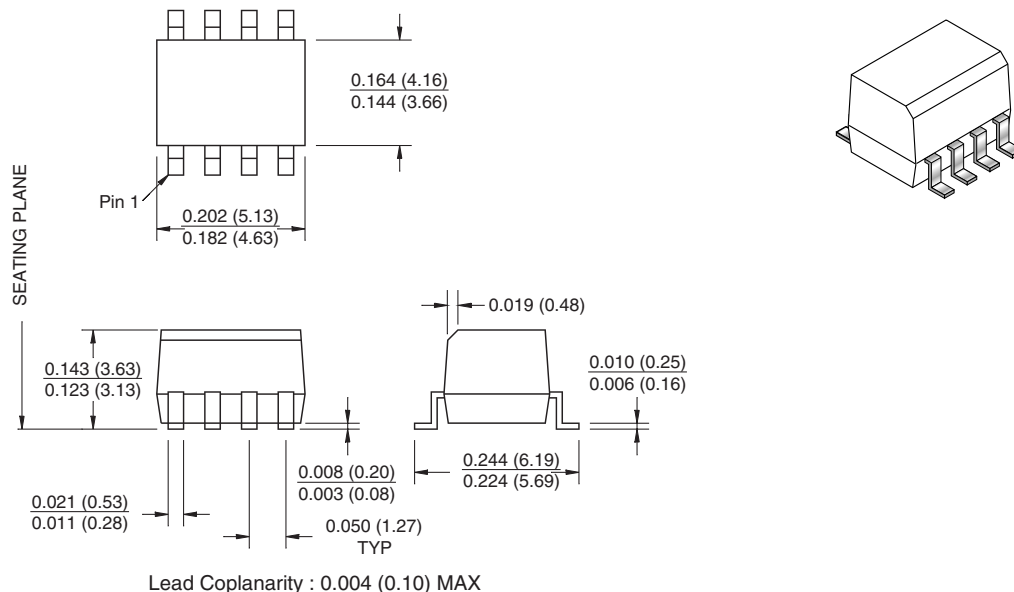
## Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

## Description

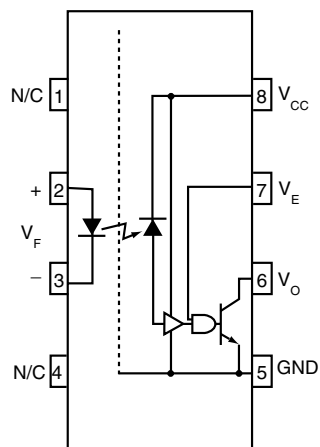
The HCPL06XX optocouplers consist of an AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate with a storable output (single channel devices). The devices are housed in a compact small-outline package. This output features an open collector, thereby permitting wired OR outputs. The HCPL0600, HCPL0601 and HCPL0611 output consists of bipolar transistors on a bipolar process while the HCPL0637, HCPL0638, and HCPL0639 output consists of bipolar transistors on a CMOS process for reduced power consumption. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. An internal noise shield provides superior common mode rejection.

## Package Dimensions

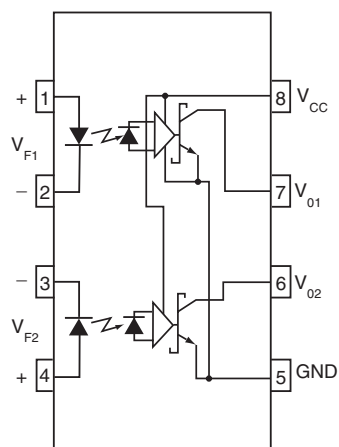


### Note:

All dimensions are in inches (millimeters)



Single-channel circuit drawing  
(HCPL0600, HCPL0601 and HCPL0611)



Dual-channel circuit drawing  
(HCPL0637, HCPL0638 and HCPL0639)

**TRUTH TABLE (Positive Logic)**

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H*	NC*	L*
L*	NC*	H*

\*Dual channel devices or single channel devices with pin 7 not connected.  
A 0.1 $\mu$ F bypass capacitor must be connected between pins 8 and 5. (See note 1)

**Absolute Maximum Ratings** (No derating required up to 85°C)

Symbol	Parameter		Value	Units
T <sub>STG</sub>	Storage Temperature		-40 to +125	°C
T <sub>OPR</sub>	Operating Temperature		-40 to +85	°C
<b>EMITTER</b>				
I <sub>F</sub>	DC/Average Forward Input Current (each channel)	Single Channel	50	mA
		Dual Channel		
V <sub>E</sub>	Enable Input Voltage Not to exceed V <sub>CC</sub> by more than 500mV	Single Channel	5.5	V
V <sub>R</sub>	Reverse Input Voltage (each channel)		5.0	V
P <sub>I</sub>	Power Dissipation	Single Channel	45	mW
		Dual Channel		
<b>DETECTOR</b>				
V <sub>CC</sub> (1 minute max)	Supply Voltage		7.0	V
I <sub>O</sub>	Output Current (each channel)	Single Channel	50	mA
		Dual Channel	15	
V <sub>O</sub>	Output Voltage (each channel)		7.0	V
P <sub>O</sub>	Collector Output Power Dissipation	Single Channel	85	mW
		Dual Channel	85	

**Recommended Operating Conditions**

Symbol	Parameter		Min.	Max.	Units
I <sub>FL</sub>	Input Current, Low Level		0	250	μA
I <sub>FH</sub>	Input Current, High Level		*6.3	15	mA
V <sub>CC</sub>	Supply Voltage, Output		4.5	5.5	V
V <sub>EL</sub>	Enable Voltage, Low Level	Single Channel only	0	0.8	V
V <sub>EH</sub>	Enable Voltage, High Level	Single Channel only	2.0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature		-40	+85	°C
N	Fan Out (TTL load)	Single Channel		8	TTL Loads
		Dual Channel		5	
R <sub>L</sub>	Output Pull-up		330	4K	Ω

\*6.3mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less

**Electrical Characteristics** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  Unless otherwise specified.)

**Individual Component Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.**	Max.	Unit
<b>EMITTER</b>						
$V_F$	Input Forward Voltage	$I_F = 10\text{mA}$ $T_A = 25^\circ\text{C}$			1.8	V
					1.75	
$B_{VR}$	Input Reverse Breakdown Voltage	$I_R = 10\mu\text{A}$	5.0			V
$\Delta V_F/\Delta T_A$	Input Diode Temperature Coefficient	$I_F = 10\text{mA}$		-1.5		mV/ $^\circ\text{C}$
<b>DETECTOR</b>						
$I_{CCH}$	High Level Supply Current	$I_F = 0\text{mA}$ , $V_{CC} = 5.5\text{V}$	$V_E = 0.5\text{V}$ Single Channel		10	mA
			Dual Channel		15	
$I_{CCL}$	Low Level Supply Current	$I_F = 10\text{mA}$ , $V_{CC} = 5.5\text{V}$	$V_E = 0.5\text{V}$ Single Channel		13	mA
			Dual Channel		21	
$I_{EL}$	Low Level Enable Current	$V_{CC} = 5.5\text{V}$ , $V_E = 0.5\text{V}$			-1.6	mA
$I_{EH}$	High Level Enable Current	$V_{CC} = 5.5\text{V}$ , $V_E = 2.0\text{V}$			-1.6	mA
$V_{EH}$	High Level Enable Voltage	$V_{CC} = 5.5\text{V}$ , $I_F = 10\text{mA}$	2.0			V
$V_{EL}$	Low Level Enable Voltage	$V_{CC} = 5.5\text{V}$ , $I_F = 10\text{mA}^{(2)}$			0.8	V

**Switching Characteristics** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $I_F = 7.5\text{mA}$  Unless otherwise specified.)

Symbol	AC Characteristics	Test Conditions	Device	Min.	Typ.	Max.	Unit
$T_{PLH}$	Propagation Delay Time to Output High Level	$R_L = 350\Omega$ , $C_L = 15\text{pF}^{(3)}$ (Fig. 20) $T_A = 25^\circ\text{C}$	All	20		75	ns
						100	
$T_{PHL}$	Propagation Delay Time to Output Low Level	$R_L = 350\Omega$ , $C_L = 15\text{pF}^{(4)}$ (Fig. 20) $T_A = 25^\circ\text{C}$	All	25		75	ns
						100	
$ T_{PHL} - T_{PLH} $	Pulse Width Distortion	$R_L = 350\Omega$ , $C_L = 15\text{pF}$ (Fig. 20)	All			35	ns
$t_r$	Output Rise Time (10-90%)	$R_L = 350\Omega$ , $C_L = 15\text{pF}^{(5)}$ (Fig. 20)	Single Ch		50		ns
			Dual Ch		17		
$t_f$	Output Fall Time (90-10%)	$R_L = 350\Omega$ , $C_L = 15\text{pF}^{(6)}$ (Fig. 20)	Single Ch		12		ns
			Dual Ch		5		
$t_{ELH}$	Enable Propagation Delay Time to Output High Level	$I_F = 7.5\text{mA}$ , $V_{EH} = 3.5\text{V}$ , $R_L = 350\Omega$ , $C_L = 15\text{pF}^{(7)}$ (Fig. 21)	HCPL0600 HCPL0601 HCPL0611		20		ns
$t_{EHL}$	Enable Propagation Delay Time to Output Low Level	$I_F = 7.5\text{mA}$ , $V_{EH} = 3.5\text{V}$ , $R_L = 350\Omega$ , $C_L = 15\text{pF}^{(8)}$ (Fig. 21)	HCPL0600 HCPL0601 HCPL0611		20		ns
$ICM_{ H }$	Common Mode Transient Immunity (at Output High Level)	$R_L = 350\Omega$ , $T_A = 25^\circ\text{C}$ , $I_F = 0\text{mA}$ , $V_{OH}(\text{Min.}) = 2.0\text{V}^{(9)}$ (Fig. 22, 23)	$ V_{CM}  = 10\text{V}$	HCPL0600 HCPL0637			V/ $\mu\text{s}$
			$ V_{CM}  = 50\text{V}$	HCPL0601 HCPL0638	5000		
			$ V_{CM}  = 1,000\text{V}$	HCPL0611	10,000		
				HCPL0639	25,000		
$ICM_{ L }$	Common Mode Transient Immunity (at Output Low Level)	$R_L = 350\Omega$ , $T_A = 25^\circ\text{C}$ , $I_F = 7.5\text{mA}$ , $V_{OL}(\text{Max.}) = 0.8\text{V}^{(10)}$ (Fig. 22, 23)	$ V_{CM}  = 10\text{V}$	HCPL0600 HCPL0637			V/ $\mu\text{s}$
			$ V_{CM}  = 50\text{V}$	HCPL0601 HCPL0638	5000		
			$ V_{CM}  = 1,000\text{V}$	HCPL0611	10,000		
				HCPL0639	25,000		

**Transfer Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  Unless otherwise specified.)

Symbol	DC Characteristics	Test Conditions	Min.	Typ.**	Max.	Unit
$I_{OH}$	High Level Output Current	$V_{CC} = 5.5\text{V}$ , $V_O = 5.5\text{V}$ , $I_F = 250\mu\text{A}$ , $V_E = 2.0\text{V}^{(2)}$			100	$\mu\text{A}$
$V_{OL}$	Low Level Output Voltage	$V_{CC} = 5.5\text{V}$ , $I_F = 5\text{mA}$ , $V_E = 2.0\text{V}$ , $I_{OL} = 13\text{mA}^{(2)}$			0.6	V
$I_{FT}$	Input Threshold Current	$V_{CC} = 5.5\text{V}$ , $V_O = 0.6\text{V}$ , $V_E = 2.0\text{V}$ , $I_{OL} = 13\text{mA}$			5	mA

**Isolation Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  Unless otherwise specified.)

Symbol	Characteristics	Test Conditions	Min.	Typ.**	Max.	Unit
$I_{I-O}$	Input-Output Insulation Leakage Current	Relative humidity = 45%, $T_A = 25^{\circ}\text{C}$ , $t = 5\text{s}$ , $V_{I-O} = 3000\text{VDC}^{(11)}$			1.0*	$\mu\text{A}$
$V_{ISO}$	Withstand Insulation Test Voltage	$R_H < 50\%$ , $T_A = 25^{\circ}\text{C}$ , $I_{I-O} \leq 2\mu\text{A}$ , $t = 1\text{min.}^{(11)}$	3750			$V_{RMS}$
$R_{I-O}$	Resistance (Input to Output)	$V_{I-O} = 500\text{V}^{(11)}$		$10^{12}$		$\Omega$
$C_{I-O}$	Capacitance (Input to Output)	$f = 1\text{MHz}^{(11)}$		0.6		pF

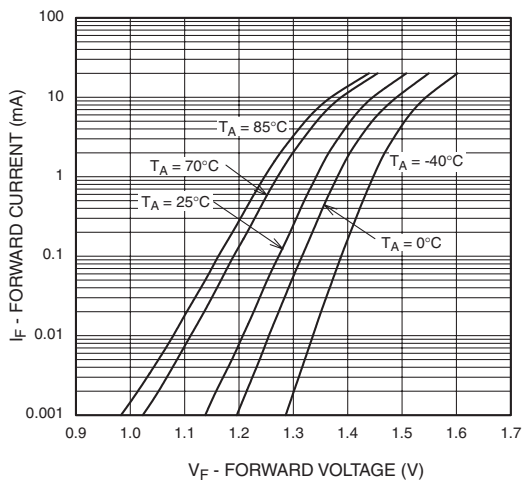
\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

**Notes:**

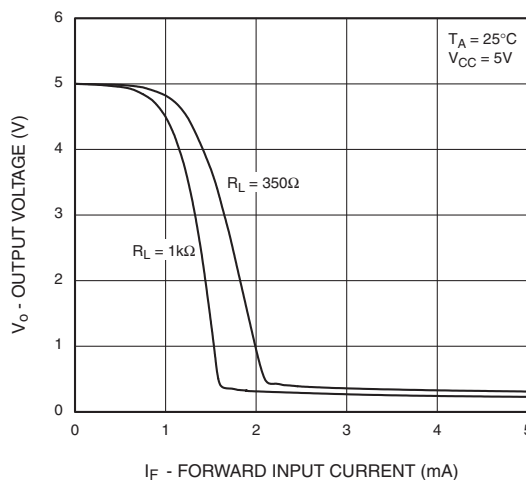
1. The  $V_{CC}$  supply to each optoisolator must be bypassed by a  $0.1\mu\text{F}$  capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package  $V_{CC}$  and GND pins of each device.
2. Enable Input – No pull up resistor required as the device has an internal pull up resistor.
3.  $t_{PLH}$  – Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
4.  $t_{PHL}$  – Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
5.  $t_r$  – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
6.  $t_f$  – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
7.  $t_{ELH}$  – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
8.  $t_{EHL}$  – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
9.  $CM_H$  – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e.,  $V_{OUT} > 2.0\text{V}$ ). Measured in volts per microsecond ( $\text{V}/\mu\text{s}$ ).
10.  $CM_L$  – The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e.,  $V_{OUT} < 0.8\text{V}$ ). Measured in volts per microsecond ( $\text{V}/\mu\text{s}$ ).
11. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.

## Typical Performance Curves (HCPL0600, HCPL0601 and HCPL0611 only)

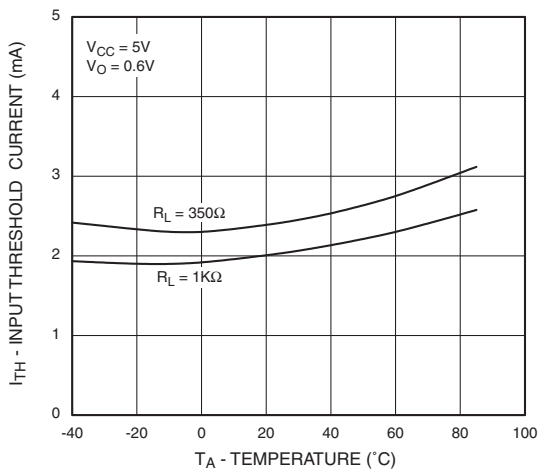
**Fig. 1 Forward Current vs. Input Forward Voltage**



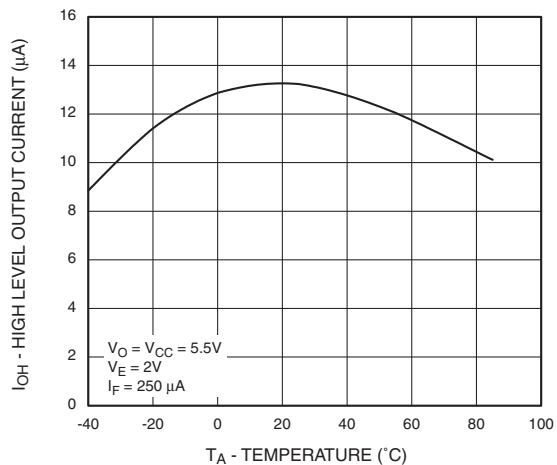
**Fig. 2 Output Voltage vs. Forward Current**



**Fig. 3 Input Threshold Current vs. Temperature**

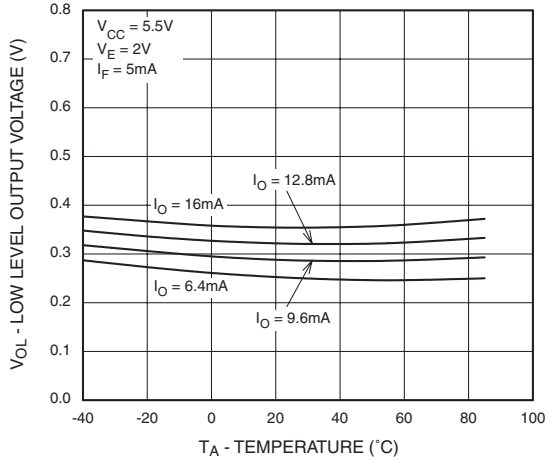


**Fig. 4 High Level Output Current vs. Temperature**

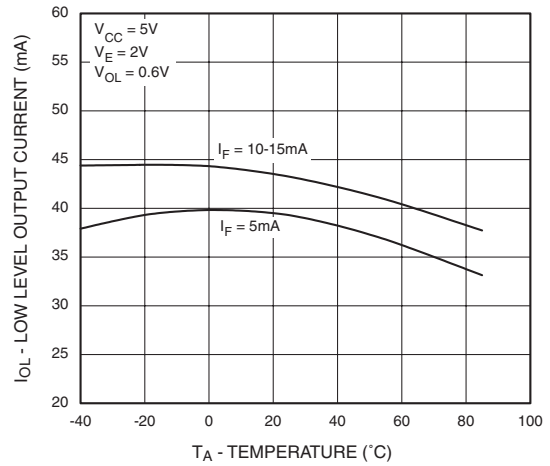


## Typical Performance Curves (HCPL0600, and HCPL0601 and HCPL0611 only)

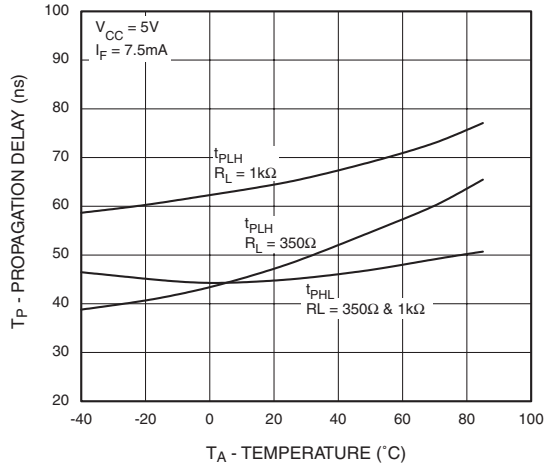
**Fig. 5 Low Level Output Voltage vs. Temperature**



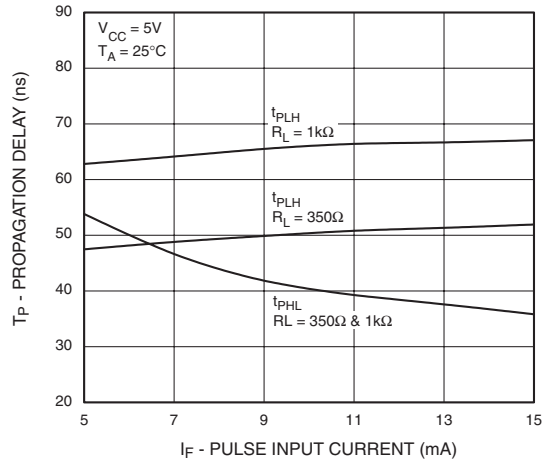
**Fig. 6 Low Level Output Current vs. Temperature**



**Fig. 7 Propagation Delay vs. Temperature**

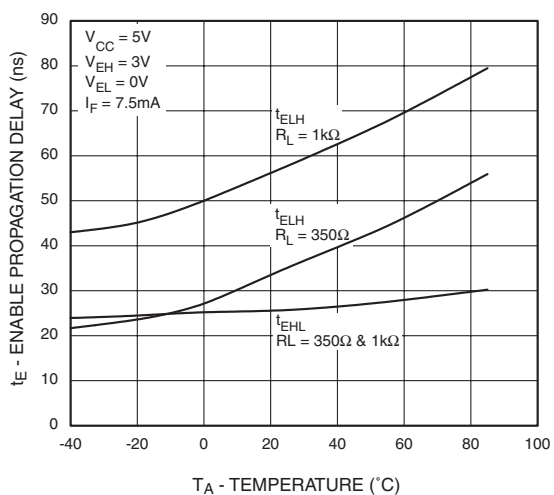


**Fig. 8 Propagation Delay vs. Pulse Input Current**

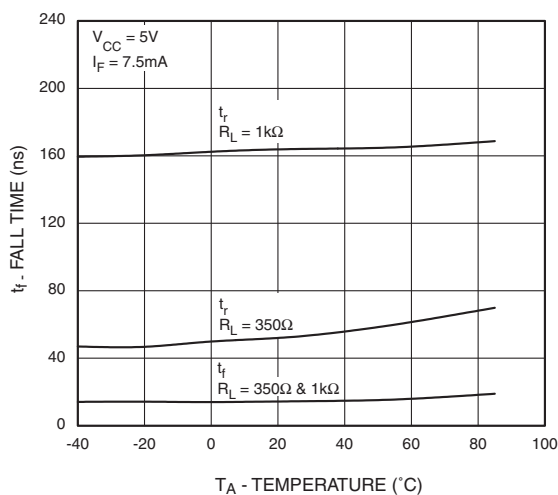


## Typical Performance Curves (HCPL0600, HCPL0601 and HCPL0611 only)

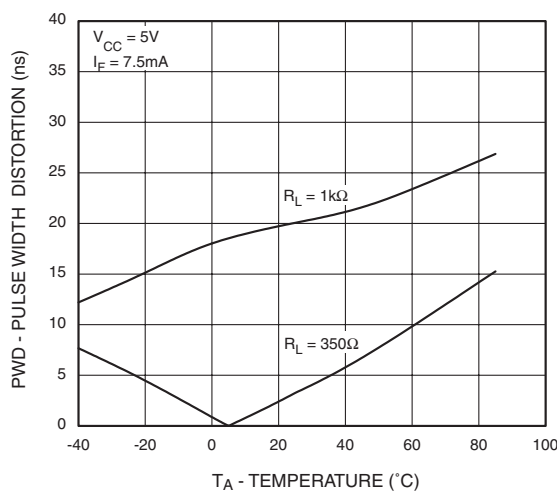
**Fig. 9 Typical Enable Propagation Delay vs. Temperature**



**Fig. 10 Typical Rise and Fall Time vs. Temperature**



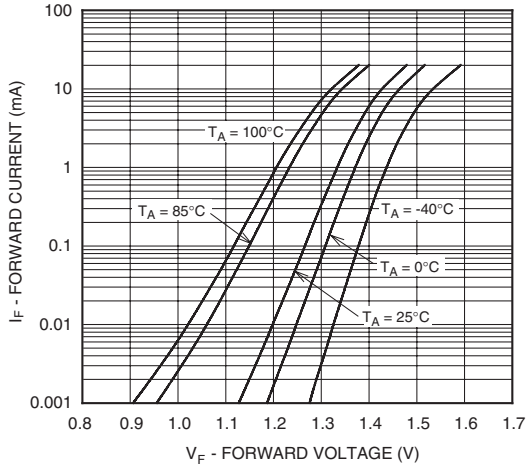
**Fig. 11 Typical Pulse Width Distortion vs. Temperature**



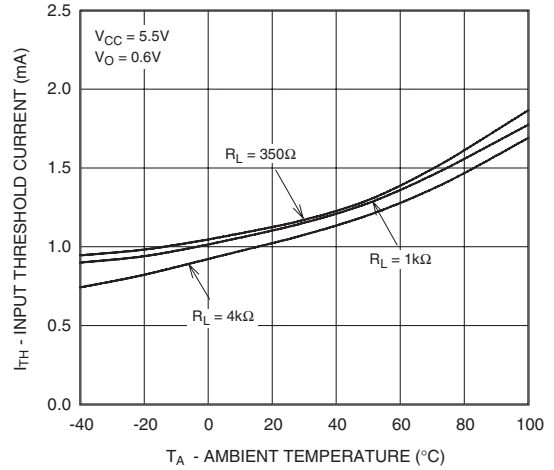


## Typical Performance Curves (HCPL0637, HCPL0638 and HCPL0639 only)

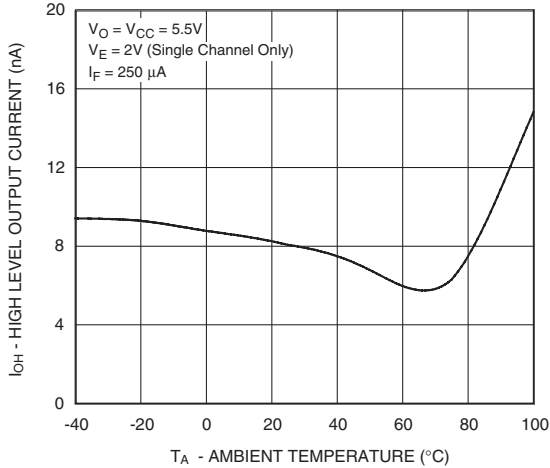
**Fig. 12 Input Forward Current vs. Forward Voltage**



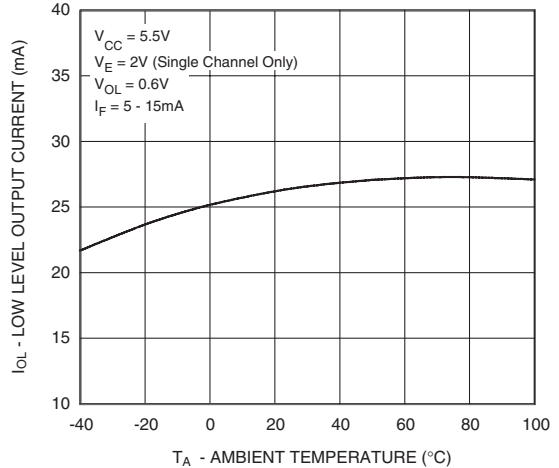
**Fig. 13 Input Threshold Current vs. Ambient Temperature**



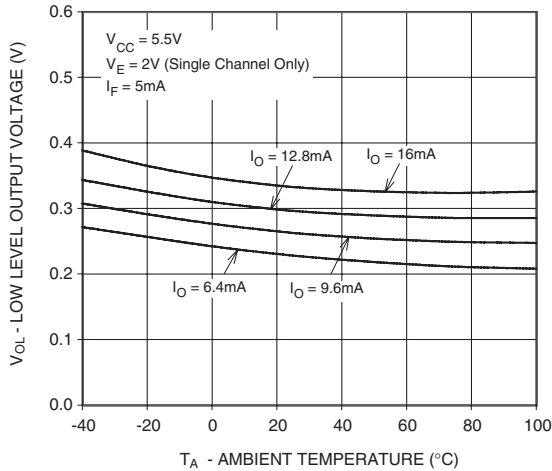
**Fig. 14 High Level Output Current vs. Ambient Temperature**



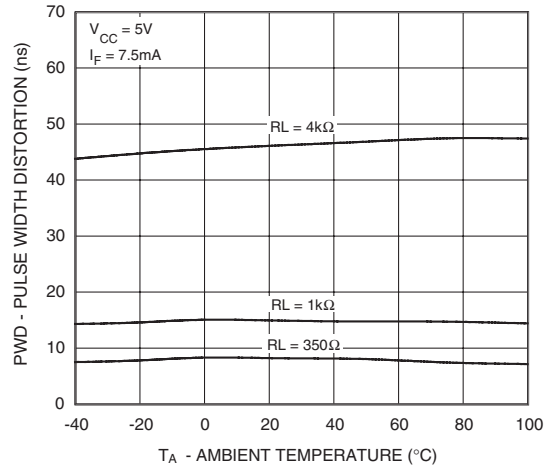
**Fig. 15 Low Level Output Current vs. Ambient Temperature**



**Fig. 16 Low Level Output Voltage vs. Ambient Temperature**

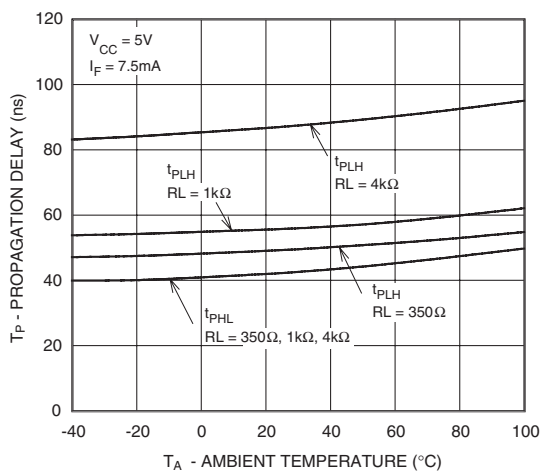


**Fig. 17 Pulse Width Distortion vs. Ambient Temperature**

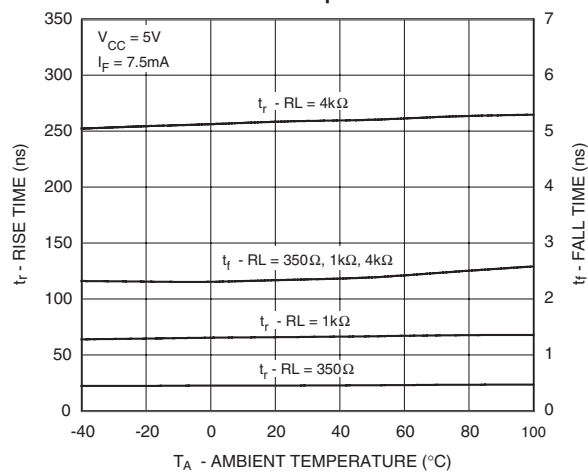


### Typical Performance Curves (HCPL0637, HCPL0638 and HCPL0639 only)

**Fig. 18 Propagation Delay vs. Ambient Temperature**



**Fig. 19 Rise and Fall Times vs. Ambient Temperature**



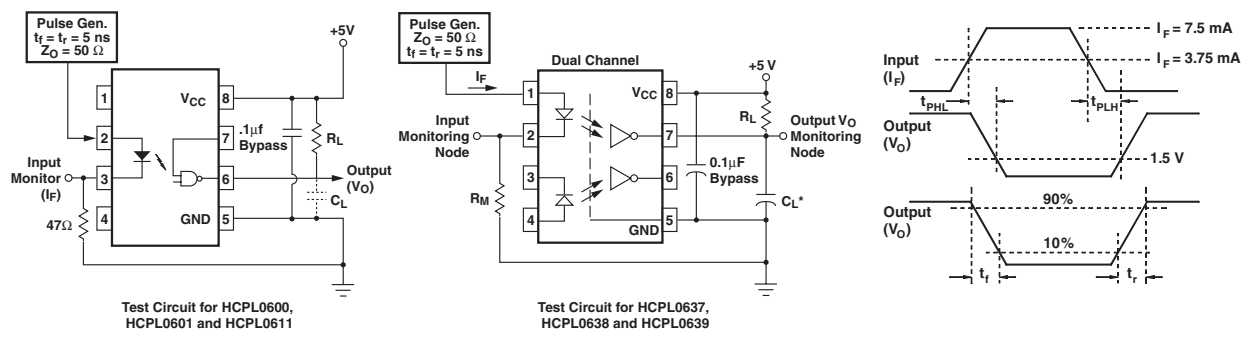


Fig. 20 Test Circuit and Waveforms for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$ .

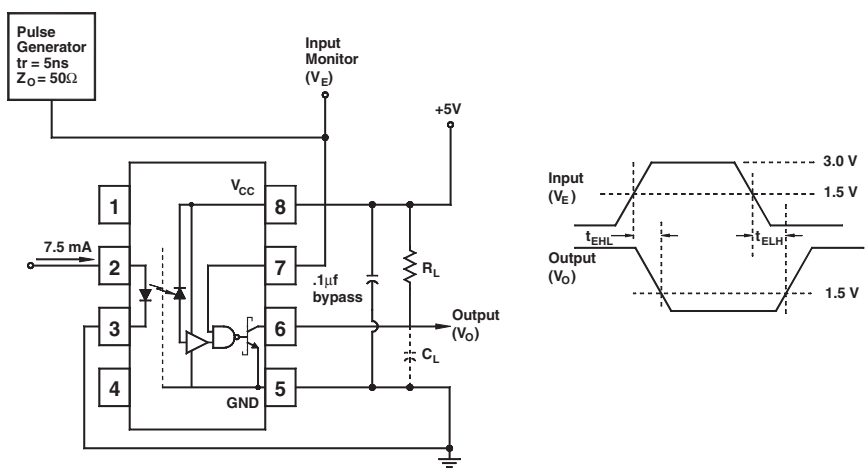
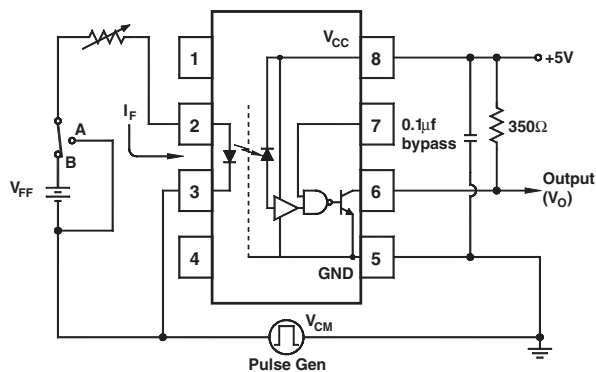


Fig. 21 Test Circuit  $t_{EHL}$  and  $t_{ELH}$ .



Test Circuit for HCPL0600, HCPL0601, and HCPL0611

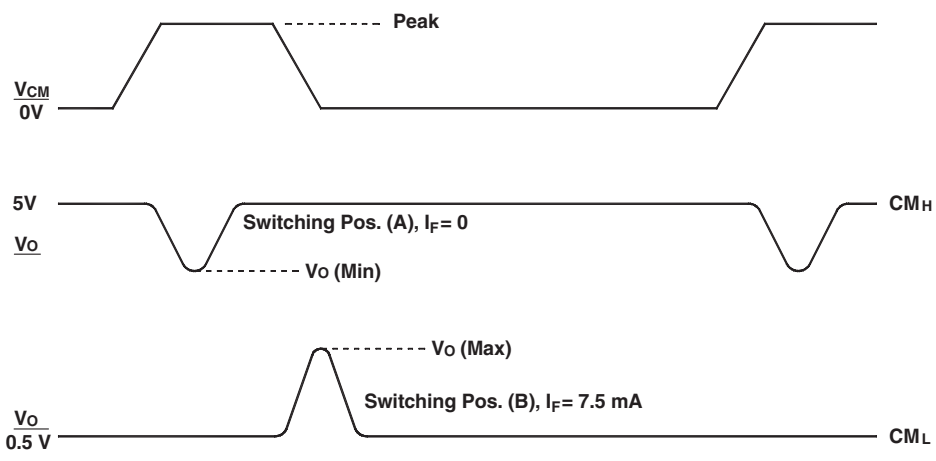
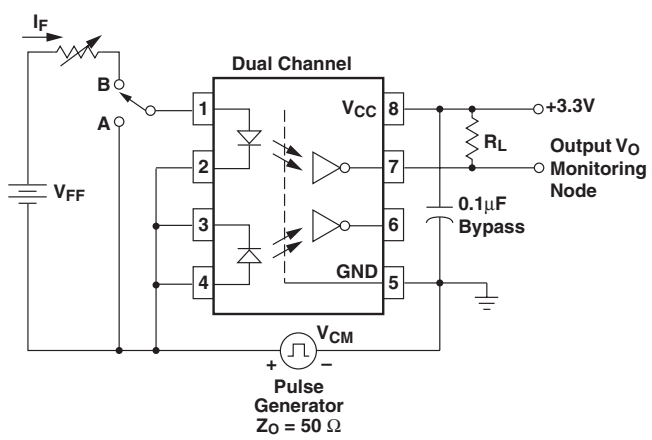


Fig. 22 Test Circuit Common Mode Transient Immunity (HCPL0600, HCPL0601 and HCPL0611)



Test Circuit for HCPL0637, HCPL0638 and HCPL0639

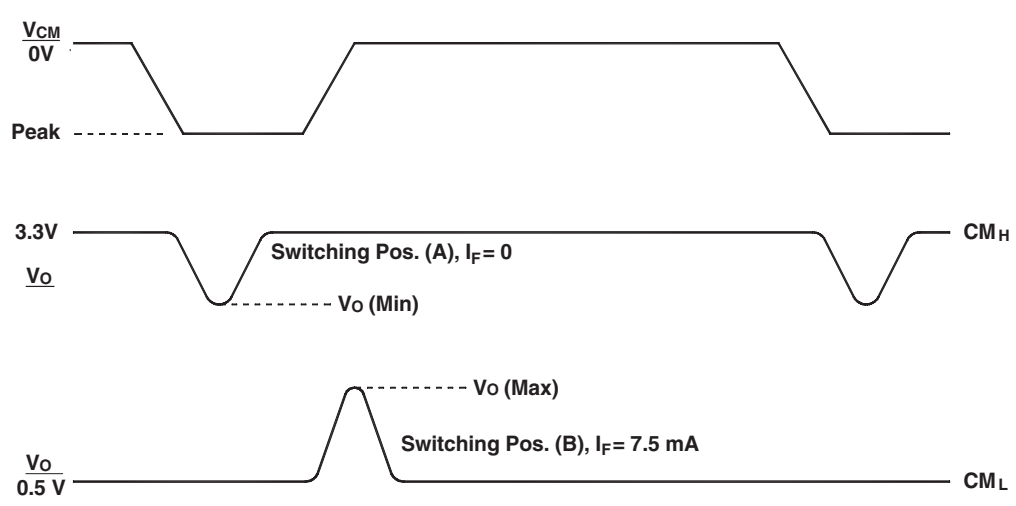
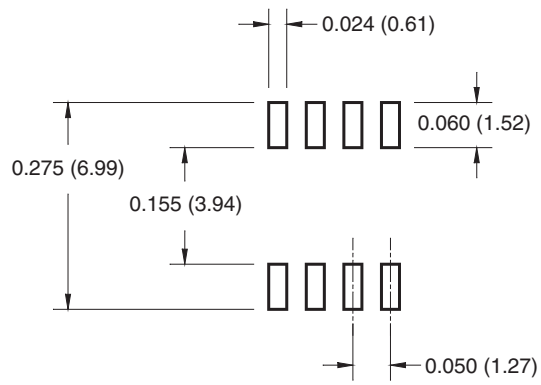


Fig. 23 Test Circuit Common Mode Transient Immunity (HCPL0637, HCPL0638 and HCPL0639)

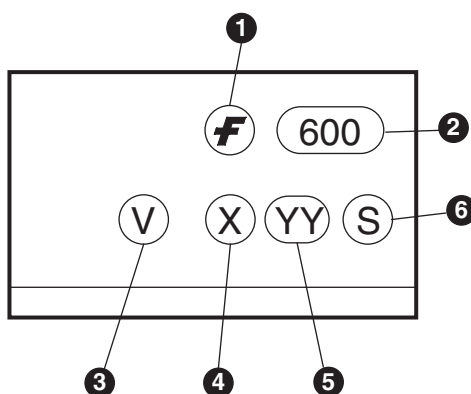
### 8-Pin Small Outline



### Ordering Information

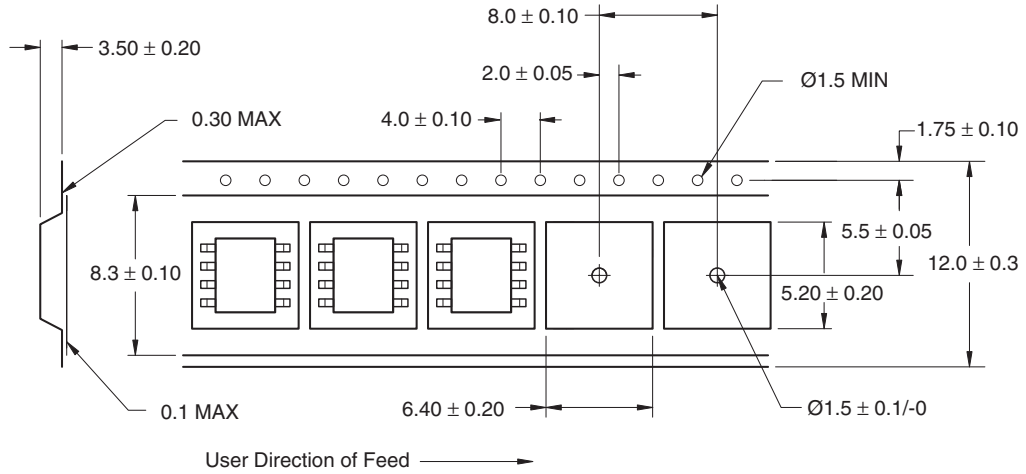
Option	Order Entry Identifier	Description
No Suffix	HCPL0600	Shipped in tubes (50 units per tube)
V	HCPL0600V	VDE0884 (pending approval)
R1	HCPL0600R1	Tape and Reel (500 units per reel)
R1V	HCPL0600R1V	VDE0884 (pending approval), Tape and Reel (500 units per reel)
R2	HCPL0600R2	Tape and Reel (2500 units per reel)
R2V	HCPL0600R2V	VDE0884 (pending approval), Tape and Reel (2500 units per reel)

### Marking Information

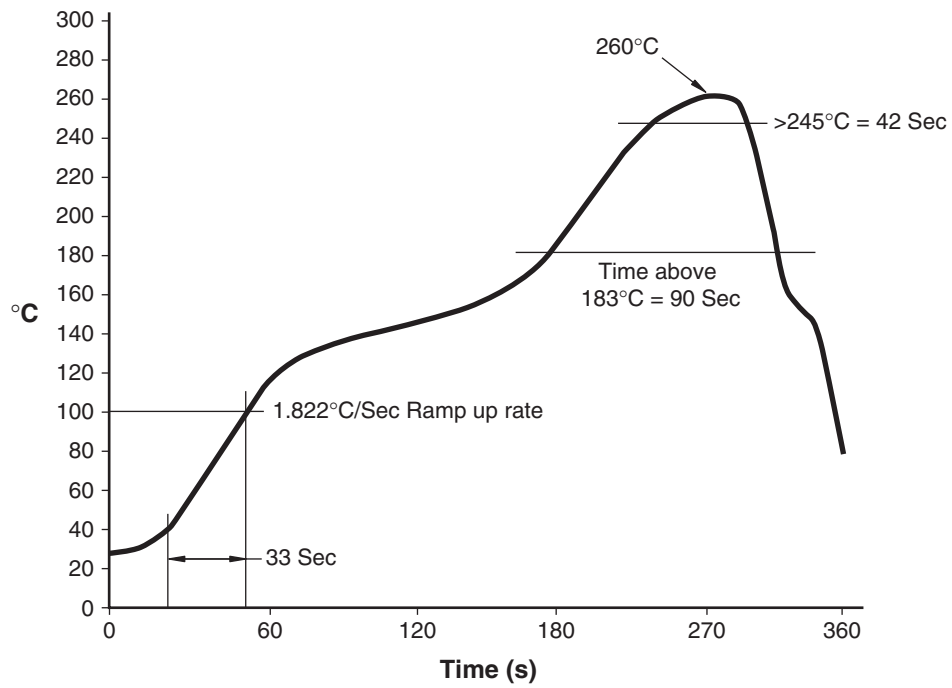


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

### Carrier Tape Specifications



### Reflow Profile





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Bottomless™	GTO™	OPTOLOGIC®	SPM™	Wire™
Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	
CoolFET™	I <sup>2</sup> C™	PACMAN™	SuperFET™	
CROSSVOLT™	i-Lo™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E <sup>2</sup> CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT®	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FAST <sub>r</sub> ™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPST™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		μSerDes™	TruTranslation™	
The Power Franchise®		ScalarPump™	UHC®	
Programmable Active Droop™				

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### PRODUCT STATUS DEFINITIONS

#### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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