CE6353

Nordig Unified DVB-T COFDM Terrestrial Demodulator for PC-TV and Hand-held Digital TV (DTV)

Data Sheet

Features

February 2006

- Compliant with ETSI 300 744 DVB-T, Unified Nordig and DTG performance specifications
- High performance with fast fully blind acquisition and tracking capability
- Low power consumption: less than 0.32 W, and eco-friendly standby and sleep modes
- Digital filtering of adjacent channels
- Single 8 MHz SAW filter for 6, 7 & 8 MHz OFDM
- Superior single frequency network performance
- Fast AGC to track out signal fades
- Good Doppler tracking capability
- Enhanced frequency capture range to include triple offsets
- External 4 MHz clock or single low-cost 20.48 MHz crystal, tolerance up to +/-200 ppm
- Automatic mode (2 K/8 K), guard and spectral inversion detection
- Very low driver software overhead due to on-chip state-machine control
- Novel RF level detect facility via a separate ADC
- Pre and post Viterbi-decoder bit error rates, and uncorrectable block count

Ordering Information

DJCE6353 882077	64 Pin LQFP	Trays
WJCE6353 882206	64 Pin LQFP*	Trays
DJCE6353 S L9EN 882128	64 Pin LQFP	Tape and Reel
WJCE6353 S L9G5 882170	64 Pin LQFP*	Tape and Reel

*Pb Free Matte Tin

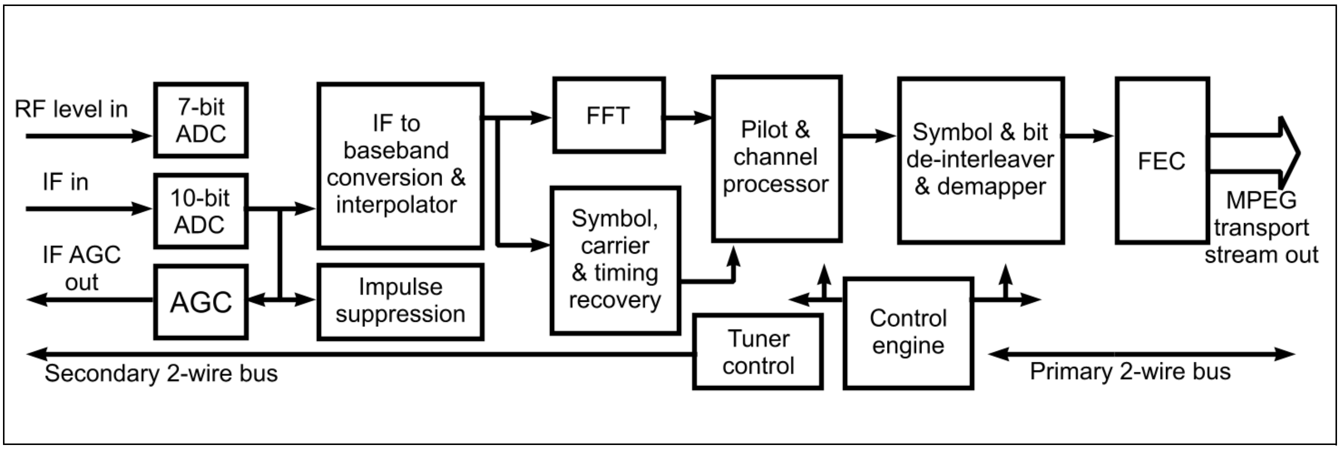

Figure 1 - Block Diagram

Applications

- Digital terrestrial set-top boxes
- Integrated digital televisions
- Personal video recorders
- PC-TV receivers
- Portable applications

Description

The CE6353 is a superior fourth generation fully compliant ETSI ETS300 744 COFDM demodulator that exceeds, with margin, the performance requirements of all known DVB-T digital terrestrial television standards, including Unified Nordig and DTG.

A high performance 10 bit on-chip ADC is used to sample the 44 or 36 MHz IF analog signal. Advanced digital filtering of the upper and lower channel enables a single 8 MHz channel SAW filter to be used for 6, 7 and 8 MHz OFDM signal reception. All sampling and other internal clocks are derived from a single 20.48 MHz crystal or a 4 MHz clock input, the tolerance of which may be relaxed as much as 200 ppm.

The CE6353 has a wide frequency capture range able to automatically compensate for the combined offset introduced by the tuner xtal and broadcaster triple frequency offsets.

An on-chip state machine controls all acquisition and tracking operations of the CE6353 as well as controlling the tuner via a 2-wire bus. Any frequency range can be automatically scanned for digital TV channels. This mechanism ensures minimal interaction, maximum flexibility and fast acquisition - very low software overhead.

Also included in the design is a 7-bit ADC to detect the RF signal strength and thereby efficiently control the tuner RF AGC.

Users have access to all the relevant signal quality information, including input signal power level, signal-to-noise ratio, pre-Viterbi BER, post-Viterbi BER, and the uncorrectable block counts. The error rate monitoring periods are programmable over a wide range.

The device is packaged in a 10 x 10 mm 64-pin LQFP and is very low power.

Table of Contents

List of Figures

List of Tables

1.0 Pin & Package Details

1.1 Pin Outline

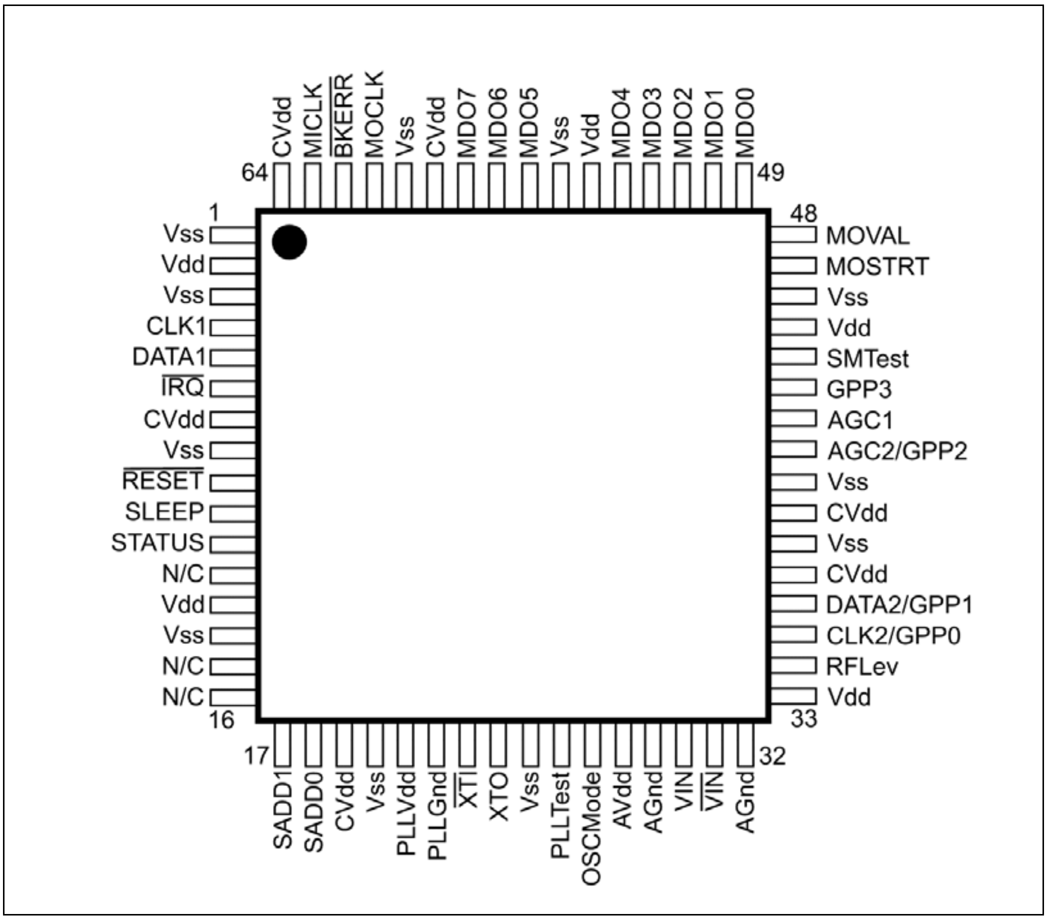

Figure 2 - Pin Outline

1.2 Pin Allocation

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Vss	17	SADD1	33	Vdd	49	MDO0
2	Vdd	18	SADD0	34	RFLEV	50	MDO1
3	Vss	19	CVdd	35	CLK2/GPP0	51	MDO2
4	CLK1	20	Vss	36	DATA2/GPP1	52	MDO3
5	DATA1	21	PLLVdd	37	CVdd	53	MDO4
6	$\overline{\text{IRQ}}$	22	PLLGND	38	Vss	54	Vdd
7	CVdd	23	$\overline{\text{XTI}}$	39	CVdd	55	Vss
8	Vss	24	XTO	40	Vss	56	MDO5
9	$\overline{\text{RESET}}$	25	Vss	41	AGC2/GPP2	57	MDO6
10	SLEEP	26	PLLTEST	42	AGC1	58	MDO7
11	STATUS	27	OSCMODE	43	GPP3	59	CVdd
12		28	AVdd	44	SMTEST	60	Vss
13	Vdd	29	AGnd	45	Vdd	61	MOCLK
14	Vss	30	VIN	46	Vss	62	$\overline{\text{BKERR}}$
15		31	$\overline{\text{VIN}}$	47	MOSTRT	63	MICLK
16		32	AGnd	48	MOVAL	64	CVdd

Table 1 - Pin Names - numeric

Function	Pin	Function	Pin	Function	Pin	Function	Pin
AGC1	42	GPP3	43	PLLTEST	26	Vdd	54
AGC2/GPP2	41	$\overline{\text{IRQ}}$	6	PLLVdd	21	VIN	30
AGnd	29	MDO0	49	$\overline{\text{RESET}}$	9	$\overline{\text{VIN}}$	31
AGnd	32	MDO1	50	RFLEV	34	Vss	1
AVdd	28	MDO2	51	SADD0	18	Vss	3
$\overline{\text{BKERR}}$	62	MDO3	52	SADD1	17	Vss	8
CLK1	4	MDO4	53	N/C	16	Vss	14
CLK2/GPP0	35	MDO5	56	N/C	15	Vss	20
CVdd	7	MDO6	57	N/C	12	Vss	25
CVdd	19	MDO7	58	SLEEP	10	Vss	38
CVdd	37	MICLK	63	SMTEST	44	Vss	40
CVdd	39	MOCLK	61	STATUS	11	Vss	46

Table 2 - Pin Names - alphabetical order

CVdd	59	MOSTRT	47	Vdd	2	Vss	55
CVdd	64	MOVAL	48	Vdd	13	Vss	60
DATA1	5	OSCMODE	27	Vdd	33	$\overline{\text{XTI}}$	23
DATA2/GPP1	36	PLLGND	22	Vdd	45	XTO	24

Table 2 - Pin Names - alphabetical order (continued)

1.3 Pin Description

Pin Description Table

Pin No	Name	Pin Description	I/O	Type	V	mA
MPEG pins						
47	MOSTRT	MPEG packet start	O	CMOS Tristate	3.3	1
48	MOVAL	MPEG data valid	O		3.3	1
49-53, 56-58	MDO(0:4)/MDO(5:7)	MPEG data bus	O		3.3	1
61	MOCLK	MPEG clock out	O		3.3	1
62	$\overline{\text{BKERR}}$	Block error	O		3.3	1
63	MICLK	MPEG clock in	I	CMOS	3.3	
11	STATUS	Status output	O		3.3	1
6	$\overline{\text{IRQ}}$	Interrupt output	O	Open drain	5	6
Control pins						
4	CLK1	Serial clock	I	CMOS	5	
5	DATA1	Serial data	I/O	Open drain	5	6
23	$\overline{\text{XTI}}$	Low phase noise oscillator	I	CMOS		
24	XTO		O			
10	SLEEP	Device power down	I		3.3	
12, 15-18	SADD(4:0)	Serial address set	I		3.3	
44	SMTEST	Production test (only set low)	I		3.3	
35	CLK2/GPP0	Serial clock tuner	I/O	Open drain	5	6
36	DATA2/GPP1	Serial data tuner	I/O		5	6
42	AGC1	Primary AGC	O		5	6
41	AGC2/GPP2	Secondary AGC	I/O		5	6
43	GPP(3)	General purpose I/O	I/O		5	6
9	$\overline{\text{RESET}}$	Device reset	I	CMOS	5	
27	OSCMODE	Crystal oscillator mode	I	CMOS	3.3	
26	PLLTEST	PLL analog test	O	(tristated)		

Pin Description Table (continued)

Pin No	Name	Pin Description	I/O	Type	V	mA
Analog inputs						
30	VIN	positive input	I			
31	$\overline{\text{VIN}}$	negative input	I			
34	RFLEV	RF level	I			
Supply pins						
21	PLLVdd	PLL supply	S		1.8	
22	PLLGnd		S		0	
7, 19, 37, 39, 59, 64	CVdd	Core logic power	S		1.8	
2, 13, 45, 54,	Vdd	I/O ring power	S		3.3	
1, 3, 8, 14, 20, 25, 38, 40, 46, 55, 60	Vss	Core and I/O ground	S		0	
28	AVdd	ADC analog supply	S		1.8	
29, 32	AGnd		S		0	
33	Vdd	2nd ADC supply	S		3.3	

2.0 Functional Description

A functional block diagram of the CE6353 OFDM demodulator is shown in Figure 3. This accepts an IF analog signal and delivers a stream of demodulated soft decision data to the on-chip Viterbi decoder. Clock, timing and frequency synchronization operations are all digital and there are no analog control loops except the AGC. The frequency capture range is large enough for all practical applications. This demodulator has novel algorithms to combat impulse noise as well as co-channel and adjacent channel interference. If the modulation is hierarchical, the OFDM outputs both high and low priority data streams. Only one of these streams is FEC-decoded, but the FEC can be switched from one stream to another with minimal interruption to the transport stream.

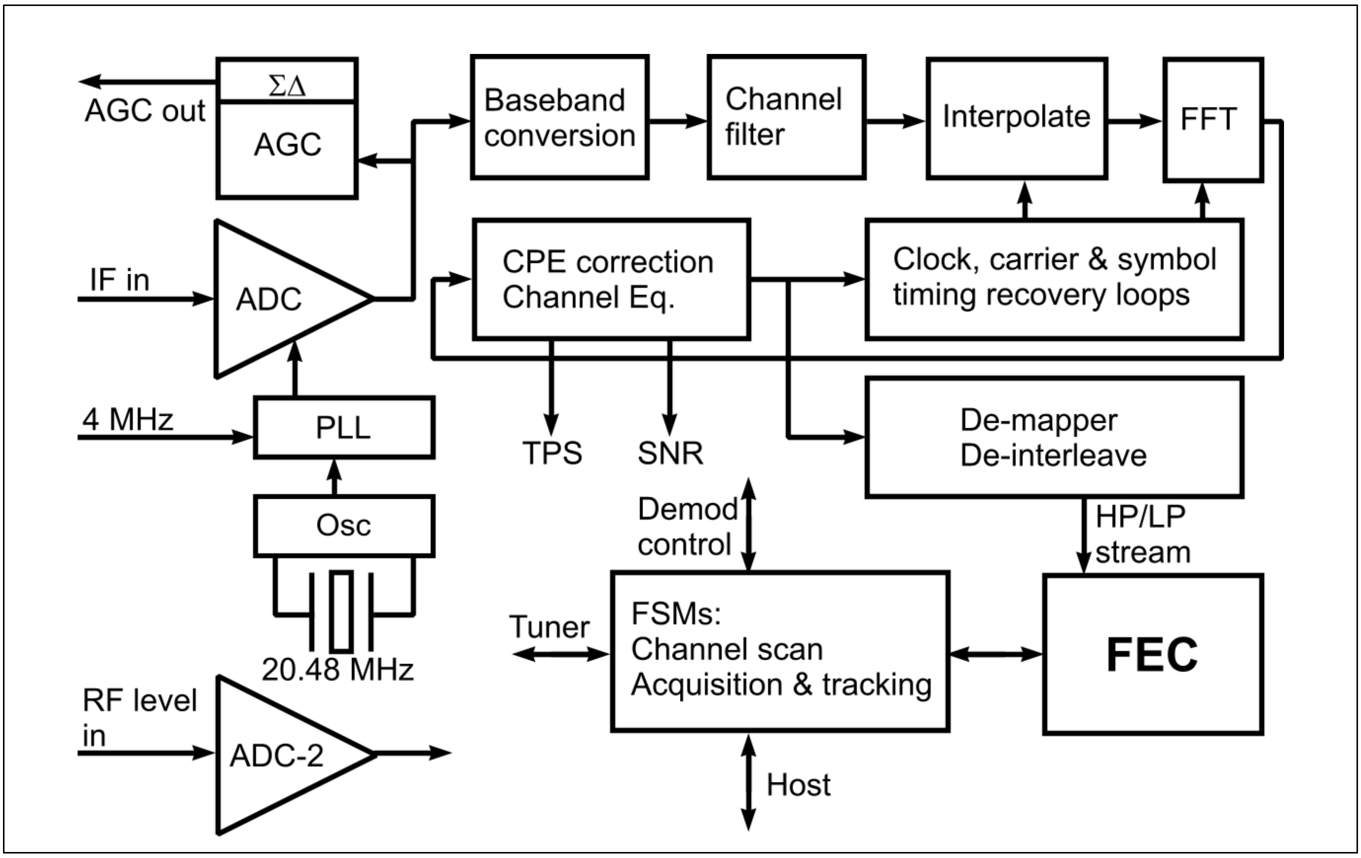

Figure 3 - OFDM Demodulator Diagram

The FEC module shown in Figure 4 consists of a concatenated convolutional (Viterbi) and Reed-Solomon decoder separated by a depth-12 convolutional de-interleaver. The Viterbi decoder operates on 5-bit soft decisions to provide the best performance over a wide range of channel conditions. The trace-back depth of 128 ensures minimum loss of performance due to inevitable survivor truncation, especially at high code rates. Both the Viterbi and Reed-Solomon decoders are equipped with bit-error monitors. The former provides the bit error rate (BER) at the OFDM output. The latter is the more useful measure as it gives the Viterbi output BER. The error collecting intervals of these are programmable over a very wide range.

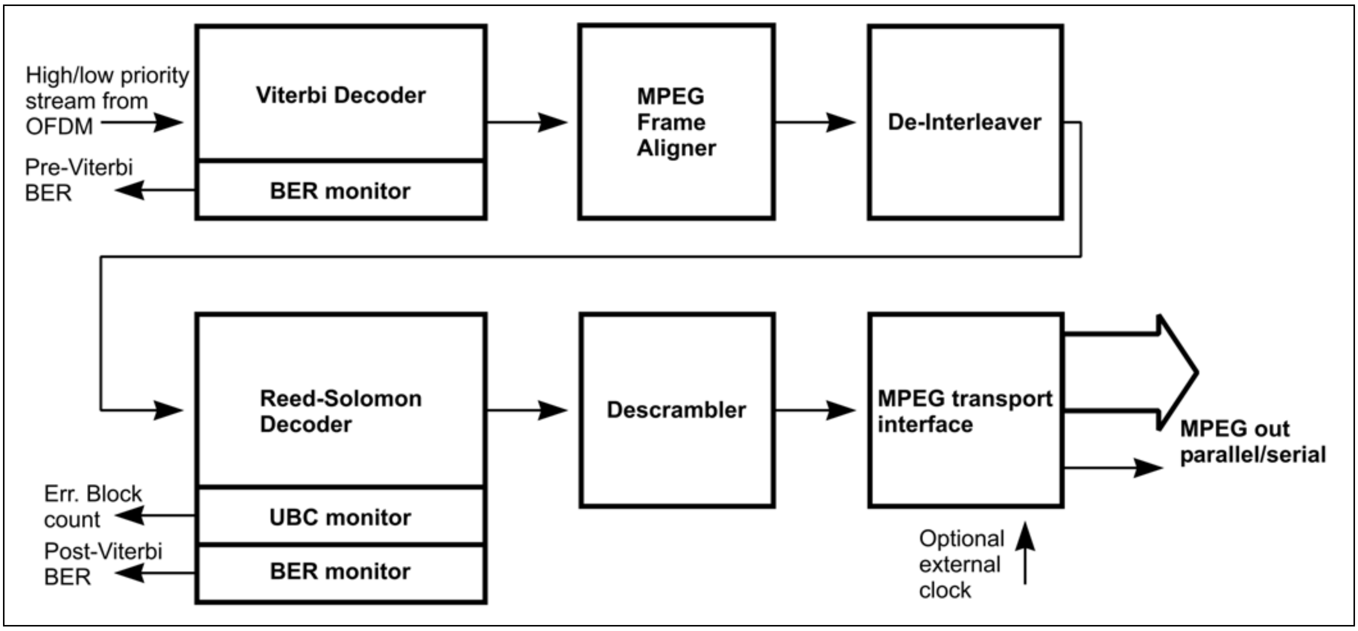

Figure 4 - FEC Block Diagram

The FSM controller shown in Figure 3 controls both the demodulator and the FEC. It also drives the 2-wire bus to the tuner. The controller facilitates the automated search of all parameters or any sub-set of parameters of the received signal. It can also be used to scan any defined frequency range searching for OFDM channels. This mechanism provides the fast channel scan and acquisition performance, whilst requiring minimal software overhead in the host driver.

The algorithms and architectures used in the CE6353 have been optimized to minimize power consumption.

2.1 Analog-to-Digital Converter

The CE6353 has a high performance 10-bit analog-to-digital converter (ADC) which can sample a 6, 7 or 8 MHz bandwidth OFDM signal, with its spectrum centred at:

- 36.17 MHz IF
- 43.75 MHz IF
- 5 - 10 MHz near-zero IF

An on-chip programmable phase locked loop (PLL) is used to generate the ADC sampling clock. The PLL is highly programmable allowing a wide choice of sampling frequencies to suit any IF frequency, and all signal bandwidths.

2.2 Automatic Gain Control

An AGC module compares the absolute value of the digitized signal with a programmable reference. The error signal is filtered and is used to control the gain of the amplifier. A sigma-delta modulated output is provided, which has to be RC low-pass filtered to obtain the voltage to control the amplifier.

The programmable AGC reference has been optimized. A large value for the reference leads to excessive ADC clipping and a small value results in excessive quantization noise. Hence the optimum value has been determined assuming the input signal amplitude to be Gaussian distributed. The latter is justified by applying the central limit theorem in statistics to the OFDM signal, which consists of a large number of randomly modulated carriers. This reference or target value may have to be lowered slightly for some applications. Slope control bits have been provided for the AGCs and these have to be set correctly depending on the gain-versus-voltage slope of the gain control amplifiers.

The bandwidth of the AGC is set to a large value for quick acquisition then reduced to a small value for tracking. The AGC is free running during OFDM channel changes and locks to the new channel while the tuner lock is being established. This is one of the features of CE6353 used to minimize acquisition time. A robust AGC lock mechanism is provided and the other parts of the CE6353 begin to acquire only after the AGC has locked.

2.3 IF to Baseband Conversion

Sampling a 36.17 MHz IF signal at 45 MHz results in a spectrally inverted OFDM signal centred at approximately 8.9 MHz. The first step of the demodulation process is to convert this signal to a complex (in-phase and quadrature) signal in baseband. A correction for spectral inversion is implemented during this conversion process. Note also that the CE6353 has control mechanisms to search automatically for an unknown spectral inversion status.

2.4 Adjacent Channel Filtering

Adjacent channels, in particular the Nicam digital sound signal associated with analog channels, are filtered prior to the FFT.

2.5 Interpolation and Clock Synchronization

CE6353 uses digital timing recovery and this eliminates the need for an external VCXO. The ADC samples the signal at a fixed rate, for example, 45.056 MHz. Conversion of the 45.056 MHz signal to the OFDM sample rate is achieved using the time-varying interpolator. The OFDM sample rate is 64/7 MHz for 8 MHz and this is scaled by factors 6/8 and 7/8 for 6 and 7 MHz channel bandwidths. The nominal ratio of the ADC to OFDM sample rate is programmed in a CE6353 register (defaults are for 45 MHz sampling and 8 MHz OFDM). The clock recovery phase locked loop in the CE6353 compensates for inaccuracies in this ratio due to uncertainties of the frequency of the sampling clock.

2.6 Carrier Frequency Synchronization

There can be frequency offsets in the signal at the input to OFDM, partly due to tuner step size and partly due to broadcast frequency shifts, typically 1/6 MHz. These are tracked out digitally, up to 1 MHz in 2 K and 8 K modes, without the need for an analog frequency control (AFC) loop.

The default frequency capture range has been set to ±286 kHz in the 2 K and 8 K mode. However, these values can be increased, if necessary, by programming an on-chip register (see 7.4.1). It is recommended that a larger capture range be used for channel scan in order to find channels with broadcast frequency shifts, without having to adjust the tuner. After the OFDM module has locked (the AFC will have been previously disabled), the frequency offset can be read from an on-chip register.

2.7 Symbol Timing Synchronization

This module computes the optimum sample position to trigger the FFT in order to eliminate or minimize inter-symbol interference in the presence of multi-path distortion. Furthermore, this trigger point is continuously updated to dynamically adapt to time-variations in the transmission channel.

2.8 Fast Fourier Transform

The FFT module uses the trigger information from the timing synchronization module to set the start point for an FFT. It then uses either a 2 K or 8 K FFT to transform the data from the time domain to the frequency domain. An extremely hardware-efficient and highly accurate algorithm has been used for this purpose.

2.9 Common Phase Error Correction

This module subtracts the common phase offset from all the carriers of the OFDM signal to minimize the effect of the tuner phase noise on system performance.

2.10 Channel Equalization

This consists of two parts. The first part involves estimating the channel frequency response from pilot information. Efficient algorithms have been used to track time-varying channels with a minimum of hardware.

The second part involves applying a correction to the data carriers based on the estimated frequency response of the channel. This module also generates dynamic channel state information (CSI) for every carrier in every symbol.

2.11 Impulse Filtering

CE6353 contains several mechanisms to reduce the impact of impulse noise on system performance.

2.12 Transmission Parameter Signalling (TPS)

An OFDM frame consists of 68 symbols and a superframe is made up of four such frames. There is a set of TPS carriers in every symbol and all these carry one bit of TPS. These bits, when combined, include information about the transmission mode, guard ratio, constellation, hierarchy and code rate, as defined in ETS 300 744. In addition, the first eight bits of the cell identifier are contained in even frames and the second eight bits of the cell identifier are in odd frames. The TPS module extracts all the TPS data, and presents these to the host processor in a structured manner.

2.13 De-Mapper

This module generates soft decisions for demodulated bits using the channel-equalized in-phase and quadrature components of the data carriers as well as per-carrier channel state information (CSI). The de-mapping algorithm depends on the constellation (QPSK, 16QAM or 64QAM) and the hierarchy (α = 0, 1, 2 or 4). Soft decisions for both low- and high-priority data streams are generated.

2.14 Symbol and Bit De-Interleaving

The OFDM transmitter interleaves the bits within each carrier and also the carriers within each symbol. The de-interleaver modules consist largely of memory to invert these interleaving functions and present the soft decisions to the FEC in the original order.

2.15 Viterbi Decoder

The Viterbi decoder accepts the soft decision data from the OFDM demodulator and outputs a decoded bit-stream. The decoder does the de-puncturing of the input data for all code rates other than 1/2. It then evaluates the branch metrics and passes these to a 64-state path-metric updating unit, which in turn outputs a 64-bit word to the survivor memory. The Viterbi decoded bits are obtained by tracing back the survivor paths in this memory. A trace-back depth of 128 is used to minimize any loss in performance, especially at high code rates.

The decoder re-encodes the decoded bits and compares these with received data (delayed) to compute bit errors at its input, on the assumption that the Viterbi output BER is significantly lower than its input BER.

2.16 MPEG Frame Aligner

The Viterbi decoded bit stream is aligned into 204-byte frames. A robust synchronization algorithm is used to ensure correct lock and to prevent loss of lock due to noise impulses.

2.17 De-interleaver

Errors at the Viterbi output occur in bursts and the function of the de-interleaver is to spread these errors over a number of 204-byte frames to give the Reed-Solomon decoder a better chance of correcting these. The de-interleaver is a memory unit which implements the inverse of the convolutional interleaving function introduced by the transmitter.

2.18 Reed-Solomon Decoder

Every 188-byte transport packet is encoded by the transmitter into a 204-byte frame, using a truncated version of a systematic (255,239) Reed-Solomon code. The corresponding (204,188) Reed-Solomon decoder is capable of correcting up to eight byte errors in a 204-byte frame. It may also detect frames with more than eight byte errors.

In addition to efficiently performing this decoding function, the Reed-Solomon decoder in CE6353 keeps a count of the number of bit errors corrected over a programmable period and the number of uncorrectable blocks. This information can be used to compute the post-Viterbi BER.

2.19 De-scrambler

The de-scrambler de-randomizes the Reed-Solomon decoded data by generating the exclusive-OR of this with a pseudo-random bit sequence (PRBS). This outputs 188-byte MPEG transport packets. The TEI bit of the packet header may be set if required to indicate uncorrectable packets.

2.20 MPEG Transport Interface

MPEG data can be output in parallel or serial mode. The output clock frequency is automatically chosen to present the MPEG data as uniformly spaced as possible to the transport processor. This frequency depends on the guard ratio, constellation, hierarchy and code rate. There is also an option for the data to be extracted from the CE6353 with a clock provided by the user.

3.0 Interfaces

3.1 2-Wire Bus

3.1.1 Host

The primary 2-wire bus serial interface uses pins:

- DATA1 (pin 5) serial data, the most significant bit is sent first.
- CLK1 (pin 4) serial clock.

The 2-wire bus address is determined by applying VDD or VSS to the SADD[4:0] pins.

In TNIM evaluation applications, the 2-wire bus address is 0001 111 R/$\overline{W}$ with the pins connected as follows:

ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]
Not programmable					SADD[1]	SADD[0]
VSS	VSS	VSS	VDD	VDD	VDD	VDD

When the CE6353 is powered up, the $\overline{RESET}$ pin 9 should be held low for at least 50 ms after VDD has reached normal operation levels. As the $\overline{RESET}$ pin goes high, the logic levels on SADD[4:0] are latched as the 2-wire bus address. ADDR[0] is the R/$\overline{W}$ bit.

The circuit works as a slave transmitter with the lsb set high or as a slave receiver with the lsb set low. In receive mode, the first data byte is written to the RADD virtual register, which forms the register sub-address. The RADD register takes an 8-bit value that determines which of 256 possible register addresses is written to by the following byte. Not all addresses are valid and many are reserved registers that must not be changed from their default values. Multiple byte reads or writes will auto-increment the value in RADD, but care should be taken not to access the reserved registers accidentally.

Following a valid chip address, the 2-wire bus STOP command resets the RADD register to 00. If the chip address is not recognized, the CE6353 will ignore all activity until a valid chip address is received. The 2-wire bus START command does NOT reset the RADD register to 00. This allows a combined 2-wire bus message, to point to a particular read register with a write command, followed immediately with a read data command. If required, this could next be followed with a write command to continue from the latest address. RADD would not be sent in this case. Finally, a STOP command should be sent to free the bus.

When the 2-wire bus is addressed (after a recognized STOP command) with the read bit set, the first byte read out is the contents of register 00.

3.1.2 Tuner

The CE6353 has a General Purpose Port that can be configured to provide a secondary 2-wire bus. See register GPP_CTL address 0x8C.

Master control mode is selected by setting register SCAN_CTL (0x62) [b3] = 1.

The allocation of the pins is: GPP0 pin 35 = CLK2, GPP1 pin 36 = DATA2.

3.1.3 Examples of 2-Wire Bus Messages

KEY:	S	Start condition	W	Write (= 0)
	P	Stop condition	R	Read (= 1)
	A	Acknowledge	NA	NOT Acknowledge
	Italics	CE6353 output	RADD	Register Address

Write operation - as a slave receiver:

S	DEVICE ADDRESS	W	***A***	RADD (n)	***A***	DATA (reg n)	***A***	DATA (reg n+1)	***A***	P

Read operation - CE6353 as a slave transmitter:

S	DEVICE ADDRESS	R	***A***	***DATA (reg 0)***	A	***DATA (reg 1)***	A	***DATA (reg 2)***	NA	P

Write/read operation with repeated start - CE6353 as a slave transmitter:

S	DEVICE ADDRESS	W	***A***	RADD (n)	***A***	S	DEVICE ADDRESS	R	***A***	***DATA (reg n)***	A	***DATA (reg n+1)***	NA	P

3.1.4 Primary 2-Wire Bus Timing

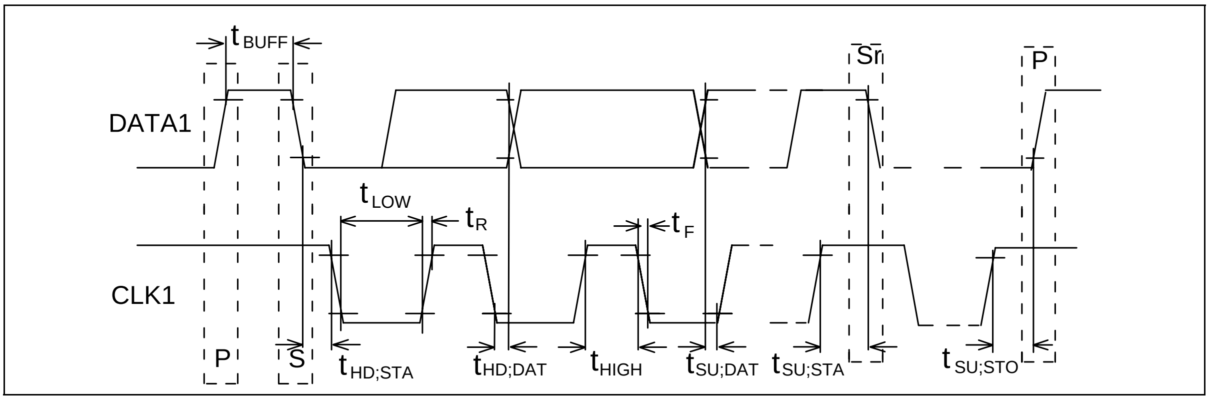

Figure 5 - Primary 2-Wire Bus Timing

Where: S = Start

Sr = Restart, i.e., start without stopping first.

P = Stop.

Parameter	Symbol	Value		Unit
		Min.	Max.	
CLK clock frequency (Primary)	f_{CLK}	0	400 [1]	kHz
Bus free time between a STOP and START condition.	t_{BUFF}	200		ns
Hold time (repeated) START condition.	$t_{HD;STA}$	200		ns
LOW period of CLK clock.	t_{LOW}	1300		ns
HIGH period of CLK clock.	t_{HIGH}	600		ns
Set-up time for a repeated START condition.	$t_{SU;STA}$	200		ns
Data hold time (when input).	$t_{HD;DAT}$	100		ns
Data set-up time	$t_{SU;DAT}$	100		ns
Rise time of both CLK and DATA signals.	t_R		note [2]	ns
Fall time of both CLK and DATA signals, (100 pF to ground).	t_F	20		ns
Set-up time for a STOP condition.	$t_{SU;STO}$	200		ns

Table 3 - Timing of 2-Wire Bus

1. If operating with an external 4 MHz clock, the serial clock frequency is reduced to 100 kHz maximum.
2. The rise time depends on the external bus pull up resistor. Loading prevents full speed operation.

3.2 MPEG

3.2.1 Data Output Header Format

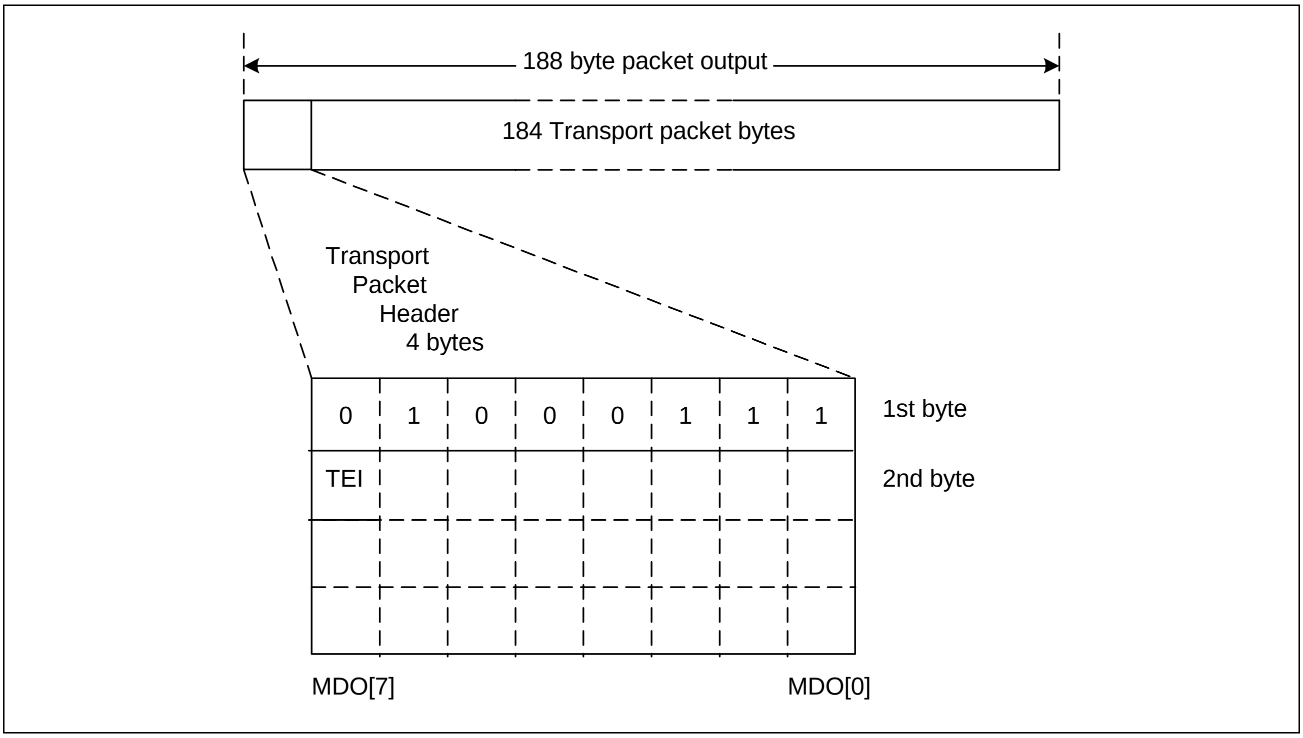

Figure 6 - DVB Transport Packet Header Byte

After decoding the 188-byte MPEG packet, it is output on the MDO pins in 188 consecutive clock cycles.

Additionally when the TEI_En bit in the OP_CTRL_0 register (0x5A) is set high (default), the TEI bit of any uncorrectable packet will automatically be set to ‘1’. If TEI_En bit is low then TEI bit will not be changed (but note that if this bit is already 1, for example, due to a channel error which has not been corrected, it will remain high at output).

3.2.2 MPEG Data Output Signals

The $\overline{\text{MPEGEN}}$ bit in the CONFIG register must be set low to enable the MPEG data. The maximum movement in the packet synchronization byte position is limited to ±1 output clock period. MOCLK will be a continuously running clock once symbol lock has been achieved, and is derived from the symbol clock. MOCLK is shown in Figure 7 with MOCLKINV = ‘1’, the default state, see register 0x50.

All output data and signals (MDO[7:0], MOSTRT, MOVAL & $\overline{\text{BKERR}}$) change on the negative edge of MOCLK (MOCLKINV = 1) to present stable data and signals on the positive edge of the clock.

A complete packet is output on MDO[7:0] on 188 consecutive clocks and the MDO[7:0] pins will remain low during the inter-packet gaps. MOSTRT goes high for the first byte clock of a packet. MOVAL goes high on the first byte of a packet and remains high until the last byte has been clocked out. $\overline{\text{BKERR}}$ goes low on the first byte of a packet where uncorrectable bytes are detected and will remain low until the last byte has been clocked out.

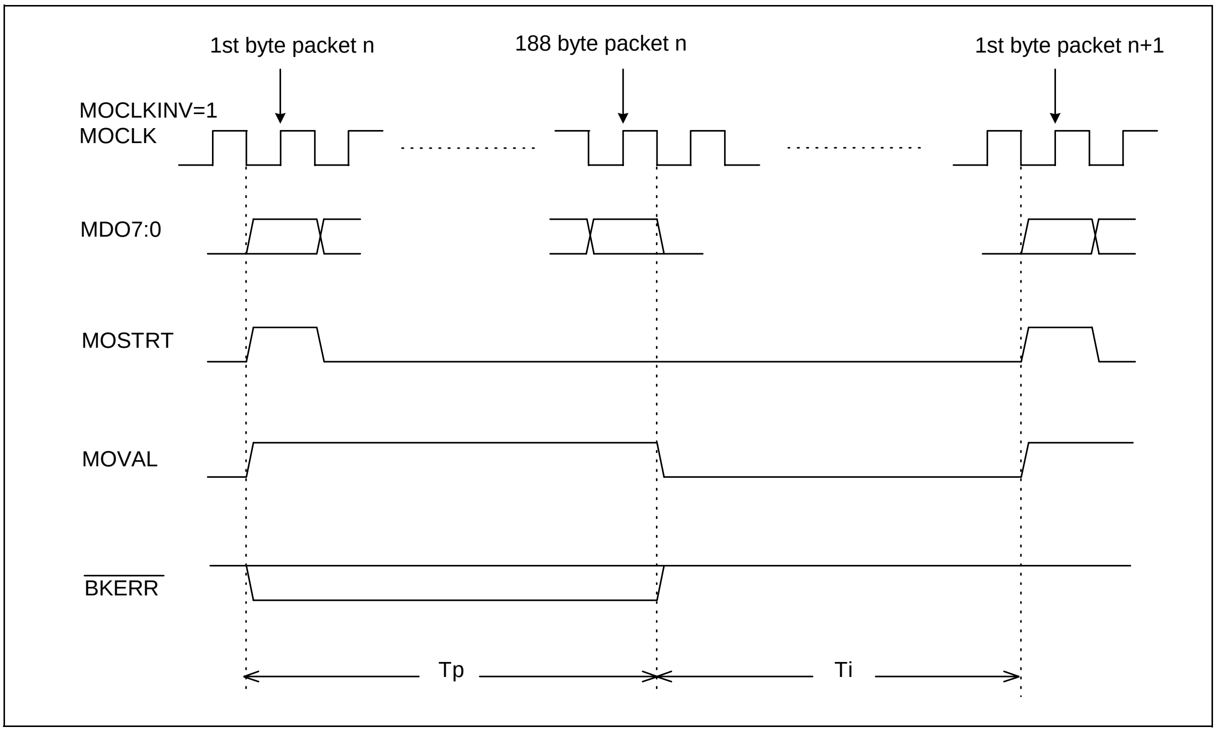

Figure 7 - MPEG Output Data Waveforms

3.2.3 MPEG Output Timing

Maximum delay conditions: VDD = 3.0V, CVDD = 1.62V, Tamb = 80^{O}C, Output load = 10pF.

Minimum delay conditions: VDD = 3.6V, CVDD = 1.98V, Tamb = -10^{O}C, Output load = 10pF.

MOCLK frequency = 45.06 MHz.

3.2.4 MOCLKINV = 1

Parameter	Delay conditions		Units
	Maximum	Minimum	
Data output delay t_D	3.0	1.0	ns
Setup Time t_{SU}	7.0	10.0	
Hold Time t_H	7.0	10.0	

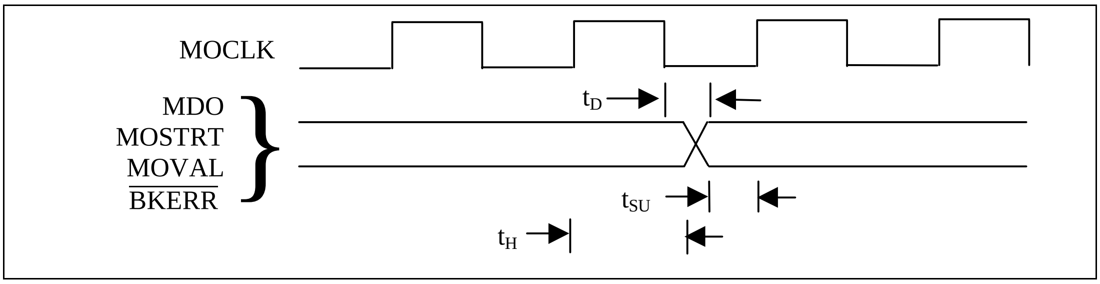

Figure 8 - MPEG Timing - MOCLKINV = 1

3.2.5 MOCLKINV = 0

MDOSWAP = 0

Parameter	Delay conditions		Units
	Maximum	Minimum	
Data output delay t_D	3.0	1.0	ns
Setup Time t_{SU}	18.0	20.0	
Hold Time t_H	1.0	0.2	

The hold time is better when MOCLKINV = 1, therefore this should be used if possible.

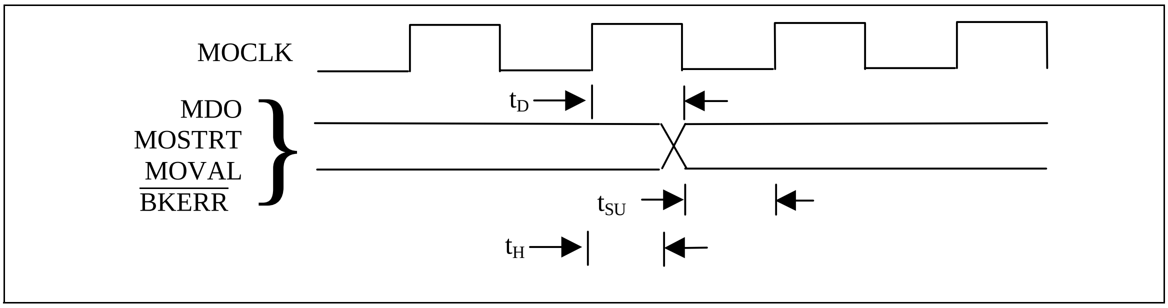

Figure 9 - MPEG Timing - MOCLKINV = 0

4.0 Electrical Characteristics

4.1 Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Units
Power supply voltage:	periphery	VDD	3.0	3.3	3.6	V
	core	CVDD	1.62	1.8	1.98	V
Power supply current:	periphery [1]	IDD_P		1		mA
	core	IDD_C		170		mA [2]
Input clock frequency [3]		XTI	16.00	20.48	25.00	MHz
CLK1 primary serial clock frequency [4]		fCLK			400	kHz
Ambient operating temperature			-10		80	°C

1. Current from the 3.3 V supply will be mainly dependent on the external loads.
2. Current given is for optimum performance, lower current is possible with reduced performance.
3. The min/max frequencies given are those supported by the oscillator cell. Required system frequencies are as defined in the design manual. Frequencies outside these limits are acceptable with an external clock signal.
4. If operating with an external 4 MHz clock, the serial clock frequency is reduced to 100 kHz maximum.

4.2 Absolute Maximum Ratings

Maximum Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Power supply	VDD	-0.3	+3.6	V
	CVDD	-0.3	+2.0	V
Voltage on input pins (5 V rated)	VI	-0.3	5.5	V
Voltage on input pins (3.3 V rated)	VI	-0.3	VDD + 0.3	V
Voltage on output pins (5 V rated)	VO	-0.3	5.5	V
Voltage on output pins (3.3 V rated)	VO	-0.3	VDD + 0.3	V
Storage temperature	TSTG	-55	150	°C
Operating ambient temperature	TOP	-10	80	°C
Junction temperature	TJ		125	°C

Note: Stresses exceeding these listed under absolute maximum ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

4.3 DC Electrical Characteristics

DC Electrical Characteristics

Parameter	Conditions	Pins	Symbol	Min.	Typ.	Max.	Unit
Operating periphery voltage			VDD	3.0	3.3	3.6	V
core			CVDD	1.62	1.8	1.98	V
Supply current [1]	1.62≥CVDD≥1.98		IDDCORE		170		mA
Supply current sleep mode					300		μA
Outputs							
Output levels	IOH 2mA 3.0≥VDD≥3.6	MDO(7:0), MOVAL, MOSTRT, MOCLK, STATUS, BKERR	VOH	2.4			V
	IOL 2mA 3.0≥VDD≥3.6		VOL			0.4	V
	IOL 6mA 3.0≥VDD≥3.6	GPP(3:0), DATA1, AGC1, AGC2, IRQ	VOL			0.4	V
Output capacitance	Not including track	MDO(7:0), MOVAL, MOSTRT, MOCLK, STATUS, BKERR			3.0		pF
		GPP(3:0), DATA1, AGC1, AGC2,IRQ			3.6		pF
Output leakage (tri-state)						1	μA
Inputs							
Input levels	3.0≥VDD≥3.6 -0.5 ≥ Vin ≥ VDD+0.5V	MICLK, SADD(4:0) SLEEP, OSCMODE	VIH	2.0			V
Input levels	3.0≥VDD≥3.6 -0.5 ≥ Vin ≥ +5.5V	GPP(3:0), CLK1, DATA1, RESET	VIH	2.0			V
Input levels	3.0≥VDD≥3.6	All inputs	VIL			0.8	V
Input leakage Current	Capacitances do not include track	SLEEP, SMTEST, MICLK, CLK1, OSCMODE				±1	μA
Input capacitance					1.8		pF
Input capacitance		SADD(4:0), DATA1, GPP(3:0)			3.6		pF

[1] Current given is for optimum performance, lower current is possible with reduced performance.

4.4 Crystal Specification and External Clocking

Parallel resonant fundamental frequency (preferred)	20.4800 MHz
Tolerance over operating temperature range	± 150 ppm
Tolerance overall	± 200 ppm
Typical load capacitance	27 pF
Drive level	0.4 mW max
Equivalent series resistance	<25 Ω

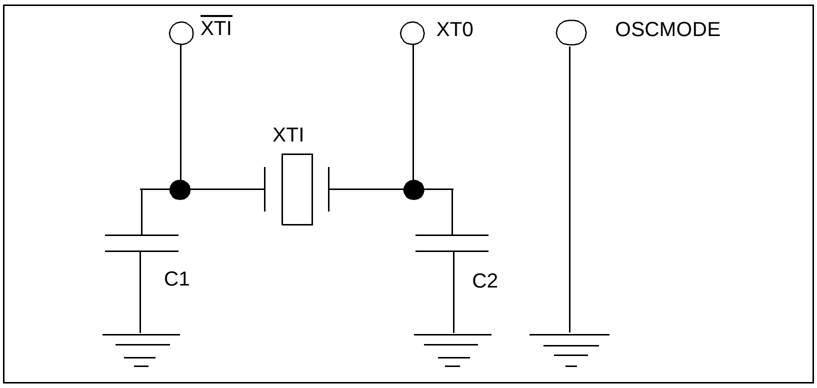

Figure 10 - Crystal Oscillator Circuit

4.4.1 Selection of External Components

The capacitor values used must ensure correct operation of the Pierce oscillator such that the total loop gain is greater than unity. Correct selection of the two capacitors is very important and the following method is recommended to obtain values for C1 and C2.

4.4.1.1 Loop Gain Equation

Although oscillation may still occur if the loop gain is just above 1, a loop gain of between 5 and 25 is optimum to ensure that oscillations will occur across all variations in temperature, process and supply voltage, and that the circuit will exhibit good start-up characteristics.

Equation 1 - $$A = \frac{C_{out} \cdot g_m}{C_{in}} \left[\frac{C_{out} + C_{in}}{R_f . C_{in}} + \frac{1}{Z_{in}} + \frac{1}{Z_o} \right]^{-1}$$

Equation 2 - $$\cdot\ Z_{in} = \frac{1}{(2.\pi.f.C_{out})^2.ESR}$$

4.4.1.2 List of Equation Parameters

A	total loop gain (between 5 and 25)
Cin	C1 + Cpar
Cout	C2 + Cpar
Cpar	parasitic capacitance associated with each oscillator pin ($\overline{\text{XTI}}$ and XTO). It consists of track capacitances, package capacitance and cell input capacitance. Normally Cpar ≈ 4pF.
Zo	9.143 kΩ - output impedance of amplifier at 1.8 V operation - typical
gm	8.736 mA/V - transconductance of amplifier at 1.8 V operation -typical
Rf	2.3 MΩ - internal feedback resistor
ESR	maximum equivalent series resistance of crystal - given by crystal manufacturer (Ω)
f	fundamental frequency of crystal (Hz)

4.4.1.3 Calculating Crystal Power Dissipation

To calculate the power dissipated in a crystal the following equation can be used.

Equation 3 - $P_c = \dfrac{V_{pp}^2}{8.Z_{in}}$

Pc = power dissipated in crystal at resonant frequency (W)

Vpp = maximum peak to peak output swing of amplifier is 1.8 V for all CVDD

Zin = crystal network impedance (see Equation 2)

4.4.1.4 Capacitor Values

Using the loop gain limits ($5 \leq A \leq 25$), the maximum and minimum values for C1 and C2 can be calculated with Equation 4 below.

Equation 4 - $C_{in} = C_{out} = \sqrt{\left[\dfrac{g_m}{A} - \dfrac{2}{R_f} - \dfrac{1}{Z_o}\right] . \dfrac{1}{(2.\pi.f)^2.ESR}}$ when: $C_1 = C_2 = C_{out} - C_{par}$

Note: Equation 4 was derived from Equation 1 and Equation 2 using the premise that C1 = C2.

Within these limits, any value for C1 and C2 can now be selected. Normally C1 and C2 are chosen such that the resulting crystal load capacitance C_L (see Equation 5) is close to the crystal manufacturers recommended C_L (standard values for C_L are 15 pF, 20 pF and 30 pF). The crystal will then operate very near its specified frequency.

Equation 5 - $C_L = \dfrac{C_{out} . C_{in}}{C_{out} + C_{in}} + C_{par12}$

C_{par12} = parasitic capacitance between the $\overline{\text{XTI}}$ and XTO pins. It consists of the IC package’s pin-to-pin capacitance (including any socket used) and the printed circuit board’s track-to-track capacitance.

C_{par12} ≈ 2pF.

If some frequency pulling can be tolerated, a crystal load capacitance different from the crystal manufacturer’s recommended C_L may be acceptable. Larger values of C_L tend to reduce the influence of circuit variations and tolerances on frequency stability. Smaller values of C_L tend to reduce startup time and crystal power dissipation. Care must however be taken that C_L does not fall outside the crystal pulling range or the circuit may fail to start up altogether. It is also possible to quote C_L to the crystal manufacturer who can then cut a crystal to order which will resonate, under the specified load conditions, at the desired frequency.

Finally the power dissipation in the crystal must be checked. If Pc is too high C1 and C2 must be reduced. If this is not feasible C2 alone may be reduced. Unbalancing C1 and C2 will, however, require checking if the loop gain condition is still satisfied. This must be done using Equation 1.

Note: $2 \geq \dfrac{C_2}{C_1} \geq 0.5$

4.4.1.5 Oscillator/Clock Application Notes

- On the printed circuit board, the tracks to the crystal and capacitors must be made as short as possible. Other signal tracks must not be allowed to cross through this area. The component tracks should preferably be ringed by a ground track connected to the chip ground (0 V) on adjacent pins either side of the crystal pins. It is also advisable to provide a ground plane for the circuit to reduce noise.
- External clock signals, applied to $\overline{\text{XTI}}$ and/or XTO, must not exceed the cell supply limits (i.e., 0V and CVDD) and current into or out of XTI and/or XTO must be limited to less than 10mA to avoid damaging the cell's amplitude clamping circuit.
- An external, DC coupled, single ended square wave clock signal may be applied to $\overline{\text{XTI}}$ if OSCMODE = 0. To limit the current taken from the signal source a resistor should be placed between the clock source and XTI. The recommended value for this series resistor is 470 Ω for a clock signal switching between 0 V and CVDD. The current the clock source needs to source/sink is then $\leq$1.9 mA. The XTO pin must be left unconnected in this configuration.
- AC coupling of a single ended external clock to $\overline{\text{XTI}}$, with OSCMODE = 0, is not recommended. The duty cycle of the OSCOUT signal cannot be guaranteed in such a configuration.
- AC coupling of a single ended external clock to $\overline{\text{XTI}}$, with OSCMODE = 1, is possible. It is recommended that the circuit shown in Figure 11 be used to correctly bias the oscillator inputs: The common-mode voltage VCM for XTI and XTO, (set by the 36 kΩ and 22 kΩ resistors) must be 800 mV < VCM < CVDD and the amplitude Vpp of the clock signal must be >100 mV.

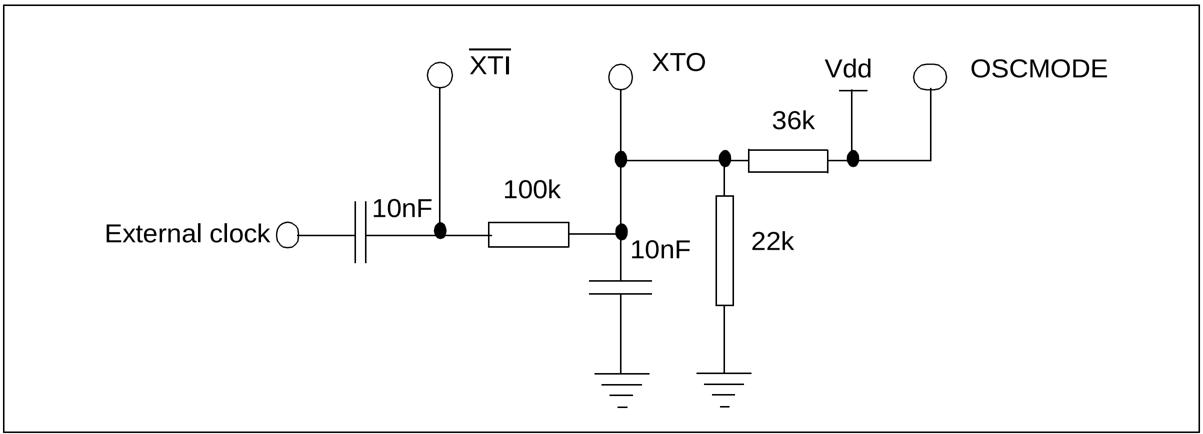

Figure 11 - External Clocking via AC Coupling

- External, differential clock signals may be applied to $\overline{\text{XTI}}$ and XTO if OSCMODE = 1. The common-mode voltage VCM for the differential clock signals must be 800 mV < VCM < CVDD, and the peak-to-peak signal amplitude Vpp must be >100 mV. It is recommended that differential clock signals have VCM = 1.0V. For Vpp > 400 mV a resistor of $\geq$390 Ω in series with XTI or XTO may be required to limit the current taken from or supplied to the clock sources.

5.0 Application Circuit

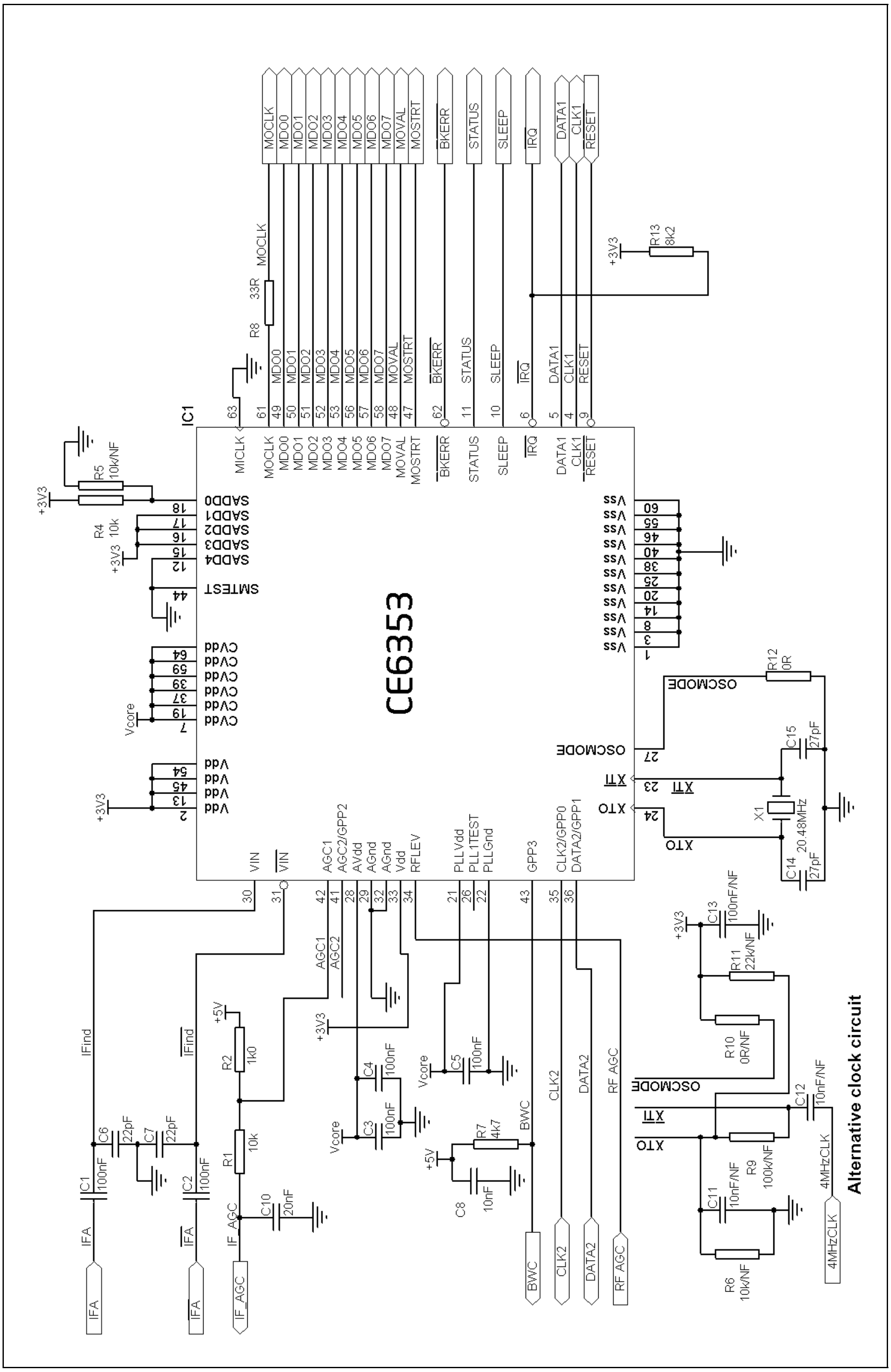

Figure 12 - Typical Application Circuit