EPSON

SED1793D0B

TFT LCD Driver

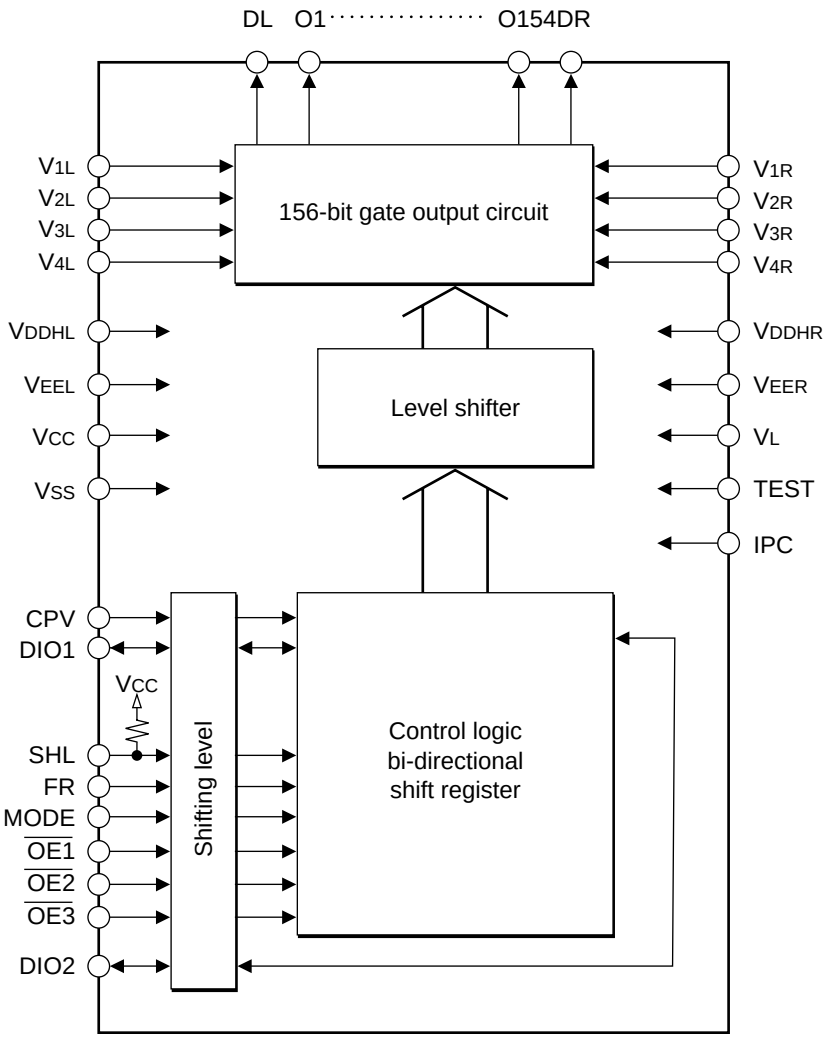
■ DESCRIPTION

The gate driver IC SED1793 is designed to drive an SVGA and XGA display TFT-LCD panel and enables capacity combining drive and punch-through voltage compensatory drive thanks to gate output voltage control. The maximum gate output voltage amplitude is 40 V, enabling negative voltage output. It also enables double ON gate drive, which outputs ON twice in the same field during "H" reverse rotation drive.
This IC has a built-in power supply circuit for the internal logic and you can select whether or not to use it. When using the circuit, no internal logic power needs to be supplied.
The bump layout of this IC is designed for COG mounting, enabling a module architecture to be narrowed.

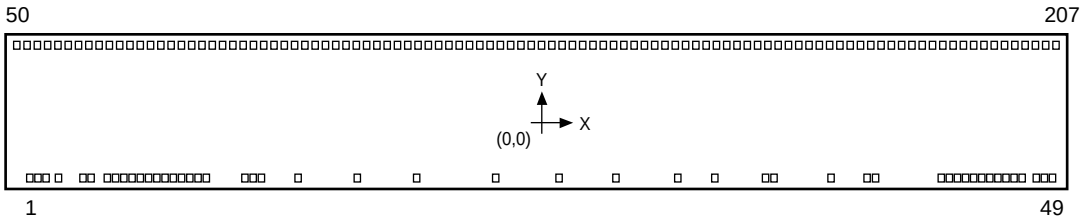
■ FEATURES

- Gate output voltage level: 4 values (V_1 to V_4)
- Gate output voltage amplitude: 40 V (max.)
- Low voltage operation available: 2.7 V (min.)
- Output shift direction-pin selection.
- Gate output voltage can be forcibly fixed thanks to the output enable function.
- Gate output negative voltage output available thanks to the level shift circuit.
- Double ON gate drive available.
- Built-in internal logic power supply circuit.
- Package to be shipped Au bump chip
  TCP
- This product is not designed to resist radiation or light.

■ BLOCK DIAGRAM



■ BUMP LAYOUT



Chip size: 15.04 mm (X) × 2.08 mm (Y)
Chip thickness: 0.625 mm (t)
Bump size: 77.6 µm × 78.4 µm (# 1 to 25 and 28 to 49)
50.4 µm × 70.4 µm (# 26)
50.4 µm × 78.4 µm (# 27)
65.6 µm × 80.0 µm (# 50 to 207)
Bump height (reference): 17 to 28 µm

■ ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_{EE}	–23.0 to +0.3	V
Supply voltage (4)	V_L	V_{EE} –0.3 to V_{EE} +7.0	V
Supply voltage (5)	$V_{DDH} – V_{EE}$	–0.3 to +45.0	V
Supply voltage (6)	V_1	–0.3 to V_{DDH} +0.3	V
Supply voltage (7)	V_2, V_3, V_4	V_{EE} –0.3 to V_{DDH} +0.3	V
Supply voltage (8)	$V_1 – V_4$	–0.3 to +45.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} +0.3	V
Input current	I_{IN}	±10	mA
Output current	I_O	±10	mA
Ambient operating temperature	Ta	–25 to +85	°C
Storing temperature	T_{stg2}	–55 to +125	°C

Notes

1. All voltages refer to V_{SS} unless otherwise specified.
2. The element may permanently break if used outside the absolute maximum ratings shown above. The element reliability may disadvantageously be affected if it is exposed to the absolute maximum rating conditions for a long time.
3. For voltages V_{DDH}, V_{EE}, V_{CC}, V_{SS} and V_L, be sure to keep the condition of "$V_{EE} \le V_L \le V_{SS} \le V_{CC} \le V_{DDH}$". For voltages V_1, V_2, V_3 and V_4, also be sure to keep the conditions of "$V_{EE} \le V_4$", "$V_1 \le V_{DDH}$" and "$V_4 \le V_2$, $V_3 \le V_1$".
4. Never float the logic system power supply while the high-voltage logic and gate output power supplies are turned on or allow V_{CC} to go under 2.6 V, otherwise, the IC reliability may disadvantageously be affected.

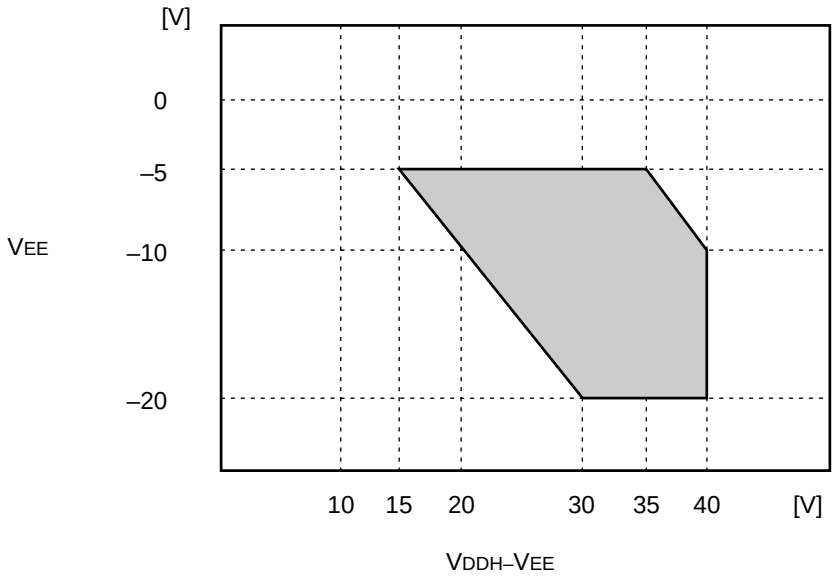
■ RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V)

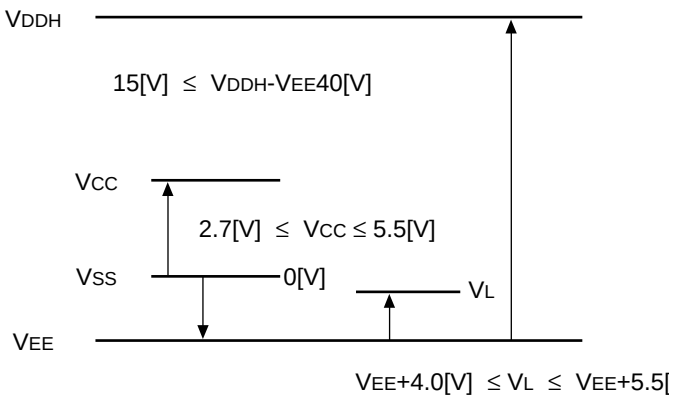
Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	+2.7 to +5.5	V
Supply voltage (2)	V_{DDH}	+10.0 to +30.0	V
Supply voltage (3)	V_{EE}	–20.0 to –5.0	V
Supply voltage (4)	V_L	–16.0 to +0.5	V
Supply voltage (5)	$V_{DDH} – V_{EE}$	+15.0 to +40.0	V
Supply voltage (6)	V_1	+8.0 to +30.0	V
Supply voltage (7)	V_2	–20.0 to +10.0	V
Supply voltage (8)	V_3	–20.0 to +20.0	V
Supply voltage (9)	V_4	–20.0 to +10.0	V
Supply voltage (10)	$V_1 – V_4$	+8.0 to +40.0	V
Operating frequency	f_{CPV}	DC to 200	kHz

Notes

1. IC operation is guaranteed within the recommended operating condition range.
2. Insert a bypass capacitor for noiseproof measures near the power supply pin.
3. Unless swinging the V_1 supply voltage, make the electric potential the same as that of V_{DDH}.
4. When swinging the V_1 supply voltage, the guaranteed output resistance, rise and fall time ratings will differ.
5. When the output voltage during an output fixed period is 1 level only, make the V_2 electric potential the same as that of V_4 and fix FR at either the V_{CC} or V_{SS} level.
6. V_{EE} + 4.0 (V) ≤ V_L ≤ V_{EE} + 5.5 (V)

The recommended operating voltage is based on the combination of the high-dielectric strength logic system power supply conditions and the logic system power supply conditions (the hatched portion in the figure below). For the internal logic power supply, keep the condition of "V_{EE} + 4.0 (V) ≤ V_L ≤ V_{EE} + 5.5 (V)".





■ ELECTRICAL CHARACTERISTICS UNDER THE RECOMMENDED OPERATING RANGE

● DC Characteristics

(Ta = –25 to +85°C, V_{CC} = 3.3 ± 0.3 V, V_{SS} = 0 V, V_{DDH} = 30 V, V_{EE} = –10 V, V_L = –5 V)

Parameter	Symbol	Condition	Rating			Units	Pin used
			Min.	Typ.	Max.		
"L" input voltage	V_{IL}	—	V_{SS}	—	V_{SS} + 0.2 × (V_{CC} – V_{SS})	V	All input pins
"H" input voltage	V_{IH}	—	V_{SS} + 0.8 × (V_{CC} – V_{SS})	—	V_{CC}	V	All input pins
"L" output voltage	V_{OL}	I_{OL} = 40 µA	V_{SS}	—	V_{SS} + 0.4	V	DIO1, DIO2
"H" output voltage	V_{OH}	I_{OH} = 40 µA	V_{CC} – 0.4	—	V_{CC}	V	DIO1, DIO2
Output resistance	R_{ON}	ΔV_1 = 0.5 V V_1 = 30 V, V_2 = 10 V, V_3 = 0 V, V_4 = –10 V	—	0.73	1.47	kΩ	O1 to O154
Input leakage current	I_{LI}	—	–1.0	—	+1.0	µA	All input pins
Input capacity	C_{IN}	Ta = 25°C	—	—	15	pF	All input pins
Static current consumption (1)	I_{CS}	—	—	(80)	250	µA	V_{CC}
Static current consumption (2)	I_{DS}	—	—	(45)	100	µA	V_{DDH}
Dynamic current consumption (1)	I_{CC}	*1	—	(150)	300	µA	V_{CC}
Dynamic current consumption (2)	I_L		—	(30)	60	µA	V_L
Dynamic current consumption (3)	I_{DDH}		—	(75)	140	µA	V_{DDHL}, V_{DDHR}

*1: SVGA display, 150 outputs, f_{DIO} = 65 Hz, f_{CPV} = $f_{\overline{OE1}}$ = 40 kHz, $\overline{OE2}$ = $\overline{OE3}$ = "H", output pin unloaded, double gate output

● AC Characteristics

- Input Timing Characteristics

(Ta = –25 to +85°C, V_{CC} = 3.3 ± 0.3 V, V_{SS} = 0 V, V_{DDH} = 30 V, V_{EE} = –10 V, V_L = –5 V)

Parameter	Symbol	Condition	Min.	Max.	Unit
CPV cycle	t_{CPV}	—	5.0	—	µs
CPV high-level pulse width	t_{CPVH}	—	1.0	—	µs
CPV low-level pulse width	t_{CPVL}	—	1.7	—	µs
Data setup time	t_{DS}	—	400	—	ns
Data hold time	t_{DH}	—	400	—	ns
$\overline{OE}$ setup time	t_{OES}	—	0 (*2)	*3	µs
$\overline{OE}$ hold time	t_{OEH}	—	0.2 (*2)	*3	µs

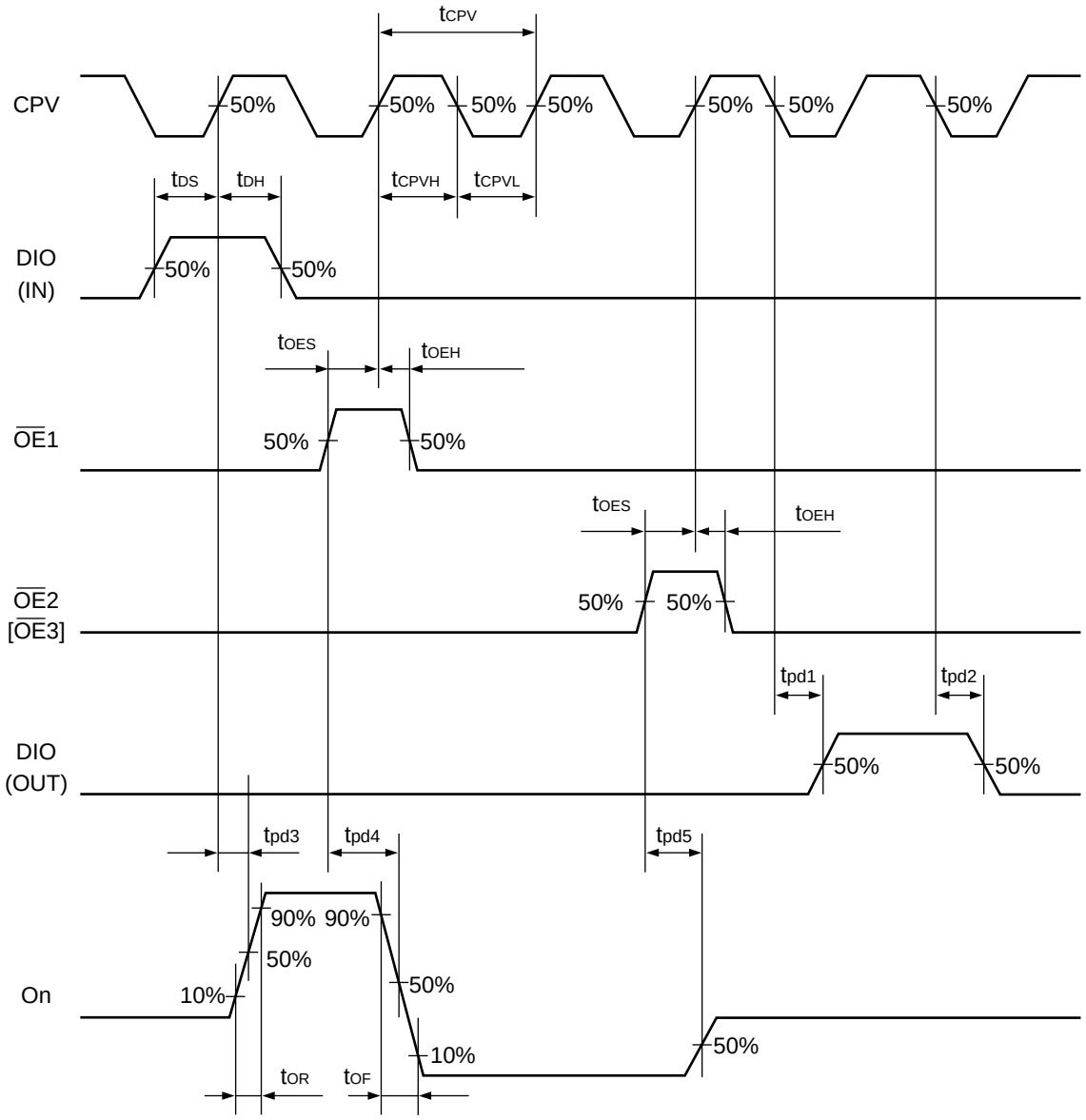
*1: The input signal rise and fall times (t_r and t_f) are specified at 30 ns or less.
*2: The values shown above will not apply when all $\overline{OE}$s are set at "L".
*3: t_{CPV} applies unless all $\overline{OE}$s are set at "H".
*4: Expected output waveform may not be obtained if the output load is large and the $\overline{OE}$ width is small.

- Output Timing Characteristics

(Ta = –25 to +85°C, V_{CC} = 3.3 ± 0.3 V, V_{SS} = 0 V, V_{DDH} = 30 V, V_{EE} = –10 V, V_L = –5 V)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
CPV to DIO output delay time		t_{pd1}	C_L = 20 pF	—	0.4	1.3	µs
		t_{pd2}		—	0.47	1.3	µs
CPV to On output delay time *1	$V_3 \rightarrow V_1$	t_{pd3}	C_L = 700 pF V_1 = 30 V, V_2 = 10 V V_3 = 0 V, V_4 = –10 V	—	0.68	1.2	µs
$\overline{OE1}$ to On output delay time	$V_4 \rightarrow V_1$	t_{pd4-1}		—	0.9	1.7	µs
	$V_1 \rightarrow V_4$	t_{pd4-2}		—	0.54	1.0	µs
$\overline{OE2}$ ($\overline{OE3}$) to On output delay time	$V_4 \rightarrow V_3$	t_{pd5-1}		—	0.55	1.0	µs
	$V_2 \rightarrow V_3$	t_{pd5-2}		—	0.45	0.8	µs
On output rise time	$V_4 \rightarrow V_1$ $V_2 \rightarrow V_1$	t_{OR}		—	1.44	2.2	µs
On output fall time	$V_1 \rightarrow V_2$ $V_1 \rightarrow V_4$	t_{OF}		—	1.2	1.8	µs

*1: Applies when $\overline{OE1}$ are set at "L".



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