



LC3564CM, 3564CT-55U/70U

64K (8192-word × 8-bit) SRAM with $\overline{OE}$, $\overline{CE1}$, and $\overline{CE2}$ Control Pins

Overview

The LC3564CM and LC3564CT-55U/70U are 8192-word × 8-bit asynchronous silicon gate CMOS SRAMs. These are full CMOS type SRAMs that adopt a six-transistor memory cell and feature fast access times, low operating power dissipation, and an ultralow standby current. These SRAMs provide three control signal inputs: an $\overline{OE}$ input for high-speed memory access, and two chip enable lines, $\overline{CE1}$ and $\overline{CE2}$, for low power mode and device selection. These means that these SRAMs are ideal for systems that require low power and battery backup, and that they support easy memory expansion. The ultralow standby current that is a feature of these SRAMs allows them to be used with capacitor backup as well. Since these SRAMs support 3-V operation, they are also appropriate for use in portable battery operated systems.

Features

- Supply voltage range: 2.7 to 5.5 V
 - In 5-V operation mode: 5.0 V ±10%
 - In 3-V operation mode: 3.0 V ±10%
- Address access time (t_{AA})
 - In 5-V operation mode:

LC3564CM, and CT-55U:	55 ns (max)
LC3564CM, and CT-70U:	70 ns (max)
 - In 3-V operation mode:

LC3564CM, and CT-70U:	200 ns (max)
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- Ultralow standby current
 - In 5-V operation mode: 1.0 μA ($T_a \leq 70^\circ\text{C}$),
3.0 μA ($T_a \leq 85^\circ\text{C}$)
 - In 3-V operation mode: 0.8 μA ($T_a \leq 70^\circ\text{C}$),
2.5 μA ($T_a \leq 85^\circ\text{C}$)
- Operating temperature range
 - In 5-V operation mode: -40 to 85°C
 - In 3-V operation mode: -40 to 85°C
- Data retention supply voltage: 2.0 to 5.5 V
- All input and output levels:
 - In 5-V operation mode: TTL compatible levels
 - In 3-V operation mode: $V_{CC} - 0.2$ V/0.2 V
- Three control inputs: $\overline{OE}$, $\overline{CE1}$, and $\overline{CE2}$
- Shared input and output pins, three-state outputs
- No clock required
- Packages
 - 28-pin SOP (450 mil) plastic package: LC3564CM
 - 28-pin TSOP (8 × 13.4 mm) plastic package: LC3564CT

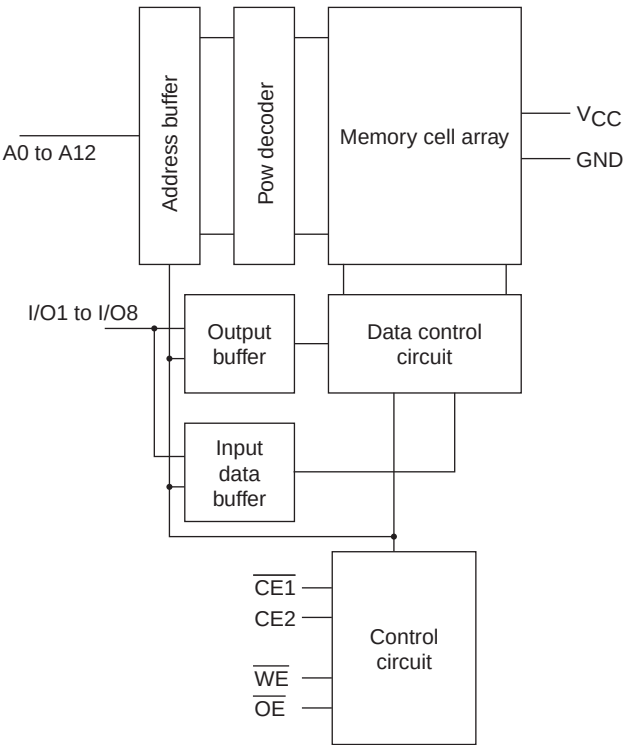
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Block Diagram



A13512

Pin Functions

A0 to A12	Address inputs
$\overline{WE}$	Read/write control input
$\overline{OE}$	Output enable input
$\overline{CE1}$, CE2	Chip enable inputs
I/O1 to I/O8	Data I/O
VCC, GND	Power supply and ground

Function Table

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	H	L	H	Data output	I _{CCA}
Write cycle	L	H	X	L	Data input	I _{CCA}
Output disable	L	H	H	H	High impedance	I _{CCA}
Not selected	H	X	X	X	High impedance	I _{CCS}
	X	L	X	X	High impedance	I _{CCS}

X : H or L

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Input voltage	V_{IN}		-0.3^* to $V_{CC} + 0.3$	V
I/O voltage	$V_{I/O}$		-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}		-40 to $+85$	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to $+125$	$^\circ\text{C}$

Note: For pulse widths less than 30 ns: -3.0 V

Input and Output Capacitances at $T_a = 25^\circ\text{C}$, $f = 1$ MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
I/O pin capacitance	$C_{I/O}$	$V_{I/O} = 0$ V		6	10	pF
Input pin capacitance	C_{IN}	$V_{IN} = 0$ V		6	10	pF

Note: These parameters are sampled, and are not measured for every unit.

[5-V Operation]

DC Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		4.5	5.0	5.5	V
Input voltage	V_{IH}		2.2		$V_{CC} + 0.3$	V
	V_{IL}		-0.3^*		$+0.8$	V

Note: For pulse widths less than 30 ns: -3.0 V

DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5 V

Parameter		Symbol	Conditions			Ratings			Unit
						min	typ *	max	
Input leakage current		I _{LI}	V _{IN} = 0 to V _{CC}			−1.0		+1.0	μA
I/O leakage current		I _{LO}	V _{CE1} = V _{IH} or V _{CE2} = V _{IL} or V _{OE} = V _{IH} or V _{WE} = V _{IL} , V _{I/O} = 0 to V _{CC}			−1.0		+1.0	μA
Output high-level voltage		V _{OH}	I _{OH} = −1.0 mA			2.4			V
Output low-level voltage		V _{OL}	I _{OL} = 2.0 mA					0.4	V
Operating supply current	V _{CC} − 0.2 V/0.2 V inputs	I _{CCA1}	V _{CE1} ≤ 0.2 V, V _{CE2} ≥ V _{CC} − 0.2 V, I _{I/O} = 0 mA, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V		Ta ≤ 70°C		0.01	1.0	μA
					Ta ≤ 85°C			3.0	
		I _{CCA4}	V _{CE1} ≤ 0.2 V, V _{CE2} ≥ V _{CC} − 0.2 V, I _{I/O} = 0 mA, DUTY = 100%	min	LC3564CM, CT-55U			45	mA
				cycle	LC3564CM, CT-70U			35	
	1 μs cycle				4				
	TTL inputs	I _{CCA2}	V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , I _{I/O} = 0 mA, V _{IN} = V _{IH} or V _{IL}					7	mA
		I _{CCA3}	V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , I _{I/O} = 0 mA, DUTY = 100%	min	LC3564CM, CT-55U			45	mA
cycle				LC3564CM, CT-70U			40		
1 μs cycle				7					
Standby mode supply current	V _{CC} − 0.2 V/0.2 V inputs	I _{CCS1}	V _{CE2} ≤ 0.2 V or V _{CE1} ≥ V _{CC} − 0.2 V V _{CE2} ≥ V _{CC} − 0.2 V		Ta ≤ 70°C		0.01	1.0	μA
					Ta ≤ 85°C			3.0	
	TTL inputs	I _{CC2}	V _{CE2} = V _{IL} or V _{CE1} = V _{IH} , V _{IN} = 0 to V _{CC}					2.0	mA

Note *: Reference values at $V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$

LC3564CM, CT-55U/70U

AC Electrical Characteristics at Ta = -40 to +85°C, V_{CC} = 4.5 to 5.5 V

Parameter	Conditions
[AC Test Conditions]	
Input pulse voltage	V _{IH} = 2.4 V, V _{IL} = 0.6 V
Input rise and fall times	5 ns
Input and output timing level	1.5 V
Output load	LC3564CM and CT-55U/70U: 30 pF + 1 TTL gate (Including the jig capacitance.)

Read Cycle

Parameter	Symbol	LC3564CM, CT				Unit
		-55U		-70U		
		min	max	min	max	
Read cycle time	t _{RC}	55		70		ns
Address access time	t _{AA}		55		70	ns
$\overline{\text{CE1}}$ access time	t _{CA1}		55		70	ns
CE2 access time	t _{CA2}		55		70	ns
$\overline{\text{OE}}$ access time	t _{OA}		30		35	ns
Output hold time	t _{OH}	10		10		ns
$\overline{\text{CE1}}$ output enable time	t _{COE1}	5		10		ns
CE2 output enable time	t _{COE2}	5		10		ns
$\overline{\text{OE}}$ output enable time	t _{OOE}	5		5		ns
$\overline{\text{CE1}}$ output disable time	t _{COD1}		20		30	ns
CE2 output disable time	t _{COD2}		20		30	ns
$\overline{\text{OE}}$ output disable time	t _{OOD}		20		25	ns

Write Cycle

Parameter	Symbol	LC3564CM, CT				Unit
		-55U		-70U		
		min	max	min	max	
Write cycle time	t _{WC}	55		70		ns
Address setup time	t _{AS}	0		0		ns
Write pulse width	t _{WP}	40		50		ns
$\overline{\text{CE1}}$ setup time	t _{CW1}	50		60		ns
CE2 setup time	t _{CW2}	50		60		ns
Write recovery time	t _{WR}	0		0		ns
$\overline{\text{CE1}}$ write recovery time	t _{WR1}	0		0		ns
CE2 write recovery time	t _{WR2}	0		0		ns
Data setup time	t _{DS}	25		35		ns
Data hold time	t _{DH}	0		0		ns
$\overline{\text{CE1}}$ data hold time	t _{DH1}	0		0		ns
CE2 data hold time	t _{DH2}	0		0		ns
$\overline{\text{WE}}$ output enable time	t _{WOE}	5		5		ns
$\overline{\text{WE}}$ output disable time	t _{WOD}		30		30	ns

LC3564CM, CT-55U/70U

[3-V Operation]

DC Allowable Operating Ranges at Ta = -40 to +85°C, VCC = 2.7 to 3.3 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	VCC		2.7	3.0	3.3	V
Input voltage	VIH		VCC - 0.2		VCC	V
	VIL		0		0.2	V

DC Electrical Characteristics at Ta = -40 to +85°C, VCC = 2.7 to 3.3 V

Parameter		Symbol	Conditions		Ratings			Unit
					min	typ *	max	
Input leakage current		ILI	VIN = 0 to VCC		-1.0		+1.0	μA
I/O leakage current		ILO	VCE1 = VIH or VCE2 = VIL or VOE = VIH or VWE = VIL, VIO = 0 to VCC		-1.0		+1.0	μA
Output high-level voltage		VOH	IOH = -0.5 mA		VCC - 0.2			V
Output low-level voltage		VOL	IOL = 1.0 mA				0.2	V
Operation supply current	VCC - 0.2 V/0.2 V inputs	ICCA1	VCE1 ≤ VIL, VCE2 ≥ VIH, IIO = 0 mA, VIN ≤ VIL or VIN ≥ VIH	Ta ≤ 70°C		0.01	0.8	μA
				Ta ≤ 85°C			2.5	
		ICCA4	VCE1 ≤ VIL, VCE2 ≥ VIH, IIO = 0 mA, DUTY = 100%	min cycle	LC3564CM, CT-70U		20	mA
				1 μs cycle		3		
Standby mode supply current	VCC - 0.2 V/0.2 V inputs	ICCS1	VCE2 ≤ 0.2 V or VCE1 ≥ VIH, VCE2 ≥ VIH	Ta ≤ 70°C		0.01	0.8	μA
				Ta ≤ 85°C			2.5	

Note *: Reference values at VCC = 3 V, Ta = 25°C

LC3564CM, CT-55U/70U

AC Electrical Characteristics at Ta = -40 to +85°C, V_{CC} = 2.7 to 3.3 V

Parameter	Conditions
[AC Test Conditions]	
Input pulse voltage	V _{IH} = V _{CC} - 0.2 V, V _{IL} = 0.2 V
Input rise and fall times	10 ns
Input and output timing level	1.5 V
Output load	LC3564CM, CT-70U : 30pF (Including the jig capacitance.)

Read Cycle

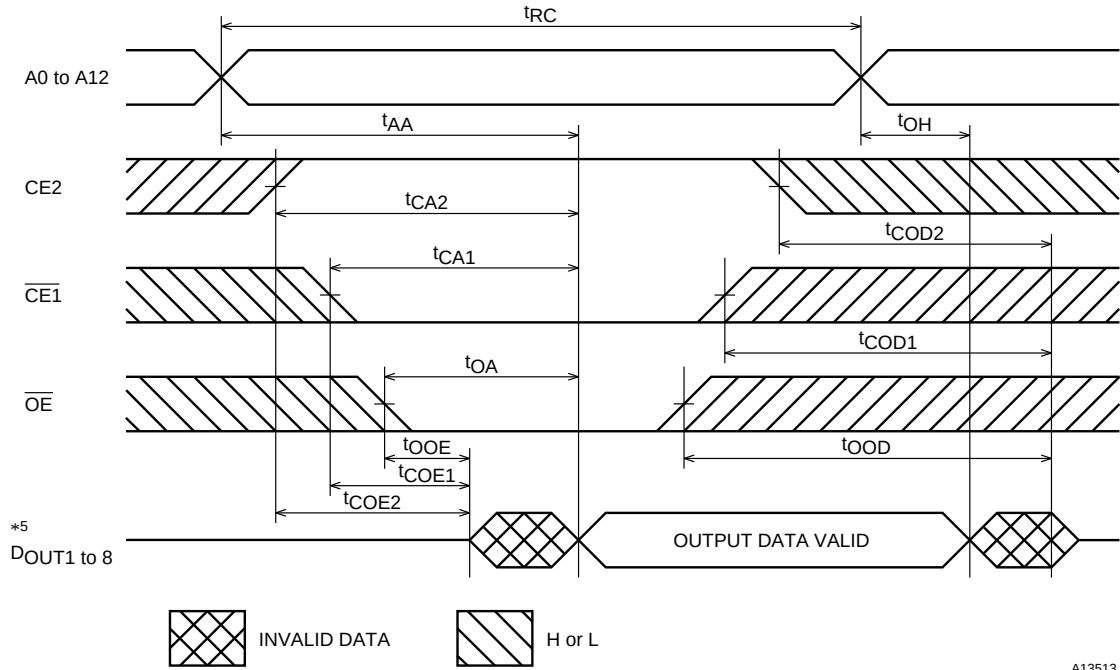
Parameter	Symbol	LC3564CM, CT-70U		Unit
		-10		
		min	max	
Read cycle time	t _{RC}	200		ns
Address access time	t _{AA}		200	ns
$\overline{\text{CE1}}$ access time	t _{CA1}		200	ns
CE2 access time	t _{CA2}		200	ns
$\overline{\text{OE}}$ access time	t _{OA}		100	ns
Output hold time	t _{OH}	20		ns
$\overline{\text{CE1}}$ output enable time	t _{COE1}	20		ns
CE2 output enable time	t _{COE2}	20		ns
$\overline{\text{OE}}$ output enable time	t _{OOE}	10		ns
$\overline{\text{CE1}}$ output disable time	t _{COD1}		60	ns
CE2 output disable time	t _{COD2}		60	ns
$\overline{\text{OE}}$ output disable time	t _{OOD}		50	ns

Write Cycle

Parameter	Symbol	LC3564CM, CT-70U		Unit
		-70		
		min	max	
Write cycle time	t _{WC}	200		ns
Address setup time	t _{AS}	0		ns
Write pulse width	t _{WP}	140		ns
$\overline{\text{CE1}}$ setup time	t _{CW1}	150		ns
CE2 setup time	t _{CW2}	0		ns
Write recovery time	t _{WR}	0		ns
$\overline{\text{CE1}}$ write recovery time	t _{WR1}	0		ns
CE2 write recovery time	t _{WR2}	130		ns
Data setup time	t _{DS}	0		ns
Data hold time	t _{DH}	0		ns
$\overline{\text{CE1}}$ data hold time	t _{DH1}	0		ns
CE2 data hold time	t _{DH2}	10		ns
$\overline{\text{WE}}$ output enable time	t _{WOE}			ns
$\overline{\text{WE}}$ output disable time	t _{WOD}		60	ns

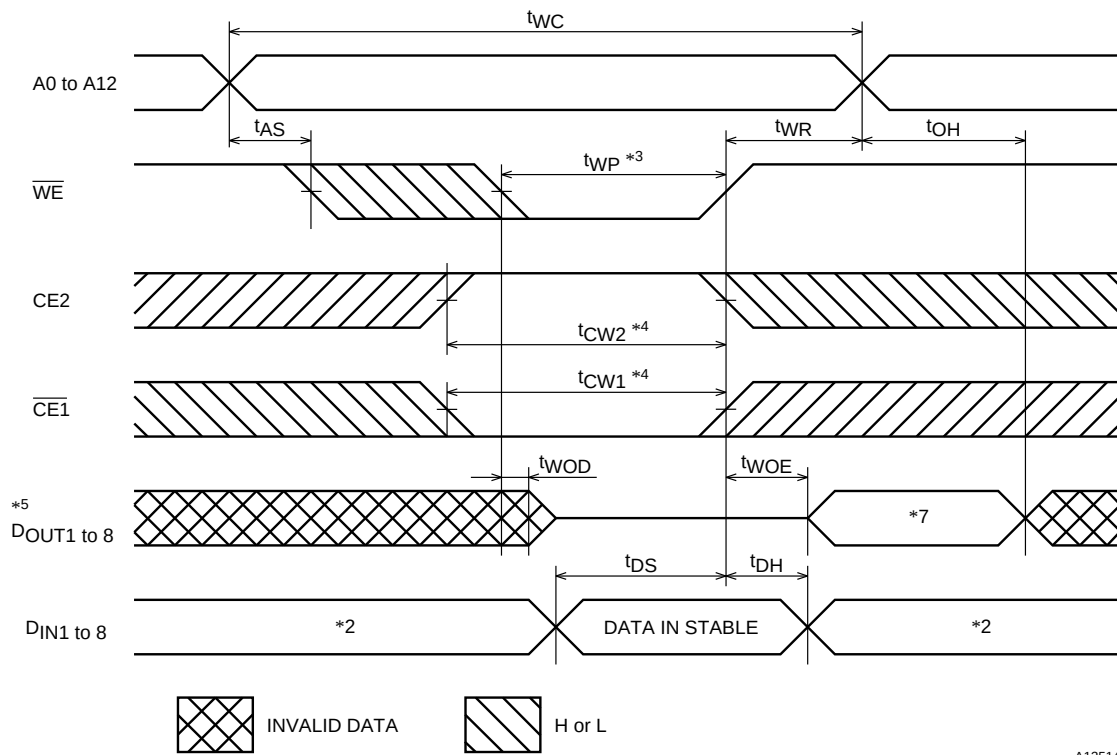
Timing Charts

Read Cycle *1



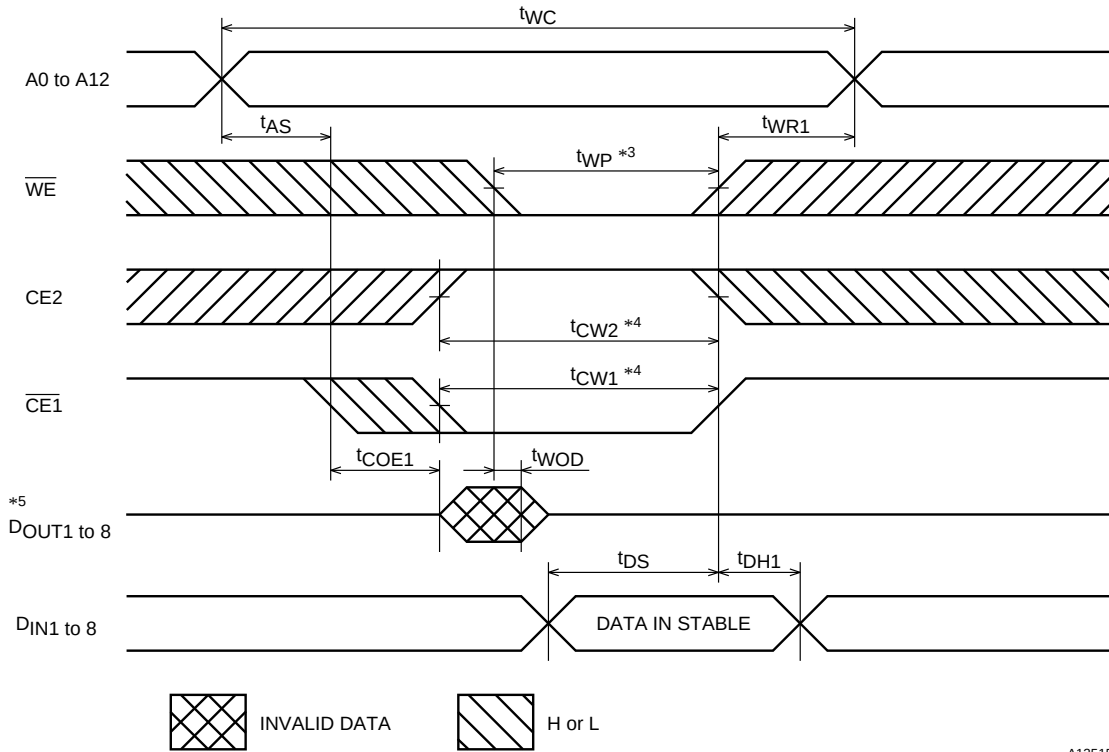
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Write Cycle (1): WE Write *6



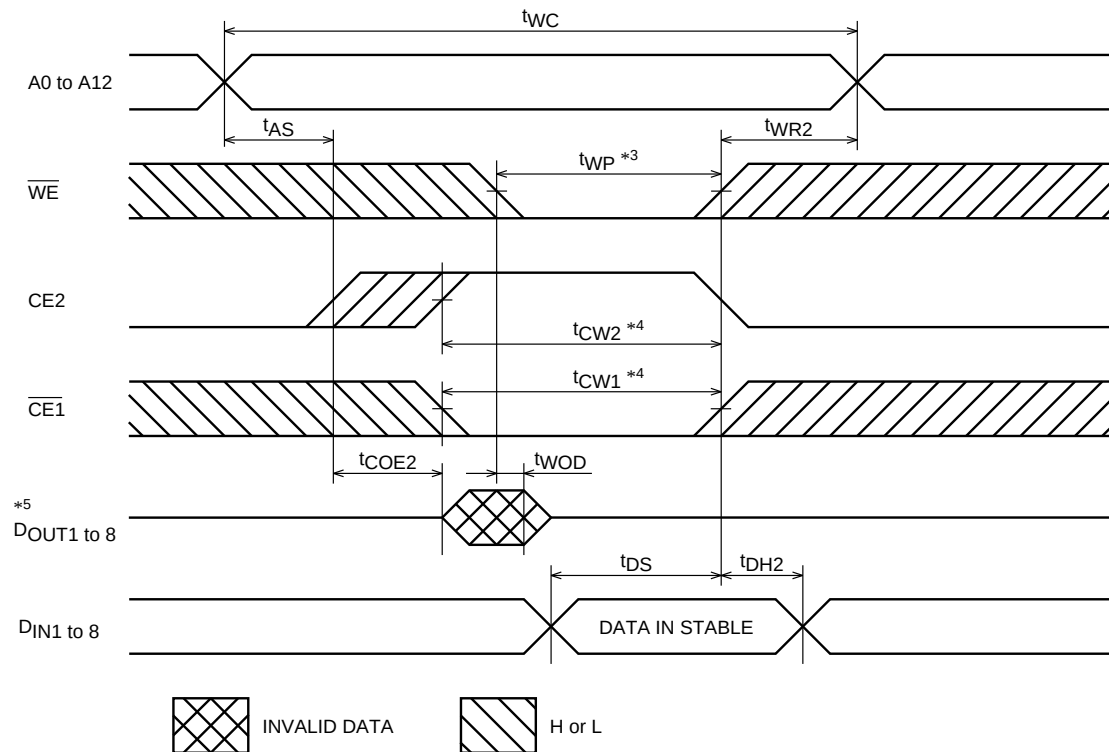
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Write Cycle (2): $\overline{\text{CE1}}$ Write *6



A13515

Write Cycle (3): CE2 Write *6



A13516

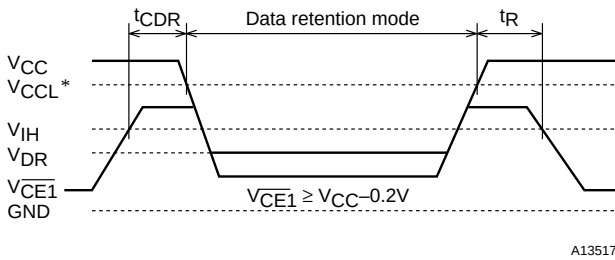
- Notes:
1. Hold $\overline{\text{WE}}$ high during the read cycle.
 2. Applications must not apply reverse phase signals to the D_{OUT} pins when those pins are in the output state.
 3. The time t_{WP} is the period when $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are low and CE2 is high, and is defined as the time from the fall of $\overline{\text{WE}}$ until either $\overline{\text{CE1}}$ or $\overline{\text{WE}}$ rises, or CE2 falls, whichever occurs first.
 4. The times t_{CW1} and t_{CW2} are periods when $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are low and CE2 is high. They are defined as the times from the fall of $\overline{\text{CE1}}$ or the rise of CE2 to the rise of $\overline{\text{CE1}}$ and $\overline{\text{WE}}$, or the fall of CE2 , whichever occurs first.
 5. The D_{OUT} pins will be in the high-impedance state if either $\overline{\text{OE}}$ is high, $\overline{\text{CE1}}$ is high, CE2 is low, or $\overline{\text{WE}}$ is low.
 6. $\overline{\text{OE}}$ must be held either at V_{IH} or V_{IL} during the write cycle.
 7. The D_{OUT} pins have the same phase as the write cycle write data.

Data Retention Characteristics at $T_a = -40$ to $+85^\circ\text{C}$

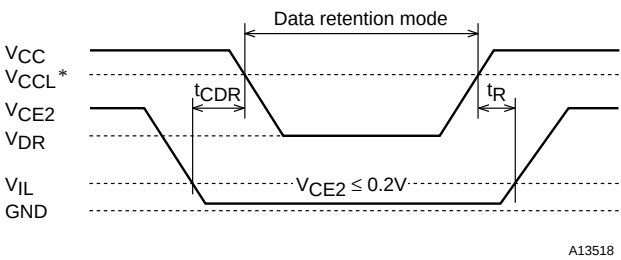
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Data retention supply voltage	V_{DR}	$V_{CE2} \leq 0.2\text{ V}$ or $V_{CE1} \geq V_{CC} - 0.2\text{ V}$, $V_{CE2} \geq V_{CC} - 0.2\text{ V}$	2.0		5.5	μA
Data retention supply current	I_{CCDR}	$V_{CC} = 3\text{ V}$, $V_{CE2} \leq 0.2\text{ V}$, or $V_{CE1} \geq V_{CC} - 0.2\text{ V}$, $V_{CE2} \geq V_{CC} - 0.2\text{ V}$			0.8	μA
		$T_a \leq 70^\circ\text{C}$ $T_a \leq 85^\circ\text{C}$			2.5	
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		t_{RC}^*			ns

Note *: t_{RC} is the read cycle time.

Data Retention Waveforms (1): $\overline{\text{CE1}}$ Control



Data Retention Waveforms (2): CE2 Control



Note *: In 5-V operation: 4.5 V
In 3-V operation: 2.7 V

Notes on Circuit Design

When actually design a circuit using these devices, take the following points into consideration and design the circuit so that none of the maximum rating items are ever exceeded.

- Variations in the supply voltage
- Variations in the electrical characteristics of components such as semiconductor devices, resistors, and capacitors.
- Ambient temperature
- Variations in input and clock signals
- Possible application of abnormal pulses

Also, these devices must be operated within the ranges stipulated in the allowable operating ranges.

If CMOS IC input pins are left open, intermediate potential input voltages may occur leading to incorrect operation due to through currents or other phenomenon. Applications must handle unused input pins appropriately.

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