ZR33771

PRELIMINARY

VIDEO-RATE 2-D CONVOLVER

FEATURES

- High performance, video-rate 2-D convolver
- Supports up to 45MHz sampling rates
- 9-bit coefficients, 8-bit data
- Symmetric and antisymmetric kernel sizes up to 7x7
- Asymmetric kernel sizes up to 4x4
- 24-bit accumulator, 16-bit output
- Bias, shift and limit post-processing
- Dual on-chip coefficient register banks
- Low power, high-speed CMOS technology
- 100-pin plastic QFP and 84-pin ceramic PGA packages

APPLICATIONS

- Video-Rate Filtering
- Video Scan Rate Conversion
- Image Enhancement
- Bilinear Interpolation for Image Zooming
- Image Filtering
- Adaptive Image Filtering
- Edge Detection
- Edge Enhancement

GENERAL DESCRIPTION

The ZR33771 is a high-performance, video-rate 2-D convolver with post-processing features. The kernel size is variable from 2x2 asymmetric to 7x7 symmetric. The coefficients are represented in 9-bit two's complement notation. The data can be represented in either 8-bit unsigned or 8-bit two's complement notation.

Kernel size and type, data representation and post-processing operations are specified by five 9-bit internal mode registers.

Coefficients are supplied by one of two on-chip register banks. The active register bank can be selected "on the fly".

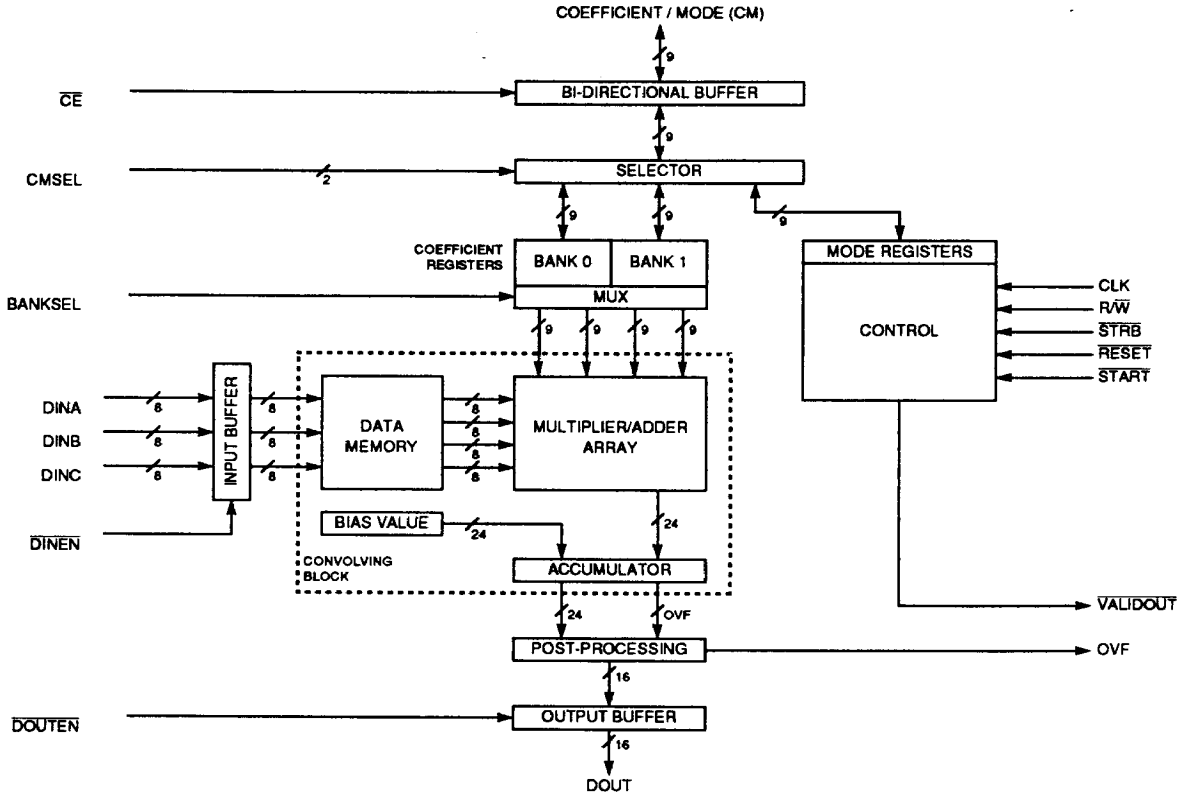


FIGURE 1. ZR33771 BLOCK DIAGRAM

INTERFACE SIGNAL DESCRIPTION

Name	I/O/Z[1]	Function
V_{CC}	I	+5V inputs.
V_{SS}	I	Ground inputs.
CLK	I	System clock input. All timing specifications for DINA, DINB, DINC, DOUT, BANKSEL, OVF, $\overline{START}$, and $\overline{VALIDOUT}$ are referenced to the rising edge of this signal.
R/$\overline{W}$	I	Selects between read and write of the coefficient registers or the mode registers. 0- write, 1- read.
$\overline{RESET}$	I	Reset input. Used to clear the internal data memory, Post Processing block and initialize the accumulator. It does not affect the coefficient or mode registers, DOUT and OVF signals.
$\overline{START}$	I	Starts convolution input. This signal is latched internally. $\overline{RESET}$ clears this latch.
$\overline{CE}$	I	When active, the CM bus is enabled for read/write operations.
DINA[7:0]	I	Data Input bus A.
DINB[7:0]	I	Data Input bus B.
DINC[7:0]	I	Data Input bus C.
DOUT[15:0]	O/Z	Data output bus. Result values are latched at the output and change only when the next valid result is latched.
CM[8:0]	I/O/Z	Bidirectional bus used to sequentially read or write the coefficient and mode registers.
$\overline{DINEN}$	I	Input signal which enables the DIN buses when low. Otherwise, zeros are applied to data memory.
BANKSEL	I	Specifies the coefficient bank to use in the convolution. 0-bank 0, 1-bank 1.
CMSEL[1:0]	I	Specifies the register group to be transferred: 00 - Mode registers 01 - Read/write disabled 10 - Coefficient bank 0 11 - Coefficient bank 1 The register address is reset every time that CMSEL or R/$\overline{W}$ is changed. Consecutive words are then transferred upon each assertion of $\overline{STRB}$. If the mode registers are transferred, and no bias is specified (in the first mode word), the address will recycle after 3 transfers. Otherwise it will recycle after 5 transfers. If coefficient registers are transferred, the address will recycle after the required number of coefficients are transferred, according to kernel size and type specified in the mode registers.
$\overline{STRB}$	I	The external read/write strobe of the CM bus interface. When $\overline{STRB}$ is low, coefficient or mode words are written in by the rising edge of this signal. When $\overline{STRB}$ is high, coefficient and mode register contents are latched at the CM output by the falling edge of this signal. The internal address counter is always incremented by the rising edge of this signal.
$\overline{DOUTEN}$	I	Input signal which enables the DOUT bus when low. Otherwise, the DOUT bus is either in high-impedance state or driven with all zeroes, as specified by the mode registers.
$\overline{VALIDOUT}$	O	Data output bus valid signal. This signal goes low for the duration of the first CLK cycle in which the DOUT result is valid.
OVF	O	Output signal which goes high when overflow is detected by the accumulator or in the 16-bit output. OVF is latched internally and changes only when next valid result is ready in the same way as DOUT.

1. I/O/Z denotes input, output and high impedance signals, respectively.

MODE REGISTER FUNCTIONS

There are five 9-bit mode registers designated M0 to M4. The 9-bit M0 register is written first.

M0[2:0]	Specifies the kernel type (Table 1).
M0[3]	0 - No bias added 1 - Bias added
M0[4]	0 - Truncating 1 - Rounding
M0[5]	0 - No limiting after bias addition 1 - Limiting after bias addition
M0[6]	0 - No limiting on overflow of the 16-bit output 1 - Limiting
M0[7]	0 - No zeroing of the 16-bit output when negative 1 - Zeroing
M1[2:0], M0[8]	Output width: specifies how many bits of the accumulator's 24-bit output, starting with the bit selected by M1[8:5], will appear in the DOUT bus. 1000 - 8 bits, 1001 - 9 bits, ...1111 - 15 bits, 0000 - 16 bits.
M1[3]	Specifies the output bus condition when not enabled by DOUTEN: 0 - Output in high-impedance state 1 - Zero output
M1[4]	Specifies the 8-bit data input representation: 0 - Unsigned 1 - Two's complement
M1[8:5]	Specifies which bit of the 16 least significant bits of the accumulator will be driven to the least significant bit of the output (right shift).
M2[5:0]	Most significant part (6 bits) of the bias value (two's complement representation).
M2[6]	0 - Horizontally antisymmetric kernel 1 - Horizontally symmetric kernel
M2[7]	0 - Vertically antisymmetric kernel 1 - Vertically symmetric kernel
M2[8]	0 (reserved)
M3[8:0]	"Middle" significant part (9 bits) of the bias value.
M4[8:0]	Least significant part (9 bits) of the bias value.

FUNCTIONAL DESCRIPTION

Setup

Before starting the convolution, the mode registers and at least one of the coefficient register banks have to be loaded. The loading is enabled by the $\overline{CE}$ signal. The register group to be loaded is specified by CMSEL. Addressing is automatic: the address counter is reset by changing either the CMSEL or the R/$\overline{W}$ signal. It is then incremented by the rising edge of the $\overline{STRB}$ signal which sequences the writing (or reading) operation. The mode and coefficient registers can be read back to verify contents.

The active coefficient register bank is selected by BANKSEL and can be changed "on the fly" during the convolution.

The $\overline{RESET}$ signal is used to clear all internal registers and pointers to prepare for a new convolution operation. It does not affect the mode and coefficient registers.

The $\overline{START}$ signal is used to initiate continuous convolutions.

Input Data Rate and Sequence

The maximum allowable input (and output) sampling rate is determined by the kernel size and type according to Table 1 for a clock rate of 45 MHz. For slower clocks, the rates will decrease linearly.

M0[2:0]	Kernel Size	Kernel Symmetry	Rate [MHz]
000	2x2	No	45.0
010	3x3	Yes	45.0
001	3x3	No	15.0
110	4x4	Yes	22.5
011	4x4	No	11.25
100	5x5	Yes	15.0
101	6x6	Yes	15.0
111	7x7	Yes	11.25

Note: An antisymmetric kernel is also considered to be symmetric, as are "mixed" types (e.g. horizontal symmetry and vertical antisymmetry), specified by M2[7:6].

Note: The maximum number of unique coefficients needed for any of the kernel types described above is 16.

Table 1. Kernel Size, Type and Rate

The $\overline{\text{VALIDOUT}}$ signal is asserted during the first CLK cycle in which DOUT is valid.

Three 8-bit input buses are used simultaneously. External circuitry is needed to assign the incoming pixel data to one of the buses according to the kernel size and type as shown in Table 2. The pixels are given by their relative line number. (x-Don't care). See Figures 2, 3 and 4 for examples.

The input buffers are enabled by $\overline{\text{DINEN}}$. When $\overline{\text{DINEN}}$ is not active, the input buffer will write zeroes to the data memory at the convolving block input.

kernel	symmetry	clock 1 DINA	clock 1 DINB	clock 1 DINC	clock 2 DINA	clock 2 DINB	clock 2 DINC	clock 3 DINA	clock 3 DINB	clock 3 DINC	clock 4 DINA	clock 4 DINB	clock 4 DINC	pixel period
2x2	NO	0	1	x										1
3x3	YES	0	1	2										1
4x4	YES	0	x	3	1	x	2							2
3x3	NO	x	0	x	x	1	x	x	2	x				3
5x5	YES	0	x	4	1	x	3	x	2	x				3
6x6	YES	0	x	5	1	x	4	2	x	3				3
4x4	NO	x	0	x	x	1	x	x	2	x	x	3	x	4
7x7	YES	0	x	6	1	x	5	2	x	4	x	3	x	4

Table 2. Input Sequence

Convolving Block

The convolution operation itself is performed by an array of multipliers and adders. The convolution result is maintained in a 24-bit accumulator in two's complement representation. The accumulator can be reset to a non-zero value (bias) as specified by M0[3]. The block treats the input data as 8-bit signed or unsigned according to M1[4].

The convolving block also contains data memory to hold previous pixel column data for continuous operation on sequential pixels.

The convolving block implements the following convolution equation:

$$Y_S(m,n) = \sum_{i=0}^{s-1} \sum_{j=0}^{s-1} C(i,j)\, P(m-i, n-j)$$

where s is the kernel size, P(k,l) is the data, C(i,j) is the kernel, m, k are row numbers, i is relative row number, n, l are column numbers and j is relative column number. For symmetric kernels:

$$C(i,j) = C(s-1-i,j) = C(i,s-1-j) = C(s-1-i,s-1-j)$$

(For antisymmetric kernels, the effective sign of the coefficient will change according to whether horizontal and/or vertical antisymmetry has been specified). The convolution mask coefficients must be stored in the following order (left first) in the coefficient register bank.

(For symmetric and antisymmetric kernels, only one quarter is loaded.)

2x2NS : C(1,1), C(1,0), C(0,1), C(0,0)

3X3S : C(2,2), C(2,1), C(1,2), C(1,1)

3X3NS : C(2,2), C(2,1), C(2,0), C(1,2), C(1,1), C(1,0), C(0,2), C(0,1), C(0,0)

4X4S : C(3,3), C(3,2), C(2,3), C(2,2).

4X4NS : C(3,3), C(3,2), C(3,1), C(3,0), C(2,3), C(2,2), C(2,1), C(2,0), C(1,3), C(1,2), C(1,1), C(1,0), C(0,3), C(0,2), C(0,1), C(0,0)

5X5S : C(4,4), C(4,3), C(4,2), C(3,4), C(3,3), C(3,2), C(2,4), C(2,3), C(2,2)

6X6S : C(5,5), C(5,4), C(5,3), C(4,5), C(4,4), C(4,3), C(3,5), C(3,4), C(3,3)

7X7S : C(6,6), C(6,5), C(6,4), C(6,3), C(5,6), C(5,5), C(5,4), C(5,3), C(4,6), C(4,5), C(4,4), C(4,3), C(3,6), C(3,5), C(3,4), C(3,3)

The register bank *not* selected by BANKSEL can be loaded with new values while the ZR33771 is performing convolutions. This allows the kernel coefficients to be updated without disturbing a convolution in progress. The new coefficients will be used on the following pixel-period following bank selection (by BANKSEL).

Post-Processing

The final 24-bit result can be modified in the post-processing block by several sequential operations, each one enabled or otherwise specified by the mode registers. See Figure 2.

First limiting: When overflow (positive or negative) is detected by the accumulator, the output can be limited to the largest positive or negative values (2^{23}-1 or -2^{23}), as specified by M0[5].

Shifting: The previous result can be shifted right by up to 15 bits as specified by M1[8:5], with sign extension (arithmetic right shift).

Rounding: The previous result can be rounded by adding the next least significant bit, as specified by M0[4].

Width selection: The number of bits from the previous result that will appear in the 16-bit output, beginning with the least significant, can be selected in the range of 8 to 16, as specified by M1[2:0], M0[8]. If less than 16 bits are selected, the sign (most significant bit selected) will be extended.

Second limiting: If less than 16 bits were selected in the previous operation, and the non-selected bits above the most significant bit selected were not all the same or a sign change occurred, the result can be limited appropriately to the largest positive or negative value as specified by M0[6].

Clipping of negative values: Negative values of the previous result can be forced to zero, as specified by M0[7].

OUTPUT BLOCK

The output is enabled by the $\overline{\text{DOUTEN}}$ signal. When not enabled, the output can be set to a high-impedance state or cleared (zeroed) as specified by M1[3].

Result Latency

The latency in clock cycles from input (on DINA, DINB & DINC) to valid output ($\overline{\text{VALIDOUT}}$ low) is:

Latency (CLK cycles)= 2 x PixelPeriod + 9

where PixelPeriod is defined as the number of CLK cycles required to input one column of data. See Table 2 on page 4 for these values.

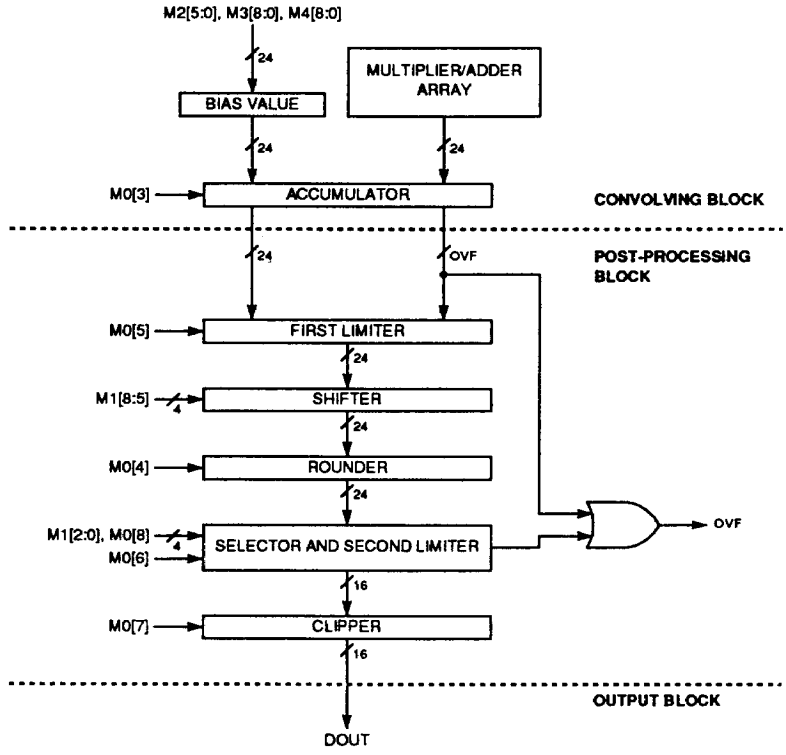


FIGURE 2. POST-PROCESSING BLOCK DIAGRAM

EXAMPLE APPLICATIONS

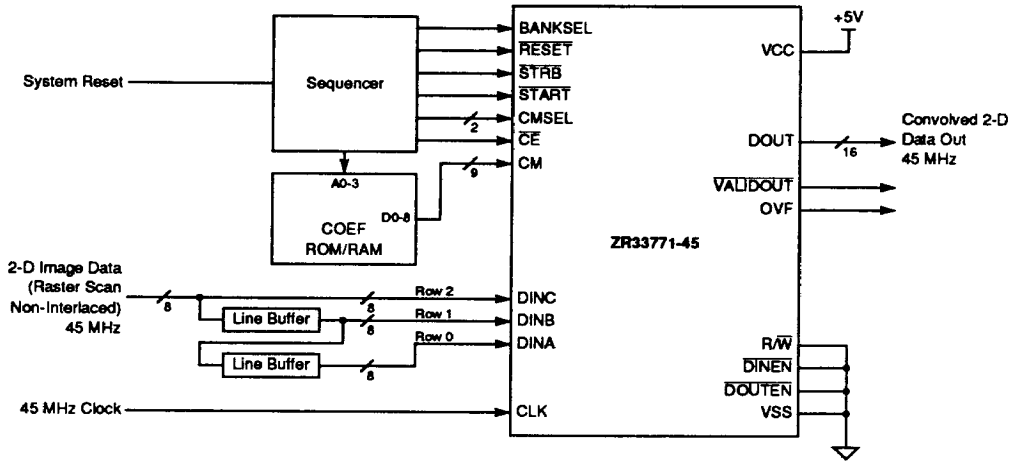


FIGURE 3. 3x3 CONVOLUTION SYMMETRIC (I/O Sampling Rate - 45.0 MHz) USING ONE ZR33771

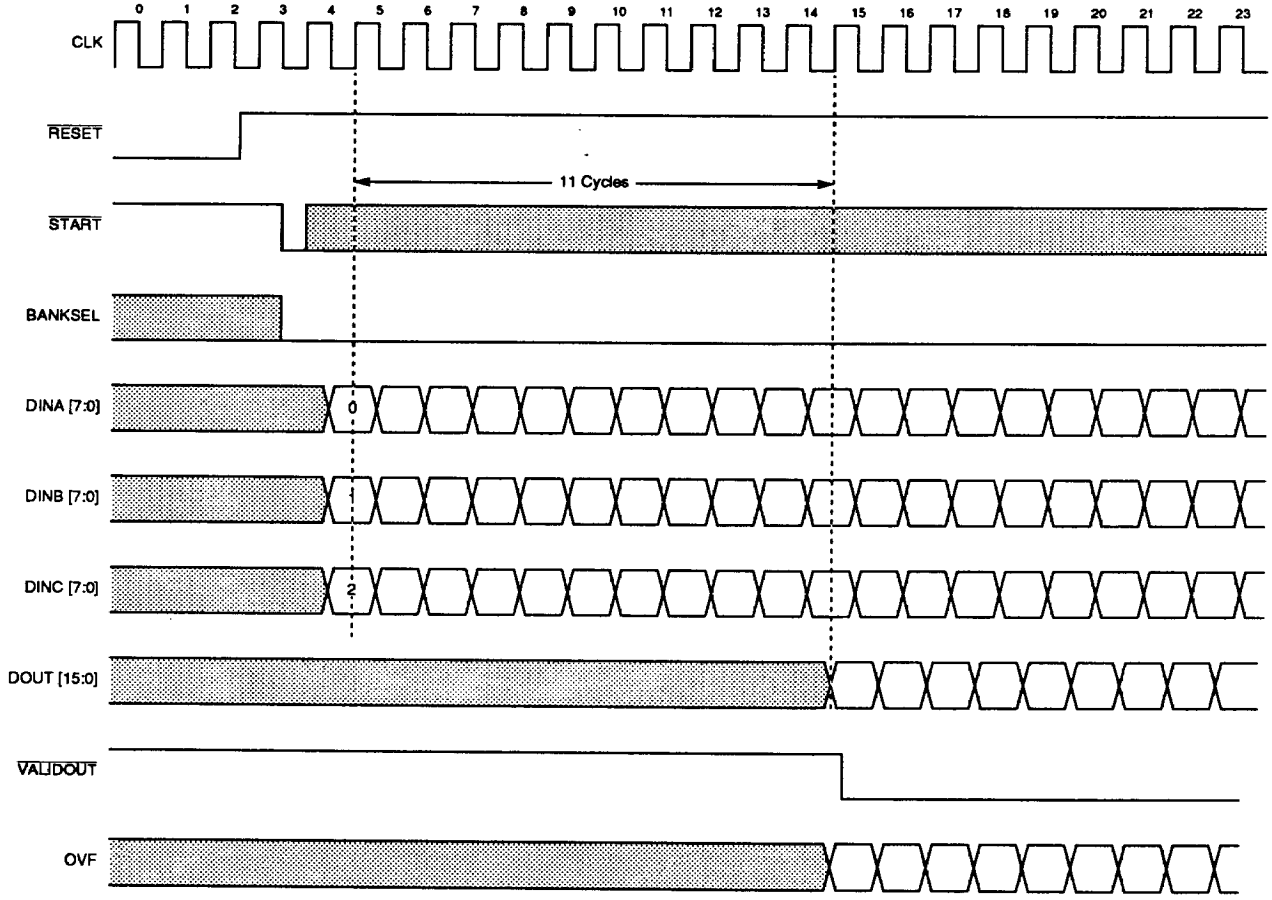


FIGURE 4. 3x3 CONVOLUTION TIMING

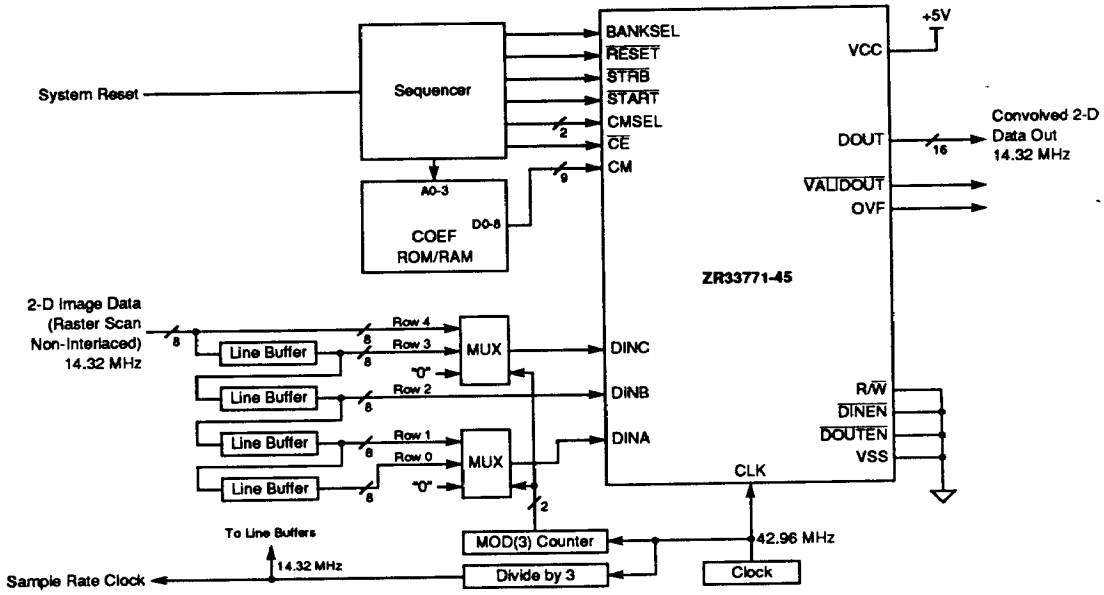


FIGURE 5. 5x5 CONVOLUTION SYMMETRIC (I/O Sampling Rate - 14.32 MHz) USING ONE ZR33771

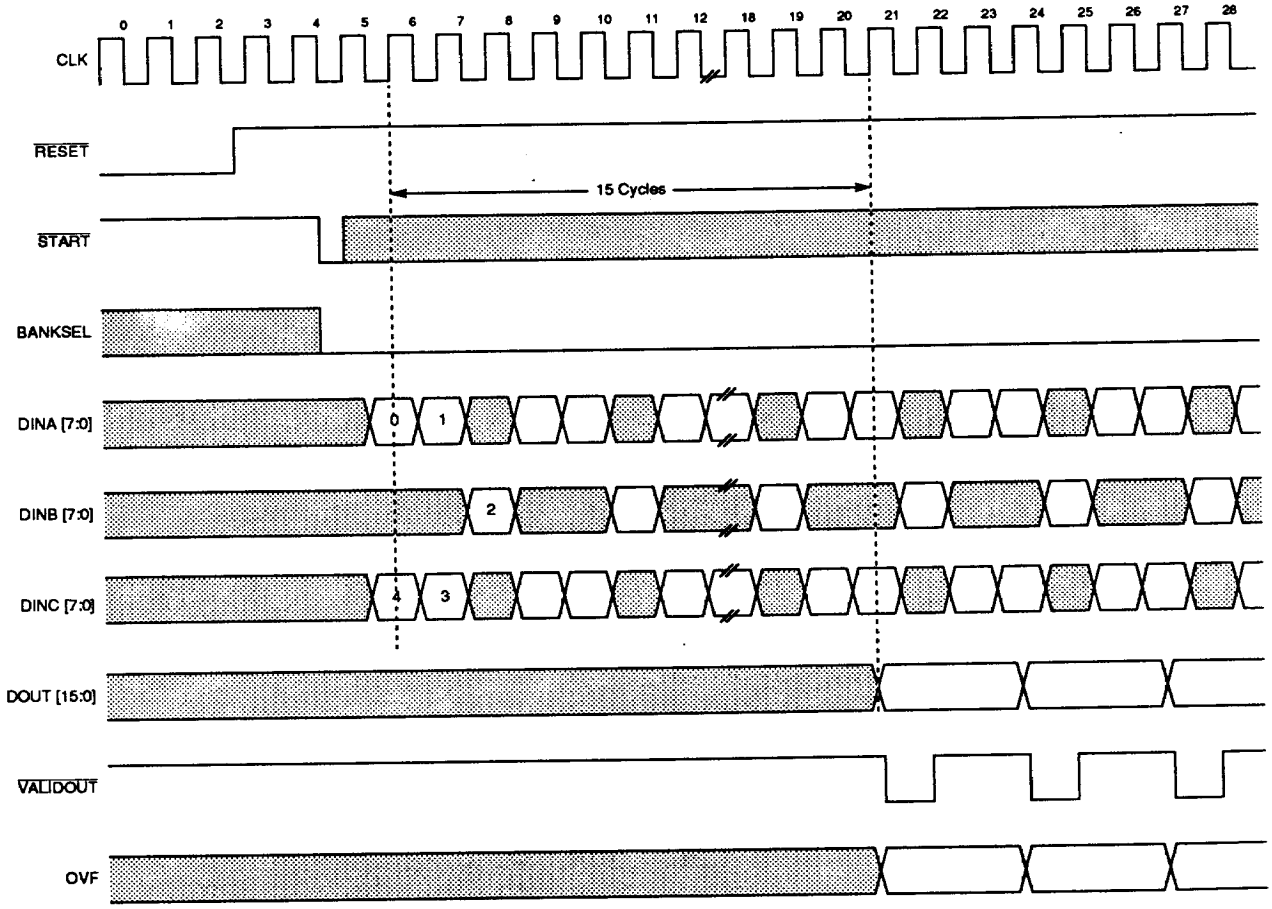


FIGURE 6. 5x5 CONVOLUTION TIMING

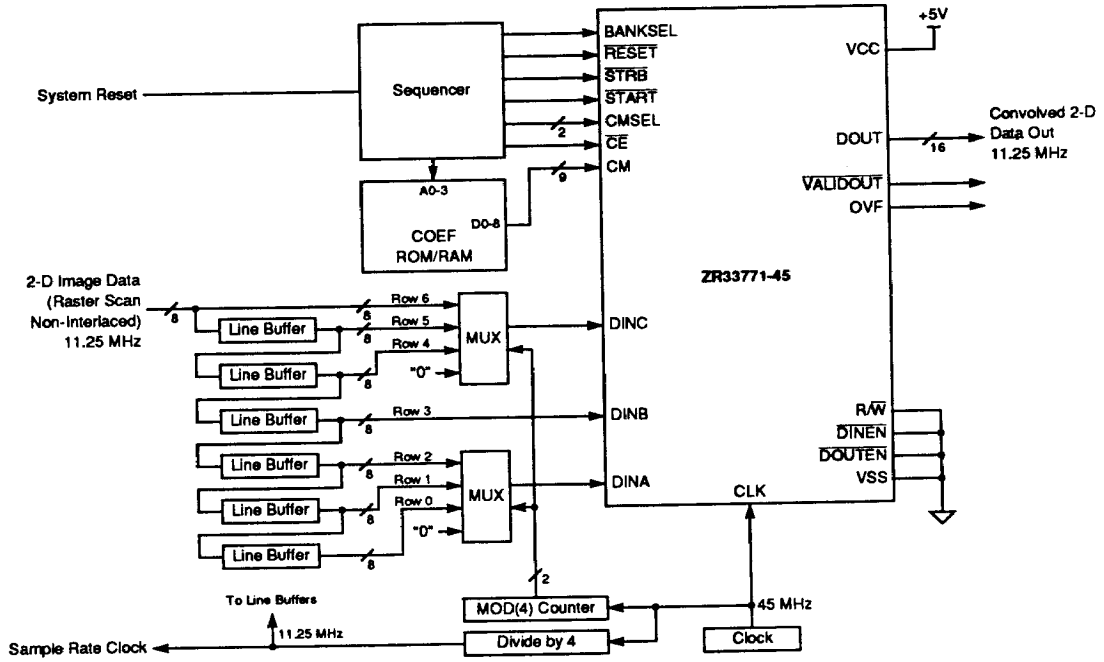


FIGURE 7. 7x7 CONVOLUTION SYMMETRIC (I/O Sampling Rate - 11.25 MHz) USING ONE ZR33771

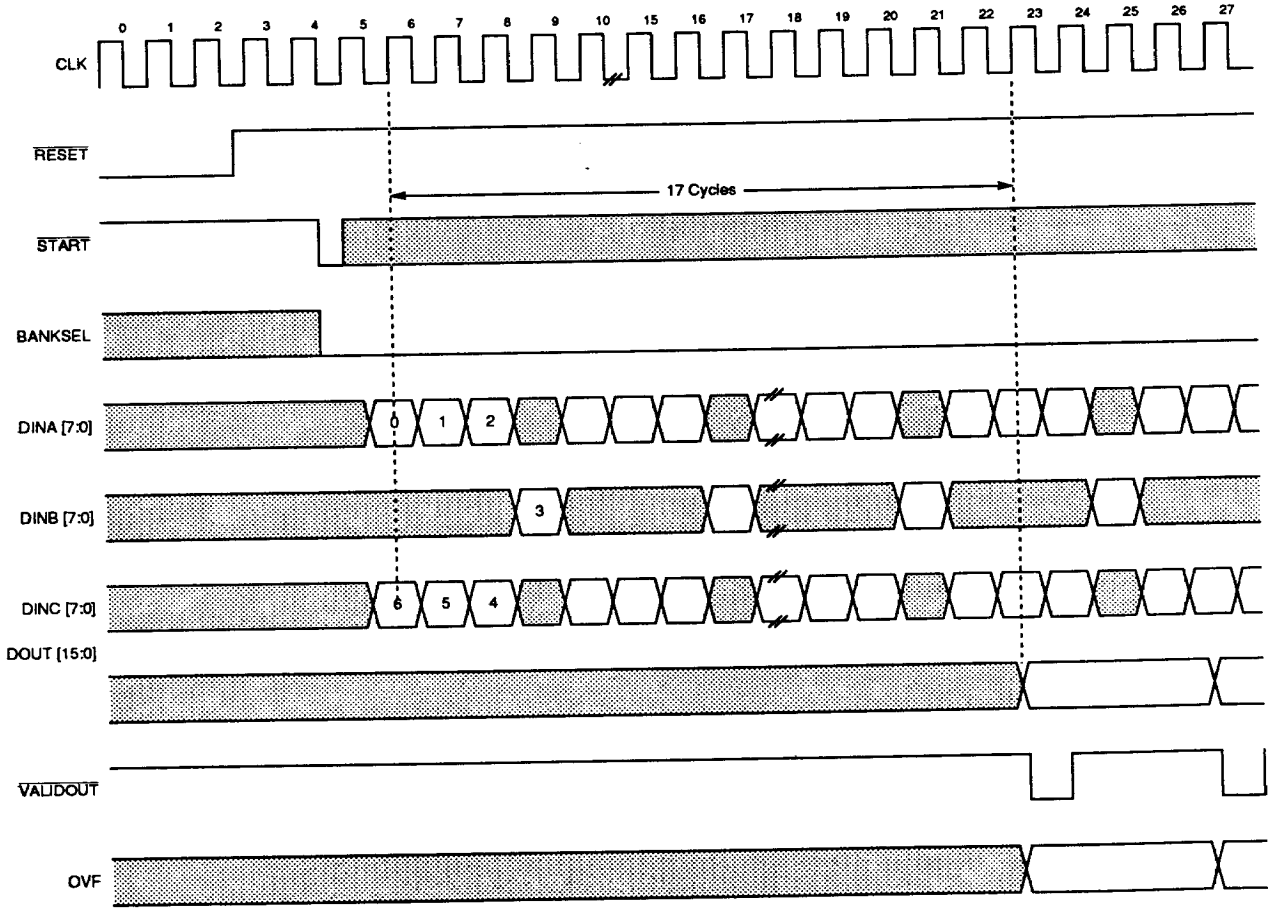


FIGURE 8. 7x7 CONVOLUTION TIMING

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage to Ground Potential Continuous ..... -0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State ..... -0.5V to +5.5V
DC Input Voltage ..... -0.5V to V_{CC}+0.5V
DC Output Current, into Outputs (not to exceed 200mA total) 20mA/output
DC Input Current ..... -10 to +3.0mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGE

Commercial Devices

Temperature ..... $0°C \leq T_A \leq +70°C$
Supply Voltage ..... $4.5V \leq V_{CC} \leq 5.5V$

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA
I_{CC}	Power Supply Current		110	mA	V_{CC}=5.5V, T=0°C @ 45MHz
I_{SC}	Standby Power Supply Current[1]		20	mA	
I_{LI}	Input Leakage Current		±10	µA	0 V < V_{IN} < V_{CC}
I_{LO}	Output Leakage Current		±10	µA	0 V < V_{OUT} < V_{CC}
C_{IN}	Input Capacitance[1]		10	pF	0.1 to 100MHz
C_{IO}	I/O, Clock and Output Capacitance[1]		10	pF	0.1 to 100MHz

1. Not tested in production. Guaranteed by characterization.

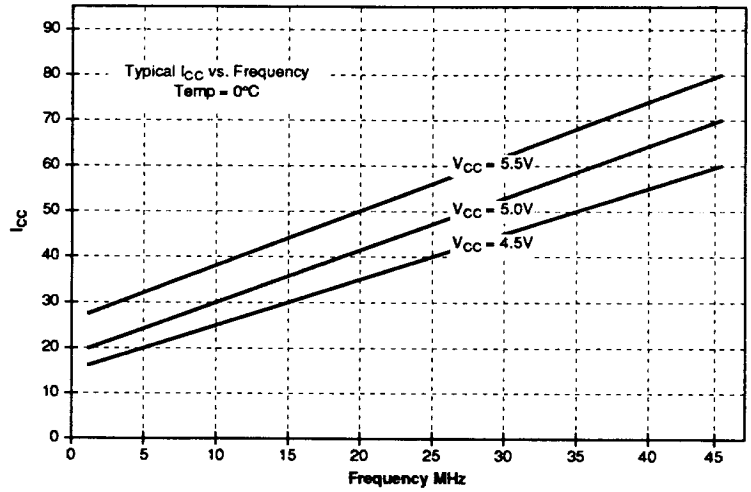


FIGURE 9. TYPICAL I_{CC} VS FREQUENCY

AC CHARACTERISTICS

Symbol	Parameter	ZR33771-45		Units	Test Conditions
		Min	Max		
t_{cp}	CLK Period	22.5	500[1]	ns	
t_{ch}	CLK High	9		ns	2.0V
t_{cl}	CLK Low	9		ns	0.8V
t_{cr}	CLK Rise		5	ns	0.8V to 2.0V
t_{cf}	CLK Fall		5	ns	2.0V to 0.8V
t_{rw}	$\overline{\text{RESET}}$ Width Low	3 t_{cp}		ns	
t_{cih}	Input Hold	3		ns	
t_{cis}	Input Setup	8		ns	
t_{cod}	CLK to Output Delay		16	ns	
t_{coh}	Output Hold[2]	3		ns	
t_{oe}	Output Enable Delay		16	ns	
t_{dis}	Output Disable Delay[2]		16	ns	
t_{sp}	$\overline{\text{STRB}}$ Period[3]	100	1000	ns	
t_{sh}	$\overline{\text{STRB}}$ High	45		ns	2.0V
t_{sl}	$\overline{\text{STRB}}$ Low	45		ns	0.8V
t_{sr}	$\overline{\text{STRB}}$ Rise		5	ns	0.8V to 2.0V
t_{sf}	$\overline{\text{STRB}}$ Fall		5	ns	2.0V to 0.8V
t_{sch}	CMSEL, $\overline{\text{CE}}$ and R/$\overline{\text{W}}$ Input Hold	0		ns	From falling edge of $\overline{\text{STRB}}$
t_{scs}	CMSEL, $\overline{\text{CE}}$ and R/$\overline{\text{W}}$ Input Setup	12		ns	From falling edge of $\overline{\text{STRB}}$
t_{sih}	CM Input Hold	0		ns	From rising edge of $\overline{\text{STRB}}$
t_{sis}	CM Input Setup	10		ns	From rising edge of $\overline{\text{STRB}}$
t_{sod}	$\overline{\text{STRB}}$ to CM Output Delay		50	ns	From falling edge of $\overline{\text{STRB}}$

1. CLK may be stopped without affecting the coefficient or mode register contents. However, internal data memory contents will be lost.
2. Not tested in production. Guaranteed by characterization.
3. This parameter is externally driven and independent of CLK.

AC TESTING

A.C. testing, inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Input and output timing measurements are made a t 1.5V for both logic "1" and "0".

FIGURE 10. AC TESTING INPUT, OUTPUT

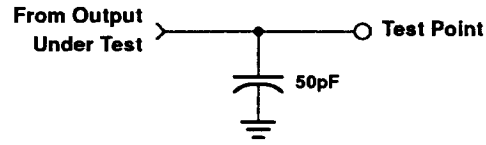


FIGURE 11. NORMAL AC TEST LOAD

AC TIMING DIAGRAMS

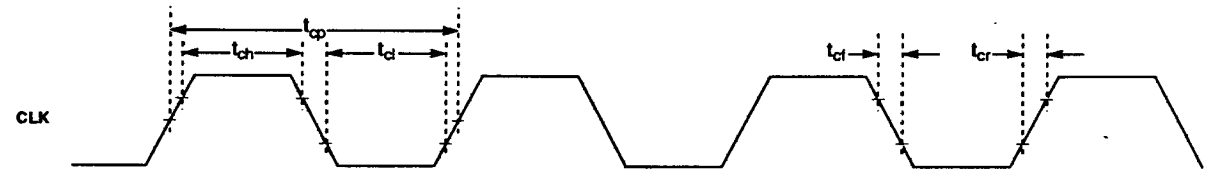
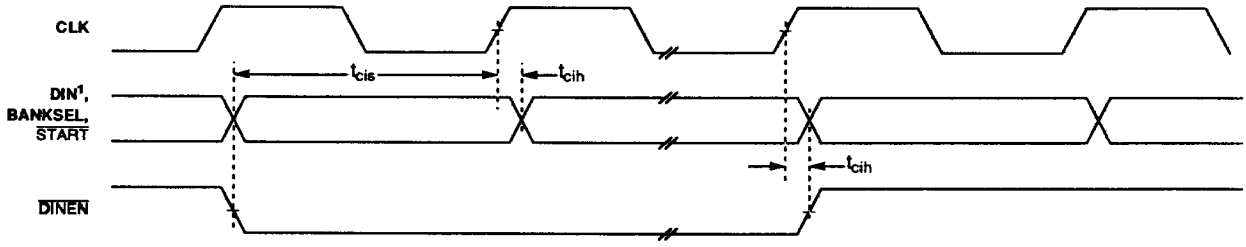
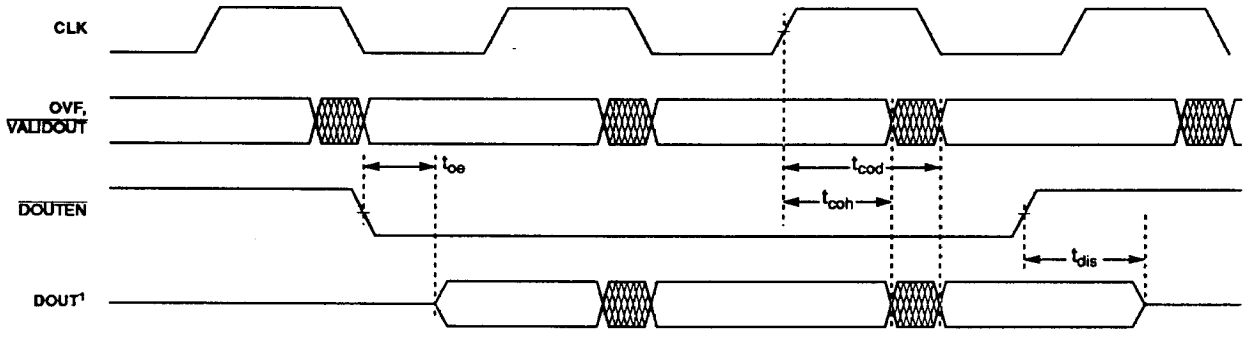


FIGURE 12. CLOCK AC CHARACTERISTICS



1. DIN refers to any of the DINA, DINB or DINC inputs

FIGURE 13. INPUT SETUP AND HOLD



1. DOUT can driven to high impedance or zeroed, depending on M1[3].

FIGURE 14. OUTPUT DELAY

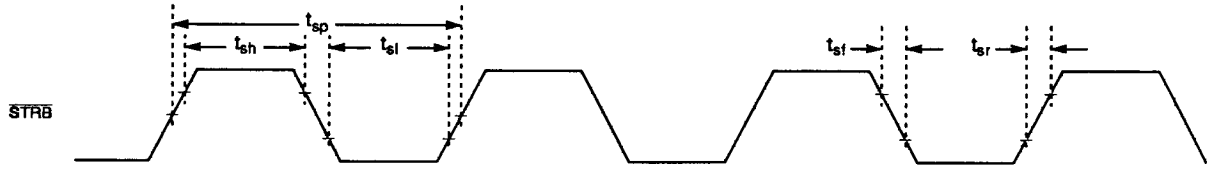


FIGURE 15. $\overline{\text{STRB}}$ AC CHARACTERISTICS

AC TIMING DIAGRAMS (Continued)

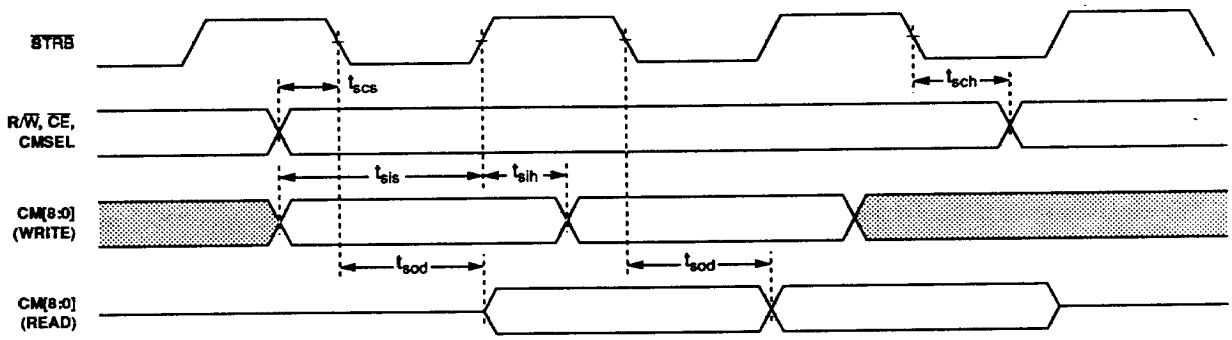


FIGURE 16. COEFFICIENT/MODE REGISTERS WRITE SETUP AND HOLD AND READ DELAY

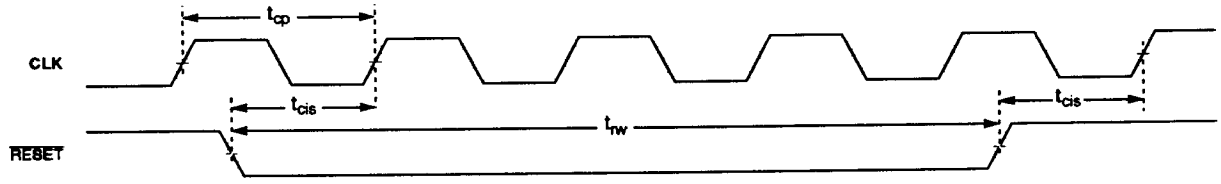


FIGURE 17. RESET & WIDTH TIMING

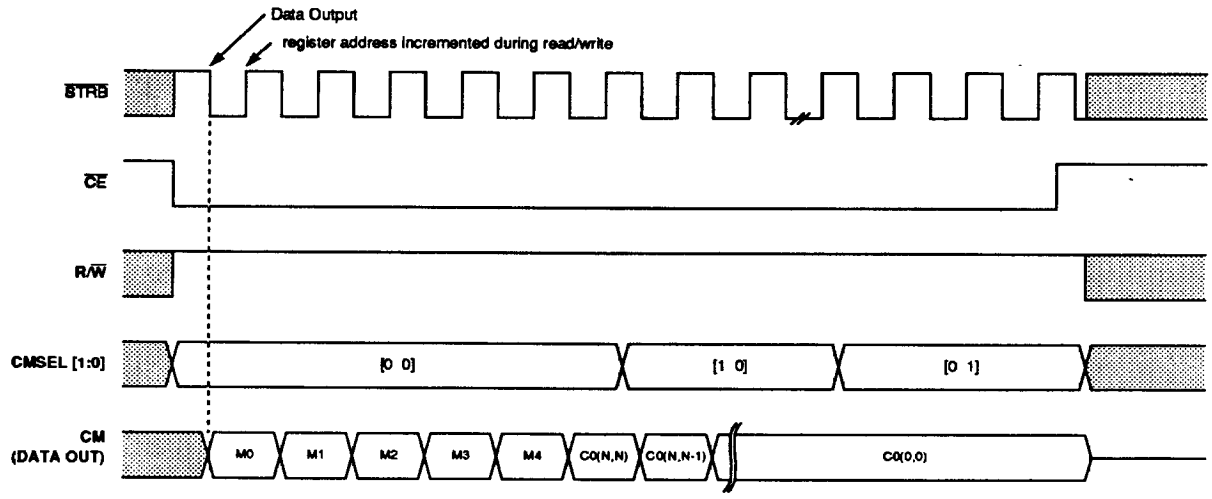


FIGURE 18. COEF/MODE REGISTERS READ OPERATION

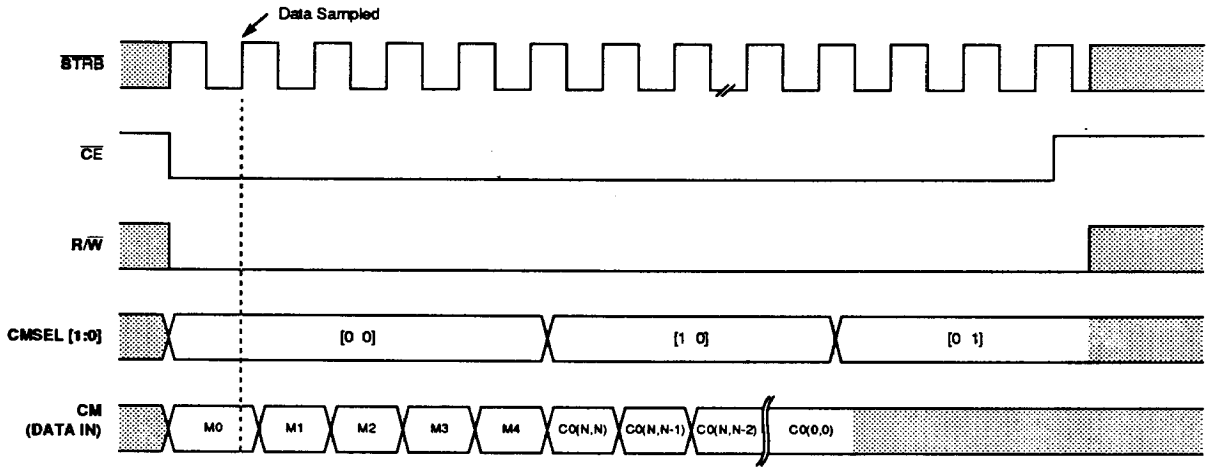


FIGURE 19. COEF/MODE REGISTERS WRITE OPERATION

NOTES:

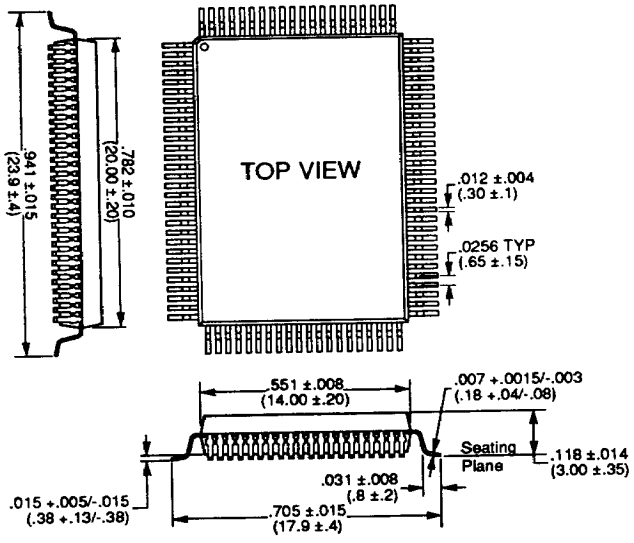
1. If no bias is specified (M0[3]=0), then register address will recycle after 3 writes/reads: M0, M1, M2, M0, M1, M2,..., otherwise, if M0[3]=1, address recycles after 5 writes/reads: M0, M1, M2, M3, M4, M0, M1, M2,....
2. Number of coefficients written/read depends on kernel size and symmetry setting (bits M0[2:0] in Mode Registers). See ZR33771 datasheet for Mode Settings (page 3, Table 1) and Coefficient storage order (page 4).
3. Register and coefficient addressing reset whenever R/$\overline{W}$ and/or CMSEL change. Addressing recycles, otherwise. (See note 1).

PACKAGE INFORMATION (Continued)

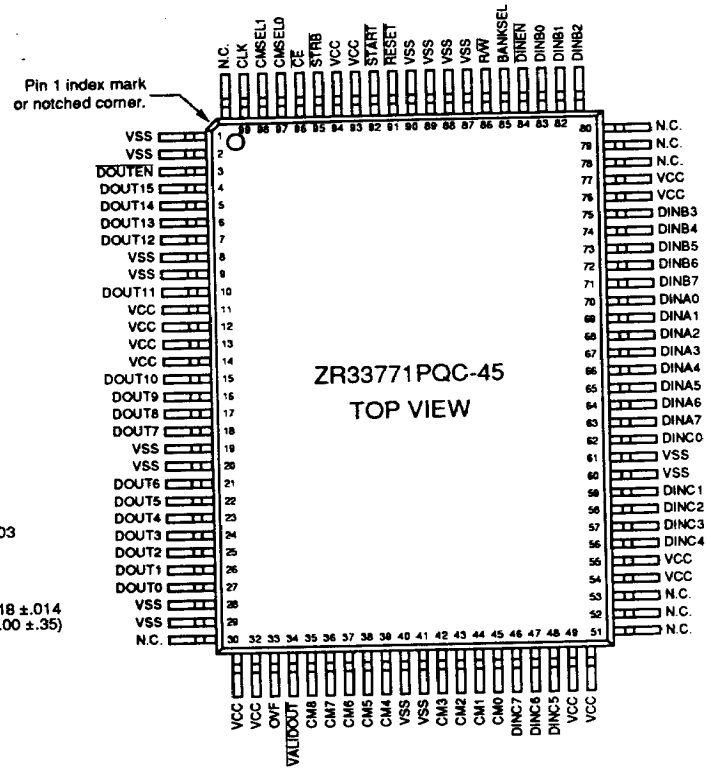
100-Pin Flat Pack Pin Assignment[1]

Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type
1	VSS	I	26	DOUT1	O/Z	51	N.C.	-	76	VCC	I
2	VSS	I	27	DOUT0	O/Z	52	N.C.	-	77	VCC	I
3	$\overline{\text{DOUTEN}}$	I	28	VSS	I	53	N.C.	-	78	N.C.	-
4	DOUT15	O/Z	29	VSS	I	54	VCC	I	79	N.C.	-
5	DOUT14	O/Z	30	N.C.	-	55	VCC	I	80	N.C.	-
6	DOUT13	O/Z	31	VCC	I	56	DINC4	I	81	DINB2	I
7	DOUT12	O/Z	32	VCC	I	57	DINC3	I	82	DINB1	I
8	VSS	I	33	$\overline{\text{OVF}}$	O	58	DINC2	I	83	$\overline{\text{DINB0}}$	I
9	VSS	I	34	$\overline{\text{VALIDOUT}}$	O	59	DINC1	I	84	$\overline{\text{DINEN}}$	I
10	DOUT11	O/Z	35	CM8	I/O/Z	60	VSS	I	85	BANKSEL	I
11	VCC	I	36	CM7	I/O/Z	61	VSS	I	86	R/$\overline{\text{W}}$	I
12	VCC	I	37	CM6	I/O/Z	62	DINC0	I	87	VSS	I
13	VCC	I	38	CM5	I/O/Z	63	DINA7	I	88	VSS	I
14	VCC	I	39	CM4	I/O/Z	64	DINA6	I	89	VSS	I
15	DOUT10	O/Z	40	VSS	I	65	DINA5	I	90	VSS	I
16	DOUT9	O/Z	41	VSS	I	66	DINA4	I	91	$\overline{\text{RESET}}$	I
17	DOUT8	O/Z	42	CM3	I/O/Z	67	DINA3	I	92	$\overline{\text{START}}$	I
18	DOUT7	O/Z	43	CM2	I/O/Z	68	DINA2	I	93	VCC	I
19	VSS	I	44	CM1	I/O/Z	69	DINA1	I	94	VCC	I
20	VSS	I	45	CM0	I/O/Z	70	DINA0	I	95	$\overline{\text{STRB}}$	I
21	DOUT6	O/Z	46	DINC7	I	71	DINB7	I	96	$\overline{\text{CE}}$	I
22	DOUT5	O/Z	47	DINC6	I	72	DINB6	I	97	CMSEL0	I
23	DOUT4	O/Z	48	DINC5	I	73	DINB5	I	98	CMSEL1	I
24	DOUT3	O/Z	49	VCC	I	74	DINB4	I	99	CLK	I
25	DOUT2	O/Z	50	VCC	I	75	DINB3	I	100	N.C.	-

1. I/O/Z denotes input, output and high impedance signals, respectively; N.C. = No Connect.



NOTE: Principal dimensions in inches, dimensions in brackets in mm.



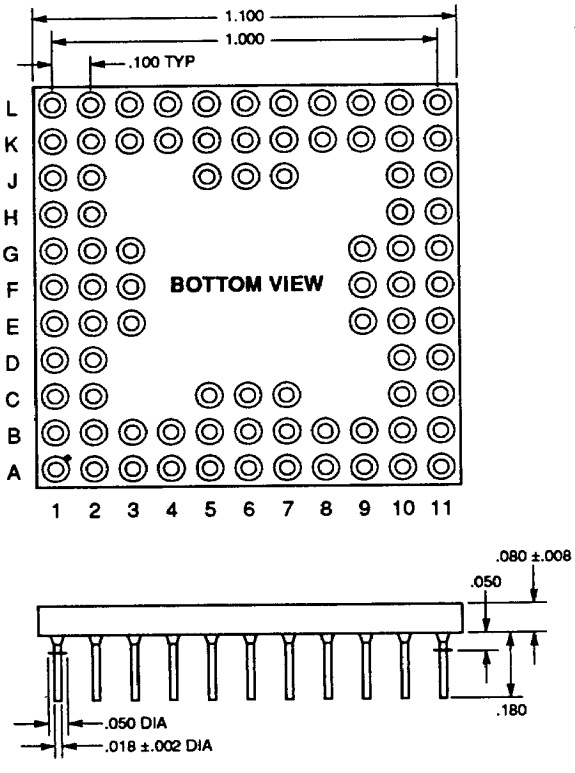
ZR33771 100-PIN PLASTIC QUAD FLAT PACK (EIAJ)

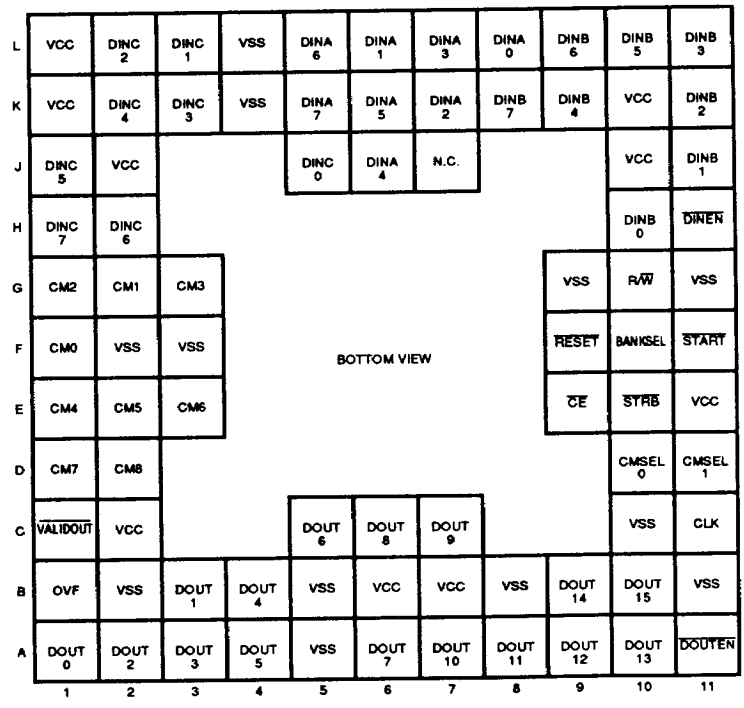
PACKAGE INFORMATION

84-Pin PGA Assignment[1]

Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type
E9	$\overline{CE}$	I	L7	DINA3	I	A1	DOUT0	O/Z	B6	VCC	I
C11	CLK	I	J6	DINA4	I	B3	DOUT1	O/Z	B7	VCC	I
F1	CM0	I/O/Z	K6	DINA5	I	A2	DOUT2	O/Z	C2	VCC	I
G2	CM1	I/O/Z	L5	DINA6	I	A3	DOUT3	O/Z	E11	VCC	I
G1	CM2	I/O/Z	K5	DINA7	I	A4	DOUT5	O/Z	J2	VCC	I
G3	CM3	I/O/Z	H10	DINB0	I	B4	DOUT4	O/Z	J10	VCC	I
E1	CM4	I/O/Z	J11	DINB1	I	C5	DOUT6	O/Z	K1	VCC	I
E2	CM5	I/O/Z	K11	DINB2	I	A6	DOUT7	O/Z	K10	VCC	I
E3	CM6	I/O/Z	L11	DINB3	I	C6	DOUT8	O/Z	L1	VCC	I
D1	CM7	I/O/Z	K9	DINB4	I	C7	DOUT9	O/Z	A5	VSS	I
D2	CM8	I/O/Z	L10	DINB5	I	A7	DOUT10	O/Z	B2	VSS	I
D10	CMSEL0	I	L9	DINB6	I	A8	DOUT11	O/Z	B5	VSS	I
D11	CMSEL1	I	K8	DINB7	I	A9	DOUT12	O/Z	B8	VSS	I
H11	$\overline{DINEN}$	I	J5	DINC0	I	A10	DOUT13	O/Z	C10	VSS	I
A11	$\overline{DOUTEN}$	I	L3	DINC1	I	B9	DOUT14	O/Z	F2	VSS	I
F10	BANKSEL	I	L2	DINC2	I	B10	DOUT15	O/Z	F3	VSS	I
J7	N.C.	-	K3	DINC3	I	G10	R/$\overline{W}$	I	G9	VSS	I
B1	OVF	O	K2	DINC4	I	F9	$\overline{RESET}$	I	G11	VSS	I
L8	DINA0	I	J1	DINC5	I	E10	$\overline{STRB}$	I	K4	VSS	I
L6	DINA1	I	H2	DINC6	I	F11	$\overline{START}$	I	L4	VSS	I
K7	DINA2	I	H1	DINC7	I	C1	$\overline{VALIDOUT}$	O			

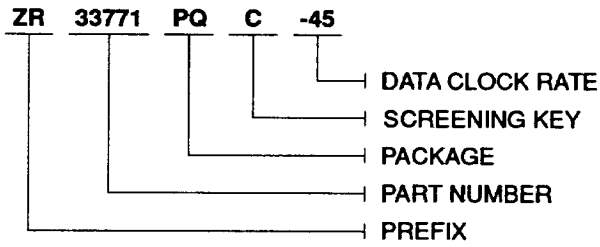
1. I/O/Z denotes input, output and high impedance signals, respectively; N.C. = No Connect.





ZR33771 84-TERMINAL PIN GRID ARRAY (PGA)

ORDERING INFORMATION



PACKAGE
PQ - Plastic Quad Flat Pack (EIAJ)
G - Pin Grid Array

DATA CLOCK RATE
45.0 MHz

SCREENING KEY
C - 0°C to +70°C (V_{CC} = 4.5V to 5.5V)

SALES OFFICES

■ ***U.S. Headquarters***
Zoran Corporation
1705 Wyatt Drive
Santa Clara, CA 95054 USA
Telephone: 408-986-1314
FAX: 408-986-1240

■ ***Israel Design Center***
Zoran Microelectronics, Ltd.
Advanced Technology Center
P.O. Box 2495
Haifa, 31024 Israel
Telephone: 972-4-551-551
FAX: 972-4-551-550

■ ***Japan Operations***
Zoran Corporation
1-5-3 Ebisu Kogetsu Bldg.
4th Floor
Shibuya-Ku, Tokyo Japan
Telephone: 81-3-3448-1980
FAX: 81-3-3448-1690