1.0 INTRODUCTION

The WD8110/LV System Controllers are designed to provide a high performance, single chip, system controller supporting all 80486SX, 80486DX, 80386SX and 80386DX CPUs in AT bus based Desktop/Laptop/Notebook/Pen-based systems.

1.1 DOCUMENT SCOPE

This document describes the function and operation of the WD8110/LV System Controller devices. It includes the description of external logic necessary for efficient use of these devices. The WD8110/LV is also referred to in this document as the System Controller.

1.2 FEATURES

- Interfaces with 80486SX, 80486SXLP, 80486DX, 80386SX and 80386DX CPUs.
- Operates at up to 33 MHz at 3.3 volts or 5 volts with the 80486SX/DX.
- Operates at up to 33 MHz with the 80386SX/DX:
- Supports single and double clock 80486SX/DX and Intel SL Enhanced processors.

DRAM control:

- Page Mode word interleaved, DRAM controller with support for 80486 burst mode.
- Supports 3-2-2-2 clock sequence, 9 CLKs with 16-byte line fill for a page hit DRAM read cycle at 33 MHz.
- Optional 3-1-1-1 clock sequence, 6 CLKs with 16-byte line fill for static column mode DRAMs at CPU speeds of 16 MHz and 20 MHz.
- Zero Wait State writes at 16 MHz and 20 MHz to DRAMs for 80486SX/DX.
- One Wait State writes to DRAMs for 80386SX/DX.
- One Wait State reads from DRAMs for Page Hit access for 80386SX/DX.
- Supports memory in five DRAM banks for a maximum of 256 Mbytes, using 256 Kbit, 1 Mbit, 4 Mbit and 16 Mbit DRAMs and special DRAMs such as 512K by 9, 1M by 18 and 2M by 9.
- Supports major DRAM standards, including Asymmetrical DRAMs, Static Column DRAMs and 88-pin DRAM cards.
- Self-adjusting output drivers minimize output rise/fall time variations and reduce EMI and ground noise.
- DRAM address multiplexer capable of driving 450 pF with adjustable strength drivers.
- Features CAS before RAS refresh and slow refresh for low power.
- Supports slow refresh and self refresh DRAMs at 120 µs.
- I/O pin mapping for board testability
- 32-bit direct interface with internal parity generation and checking with no DRAM data buffers required.

Power Management:

- Low power 0.9 micron CMOS technology.
- Provides power control with suspend and resume mode operations.
- 3 volt suspend to hard disk and Hibernation.
- Sleep Mode provides:
  - Stop clock for static CPU for power saving.
  - Processor power down.
- Provides automatic processor clock switching for 80386.
- Automatic CPU speedup (AutoFast).
  - Clock Scaling
  - Clock Throttling
- Supports multiple CPU speeds.
- Supports System Management Interrupt (SMI) for efficient power management.
- Provides peripheral and I/O power control with trapping on I/O address ranges for SMI operations.
- Supports a fully programmable 16-bit decode.
- Provides System Activity Monitor (SAM) for power management.

- Stop DMA clock.
- 3.3V low voltage operation with on-chip translators for 5 volt AT bus (split rail operation).
- 3 volt and 5 volt mixed mode.

Chip Set Features:

- High speed DMA.
- Three fully programmable chip selects with PMC timers.
- Built in Immunizer™ for virus protection.
- Connects directly to the AT Data Bus SD(15:00).
- Supports a Video Local Bus Interface (VLBI) for a 32-bit Video Graphic Array (VGA) interface.
- Bank switched BIOS ROM up to 512 KB.

1.3 WD8110/LV POWER MANAGEMENT

Power Management Control (PMC) is used for powering down the processor or peripherals and includes processor stop clock, slow clock, automatic processor clock speed switching modes and CAS before RAS slow refresh. Suspend and resume is supported and low power DRAM is refreshed while the processor and other power consuming devices are turned off. The power drain for the core logic and VGA controller is less than 2 mA in this mode. Power and clock speed may be controlled by the Keyboard Controller, transparently to the 80386 or 80486.

The System Activity Monitor (SAM) is a transparent feature that replaces the functions previously performed by software. It senses when the system has been idle for a previously programmed period of time and determines a clean break point in which to perform power down activities such as suspend.

The system controller also supports System Management Interrupt (SMI) with complete I/O trapping of up to six separate I/O ranges. Each range has an independent timer which can generate an SMI after a programmed period of time during which there was no I/O access to that range.

1.3.1 Desktop Applications

The WD8110/LV provides a high performance solution with a flexible memory controller architecture, including support for five banks of memory. The WD8110/LV can fully support an external look-aside cache or a combination primary and secondary cache. This feature makes it particularly suitable for use with cached microprocessors where it maintains cache coherency via its built-in bus snooping capability. In addition, the WD8110/LV supports Video Local Bus Interface (VLBI) for enhanced graphics performance.

The built-in power management features of the WD8110/LV allows a high performance yet power efficient desk top solution.

1.3.2 Portable Applications

The WD8110LV is an ideal choice because of its advanced power management features and power saving 3.3 volt operation, which delivers long battery life in a compact footprint. This makes it a perfect choice for laptop, notebook, pen-based and palmtop computers.

The five bank memory controller on the WD8110LV provides the user with great flexibility in the selection of 3.3 volt DRAMs to meet system memory requirements in low voltage platforms. The WD8110LV memory controller supports JEDEC standard 3.3 volt DRAM in various configurations, including the JEIDA standard 88-pin DRAM card.

The WD8110/LV can be paired with the appropriate support devices from Western Digital to deliver the most efficient solution for any platform. For 5 volt desktop or portable platforms, the WD8110/LV can be used with the WD76C20 Peripheral Controller and the WD76C30 I/O Controller. The WD8110 may also be used with the WD7615 Buffer Manager device and a generic Super I/O chip to implement a low cost desktop platform. For 3.3 volt applications, the WD8110LV can be used with the WD76C20ALV and WD76C30ALV, both of which incorporate level translators (split rail operation). For subnotebook and palmtop type applications, WD7625LV buffer manager and WD8120LV Super I/O can be added to the WD8110LV based solution to achieve a very compact footprint.

The WD8110/LV is a fifth generation system controller device derived from core chips with proven compatibility and design maturity in several of the industry's leading desktop and portable platforms. Designed with the state of the art 0.9 micron high performance CMOS process, the WD8110/LV family maintains architectural compatibility with Western Digital's WD7600 and WD7855 systems logic chip sets while incorporating many additional performance enhancements.

1.3.3 WD8110/LV Power Management

With its built-in advanced power management features, the WD8110/LV delivers the lowest system power consumption and longest battery life in portable systems. The following information summarizes the key power management features offered by the WD8110/LV architecture.

1.3.3.1 Automatic CPU Speedup (AutoFast)

Depending on system activity, CPU speed automatically adjusts for slow speed when there is no activity and automatic speedup when activity is detected.

1.3.3.2 CPU Sleep and Power-Down

The processor can be dynamically powered down during the idle periods (e.g. between keystrokes) and restored when any unmasked interrupt occurs. In case of a static processor, the CPU is simply operated at zero hertz during idle periods. This feature does not require SMI.

1.3.3.3 Suspend and Resume Mode

Suspend is triggered either by one of several user-defined events or a programmable timeout. During suspend, the system is shut down except for the WD8110/LV, system memory, video memory and the video controller chip. These devices are sustained by a very slow clock until the WD8110/LV detects either the appropriate resume conditions or a modem ring indicator and the power is restored.

1.3.3.4 Peripheral Power Control

All peripherals are powered down during Idle periods or Suspend conditions. The WD8110 features eight user-definable and eight dedicated outputs to control the LCD panel, backlight, keyboard controller, power supply and other user-selected functions. The power consumption of disk drives can be controlled by way of the drive's built-in power modes. I/O ports are managed through software control.

1.3.3.5 System Activity Monitor

The system activity monitor watches all hardware inputs and allows detection of idle conditions in the system following a programmable period of system inactivity.

1.3.3.6 System Management Interrupt (SMI) Support

Supports the high-level System Management Interrupt and I/O Trapping for flexible and fully transparent Power Management.

1.3.3.7 Hibernation Support

All registers within the WD8110/LV are readable including 8254 compatible timers, 8259 compatible interrupt controllers and 8237 DMA controllers. This allows for the entire system state to be easily stored to a file on the hard disk drive to allow complete system power-off and transparent restore.

1.3.3.8 Slow Refresh

Slow 120 µs refresh is an option in both runtime and suspend mode.

1.3.3.9 DMA Stop Clock

DMA clock automatically stops when there is no DMA activity and automatically restarts on any unmasked DMA request.

1.4 ORDERING INFORMATION

Part Number	Description
WD8110ZZ A6	5 volt 33 MHz operation
WD8110LVZZ A6	3.3/5 volt 25 MHz operation
WD8110LVZZ33 A6	3.3/5 volt 33 MHz operation

NOTE: A6 = Shipment in dry packed trays - 24 parts per tray.

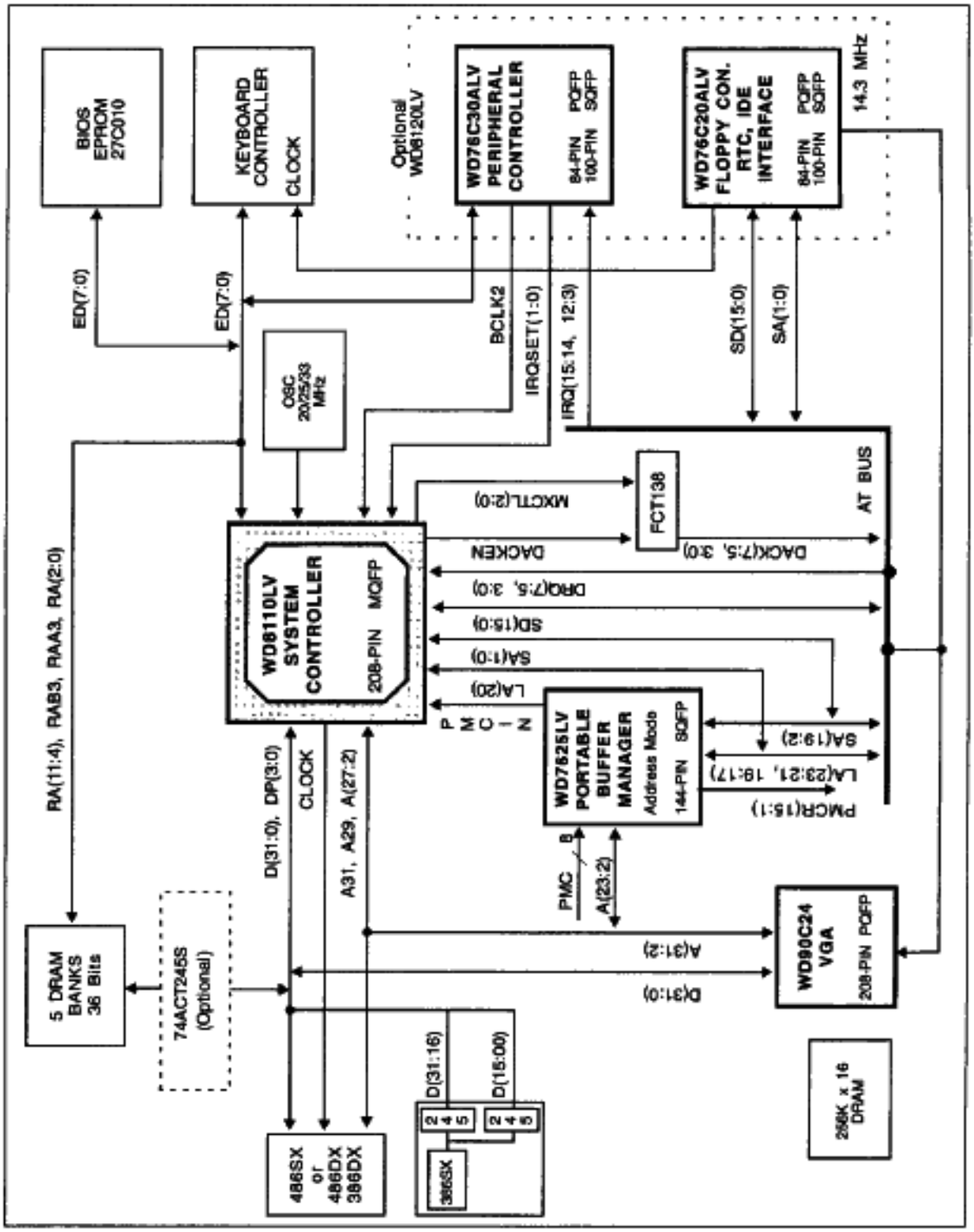


FIGURE 1-1. WD8110LV LOW VOLTAGE SYSTEM BLOCK DIAGRAM

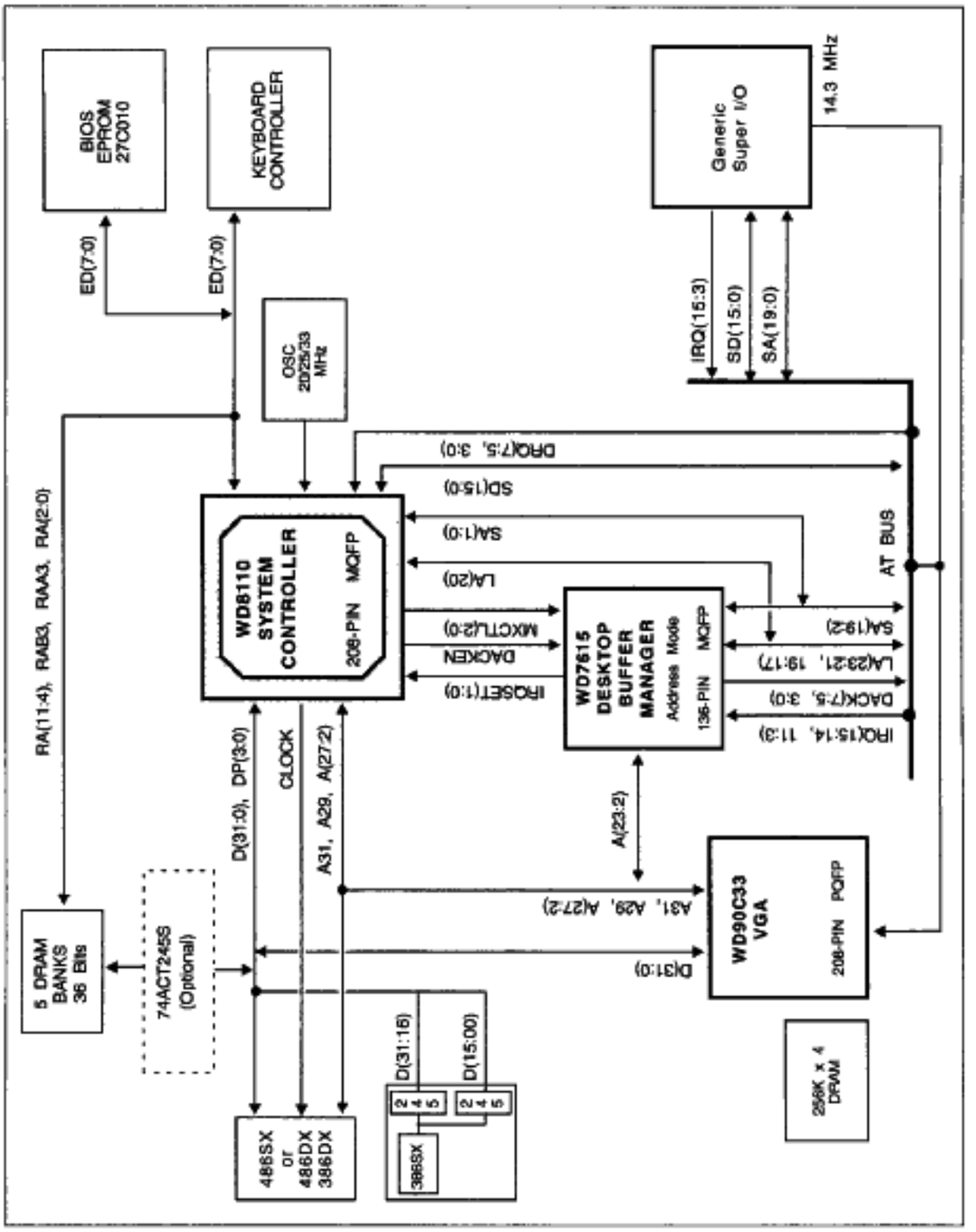


FIGURE 1-2. WD8110 DESKTOP SYSTEM BLOCK DIAGRAM

2.0 ARCHITECTURE

Both versions of the System Controller are composed of nine major blocks:

- Initialization and clocking
- AT bus
- 80486SX/DX 80386SX/DX and local bus interface
- Data bus
- DRAM Memory control
- Power Management Control (LV System Controllers only)
- Register File
- Video Local Bus Interface (VLBI) control

Sections 2.1 through 2.8 provide an overview of these blocks and are described in more detail in Sections 4 through 11.

2.1 INITIALIZATION AND CLOCKING

At power up, the System Controller receives RSTIN which is used to reset the AT bus and assert CPURES to reset the CPU. CPURES is held for 1 ms beyond the removal of RSTIN.

During Power-On-Reset, all configuration strap options are sampled. Refer to Section 4.0 for a more detailed description of the strapping and clock options.

2.1.1 CPU Mode Selection

During Power-On-Reset:

If MODE486 is sampled high, the 80486SX/DX CPU mode is selected. In this mode SXM is ignored.

If MODE486 is low and SXM sampled high, the 80386DX mode is selected.

If MODE486 and SXM are sampled low, the 80386SX mode is selected.

2.1.2 Clocking

CLK14 is a 14.318 MHz clock for the 8254 compatible timers and is switched to 32 KHz by the WD76C20ALV during a suspend operation and from 32 KHz to 14.318 MHz during a resume operation.

BCLK2 is an input used to generate either an 8 or 10 MHz bus clock (SYSCLK), or during certain low power modes, the main processor clock (CPUCLK).

CPUCLK is the processor clock and may be derived from OSCIN or BCLK2.

SYSCLK is the system clock and is used to drive the AT Bus. SYSCLK may be derived from CPUCLK or BCLK2.

2.2 AT BUS

The AT bus provides the logic necessary to control the system clock, memory read and write access, I/O read and write cycles, data bus direction, data and interrupt requests and speaker driver.

2.3 80486SX/DX 80386SX/DX AND LOCAL BUS INTERFACE

This block enables the CPU to interface with the Local bus. A31, A29 and A(27:2) are connected directly to the 80486SX/DX. For AT Bus Master and DMA cycles, this block forces A31, A29 and A(27:24) low for invalidation of the cache internal to the 80486SX/DX. A30 and A28 are forced low during invalidation by external pulldown resistors. The CPU bus interface logic within the System Controller monitors 80486SX/DX bus cycles and controls the 32-bit DRAM interface and internal AT bus controller logic. If LDS32 is asserted before T2 by a 32-bit local bus device such as a video controller or WEITEK4167, then the System Controller waits for the local device to generate RDYIN to complete the cycle. For all other cycles, the System Controller completes the cycle by returning either BRDY486 or RDY486.

In 80386DX Mode the System Controller always returns RDY486 and does not perform any burst cycles.

In 80386SX Mode the System Controller converts SXA1, SXBHE and SXBLE to internal BE(3:0) and generates control signals SXLOWEN and

$\overline{\text{SXSWPEN}}$ for 32-bit to 16-bit data path on the CPU board.

2.4 DATA BUS

The Data Bus is a 32-bit (four bytes) bidirectional bus that connects to the processor's System Controller and 32-bit DRAM.

2.5 DRAM MEMORY CONTROL

This block controls the access of up to 256 Mbytes of DRAM in five banks. All versions of the System Controller support Page Mode word interleaved DRAM control with support for 486 Burst Mode.

2.6 POWER MANAGEMENT CONTROL

The Power Management Control (PMC) is internal logic which interfaces with external multiplexers and latches. It has the ability to power down the main processor only or the main processor and peripherals, conserving power essential to portable notebook/laptop computers. When in a power down state, the WD8110LV tristates the CPUCLK, $\overline{\text{RDY486}}$, $\overline{\text{BRDY486}}$, HOLDR, INTRQ and NMI output signals to the main processor. Also contained within this functional block are the SMI and SAM logic.

2.7 REGISTER FILE

The register file provides software control of the interface signals. The function of each register is described in the same section as the logic block which it controls. Some registers, such as the Bus Timing and Power Down Control Register at Port 1872H, serve more than one area. In this instance, the register description appears only in one section but is referred to in all appropriate sections.

The registers and the section in which they are described, are listed in Table 2-1.

In most cases, the registers are addressed by all 16 address bits, A15 through A00. When the address is expressed as a three digit number within the text, i.e., 092H - ALT A20 GATE and HOT RESET, only address bits A09 through A00 are used while A15 through A10 are ignored. If the address is expressed as a four digit number, all 16 address bits are used.

With the exception of the Port 70H Shadow Register at E472H, all registers located at Ports 1072H through FC72H are locked and inaccessible until unlocked by performing an eight bit I/O write of DA to the Lock/Unlock Register at Port F073H. Writing anything other than DA locks the registers. The lock/unlock status can be determined by reading the Lock/Unlock Status Register at Port FC72H twice. If the T bit (bit 15) toggles, the registers are unlocked. If the registers are locked, the read cycle is directed to the AT bus and the data is undetermined.

The Extended Setup Facility (ESF) provides a means of programming the memory control I/O registers in the System Controller. The ESF register address is written to Ports 74H and 75H. The data addressed by these ports can be accessed from data Port 700H.

Port 74H bits 7:0 = LSB of the ESF address.
Port 75H bits 7:0 = MSB of the ESF address.
Port 700H = data port for ESF.

Optionally the ESF address can be written to Port 4872H, and ESF data may be accessed at Port 5072H.

All ESF I/O ports are accessed as 8-bit ports. All System Controller I/O ports are within ESF:190H through 1A5H and 1ACH through 1AFH. All other ESF addresses are reserved for future use.

2.7.1 Lock Status Register

Port Address FC72H – Read only

Bits 11:03 are particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

15	14	13	12	11	10	09	08
T	Not Used			DMA#2 CH3	CH2	CH1	CH0

07	06	05	04	03	02	01	00
DMA#1 CH3	CH2	CH1	CH0	P	Not Used		

Signal Name	Default At RSTIN
All signals	None

Bit 15 - T, Toggle

Changes state after every read of this port.

Bits 14:12 - Not used, state is ignored

Bits 11:08 - DMA #2, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #2. For a description of the Mask Registers, refer to Section 5.4.11.

1 = Channel enabled

0 = Channel disabled

Bits 07:04 - DMA #1, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #1. For a description of the Mask Registers, refer to Section 5.4.11.

1 = Channel enabled

0 = Channel disabled

Bit 03 - P, Parallel Port Direction

The P bit represents the state of the Direction Bit (bit 5) of the parallel port Write Control Register. For a description of this bit, refer to the WD76C30 Data Book, Section 4.3.

Bits 02:00 - Not used, state is ignored

2.7.2 Lock/Unlock Register

Port Address F073H – Write only

15	14	13	12	11	10	09	08
Not Used							

07	06	05	04	03	02	01	00
L/UL							

Signal Name	Default At RSTIN
All signals	None

Bits 15:08 - Not used, state is ignored

Bits 07:00 - L/UL, Lock/Unlock

L/UL = DA -

11011010 unlocks the registers, allowing read and write access to the registers. Refer to Table 2-1 for the registers capable of being locked.

L/UL ≠ DA -

Anything other than 11011010 locks the registers. Any attempt to access a locked register I/O port address goes to the AT bus rather than the locked register.

2.8 VLBI CONTROL

The Video Local Bus Interface (VLBI) control is internal logic which interfaces with the local bus video controllers. It has the ability to determine whether the current CPU cycle should be processed by the local bus device or the WD8110LV System Controller.

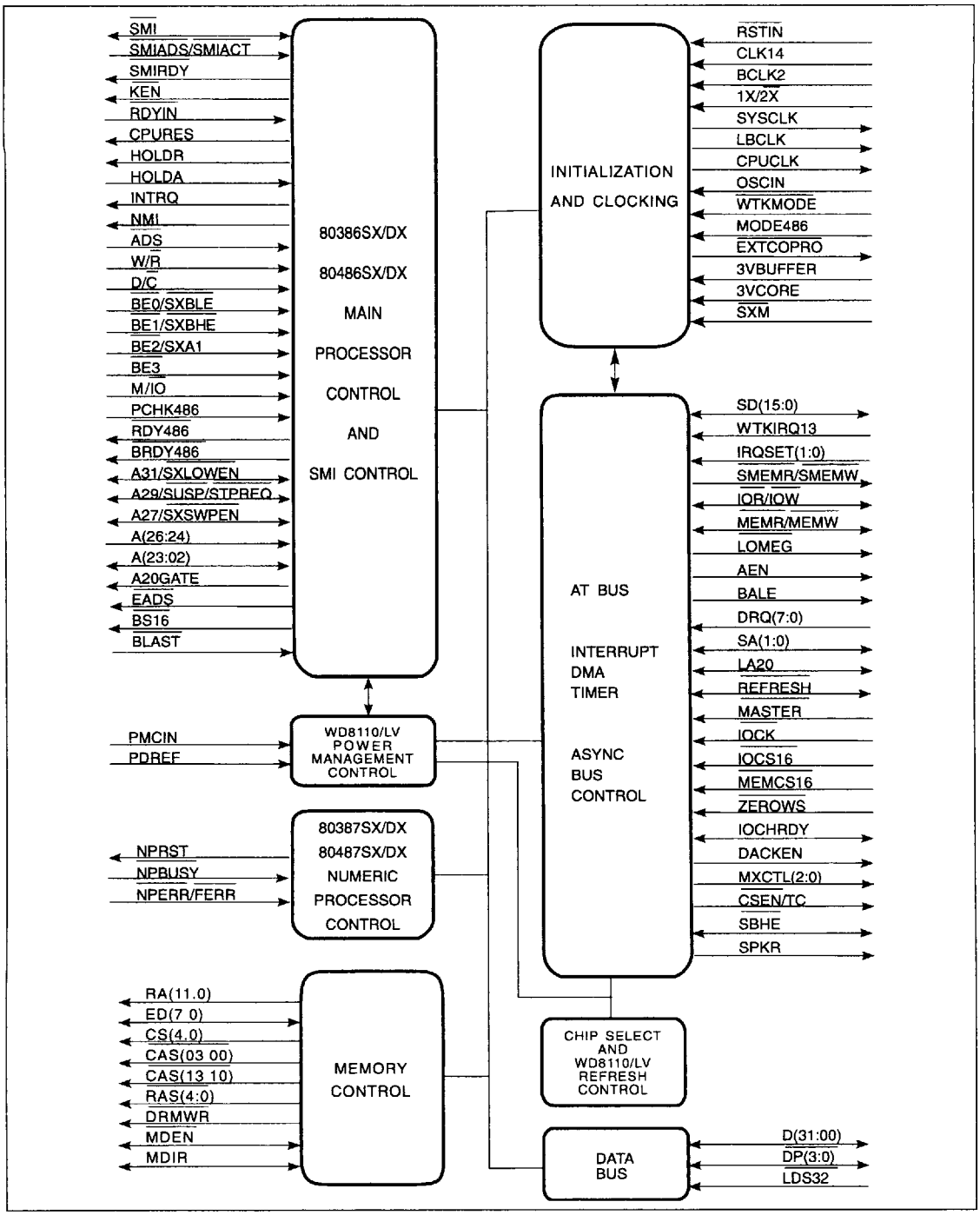


FIGURE 2-1. WD8110/LV BLOCK DIAGRAM

PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
000 - 00F ①	DMA Control #1 (Channel 0:3)	No	5.4, 5.6,
020 - 021 ②	Interrupt Controller #1	No	5.5
040	Timer 0, Time of Day	No	5.6, 5.7
041	Timer 1, Refresh	No	5.6, 5.7
042	Timer 2, Speaker	No	5.6, 5.7
043	Control Word	No	5.6, 5.7
060 - 06E even	Keyboard Controller	No	7.4, Tables 7-1:3
061 - 06F odd	Port B Parity Error and I/O Channel Check	No	5.9
070 - 07E even	Real-Time Clock Address	No	5.8.1
071 - 07F odd	Real-Time Clock Data	No	5.8.2
74	LSB of the ESF address	No	2.7, 6.4
75	MSB of the ESF address	No	2.7, 6.4
080 - 09F	(except 092H) DMA Page	No	5.7, Table 5-8
092	Lock Pass, ALT A20 Gate and Hot Reset	No	5.8.3
0A0 - 0A1 ②	Interrupt Control Slave #2	No	5.4, 5.6
0C0 - 0DE ①	DMA Control #2 (Channel 4:7)	No	5.4
0EC	Busy Bypass Control	No	A.4
0EE	Fast A20 Gate Control	No	A.5
0EF	Fast CPU Reset Control	No	A.6
0F0	Clear NPBUSY	No	5.3.2
0F1	Reset 80387	No	5.3.3
0F9	Disable Privy	No	A.3
0FB	Enable Privy	No	A.2
ESF190	Bank 0:1 Address Mux Control	Yes	6.4.2.1
ESF191	Bank 2:3 Address Mux Control	Yes	6.4.2.2
ESF192	Bank 0 Size Control	Yes	6.4.3.1
ESF193	Split Address Start	Yes	6.4.6
ESF194	Bank 0 Start Address	Yes	6.4.7
ESF195	Bank 1 Start Address	Yes	6.4.7
ESF196	Bank 2 Start Address	Yes	6.4.7
ESF197	Bank 3 Start Address	Yes	6.4.7
ESF198	DRAM Mode	Yes	6.4.8
ESF199	DRAM Parameters Bank 0	Yes	6.4.10
ESF19A	Bank 1 Size Control	Yes	6.4.3.2
ESF19B	Bank 2 Size Control	Yes	6.4.3.3
ESF19C	Bank 3 Size Control	Yes	6.4.3.4
ESF19D	Bank 4 Size Control	Yes	6.4.3.5
ESF19E	Bank 4 Start Address	Yes	6.4.7
ESF19F	System Configuration	Yes	6.4.1
ESF1A0	Bank 4 Address Mux Control	Yes	6.4.2.3
ESF1A1	DRAM Parameters Bank 1	Yes	6.4.10
ESF1A2	DRAM Parameters Bank 2	Yes	6.4.10
ESF1A3	DRAM Parameters Bank 3	Yes	6.4.10
ESF1A4	DRAM Write Cycle Parameters Banks (3:0)	Yes	6.4.10
ESF1A5	DRAM Parameters Bank 4	Yes	6.4.10
ESF1A8	Static Column or Page Mode	Yes	6.4.9
ESF1A9	Memory Shadow Control 2	Yes	6.4.4.2
ESF1AA	Memory Shadow Control	Yes	6.4.4.1
ESF1AB	Split Memory Control and SMI RAM Start Address	Yes	6.4.5.1
700	ESF Data Port	No	2.7, 6.4
1072	CPU Clock Control	Yes	4.2.6

TABLE 2-1. REGISTER INDEX

PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
1872	Bus Timing and Power Down Control	Yes	5.3.1
2072	Refresh Control, Serial and Parallel Chip Selects	Yes	7.1
2872	RTC, PVGA, Chip Selects	Yes	7.2
3072	Programmable Chip Select Address	Yes	7.3
3872	General Purpose I/O Write	Yes	11.1.2
3C72	DMA Shadow 1	Yes	8.14.1
4472	DMA Shadow 2	Yes	8.14.2
4872	ESF Address	Yes	6.4
4C72	DMA Shadow 3	Yes	8.14.3
5072	ESF Data	Yes	6.4
5472	SMI Auxiliary Control	Yes	9.3
5C72	Programmable CS2 and CS3 Control	Yes	9.4
6472	Programmable CS2 Address	Yes	9.5
6C72	Programmable CS3 Address	Yes	9.6
7072	PMC Output Control 7:0	Yes	8.4
7472	Backlight Mouse And SMI Control	Yes	6.5
7872	PMC Output Control 15:8	Yes	8.4
7C72	SMI I/O Trap Control	Yes	9.1.2
8072	PMC Timers	Yes	8.5
8472	IBM I/O Trap	Yes	9.1.1
8872	PMC Inputs 7:0	Yes	8.6
8C72	Stop Clock Control	Yes	4.2.7
9072	NMI Status	Yes	8.8
9472	General Purpose I/O Control	Yes	11.1.1
9872	Diagnostic	Yes	10.1
9C72	SMI I/O Timeout Control 1	Yes	9.2.1
A072	Delay Line Diagnostic	Yes	10.2
A472	SMI I/O Timeout Count 2	Yes	9.2.2
A872	Test Enable	Yes	10.3
AC72	SMI I/O Timeout Count 3	Yes	9.2.3
B072	Activity Monitor Control	Yes	8.12
B472	Enhanced DMA Clock	Yes	4.2.8
B872	DMA Mode Shadow	Yes	5.4.15
BC72	Enhanced DMA Clock	Yes	4.2.8
C072	ROM Bank Select Control	Yes	4.3
C472	Scratchpad A	Yes	11.2
CC72	Scratchpad B	Yes	11.2
C872	PMC Interrupt Enables	Yes	8.7
D072	Serial/Parallel Shadow	Yes	8.9
D472	Interrupt Controller Shadow	Yes	8.10
D872	Activity Monitor Mask	Yes	8.13
DC72	Test Status	Yes	10.4
E472	Port 70H Shadow	No	8.11
F072	48 MHz Oscillator Disable	Yes	7.4, Table 7-3
F073	Lock/Unlock	No	2.7.2
F472	48 MHz Oscillator Enable	Yes	7.4, Table 7-3
FC72	Lock Status	Yes	2.7.1

① See Table 5-4. DMA Controller/Channel Function Map
② See Table 5-6. Interrupt Controller Function Map

TABLE 2-1. REGISTER INDEX (Continued)

3.0 SIGNAL DESCRIPTION

Table 3-1 provides a list of signal to pin assignments for the WD8110/LV 208-pin MQPF package. Table 3-2 provides a description of the signals controlled by the WD8110/LV.

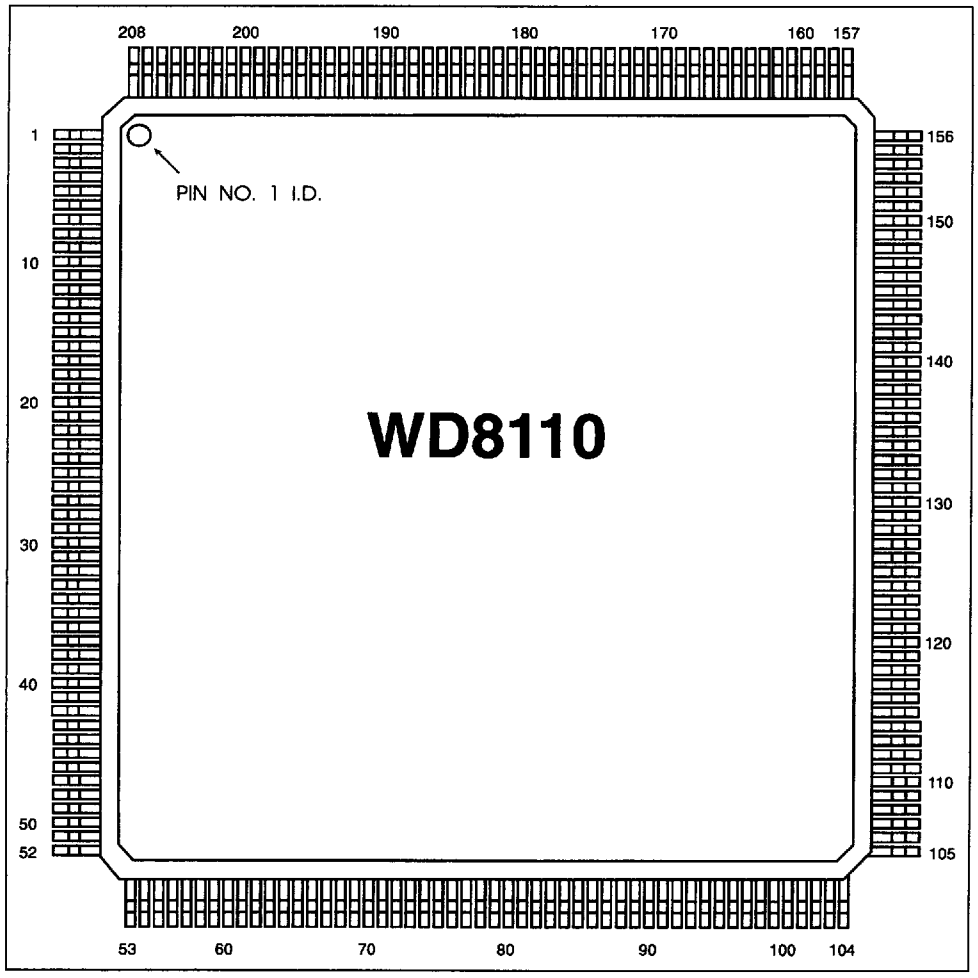


FIGURE 3-1. 208-PIN MQFP PACKAGE

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - AEN	40 - REFRESH	76 - A10	106 - CPUCLK
2 - BALE	41 - VSS	77 - A9	107 - LBCLK
3 - SYSCLK	42 - SBHE	78 - A8	108 - EADS
4 - LOWMEG	43 - LA20	79 - A7	EXCOP
SMEMR	44 - IOW	80 - VSS	109 - VSS
5 - SD15	45 - IOR	81 - A6	110 - RAS0
6 - SD14	46 - MEMW	82 - A5	111 - RAS1
7 - SD13	47 - MEMR	83 - A4	112 - RAS2
8 - SD12	48 - SA1	84 - A3	113 - RAS3
9 - SD11	49 - SA0	85 - A2	114 - RAS4
10 - SD10	50 - MDEN	86 - RDYIN	115 - CAS03
11 - SD9	51 - MDIR	87 - BE3	116 - CAS02
12 - SD8	52 - NMI	88 - VDD3V	117 - VSS
13 - SD7	53 - DRMWR	89 - BE2	118 - CAS01
14 - VSS	54 - INTRQ	SXA1	119 - CAS00
15 - SD6	55 - A31	90 - BE1	120 - VDD3V
16 - SD5	SXLOWEN	SXBHE	121 - CAS13
17 - VDD5V	56 - A29	91 - BE0	122 - CAS12
18 - SD4	SUSP	SXBLE	123 - CAS11
19 - SD3	STP_REQ	92 - NPERR	124 - CAS10
20 - SD2	DFS_REQ	FERR	125 - ADS
21 - SD1	57 - A27	93 - BRDY486	126 - W/R
22 - SD0	SXSWPEN	94 - GPREGWR	127 - D/C
23 - CLK14	58 - A26	NPBUSY	128 - M/IO
24 - MASTER	59 - A25	95 - VSS	129 - PDREF
25 - IOCK	60 - A24	96 - ROMBA16	130 - LDS32
26 - IOCHRDY	61 - A23	3VBUFFER	131 - VSS
27 - ZEROWS	62 - A22	97 - ROMBA17	132 - PMCIN
28 - VSS	63 - A21	3VCORE	133 - SUSPA
29 - MEMCS16	64 - A20	98 - ROMBA18	DFS_RDY
30 - IOCS16	65 - A19	SXM	134 - PCHK486
31 - DRQ7	66 - VSS	99 - CPURES	135 - BLAST
32 - DRQ6	67 - A18	100 - NPRST	136 - RA0
33 - DRQ5	68 - A17	101 - SMIRDY	ED0
34 - DRQ3	69 - A16	WTKMODE	137 - RA1
35 - DRQ2	70 - A15	FLUSH	ED1
36 - DRQ1	71 - VDD3V	102 - SMI	138 - RA2
37 - VDD5V	72 - A14	103 - KEN	ED2
38 - DRQ0	73 - A13	MODE486	139 - VDD3V
39 - SMEMW	74 - A12	104 - BCLK2	140 - RA3A
WTKIRQ13	75 - A11	105 - OSCIN	CS3

TABLE 3-1. 208-PIN MQFP - SIGNAL/PIN ASSIGNMENTS

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
141 - RA3B	152 - $\overline{\text{RDY486}}$	171 - D13	192 - D31
CS4	153 - $\overline{\text{CSEN}}$	172 - D14	193 - IRQSET0
142 - RA4	TC	173 - VDD3V	194 - VSS
ED3	CLKTEST	174 - D15	195 - IRQSET1
143 - RA5	154 - MXCTL0	175 - D16	196 - $\overline{\text{SMIADS}}$
ED4	155 - MXCTL1	176 - D17	$\overline{\text{SMIACT}}$
144 - RA6	156 - MXCTL2	177 - D18	197 - HOLDA
ED5	157 - D0	178 - D19	198 - $\overline{\text{RSTIN}}$
145 - RA7	158 - D1	179 - D20	199 - HOLDR
ED6	159 - D2	180 - D21	200 - SPKR
146 - VSS	160 - D3	181 - VSS	201 - DP0
147 - RA8	161 - D4	182 - D22	202 - VSS
ED7	162 - D5	183 - D23	203 - DP1
148 - RA9	163 - D6	184 - D24	204 - DP2
CS0	164 - D7	185 - D25	205 - DP3
149 - RA10	165 - D8	186 - D26	206 - $\overline{\text{EXBUSY}}$
CS1	166 - VSS	187 - D27	$\overline{\text{GPREGRD}}$
150 - RA11	167 - D9	188 - D28	207 - BS16
CS2	168 - D10	189 - D29	208 - DACKEN
151 - A20GT	169 - D11	190 - VDD3V	
1X/$\overline{\text{2X}}$	170 - D12	191 - D30	

TABLE 3-1. 208-PIN MQFP - SIGNAL/PIN ASSIGNMENTS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			INITIALIZATION AND CLOCKING
3	SYSCLK	O	**System Clock** Translate +5 In asynchronous bus mode, SYSCLK is equal to BCLK2 divided by two or four, depending on the BUS_MOD bits in the Bus Timing Register at Port 1872H. See Section 5.3.1. In synchronous bus mode, SYSCLK is equal to CPUCLK divided by two or four, depending on the BUS_MOD bits in the Bus Timing Register at Port 1872H. See Section 5.3.1.
23	CLK14	I	**Clock 14** Translate +5 CLK14 is derived from a 14.318 MHz crystal oscillator and is used internally for the 8254 compatible timers. CLK14 is externally switched to 32 KHz during a suspend and resume.
96	3VBUFFER	I	**3 Volt Buffer** Pin 96 is shared by 3VBUFFER and ROMBA16. Refer to Miscellaneous group for a description of ROMBA16. 3VBUFFER is sampled during Power-On Reset . Low = AT Bus I/O Buffer operates at 5 volts. High = AT Bus I/O Buffer operates at 3 volts.
97	$\overline{3VCORE}$	I	**3 Volt Core** Pin 97 is shared by $\overline{3VCORE}$ and ROMBA17. Refer to Miscellaneous group for a description of ROMBA17. $\overline{3VCORE}$ is sampled during Power-On Reset . Low = Core operates at 3 volts. High = Core operates at 5 volts.
98	$\overline{SXM}$	I	**80386SX or 386/486 Mode Select** Translate +3 Pin 98 is shared by $\overline{SXM}$ and ROMBA18. Refer to Miscellaneous group for a description of ROMBA18. MODE486 on pin 103 must also be low during Power-On-Reset to enable $\overline{SXM}$. Low = 80386SX mode. High = 80386DX mode.

Translate +3 - This signal may only be connected to a 3 volt signal bus when the System Controller VDD Core pins are powered by 3.3 volts.

Translate +5 - This signal may be connected to a 5 volt signal bus when the System Controller core is powered by 3.3 volts. These signals are internally translated and require that the VDDAT pins be connected to a +5 volt source.

TABLE 3-2. SIGNAL DESCRIPTIONS

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			INITIALIZATION AND CLOCKING (Cont.)
101	$\overline{\text{WTKMODE}}$	I	**Weitek Mode** Translate +3 Pin 101 is shared by $\overline{\text{WTKMODE}}$, $\overline{\text{SMIRDY}}$ and $\overline{\text{FLUSH}}$. Refer to Main Processor Control group for a description of $\overline{\text{SMIRDY}}$and $\overline{\text{FLUSH}}$. $\overline{\text{WTKMODE}}$ is sampled during Power-On-Reset. If low, Weitek Mode is selected and pin 56 functions as A29, pin 39 as WTKIRQ13 and pin 4 as $\overline{\text{LOWMEG}}$. If high, pin 56 functions as $\overline{\text{STP\_REQ}}$, $\overline{\text{DFS\_REQ}}$ or $\overline{\text{SUSP}}$. Refer to Main Processor Control group for a description of pin 56.
103	MODE486	I	**80386/80486 Mode** Translate +3 Pin 103 is shared by MODE486 and $\overline{\text{KEN}}$. Refer to Main Processor Control group for a description of $\overline{\text{KEN}}$. During Power-On-Reset, pin 103 is MODE486. A high at this time selects the 80486 mode, a low selects the 80386 mode. Selecting the 80386 mode allows $\overline{\text{SXM}}$ on pin 98 to select between 80386SX mode and 80386DX mode.
104	BCLK2	I	**Bus Clock** Translate +3 BCLK2 is used to generate an 8 MHz or 10 MHz expansion bus clock. For an 8 MHz bus, BCLK2 is a 16 MHz or 32 MHz input signal. For a 10 MHz bus clock, BCLK2 is a 20 or 40 MHz input signal. BCLK2 may also be used to drive the processor clock.
105	OSCIN	I	**Oscillator In** Translate +3 OSCIN is connected to an external oscillator and is used to generate the CPUCLK. This frequency may be divided by one or two, depending upon 1X/$\overline{\text{2X}}$ at power up.
106	CPUCLK	O	**386/486 CPU Clock** Translate +3 At Power-On-Reset, if 1X/$\overline{\text{2X}}$ is strapped high CPUCLK source defaults to the OSCIN input at pin 105. If 1X/$\overline{\text{2X}}$ is strapped low, CPUCLK source defaults to BLCK2 at pin 104. After Power-On-Reset, the CPUCLK source can be changed depending upon the setting of the SRC bit at Port Address 1072H.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			INITIALIZATION AND CLOCKING (Cont.)
107	LBCLK	O	**Local Bus Clock** Translate +3 LBCLK is a derivative of CPUCLK divided by 2 for use with VESA local bus devices. When 1X/$\overline{2X}$ is strapped low, LBCLK is phase synchronized 1X CLK for the local bus. When 1X/$\overline{2X}$ is strapped high, CPUCLK should be used instead of LBCLK.
108	$\overline{EXCOP}$	I	**External 80387 Coprocessor** Translate +3 Pin 108 is shared by $\overline{EXCOP}$ and $\overline{EADS}$. Refer to Main Processor Control group for a description of $\overline{EADS}$. $\overline{EXCOP}$ is sampled during Power-On-Reset. If low, an external 80387 is supported, coprocessor error handling logic is enabled, and pins 206 and 94 function as $\overline{EX-BUSY}$ and NPBUSY. If high, pins 206 and 94 function as $\overline{GPREGRD}$ and $\overline{GPREGWR}$.
151	1X/$\overline{2X}$	I	**Single/Double Phase CPU Clock** Translate +3 Pin 151 is shared by 1X/$\overline{2X}$ and A20GATE. Refer to Main Processor Control group for a description of A20GATE. The 1X/$\overline{2X}$ strapping option is sampled during Power-On-Reset. When low, OSCIN at pin 105 is divided by 2 internally to maintain phase relationship with CPUCLK. When high, OSCIN is not divided.
153	CLKTEST	I	**Clock Test** Translate +3 Pin 153 is shared by CLKTEST, $\overline{CSEN}$ and TC. Refer to AT BUS group for a description of $\overline{CSEN}$ and TC. CLKTEST is sampled during Power-On-Reset. When low, test mode is selected. When high, normal operation is selected.
198	$\overline{RSTIN}$	I	**System Reset In** Translate +3 $\overline{RSTIN}$ is derived from the mother board power good circuit. It drives a CMOS input level Schmitt Trigger and is used to reset the entire system at power up For a detailed description, refer to Section 4.1 Power Up Reset.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			AT BUS
156 155 154	MXCTL2 MXCTL1 MXCTL0	O O O	**Multiplexer Control(2:0)** Translate +3 MXCTL(2:0), controls external multiplexers for the selection of input signals IRQSET1, IRQSET0 and PMCIN and, along with DACKEN, generates DACK(7:5), DACK(3:0) and BUS_RST. Refer to Table 5-1 and Figure 5-1.
208	DACKEN	O	**DACK Enable** Translate +3 When DACKEN is asserted, MXCTL(2:0) are used to generate DACK(7:5), DACK(3:0) and BUS_RST. Refer to Table 5-1 and Figure 5-1.
195	IRQSET1	I	**Interrupt Request Set 1** Translate +3 MXCTL(2:0) along with one of the following: A20GT, IRQ1, IRQ(3:7) or IRQ12, selects IRQSET1. Refer to Table 5-1 and Figure 5-1.
193	IRQSET0	I	**Interrupt Request Set 0** Translate +3 MXCTL(2:0) along with one of the following: ROM8, RESCPU, IRQ(15:14), IRQ(11:9), or IRQ8 selects IRQSET0. Refer to Table 5-1 and Figure 5-1.
31:33 34:36 38	DRQ(7:5) DRQ(3:1) DRQ0	I	**DRQ(7:5) DRQ(3:0) Inputs** Translate +5 These are the DRQ signals from the AT Bus. They have internal pulldown resistors.
5:13 15:16 18:22	SD(15:7) SD(6:5) SD4:SD0	I/O	**AT Data Bus** Translate +5 SD(15:0) are connected directly to the AT Data Bus. SD(7:0) have internal programmable pullup resistors. See Port Address 8C72H in Section 4.2.7
39	WTKIRQ13	I	**WEITEK IRQ13** Translate +5 In WEITEK mode, pin 39 is an input from the WEITEK coprocessor and ORed internally to generate an IRQ13 interrupt.
	SMEMW	O	**S Memory Write** When not in WEITEK mode, pin 39 is an output and asserted for AT Bus memory write cycles when the AT Bus address is below 1 Mbyte.
4	LOWMEG	O	**First Megabyte** Translate +5 In weitek mode, LOWMEG is output to the WD7615 when the AT bus address is below 1 Mbyte.
	SMEMR	O	**S Memory Read** When not in Weitek mode, pin 4 is SMEMR. When asserted, SMEMR indicates a read cycle with an address below 1 Mbyte

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			AT BUS (Cont.)
46	$\overline{\text{MEMW}}$	I/O	**Memory Write** Translate +5 In Master Mode $\overline{\text{MEMW}}$ is an input. $\overline{\text{MEMW}}$ is asserted by the System Controller as an output when a DMA or processor memory write to the AT Bus is to take place.
47	$\overline{\text{MEMR}}$	I/O	**Memory Read** Translate +5 In Master Mode, $\overline{\text{MEMR}}$ is an input. $\overline{\text{MEMR}}$ is asserted by the System Controller as an output when a DMA or processor memory read from the AT Bus is to take place.
44	$\overline{\text{IOW}}$	I/O	**I/O Write** Translate +5 In Master Mode, $\overline{\text{IOW}}$ is an input. $\overline{\text{IOW}}$ is asserted by the System Controller as an output when a DMA or processor I/O write to the AT Bus is to take place.
45	$\overline{\text{IOR}}$	I/O	**I/O Read** Translate +5 In Master Mode, $\overline{\text{IOR}}$ is an input. $\overline{\text{IOR}}$ is asserted by the System Controller as an output when a DMA or processor I/O read from the AT Bus is to take place.
42	$\overline{\text{SBHE}}$	I/O	**System Bus High Enable** Translate +5
49	SA0	I/O	**System Address 0**
48	SA1	I/O	**System Address 1** In Master Mode, these are input signals asserted by the Bus Master. When not in Master Mode, these are output signals used by the AT Address Bus.
43	LA20	I/O	**Early Address 20** Translate +5 In Master Mode, LA20 is an input signal asserted by the Bus Master to place an address bit on A20. When not in Master Mode,LA20 is an output asserted by the System Controller to place address bit A20 on the AT Bus LA20 line.
24	$\overline{\text{MASTER}}$	I	**Master** Translate +5 $\overline{\text{MASTER}}$ is asserted by the Bus Master to indicate that a Bus Master cycle is occurring. This causes $\overline{\text{SBHE}}$, SA0, SA1, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$ and $\overline{\text{LA20}}$ to be selected as input signals.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			AT BUS (Cont.)
40	$\overline{\text{REFRESH}}$	I/O	**Refresh** Translate +5 As an input, $\overline{\text{REFRESH}}$ is asserted by the Bus Master in conjunction with $\overline{\text{MEMR}}$ to refresh memory on the AT Bus and DRAM controlled by the System Controller. As an output, $\overline{\text{REFRESH}}$ is asserted by the System Controller to refresh memory on the AT Bus.
153	$\overline{\text{CSEN}}$	O	**Chip Select Enable** Translate +3 Pin 153 is shared by $\overline{\text{CSEN}}$, TC and CLKTEST. Refer to Initialization And Clocking group for a description of CLKTEST. $\overline{\text{CSEN}}$ enables the decoding of CS(4:0) for up to 32 chip selects.
	TC	O	**Terminal Count** TC is used by the WD76C20 during DMA cycles for generating TC on the AT bus.
26	IOCHRDY	I	**I/O Channel Ready** Translate +5 IOCHRDY initiates wait states during AT bus cycles.
27	$\overline{\text{ZEROWS}}$	I	**Zero Wait State** Translate +5 $\overline{\text{ZEROWS}}$ initiates a zero wait AT bus cycle.
30	$\overline{\text{IOCS16}}$	I	**16 Bit I/O Cycle** Translate +5 $\overline{\text{IOCS16}}$ initiates a 16-bit AT Bus cycle.
29	$\overline{\text{MEMCS16}}$	I	**16-Bit Memory Cycle** Translate +5 $\overline{\text{MEMCS16}}$ initiates a 16-bit memory AT Bus cycle.
1	AEN	O	**Address Enable** Translate +5 AEN is asserted by the System Controller while performing DMA and Refresh cycles.
2	BALE	O	**AT Bus Address Latch Enable** Translate +5 BALE is synchronous with the Bus Clock (BCLK2).
25	$\overline{\text{IOCK}}$	I	**I/O Channel Check** Translate +5 When asserted, $\overline{\text{IOCK}}$ indicates that a bus or memory error has occurred on the AT Bus and generates an NMI to the processor.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			MAIN PROCESSOR CONTROL
102	$\overline{SMI}$	I/O	**System Management Interrupt** Translate +3 Request to and from the processor. (Open collector)
196	$\overline{SMIADS}$ $\overline{SMIACT}$	I	**System Management Interrupt Address Strobe** **System Management Interrupt Active** Translate +3 $\overline{SMIADS}$ and $\overline{SMIACT}$ are signals from the CPU for supporting SMI cycles. For AMD and Cyrix CPUs pin 196 is $\overline{SMIADS}$. For Intel CPUs pin 196 is $\overline{SMIACT}$.
101	$\overline{SMIRDY}$	O	**System Management Interrupt Ready** Translate +3 Pin 101 is shared by $\overline{SMIRDY}$, $\overline{FLUSH}$ and $\overline{WTKMODE}$. Refer to Initialization And Clocking group for a description of $\overline{WTKMODE}$. Whether pin 101 functions as $\overline{SMIRDY}$ or $\overline{FLUSH}$ is controlled by bit 13 at Port Address 7C72H. $\overline{SMIRDY}$ is the ready signal for $\overline{SMI}$ operations.
	$\overline{FLUSH}$	O	**Flush Cache** $\overline{FLUSH}$ is asserted to the 80486 to flush its internal Cache.
91	$\overline{BE0}$ $\overline{SXBLE}$	I	**Byte Enable 0** Translate +3 **SX Bus Low Enable** In 80386DX or 80486 mode this is $\overline{BE0}$, the Byte Enable 0 signal from the CPU. In 80386SX mode this is $\overline{BLE}$, the Bus Low Enable signal and indicates a transfer of the low byte on the processor data bus.
90	$\overline{BE1}$ $\overline{SXBHE}$	I	**Byte Enable 1** Translate +3 **SX Bus High Enable** In 80386DX or 80486 mode this is $\overline{BE1}$, the Byte Enable 1 signal from the CPU. In 80386SX mode this is $\overline{BHE}$, the Bus High Enable signal and indicates a transfer of the high byte on the processor data bus.
89	$\overline{BE2}$ SXA1	I	**Byte Enable 2** Translate +3 **SX Processor Address Bit 1** In 80386DX or 80486 mode this is $\overline{BE2}$, the Byte Enable 2 signal from the CPU. In 80386SX mode this is bit 1 (A1) of the processor address bus.
87	$\overline{BE3}$	I	**Byte Enable 3** Translate +3 In 80386DX or 80486 mode this is $\overline{BE3}$, the Byte Enable 3 signal from the CPU.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			MAIN PROCESSOR CONTROL (Cont.)
125	$\overline{ADS}$	I	**Address Status** Translate +3 $\overline{ADS}$ is the address status signal from the processor.
128	M/$\overline{IO}$	I	**Memory Or I/O** Translate +3 When high, M/$\overline{IO}$ indicates a processor memory cycle. When low, M/$\overline{IO}$ indicates a processor I/O cycle.
127	D/$\overline{C}$	I	**Data Control** Translate +3 D/$\overline{C}$ is the Data Control signal of the processor. When high, a data transfer occurs. When low, a control operation occurs.
126	W/$\overline{R}$	I	**Write Or Read** Translate +3 W/$\overline{R}$ is the write or read signal from the processor. When W/$\overline{R}$ is high, a write occurs. When W/$\overline{R}$ is low, a read occurs.
199	HOLDR	O	**Hold Request** Translate +3 Hold cycle request to the processor.
197	HOLDA	I	**Hold Acknowledge** Translate +3 Hold acknowledge from the processor.
52	NMI	O	**Non-Maskable Interrupt** Translate +3 Processor non-maskable interrupt cycle request.
134	$\overline{PCHK486}$	I	**Parity Check 80486** Translate +3 When in 80486 mode, $\overline{PCHK486}$ is an input signal, asserted by the 80486 during CPU memory reads, to indicate that a parity error has occurred. $\overline{PCHK486}$ is latched internally to generate an NMI.
152	$\overline{RDY486}$	O	**Ready 80486** Translate +3 $\overline{RDY486}$ terminates non-burst 80486 cycles or all 80386 cycles. It is externally ORed with other ready sources, such as 387RDYO, VLBIRDY and WEITEKRDY, before going to the CPU.
93	$\overline{BRDY486}$	O	**Burst Ready 80486** Translate +3 During 80486 mode, $\overline{BRDY486}$ asserted indicates a Burst is ready for a 80486 burst cycle.
54	INTRQ	O	**Interrupt Request** Translate +3 Processor interrupt cycle request.

TABLE 3-2. SIGNAL DESCRIPTION (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			MAIN PROCESSOR CONTROL (Cont.)
103	$\overline{\text{KEN}}$	O	**Cache Enable** Translate +3 Pin 103 is shared by $\overline{\text{KEN}}$ and MODE486. Refer to Initialization And Clocking group for a description of MODE486. During normal operations $\overline{\text{KEN}}$ is an output to the 80486. $\overline{\text{KEN}}$ is always asserted during T1 cycles and de-asserted for non-cache cycles.
99	CPURES	O	**CPU Reset** Translate +3 When asserted, CPURES is a synchronous reset for the processor.
86	$\overline{\text{RDYIN}}$	I	**Processor Ready In** Translate +3 $\overline{\text{RDYIN}}$ is the processor $\overline{\text{READY}}$ signal after all sources are OR'ed together.
151	A20GATE	O	**A20 Gate** Translate +3 Pin 151 is shared by A20GATE and 1X/$\overline{\text{2X}}$. Refer to Initialization And Clocking group for a description of 1X/$\overline{\text{2X}}$. A20 from Port 92H is ORed with the Keyboard Controller output and is directly connected to A20GTX of the 80486 CPU.
108	$\overline{\text{EADS}}$	O	**External Address Valid Input** Translate +3 Pin 108 is shared by $\overline{\text{EADS}}$ and $\overline{\text{EXCOP}}$. Refer to Initialization And Clocking group for a description of $\overline{\text{EXCOP}}$. $\overline{\text{EADS}}$ connects to the 80486 EADS input to run cache invalidation cycles.
207	$\overline{\text{BS16}}$	O	**BUS SIZE 16** Translate +3 $\overline{\text{BS16}}$ is asserted to the 80386/80486 processor whenever an AT Bus cycle is generated.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			MAIN PROCESSOR CONTROL (Cont.)
55	A31	I/O	**Processor Address Bus A(31:2)** Translate +3
	SXLOWEN	O	For 80486 and 80386DX cycles, A(31:2) are inputs.
56	A29	I/O	For Master cycles, A(23:2) are inputs.
	SUSP	O	For DMA and refresh cycles, A(23:2) are outputs.
	STP_REQ	O	
	DFS_REQ	O	For Cache invalidation during DMA and Master cycles A31,
57	A27	I	A29 and A(27:24) outputs are forced low.
	SXSWPEN	O	
58:60	A(26:24)	I/O	**SXLOWEN, SXSWPEN**
			In 80386SX mode A(31:24) are not used and are forced low in-
61:65	A(23:19)	I/O	ternally. Pins 55 and 57 become outputs SXLOWEN and
67:70	A(18:15)	I/O	SXSWPEN which provide buffer control for the 80386SX CPU
72:79	A(14:7)	I/O	data buffers.
81:85	A(6:2)	I/O	
			Suspend (SUSP), Stop Clock Request (STP_REQ), Dynamic Frequency Shift Request (DFS_REQ)
			In Weitek mode, pin 56 is A29. When A29 = 0, A31 = 1 and M/IO on pin 128 = 1, a Weitek cycle is decoded internally.
			When not in Weitek mode, pin 56 serves as:
			Stop Clock Request (STP_REQ) for Intel CPUs.
			Suspend (SUSP) for Cyrix CPUs.
			DFS Request (DFS_REQ) for IBM BL CPU.
133	SUSPA	I	**Suspend Acknowledge** Translate +3
			For Cyrix CPUs pin 133 is SUSPA, a response to SUSP on pin 56.
	DFS_RDY	I	**DFS Ready**
			For IBM CPUs pin 133 is DFS_RDY, a response to DFS_REQ on pin 56.
135	BLAST	I	**Blast** Translate +3
			In 80486 Mode, BLAST is input from the 80486 to indicate the end of the last burst cycle.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			NUMERIC PROCESSOR CONTROL
92	NPERR	I	**Numeric Processor Error** Translate +3 80386 Mode - NPERR is the error signal from the 80387 numeric processor. If asserted while NPBUSY is active, an internal IRQ13 is asserted.
	FERR	I	**Floating Point Error** 80486 Mode - This is the FERR from the 80486. When asserted, it generates an internal IRQ13.
94	NPBUSY	I	**Numeric Processor Busy** Pin 94 is shared by NPBUSY and GPREGWR, refer to Miscellaneous group for a description of GPREGWR. When operating in External Coprocessor Mode, pin 94 is NPBUSY, the busy status of the 80387 coprocessor. If NPERR goes low while NPBUSY is active, an internal IRQ13 is generated and the EXBUSY output on pin 206 goes active.
100	NPRST	O	**Numeric Processor Reset** Translate +3 In External Coprocessor Mode (EXCOP asserted), this pin is NPRST and is used to reset the numeric processor.
			DRAM MEMORY CONTROL
51	MDIR	O	**Memory Direction** Translate +3 MDIR determines the direction of the DRAM data buffers if required. When high, the direction is from CPU Data Bus to Memory Data Bus. When low, the direction is from Memory Data Bus to CPU Data Bus.
53	DRMWR	O	**DRAM Write** Translate +3 DRMWR operates as one DRAM write enable for all DRAMs in all banks. It must be buffered externally if the load exceeds 450 pF.
50	MDEN	O	**Memory Data Enable** Translate +3 MDEN enables the memory data buffers, if required.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			DRAM MEMORY CONTROL (Cont.)
150 149 148 147 145 144 143 142 141 140 138 137 136	RA11/CS2 RA10/CS1 RA9/CS0 RA8/ED7 RA7/ED6 RA6/ED5 RA5/ED4 RA4/ED3 RA3B/CS4 RA3A/CS3 RA2/ED2 RA1/ED1 RA0/ED0	O O O I/O I/O I/O I/O I/O O O I/O I/O I/O	**DRAM Address Bits RA(11:0)** Translate +3 **EDATA Bits ED(7:0)** **Chip Select Bits CS(4:0)** **DRAM Address** RA(11:4), RA3B, RA3A and RA(2:0) are output signals controlled by the System Controller. During DRAM cycles they are used to select the DRAM row and column. RA3B is the multiplexed DRAM address for banks 1 and 3. RA3A is the multiplexed DRAM address for banks 0, 2 and 4. RA(11:0) are designed to directly drive DRAMs and have controllable output strength for driving heavy capacitive loads. If the load exceeds 450 pF, it is necessary to use external buffers. **EDATA** ED(7:0) are I/O signals representing data to or from devices such as the Keyboard Controller on the EDATA bus. **Chip Select** CS(4:0) are output only signals, decoded by external logic to provide one of 32 possible Chip Selects.
114:110	$\overline{\text{RAS}}$(4:0)	O	**Row Address Select 4:0** Translate +3 $\overline{\text{RAS}}$4:0 are the row address select signals for banks 4 through 0. $\overline{\text{RAS}}$4:0 are designed to drive up to a 150 pF load directly. For loads that exceed 150 pF, they must be buffered externally before being connected to the DRAMs.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			DRAM MEMORY CONTROL (Cont.)
115:116 118:119 121:124	$\overline{CAS0(3:2)}$ $\overline{CAS0(1:0)}$ $\overline{CAS1(3:0)}$	O	**Column Address Select 0 (3:0)** Translate +3 **Column Address Select 1 (3:0)** $\overline{CAS0(3:0)}$ are the four column address select signals for banks 4, 2 and 0. $\overline{CAS1(3:0)}$ are the four column address select signals for banks 3 and 1. There is a $\overline{CAS}$ signal for each byte in a 32 bit word. During read operations, all $\overline{CAS}$s are activated. During memory write operations, the only $\overline{CAS}$ signals that are active are those with the corresponding $\overline{BE(3:0)}$ active. $\overline{CAS0(3:0)}$ and $\overline{CAS1(3:0)}$ drive the DRAM lines directly.
			DATA BUS
192:191 189:182 180:174 172:167 165:157	D(31:30) D(29:22) D(21:15) D(14:9) D(8:0)	I/O	**Data Bits 31 Through 00** Translate +3 This is a four byte data bus connected directly to Local devices and Numeric processors. The WD8110 generates and checks even parity for each of the four bytes during CPU and DMA cycles. The parity appears on DP(3:0).
205:203 201	DP(3:1) DP0	I/O	**Data Parity 3 through 0** Translate +3 These are the even parity bits generated and checked by the WD8110 during 386 and DMA cycles. DP3 = D(31:24), DP2 = D(23:16), DP1 = D(15:8) and DP0 = D(7:0).
130	$\overline{LDS32}$	I	**Local Data Size 32** Translate +3 $\overline{LDS32}$ is asserted when a device such as Weitek 4167 or Video Local Bus Interface on the 80486 local bus will complete this cycle and generate $\overline{RDY486}$. $\overline{LDS32}$ is sampled at the end of T2.
			POWER MANAGEMENT
129	PDREF	I	**Power Down Refresh** Translate +3 PDREF is a 64 KHz signal from the WD76C20. During power down, PDREF is passed internally to $\overline{REFRESH}$ (pin 40 of the WD8110).
132	PMCIN	I	**Power Management Control Input** Translate +3 PMCIN is used to sample eight PMC inputs selected by MXCTL(2:0). See Table 5-1 and Figure 5-1.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			MISCELLANEOUS
206	EXBUSY	O	**Extended Coprocessor Busy** Translate +3 In External Coprocessor Mode (EXCOP asserted), this pin is EXBUSY and is used by external logic to generate BUSY386 and EPEREQ for 80387 error handling in AT compatible mode. **General Purpose Register IO Read** When not in External Coprocessor Mode (EXCOP de-asserted), this pin is GPREGRD and is used to enable reading 16-bit external General Purpose IO registers. Pin 206 has an internal programmable resistor. See Port Address 9472H in Section 11.1.1.
94	GPREGWR	O	**General Purpose Register IO Write** Translate +3 Pin 94 is shared by GPREGWR and NPBUSY. Refer to Numeric Processor Control group for a description of NPBUSY. Pin 94 has an internal programmable resistor. See Port Address 9472H in Section 11.1.1. When not in External Coprocessor Mode (EXCOP de-asserted), pin 94 is GPREGWR and is used to enable writing to 16-bit external General Purpose IO registers.
96 97 98	ROMBA16 ROMBA17 ROMBA18	O O O	**ROM Bank Switch 16** Translate +3 **ROM Bank Switch 17** **ROM Bank Switch 18** Pin 96 is shared by ROMBA16 and 3VBUFFER Pin 97 is shared by ROMBA17 and 3VCORE Pin 98 is shared by ROMBA18 and SXM. Refer to the Initialization And Clocking group for a description of 3VBUFFER, 3VCORE and SXM. ROMBA(16:18) control address bits for up to 512 KB of BIOS ROM mapped into the 64K regions at C0000, D0000, E0000 and F0000.. See Port Address C072H in Section 4.3 for more information.
200	SPKR	O	**Speaker** Translate +3 SPKR drives the speaker transistor and is used for diagnostics.
14, 28, 41 66, 80, 95 109, 117 131, 146 166, 181 194, 202	VSS	I	**GROUND**
17, 37	VDD5V	I	**+5 VOLTS**

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
			MISCELLANEOUS (Cont.)
71, 88, 120, 139, 173, 190	VDD3V	I	+3.3 volts in mixed voltage systems. +5 volts in 5 volt only systems

TABLE 3-2. SIGNAL DESCRIPTION (Continued)

4.0 INITIALIZATION, CLOCKING AND ROM BANK SELECTION

This section describes the system Master Reset (RSTIN) operation, control of internal clock (CLK14), bus clock (SYSCLK) and the processor clock (CPUCLK).

4.1 POWER UP RESET

The system reset signal, RSTIN, is generated externally at power up and is used to reset the entire system. When asserted, the System Controller outputs the CPURES signal to reset the CPU. At this time, the System Controller also resets the AT Bus by asserting DACKEN and MXCTL(2:0) = 100, which are decoded externally as BUS_RST (DACK4). See Sections 5.1, 5.1.1, Table 5-1 and Figure 5-1. An external RC circuit can be used to extend the time that RSTIN is asserted until the power supply reaches a proper level. CPURES and BUS_RST (AT Bus reset) signals are de-asserted 1 ms beyond the de-assertion of RSTIN.

During Power-Up-Reset the following strap options are sampled. The functions are described in Sections 4.1.1 through 4.1.7. Table 4-1 summarizes the strap options and the multiplexed signals they control. The state of these strap options may be read at Port Addresses 8C72H and C072H.

MODE486	- pin 103	SXM	- pin 98
3VBUFFER	- pin 96	3VCORE	- pin 97
1X/2X	- pin 151	EXCOP	- pin108
WTKMODE	- pin 101	CLKTEST	- pin 153

4.1.1 Type of Processor

The System Controller is capable of operating with an 80486SX/DX or 80386SX/DX processor. MODE486 and SXM determine the type of processor used.

If MODE486 is strapped high, the 80486SX/DX CPU mode is selected. In this mode SXM is ignored.

If MODE486 is strapped low and SXM strapped high, the 80386DX mode is selected.

If MODE486 and SXM are strapped low, the 80386SX mode is selected and the System Controller generates SXLOWEN and SXSWPEN signals to route 32-bit data to the 16-bit data path of the 80386SX.

4.1.2 3 Volt or 5 Volt Operation

The WD8110LV is designed to operate at 5 volts, 3 volts or a mix of 5 and 3 volts.

If 3VBUFFER is strapped low, the AT Buffer operates at 5 volts. If high the AT Buffer operates at 3 volts.

If 3VCORE is strapped low, the WD8110 core logic operates at 3 volts. If high, the core operates at 5 volts.

The following table presents the legitimate combinations.

3VBUFFER	3VCORE	
High	Low	3 Volt design, all VDD equal 3 volts.
Low	Low	IO Buffer at 5 volts, Core at 3 volts.
Low	High	5 Volt design, all VDD equal 5 volts.
High	High	Illegal combination.

4.1.3 Clock Select

1X/2X determines the type of CPUCLK.

If 1X/2X is strapped low:

The processor (for example, 80386DX) uses a double frequency input clock. At RSTIN. BCLK2 is selected as the CPUCLK source and is divided by two internally.

If 1X/2X is strapped high:

The processor (for example, 80486DX) uses an input clock that matches its operating frequency. At RSTIN, OSCIN is selected as the CPUCLK source.

The CPUCLK source as selected by 1X/2X strapping may be overridden by the SCR bit at Port 1072H.

4.1.4 External 80387 Support

EXCOP indicates whether an External 80387 Coprocessor is supported.

If EXCOP is strapped low, an External 80387 Coprocessor is supported and pins 206 and 94 operate as Extended Coprocessor Busy (EXBUSY) and Numeric Processor Busy (NPBUSY), respectively.

If EXCOP is strapped high, an External 80387 Coprocessor is not supported and pins 206 and 94 operate as General Purpose Register IO Read (GPREGRD) and General Purpose Register IO Write (GPREGWR). See Section 11.1 for a description of the General Purpose Registers.

4.1.5 Weitek Mode

WTKMODE strapping option is used to indicate that a Weitek numeric processor is supported.

If WTKMODE is strapped low, the Weitek Mode is selected and pins 39, 4 and 56 function as WTKIRQ13, LOWMEG and address bit A29, respectively.

If WTKMODE is strapped high, pins 39, 4 and 56 function as SMEMW, SMEMR and SUSP/STP_REQ/DFS_REQ, respectively.

4.1.6 Clock Test

CLKTEST must be strapped high for normal operation. CLKTEST is strapped low for factory test purposes.

SIGNAL	OPTION	MULTIPLEXED SIGNALS
Pin 103 MODE486	High = 486 Mode → Low = 386 Mode →	Pin 92 FERR NPERR
Pin 98 SXM	Low = 80386SX Mode → High = 80386DX Mode → (MODE486 must be strapped low to enable SXM)	Pin 55 Pin 57 Pin 89 Pin 90 Pin 91 SXLOWEN SXSWPEN SXA1 SXBHE SXBLE A31 A27 BE2 BE1 BE0
Pin 96 3VBUFFER	Low = AT I/O Buffer powered at 5 volts High = AT I/O Buffer powered at 3 volts	
Pin 97 3VCORE	Low = Core powered at 3.3 volts High = Core powered at 5 volts	
Pin 151 1X/2X	Low = CPU uses double frequency clock (CLK2) High = CPU uses single frequency clock (CLK)	
Pin 108 EXCOP	Low = Enable 80387 → High = Enable General Purpose Register R/W →	Pin 94 Pin 206 NPBUSY EXBUSY GPREGWR GPREGRD
Pin 101 WTKMODE	Low = Weitek Coprocessor supported → High = CPU Stop Clock supported →	Pin 4 Pin 39 Pin 56 LOWMEG WTKIRQ13 A29 SMEMR SMEMW SUSP/STP_REQ/DFS_REQ
Pin 153 CLKTEST	Low = Clock test mode High = Normal operation	

TABLE 4-1. STRAPPING OPTION SUMMARY

4.2 CLOCKING

The System Controller clocking logic makes use of seven clocks and four registers to control the selection and speed of the clocks. Some of these clocks are used internally by the System Controller. Three of the clocks are used externally by the System Bus and CPU. Figure 4-1 shows how the clocks interact with each other and the registers used to select the clock and speed.

AutoFast for 1X Clock Intel CPUs.

The Stop Grant AutoFast mode, as enabled by bit 5 at Port Address 1072H, emulates low speed CPU clock operation by periodically placing the CPU in a low power Stop Grant state. During times that autofast logic selects the lower CPU clock speed, $\overline{STP\_REQ}$ will be asserted for either 732 µs or 854 µs out of every 976 µs, effectively providing either a divide by 4 or divide by 8 of the normal clock speed. This does not change the clock to the CPU.

This enhanced mode provides key advantages over actually changing the clock speed when using a 1X clock CPU with a PLL in its clock input.

- The effective clock rate is lower than the minimum 8 MHz restriction imposed by some CPUs.
- There is far less latency in returning to high speed since there is no 1 ms requirement for the CPU's PLL to settle down as there is after a clock frequency change.

There are two methods in which the Stop Grant AutoFast mode may operate.

- $\overline{STP\_REQ}$ output pin is asserted automatically by the autofast logic.
- The autofast logic causes an SMI each time $\overline{STP\_REQ}$ must be asserted and it is the responsibility of the SMI handler to actually assert it.

Refer to I/O registers at Port Address 1072H bits 7:4 and 7472H bit 11.

Enhanced AutoFast Activity Detection Logic

The AutoFast activity detect function is designed to reduce the possibility of slowing the CPU while it is performing useful operations. This enhanced logic speeds up the CPU during memory writes to address range 128K to 1M.

Refer to the register at Port Address 7472H bit 12.

CPU Phase Lock Loop Stabilization Support

For 1X clock CPUs, incorporating a PLL in the clock input usually requires a delay of 1 ms between any change in clock frequency and the deassertion of the $\overline{STP\_REQ}$ output. CSUDLY and CSCDLY in registers 7472H and 8C72H support this requirement. They enforce a 1 to 2 ms delay for clock stop and speed change functions.

4.2.1 Internal Clock (CLK14)

CLK14 is an input signal from a 14.318 MHz crystal and is used for the control of the 8254 compatible timers. CLK14 is switched by the WD76C20 to 32 KHz during save and resume operations.

4.2.2 Internal Clock (CLK32K)

CLK32K is a 32KHz clock derived from the 64 KHz PDREF signal at pin 129, divided by two. Although its value cannot be changed, it can be read at Port Address E472H bit 15.

4.2.3 Local Bus Clock For 2X CPU Mode (LBCLK)

LBCLK is CPUCLK divided by 2 for use with VESA local bus devices. Generally, this output is only usefull when 1X/$\overline{2X}$ is strapped low. A clock selection jumper for the VESA bus is required if both 1X and 2X CPUs are used on the same motherboard. CPUCLK would be selected when a 1X CPU is used. See Figure 4-1 and CPU Clock Control register description at Port Address 1072H.

4.2.4 System Bus Clock (SYSCLK)

The AT bus is driven by SYSCLK, which is derived from either BCLK2 in asynchronous mode or CPUCLK in synchronous mode, as selected by the Bus Timing Register at Port Address 1872H. SYSCLK is always one half or one fourth the value of the selected input clock (refer to Figure 4-1).

4.2.5 Processor Clock (CPUCLK)

The Processor Clock (CPUCLK) is an output from the System Controller. At Power-Up-Reset, the CPUCLK signal defaults to the OSCIN input frequency if 1X/$\overline{2X}$ is strapped high, or to BCLK2 if 1X/$\overline{2X}$ is strapped low. CPUCLK may be changed to a lower frequency to reduce power.

In 80386 mode, CPUCLK is a 2X clock for the 80386 CPU.

After Power-On-Reset the CPUCLK may be stopped or the source and speed changed, by programming the CPU Clock Control Register at Port Address 1072H.

When CPUCLK is stopped it is in phase two. CPUCLK is restarted by an NMI or IRQ interrupt, qualified by the normal NMI and IRQ masking circuitry or by an NMI generated PMC logic. In Intel Mode $\overline{STP\_REQ}$ is automatically generated.

CPUCLK can be divided down to the processor execution rate to provide software compatibility with programs expecting a particular CPU speed, such as game software. Dividing the clock rate may also have an effect on the CPU power consumption, so CLK_SPD also provides some choices of clock duty cycle.

OSCIN or BCLK2 can be used as the CPUCLK source. This choice is determined by SRC of the CPU Clock Control Register. SRC is set automatically at power-up-reset based upon the strap options.

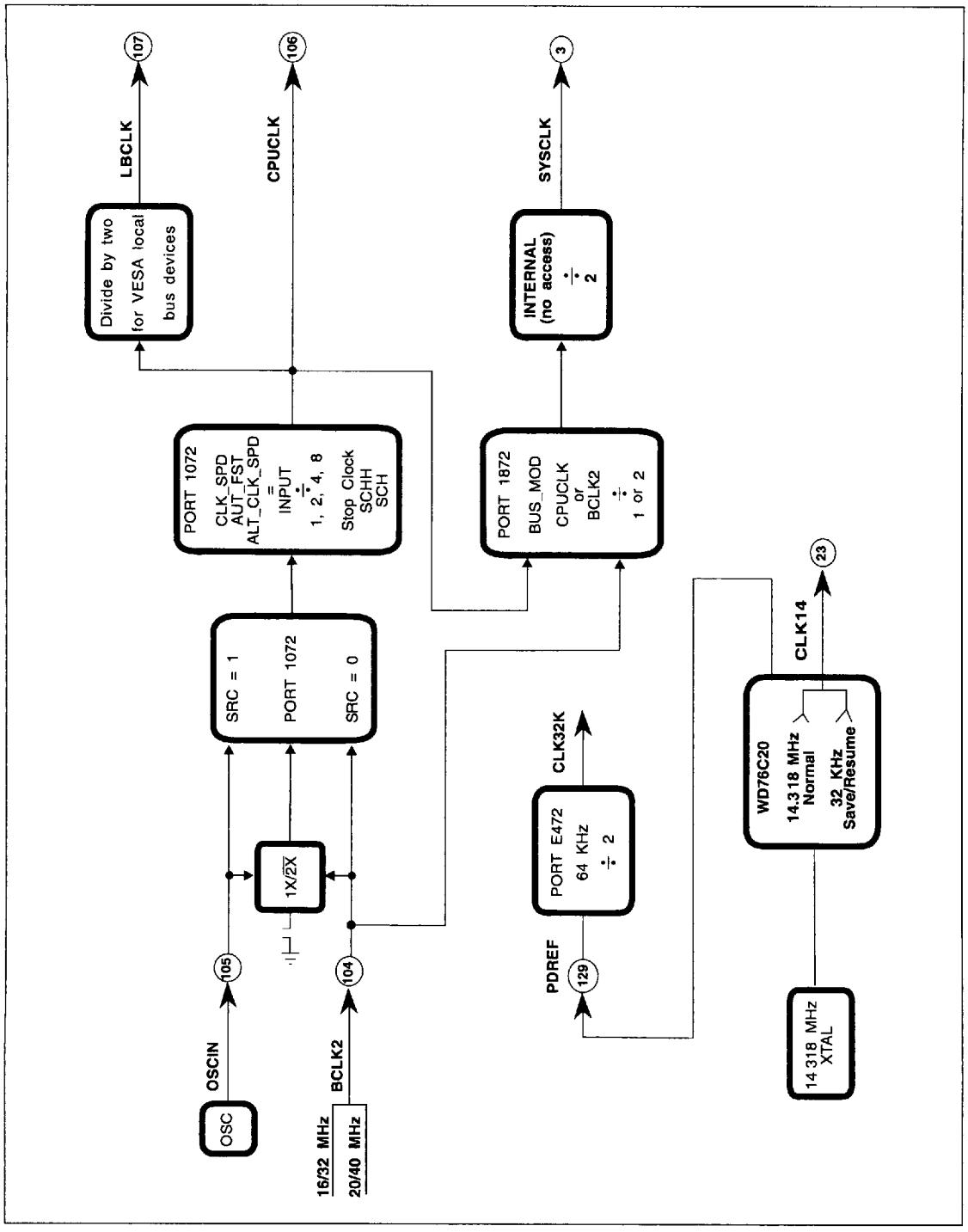


FIGURE 4-1. CLOCK CONTROL

4.2.6 CPU Clock (CPUCLK) Control Register

Port Address 1072H –
Bits 15:8, 06:00 Read and Write
Bit 07 Read, Write and Clear

15	14	13	12	11	10	09	08
SRC	CLK_SPD			AUT_ FST	ALT_CLK_SPD		

07	06	05	04	03	02	01	00
ASRE	ASMIS	SGAE	SGD4			SCHH	SCH

Signal Name	Default At RSTIN
SRC	0/1
CLK_SPD	001
AUT_FST, ALT_CLK_SPD	0000
ASRE	None
ASMIS, SGRE, SGD4	000
Bits 03, 02	None
SCH, SCHH	00

Bit 15 - SRC, CPUCLK Clock Source

SRC determines whether CPUCLK is to be driven by BCLK2 or OSCIN.

SRC = 0 -
BCK2 is the CPUCLK source.
Default for when 1X/2X is strapped low.

SRC = 1 -
OSCIN is the CPUCLK source.
Default for when 1X/2X is strapped high.

Bits 14:12 - CLK_SPD, CPUCLK Clock Speed

CLK_SPD
14 13 12

0 0 0 - Reserved
0 0 1 - source divided by 1.
0 1 0 - source divided by 2.
0 1 1 - source divided by 4, 25% duty cycle.
1 0 0 - source divided by 4, 75% duty cycle.
1 0 1 - source divided by 8, 12% duty cycle.
1 1 0 - source divided by 8, 88% duty cycle.
1 1 1 - source divided by 64, 98% duty cycle.

Bit 11 - AUT_FST, Automatic Processor Clock Speed Switching

When automatic CPUCLK switching is enabled, the processor clock is switched between high and low clock speeds, depending upon activity. If the external TURBO signal is de-asserted when auto switching is enabled, the CPUCLK is normally at the alternate clock or slower rate. When speedup activity occurs, the clock speed switches to the nominal clock rate, normally the higher, for a period of time determined by Table 4-3. When no further activity occurs, the clock speed switches back down to the alternate speed. If the external TURBO signal is asserted, the clock rate is set to the nominal clock rate specified by the CLK_SPD field.

A halt state also causes the clock rate to slow, unless the SCHH or SCH field is programmed to stop the clock. The clock restarts or returns to the faster rate when any interrupt occurs.

Table 4-3 shows the activity that triggers a higher clock rate.

AUT_FST = 0 -
Automatic Clock Switching is disabled. TURBO determines whether CLK_SPD or ALT_CLK_SPD is to be used as the CPU clock. Refer to Table 4-2 for the appropriate selection, as determined by TURBO.

AUT_FST = 1 -
Automatic CPUCLK Switching between CLK_SPD and ALT_CLK_SPD is enabled when TURBO is de-asserted. CLK_SPD is selected when TURBO is asserted. Refer to Table 4-2.

TURBO	AUT_FST	CPU CLOCK SPEED
0	X	CLK_SPD
1	0	ALT_CLK_SPD
1	1	CLK_SPD or ALT_CLK_SPD

TABLE 4-2. CLOCK SWITCH SELECTION

SPEEDUP ACTIVITY	TIME PERIOD
Hard disk interrupt, Hard disk or numeric processor I/O, SCSI, floppy, port B I/O.	1 second
Keyboard interrupt.	1 second or until next video access.
Video access or processor reset. Any NMI or IRQ interrupt, except keyboard or hard disk.	1 millisecond

TABLE 4-3. SPEEDUP ACTIVITY

Bits 10:08 - ALT_CLK_SPD, Alternate Clock Speed

ALT_CLK_SPD
10 09 08

0 0 0 - CPUCLK unchanged from CLK_SPD.
0 0 1 - source divided by 1.
0 1 0 - source divided by 2.
0 1 1 - source divided by 4, 25% duty cycle.
1 0 0 - source divided by 4, 75% duty cycle.
1 0 1 - source divided by 8, 12% duty cycle.
1 1 0 - source divided by 8, 88% duty cycle.
1 1 1 - source divided by 64, 98% duty cycle.

Bit 07 - ASRE, AutoFast Stop Request Enable

ASRE must be set to 1 to allow the autofast logic to assert $\overline{STP\_REQ}$. This permits an SMI handler to control $\overline{STP\_REQ}$ assertion when ASMIE at Port Address 7472H bit 11 is set. With ASMIE set, ASRE is automatically reset when the autofast logic determines it is time to deassert $\overline{STP\_REQ}$. This automatic reset assures that $\overline{STP\_REQ}$ cannot be reasserted until ASRE is again set by an SMI handler.

When it is more desirable to allow the autofast logic to control the assertion of $\overline{STP\_REQ}$ with no intervention by an SMI handler, ASMIE is set to 0 and ASRE will no longer be cleared automatically by the autofast logic. In this case, ASRE need only be set once. Note that ASRE can be used in this mode to gate autofast operations, since $\overline{STP\_REQ}$ cannot be asserted while ASRE is 0.

ASRE is ignored when WD8110/LV is not in the Stop Grant AutoFast mode (SGAE = 0)

ASRE = 0 -
Autofast logic cannot assert $\overline{STP\_REQ}$.

ASRE = 1 -
Autofast logic can assert $\overline{STP\_REQ}$.

Bit 06 - ASMIS, AutoFast SMI Status

ASMIS = 0 -
The autofast logic has not generated an SMI.

ASMIS = 1 -
This signals the SMI handler that the source of the SMI is a request from the autofast logic to enter the Stop Grant state. The SMI handler must clear ASMIS by writing a 1 to it. Writing a 0 has no effect. It is permissible to clear ASMIS and set ASRE simultaneously.

Bit 05 - SGAE, Stop Grant AutoFast Enable

SGAE is the master enable for the Stop Grant AutoFast mode.

SGAE = 0 -
Stop Grant AutoFast mode is not enabled.

SGAE = 1 -
Autofast logic emulates low speed operation of the CPU by periodically asserting the $\overline{STP\_REQ}$ output, thereby placing the CPU in a low power stop grant state. **For proper operation, ALT_CLK_SPD in this register must be set to 000.**

Bit 04 - SGD4, Stop Grant Divide By 4

SGD4 sets the effective clock speed divisor for stop grant emulation of low speed during autofast. SGD4 is ignored unless the WD8110/LV is in the Stop Grant AutoFast mode (bit 5 - SGAE = 1).

SGD4 = 0 -
The CPU will execute for 122 µs out of each 976 µs time period (effectively a divide by 8).

SGD4 = 1 -
The CPU will execute for 244 µs out of each 976 µs time period (effectively a divide by 4).

Bits 03:02 - Reserved for future use, must be set to zero

Bit 01 - SCHH, Stop CPUCLK at next Halt and Hold.

SCHH is applicable only for static type processors in which the clock may be stopped.

Any unmasked processor interrupt, SMI or NMI, restarts the CPUCLK. The SCHH bit remains set and the clock will be stopped again if a halt and hold condition is detected. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H or at the slower rate selected by the Refresh Control Register at Port Address 2072H.

SCHH = 0 -
Normal processor clock.

SCHH = 1 -
Stop processor clock at next halt and hold cycle.

Bit 00 - SCH, Stop CPUCLK at next Hold

SCH is applicable only for static type processors in which the clock may be stopped.

Any unmasked processor interrupt, SMI or NMI, restarts the CPUCLK and sets the SCH bit to zero. DRAM refresh continues while the processor clock is stopped. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H or at the slower rate as selected by the Refresh Control Register at Port Address 2072H.

SCH = 0 -
Normal processor clock.

SCH = 1 -
Stop processor clock at next processor hold cycle.

4.2.7 Clock Stop/Speed Control Register

Port Address 8C72H - Bits 15:10 Read only
Bits 09:00 Read and Write

This register performs the following functions:

- Reads the state of six external strap options. The remaining strap options may be read at Port Address C072H.
- Works in conjunction with the CPU Clock Control Register at Port Address 1072H to change the clock speed through AutoFast, or stop the clock, depending on whether the CPU is an IBM, Intel or Cyrix.
- Enables pullup resistors on the AT data bus SD(0:7)
- Allows actual hardware interrupts to be forced on IRQ1 (keyboard) and IRQ12 (mouse). This assists the SMI handler in replacing the function of the Keyboard controller by performing I/O traps on keyboard controller I/O locations.

15	14	13	12	11	10	09	08
		Strap Options					
Rsv.	SXM	MODE _486	EXT_ COP	3V_ BUFF	3V_ CORE	CSCD E	SCK1

07	06	05	04	03	02	01	00
Clock Control			AT_	Interrupt Generation			
SCK0	EN_ SCK	SMI_ FST	PUEN	IR12_ SL	IR1_ SL	IR12_ AL	IR1_ AL

Signal Name	Default At RSTIN
Strap Options	None
CSCDE	0
EN_IDE	0
Clock Control	0
AT_PUEN	0
Interrupt Generation	0

Bit 15 - Reserved

Bit 14 - SXM, SX Mode

SXM represents an inversion of the state of the SXM strapping option. When in 80386SX/DX mode, SXM selects between SX and DX Mode. When MODE486 is strapped high, SXM is ignored. See Section 4.1.1

SXM = 0 -
80386DX mode is selected.

SXM = 1 -
80386SX mode is selected.

Bit 13 - MODE486, 80486SX/DX Mode

MODE486 represents an inversion of the state of the MODE486 strapping option. See Section 4.1.1.

MODE486 = 0 -
The 80386SX/DX mode is selected and SXM selects between SX and DX.

MODE486 = 1 -
The 80486SX/DX mode is selected and SXM is ignored.

Bit 12 - EXCOP, External Coprocessor

EXCOP represents an inversion of the state of the EXCOP strapping option. See Section 4.1.4.

EXCOP = 0 -
An external 80387 coprocessor is not supported.

EXCOP = 1 -
An external 80387 coprocessor is supported.

Bit 11 - 3VBUFF, 3 Volt AT Buffer

3VBUFF represents the state of the 3VBUFFER strapping option. See Section 4.1.2

3VBUFF = 0 -
The AT Buffer operates at 5 volts.

3VBUFF = 1 -
The AT Buffer operates at 3.3 volts.

Bit 10 - 3VCORE, 3 Volt Core

3VCORE represents an inversion of the state of the 3VCORE strapping option. See Section 4.1.2

3VCORE = 0 -
The WD8110 Core logic is powered by 5 volts.

3VCORE = 1 -
The WD8110 Core logic is powered by 3.3 volts.

Bit 09 - CSCDE, Clock Speed Change Delay Enable

CSCDE works in conjunction with the CLK_SPD and ALT_CLK_SPD fields in the CPU Clock Control register at Port Address 1072H. CSCDE is provided for support of Intel 1X clock processors which require 1 ms for the CPU's PLL to stabilize after a frequency change.

For CSCDE to be effective the following parameters must be set:

- IBM Mode selected by bits 08:07 of this register, SCK(1:0) = 10.
- IBM 2X Clock Control Mode selected by IBM_2X (bit 13) = 1 in the Diagnostic Register at Port Address 9872H.

This mode also works for speed changes with an Intel CPU. However, Intel Clock Control Mode must still be selected by setting SCK(1:0) = 00 to stop the clock using the SCH or SCHH bits in the register at Port Address 1072H. See CSUDE bit 10 in register at Port Address 7472H.

CSCDE = 0 -
Clock Speed Change Delay disabled.

CSCDE = 1 -
A 1 to 2 ms delay is enforced between a speed change in the CPU clock and the deassertion of STP_REQ.

Bits 08:07 - SCK(1:0), Stop Clock Control Function Select

SCK(1:0)
08 07

0 0 - In Intel Mode, pin 56 provides the STP_REQ handshake with Intel CPUs that implement a stop clock hand shake. This is used to either stop the CPU clock at the next HOLD cycle when SCH in Register 1072H is set to one, or to do a halt initiated CPU clock stop when the SCHH bit in Port Address 1072H is set to one.

0 1 - In Cyrix Mode, pins 56 and 133 provide the SUSP, SUSPA handshake with Cyrix CPUs. This is used to either stop the CPU clock at the next HOLD cycle when SCH in Register 1072H is set to one, or to do a halt initiated CPU clock stop when the SCHH bit in Register 1072H is set to one.

1 0 - In IBM Mode, pins 56 and 133 provide the DFS_REQ, DFS_RDY clock frequency change handshake that occurs automatically whenever a clock speed change occurs, such as through AUT_FST

1 1 - Reserved. Do not use this configuration.

Bit 06 - ENSCK, Enable Stop Clock Handshake

ENSCK is the Master Enable for stop clock handshake functions when SCK(1:0) are set to either 00 or 01 (Intel or Cyrix mode). ENSCK has no effect when SCK(1:0) is set to 10 (IBM mode). The IBM CPU has an internal enable which performs the same function.

ENSCK = 0 -
SCK(1:0) modes 0X are disabled. However, the CPUCLK will still stop without using the handshake protocol.

ENSCK = 1 -
SCK(1:0) modes 0X are enabled.

Bit 05 - SMIFST, SMI Fast Handler Execution

SMIFST = 0 -
AUT_FST circuits not affected by SMI.

SMIFST = 1 -
AUT_FST circuitry switches the CPUCLK speed to the higher rate for the entire time SMI handler code is being executed plus 1 ms.

Bit 04 - ATPUEN, AT Bus Pullup Enable

ATPUEN = 0 -
Pullup resistors are not enabled.

ATPUEN = 1 -
Internal pullup resistors on the AT Data Bus SD(7:0) are enabled. The resistors are in the range of 30K to 100K ohms.

Bit 03 - IR12SL, IRQ12 Select

IR12SL controls the source of the IRQ12 (mouse) interrupt line presented to the Interrupt Controller.

IR12SL = 0 -
Interrupt as sampled by IRQSET1 (normal operation) is selected.

IR12SL = 1 -
IR12AL (bit 01 of this register) is selected.

Bit 02 - IR1SL, IRQ1 Select

IR1SL controls the source of the IRQ1 (keyboard) interrupt line presented to the Interrupt Controller.

IR1SL = 0 -
Interrupt as sampled by IRQSET1 (normal operation) is selected.

IR1SL = 1 -
IR1AL (bit 00 of this register) is selected.

Bit 01 - IR12AL, IRQ12 Alternate IRQ12 Source

When selected by IR12SL, IR12AL serves as IRQ12 to the Interrupt Controller. This allows software routines to force a hardware IRQ12 interrupt. IR12AL is not automatically cleared when IRQ12 is serviced, therefore it must be set/reset as needed.

Bit 00 - IR1AL, IRQ1 Alternate IRQ1 Source

When selected by IR1SL, IR1AL serves as IRQ1 to the Interrupt Controller. This allows software routines to force a hardware IRQ1 interrupt. IR1AL is not automatically cleared when IRQ1 is serviced, therefore it must be set/reset as needed.

4.2.8 Enhanced DMA Clock Registers

The WD8110 supports several enhanced DMA clocking features. To conserve power, the DMA clock can be stopped when DMA transfers are not occurring. On DMA channels 7:5, transfers can be accelerated by options to run the DMA controller clock at double speed (SYSCLK) and to eliminate the traditional wait state.

The WD8110/LV also features:

- Slow refresh
- Disable Interrupts from the Interrupt Controller

Port Address BC72H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
CH6_CLK		CH5_CLK		S_ REF	INT_ DIS	INT_ ST	SRLE

Signal Name	Default At RSTIN
All Signals	0

Bits 15:08 - Reserved

Bits 07:06 - CH6_CLK, Channel 6 DMA Clock

CH6_CLK
07 06
0 0 - SYSCLK ÷ 2, 1 Wait State
0 1 - SYSCLK, 1 Wait State
1 0 - SYSCLK ÷ 2, 0 Wait State
1 1 - Reserved

Bits 05:04 - CH5_CLK, Channel 5 DMA Clock

CH5_CLK
05 04
0 0 - SYSCLK ÷ 2, 1 Wait State
0 1 - SYSCLK, 1 Wait State
1 0 - SYSCLK ÷ 2, 0 Wait State
1 1 - Reserved

Bit 03 - S_REF, Slow Refresh

When Slow Refresh is enabled the DRAM refresh rate is slowed to 120 µs. This has no effect on the REF_DT toggle bit at Port Address 061H.

S_REF = 0 -
Slow Refresh disabled

S_REF = 1 -
Slow Refresh enabled

Bit 02 - INT_DIS, Interrupt Disable

Setting INT_DIS disables the interrupt from the Interrupt Controller. The command will not take effect immediately if the interrupt request signal from the interrupt controller is active. The command will take effect immediately if the interrupt request signal is inactive. This allows control of the interrupt regardless of the Operating System Privilege Level, since 'CLI' and 'STI' CPU instructions may be trapped.

INT_DIS = 0 -
Interrupt to CPU (INTRQ) enabled

INT_DIS = 1 -
Interrupt to CPU (INTRQ) disabled

Bit 01 - INT_ST, Interrupt Status

This enables reading of Interrupt Status regardless of Operating Privilege Level.

INT_ST = 0 -
Interrupt disable command has been performed.

INT_ST = 1 -
Interrupt disable command is pending.

Bit 00 - SRLE, Stop Request Latch Enable

With Intel processors, it may be necessary to guarantee that the $\overline{\text{STP\_REQ}}$ signal stays asserted until the stop grant bus cycle is issued. SRLE enforces that requirement. Note that SRLE only operates when Intel stop clock mode is selected (Stop Clock Control register at Port Address 8C72H bits 8:7 = 00).

SRLE = 0 -
$\overline{\text{STP\_REQ}}$ may be de-asserted before the stop grant bus cycle is issued.

SRLE = 1 -
$\overline{\text{STP\_REQ}}$ will not be de-asserted before the stop grant bus cycle is issued.

Port Address B472H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
		CH7_CLK		S_DCLK			

Signal Name	Default At RSTIN
All Signals	0

Bits 15:06 - Reserved. Must be set to 0

Bits 05:04 - CH7_CLK, Channel 7 DMA Clock

CH7_CLK
05 04
0 0 - SYSCLK ÷ 2, 1 Wait State
0 1 - SYSCLK, 1 Wait State
1 0 - SYSCLK ÷ 2, 0 Wait State
1 1 - Reserved

Bit 03 - S_DCLK, Stop DMA Clock

Setting S_DCLK causes the DMA clock to stop while there is no DMA activity. Upon any unmasked DMA request (DRQIN), the DMA clock starts up again and continues to run until 16 DMA clocks after the end of the DMA Acknowledge (DACKEN).

S_DCLK = 0 -
Disable Stop DMA Clock

S_DCLK = 1 -
Enable Stop DMA Clock

Bit 02:00 - Reserved. Must be set to 0.

4.3 ROM BANK SELECTION

Port Address C072H - Bits 15:12 Read only
Bits 11:00 Read and Write

This register performs two major functions:

- Reads the strap options CLKTEST, $\overline{\text{WTKMODE}}$ and 1X/$\overline{\text{2X}}$. The remaining strap options are read at Port Address 8C72H.
- Provides support for larger BIOS ROMs

To make it possible for the WD8110/LV to use larger BIOS ROMs, three Bank Select output pins (ROMBA18:16) have been provided. These signals normally connect to ROM address inputs 18:16 for support of up to 512K by 8 ROM or 19:17 for support of up to 1M by 8 ROM. ROMBA18:16 can be programmed to any value for each of the 64K address spaces 0CXXXXH, 0DXXXXH, 0EXXXXH and 0FXXXXH.

If ROMBA18:16 are connected to ROM address inputs 18:16, each of the 64K address spaces can access all 64K pages within the ROM. If ROMBA18:16 are connected to ROM address inputs 19:17, address spaces 0CXXXXH and 0EXXXXH can only access even numbered 64K pages in the ROM while 0DXXXXH and 0FXXXXH can only access odd numbered 64K pages.

NOTE

ROMBA18:16 are active regardless of how much ROM space has been allocated. If only 0E0000H through 0FFFFH of ROM has been enabled, the fields that control address spaces 0CXXXXH and 0DXXXXH will not perform any useful function.

15	14	13	12	11	10	09	08
RSVD	- Strap Options - CLK_ TEST	WTK_ MODE	1X/ 2X	Address 0CXXXXH CA18	CA17	CA16	Addre DA18

07	06	05	04	03	02	01	00
ss 0DXXXXH DA17	DA16	Address 0EXXXXH EA18	EA17	EA16	Address 0FXXXXH FA18	FA17	FA16

Signal Name	Default At RSTIN
Bit 15	0
Strap Options	None
CA18	1
CA17:16	0
DA18	1
DA17	0
DA16	1
EA18:17	1
EA16	0
FA18:16	1

Bit 15 - Reserved, must be written with a 0 and currently is read back as 0.

Bit 14 - CLKTEST, Clock Test

Represents the state of the CLKTEST strapping option. This test is for factory use only.

CLKTEST = 0 -
Normal operation.

CLKTEST = 1 -
Test Mode.

Bit 13 - WTKMODE, Weitek Mode

This strapping option is used to indicate that a Weitek numeric processor is supported.

WTKMODE = 0 -
Weitek Mode is not enabled and pins 39, 4 and 56 function as SMEMW, SMEMR and SUSP/STP_REQ.

WTKMODE = 1 -
Weitek Mode is enabled and pins 39, 4 and 56 function as WTKIRQ13, LOWMEG and A29, respectively.

Bit 12 - 1X/2X, Clock Select

1X/2X = 0 -
Processor uses a 2X clock input.

1X/2X = 1 -
Processor uses a 1X clock input.

Bits 11:09 - CA18:16, C Address Range

This field is placed on output pins ROMBA18:16 whenever CPU address bits 17:16 are 00, such as in CPU address space 0C0000H through 0CFFFFH .

Bits 08:06 - DA18:16, D Address Range

This field is placed on output pins ROMBA18:16 whenever CPU address bits 17:16 are 01, such as in CPU address space 0D0000H through 0DFFFFH .

Bits 05:03 - EA18:16, E Address Range

This field is placed on output pins ROMBA18:16 whenever CPU address bits 17:16 are 10, such as in CPU address space 0E0000H through 0EFFFFH .

Bits 02:00 - FA18:16, F Address Range

This field is placed on output pins ROMBA18:16 whenever CPU address bits 17:16 are 11, such as in CPU address space 0F0000H through 0FFFFFH .

5.0 AT BUS

This section describes the logic required to control the interrupts and timing between the AT bus and the System Controller.

5.1 INTERRUPT MULTIPLEXING

To reduce the number of pins required, the System Controller generates and outputs the MXCTL(2:0) and DACKEN signals used by external logic to multiplex the DACKs and IRQs down to single inputs. See Figure 5-1.

MXCTL(2:0) are set to 100 during a System Reset (RSTIN) to provide a Bus Reset (BUS_RST) and to determine whether the ROM is on the AT Bus or RA Bus. See Table 5-1.

5.1.1 DMA Acknowledge DACK(7:5), (3:0)

For desktop systems, either a Western Digital WD7615 or a 74F138 3-to-8 Decoder uses MXCTL(2:0) to generate the DACK(7:5) and DACK(3:0), which are applied to the AT Bus. The unused combination develops the AT BUS_RST (bus reset). For Laptop systems a 74FCT 138 3-to-8 Decoder is used instead of the WD7615. The decoder is enabled by the DACKEN signal from the System Controller.

5.1.2 Interrupt Requests

The Interrupt Requests are multiplexed by the WD76C30A. The multiplexing is performed as shown in Table 5-1 and Figure 5-1 and provides the System Controller with the IRQSET1 and IRQSET0 signals.

IRQSET1 and IRQSET0 and PMCIN are sampled by the System Controller using an internal clock which is twice the frequency of SYSCLK. This allows all PMC and IRQ lines to be sampled within 500 ns, when SYSCLK is 8 MHz.

The ROM AT BUS input is sampled from IRQSET0 at the completion of a RSTIN to determine BIOS ROM bus location. If ROM AT BUS is sampled low, an 8-bit ROM is on the RA Bus. If ROM AT BUS is sampled high, an 8-bit ROM is on the AT Bus. This allows the use of a greater number of EPROMS in mixed voltage systems because the requirement for 3 volt EPROMs that can tolerate 5 volt inputs can be eliminated.

The RESCPU and A20GT inputs come from the keyboard controller.

5.1.3 AT Address Bus, Data Bus and Terminal Count (TC) Signal

The AT Address Bus SA(19:2) is generated from A(19:2) with external tristate buffers in the WD7625 or WD7615.

The AT Data Bus SD(15:0) is directly controlled by WD8110/LV.

The TC signal is generated by an external gate when DACKEN and CSEN are both asserted.

5.2 POWER MANAGEMENT CONTROL PMCIN

The power control signals are placed on the PMCIN input pin by way of an eight to one multiplexer, controlled by the MXCTL(2:0) signals from the System Controller. The WD8110/LV may use a WD7625 to perform this function. See Figure 5-1. Bits 14 and 13 of Port 1872H (Section 5.3) control the power down of the processor and peripheral.

MXCTL 2 1 0	DACKEN	IRQSET0	IRQSET0	PMCIN
0 0 0	DACK0	$\overline{IRQ8}$	IRQ12	$\overline{TURBO}$
0 0 1	DACK1	IRQ9	IRQ1	PROC_PWR_GOOD
0 1 0	DACK2	IRQ10	A20GT	LCL_RQ or User Defined
0 1 1	DACK3	IRQ11	IRQ3	User Defined
1 0 0	BUS_RST	ROM AT BUS	IRQ4	User Defined
1 0 1	DACK5	$\overline{RESCPU}$	IRQ5	User Defined
1 1 0	DACK6	IRQ14	IRQ6	User Defined
1 1 1	DACK7	IRQ15	IRQ7	User Defined

TABLE 5-1. MXCTL(2:0) DECODING

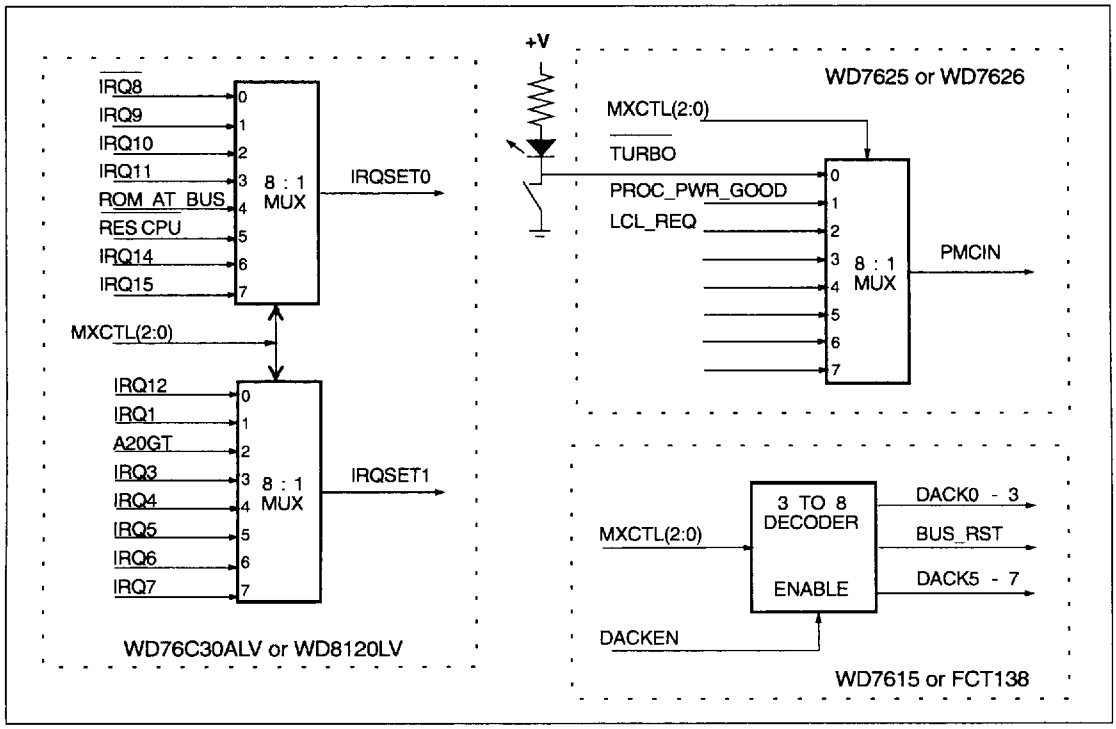


FIGURE 5-1. MXCTL(2:0) MULTIPLEXING

5.3 BUS TIMING AND NUMERIC PROCESSOR

5.3.1 Bus Timing, and Power Down Register

Port Address 1872H – Read and Write

15	14	13	12	11	10	09	08
Res.	PRO_ PD	FPD		BUS_MOD		BRQ_DEL	

07	06	05	04	03	02	01	00
BAK_DEL		WSI 16	WSM 16	WSI8		WSM8	

Signal Name	Default At RSTIN
Bit 15	0
PRO_PD	0
Bit 12	None
FPD	0
BUS_MOD	00
BRQ_DEL	00
BAK_DEL	11
WSI_16	0
WSM_16	0
WS18	10
WSM8	10

Bit 15 - Reserved. Must be set to 0.

Bit 14 - PRO_PD, Processor Power Down

When PRO_PD has been changed from zero to one, a power down sequence for the CPU will be initiated at the next Halt State and the expansion bus continues to operate normally. The processor should not be powered down if DMA cycles are likely to occur. When PRO_PD is set and a halt state occurs, the processor inputs are ignored and appear to the WD8110/LV to be in the passive state.

The input buffers connected to the processor signals do not consume power even if the processor signals do not reach ground. The internal pullups on inputs connecting to the processor are disabled to reduce power. PMC output 5 from Port Address 7072H (Processor Power Down) is set. This can be used to control the power transistor and turn off the power to the processor. All outputs going to the processor will be tristated.

When an unmasked interrupt, DRQ or NMI occurs, PMC output 5 is reset, re-powering the processor. A voltage comparator should be used to generate a Processor Power Good (PPG) signal. The PPG signal is sampled by bit 01 of the PMC Input Register at Port Address 8872H. When PPG is high, the outputs to the processor are driven and the processor is reset.

PRO_PD = 0 -
Normal processor power.

PRO_PD = 1 -
Start processor power down sequence.

Bit 13 - FPD, Full Power Down

When FPD equals one and a halt state occurs, all processor and peripheral outputs except the PMC, DRAM controls and RA/ED bus are tristated and all inputs except RSTIN, CLK14 and PMC inputs are ignored. CAS before RAS refresh will be performed if enabled by Port Address 2072H. All circuitry except the PMC and refresh timer logic is stopped and PMC output 7 (Full Power Down) from Port Address 7072H is set. This enables the powering down of all chips except DRAM, WD8110/LV, WD76C20, WD76C30A and WD90C20. The WD76C20 provides PDREF (a 64 KHz refresh signal on input pin 129) during the power down mode. This signal is then gated by the System Controller to the REFRESH signal as an output on pin 40.

When a PMC interrupt occurs, PMC output 7 at Port Address 7072H is reset, enabling the power up sequence. A CPURES and BUS_RST (see Figure 5-1) are asserted until the PMCIN 01 PPG at Port Address 8872H input is high. The tristated outputs are restored and the inputs are no longer masked. Refer to Section 8.15 for more details regarding Suspend and Resume.

FPD remains a 1 until replaced by a 0.

FPD = 0 -
No power down.

FPD = 1 -
Full power down and in standby mode.

Bit 12 - Reserved. Must be set to 0.

Bits 11:10 - BUS_MOD, Bus Mode

The System Controller defaults to Mode 00 at power up. Therefore, the AT bus logic clock is controlled by BCLK2 and is asynchronous with CPUCLK (see Figure 4-1). This allows CPUCLK to be faster than the AT Bus and vary without affecting bus timing. Normally, BCLK2 is 16 MHz as supplied by the WD76C30A. SYSCLK is a divide by two of the bus logic clock. So, if BCLK2 is 16 MHz at power up, it is divided by two again, providing a SYSCLK clock rate of 4 MHz until programmed to Mode 01. In Mode 01, the SYSCLK rate is 8 MHz for a BCLK2 of 16 MHz. Both Mode 00 and 01 are asynchronous and require appropriate synchronization delays to be established by the BRQ_DEL and BAK_DEL fields of this register.

In Modes 10 and 11, SYSCLK is synchronous with CPUCLK and synchronization delays are not needed. The bus clock mode may need to be reprogrammed when the processor clock changes.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BUS_MOD
11 10

- 0 0 - Bus logic uses BCLK2 divided by 2.
- 0 1 - Bus logic uses BCLK2 divided by 1.
- 1 0 - Bus logic uses CPUCLK divided by 2.
- 1 1 - Bus logic uses CPUCLK divided by 1.

Bits 09:08 - BRQ_DEL, Bus Request Delay

An asynchronous AT bus state machine requires a synchronization delay at the start of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BRQ_DEL
09 08

- 0 0 - 1 Bus clock delay.
- 0 1 - .5 Bus clock delay.
- 1 0 - No clock delay.
- 1 1 - Reserved.

Bits 07:06 - BAK_DEL, Bus Acknowledge Delay

The AT bus state machine has several options available for signaling the CPU control logic that an AT bus cycle has completed. The timing of this signal determines AT bus hold time for the data and address. Proper timing is determined by the CPU speed, AT bus speed and whether they are synchronous or asynchronous. The delay settings listed here are referenced to the trailing edge of the AT command strobe.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BAK_DEL
07 06

- 0 0 - No delay.
- 0 1 - -.5 Bus logic clock delay.
- 1 0 - -1 Bus logic clock delay.
- 1 1 - +.5 Bus logic clock delay.

Bit 05 - WSI16, Wait State for 16 bit I/0

WSI16 = 0 -
1 SYSCLK clock wait state.

WSI16 = 1 -
2 SYSCLK clock wait states.

Bit 04 - WSM16, Wait State for 16 bit Memory

WSM16 = 0 -
1 SYSCLK wait state.

WSM16 = 1 -
2 SYSCLK clock wait states.

Bits 03:02 - WSI8, Wait State for 8 bit I/O

WSI8
03 02

0 0 - 2 SYSCLK clock wait states.

0 1 - 3 SYSCLK clock wait states.

1 0 - 4 SYSCLK clock wait states.

1 1 - 5 SYSCLK clock wait states.

Bits 01:00 - WSM8, Wait State for 8 bit Memory

WSM8
01 00

0 0 - 2 SYSCLK clock wait states.

0 1 - 3 SYSCLK clock wait states.

1 0 - 4 SYSCLK clock wait states.

1 1 - 5 SYSCLK clock wait states.

5.3.2 Numeric Processor Busy ($\overline{\text{NPBUSY}}$) Reset

Port Address 0F0H – Write only

Writing any data to this port resets the 80387 busy signal (de-asserts $\overline{\text{NPBUSY}}$). The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

5.3.3 Numeric Processor Reset (NPRST)

Port Address 0F1H – Write only

Writing any data to this port asserts NPRST and resets the 80387. The main processor is wait stated for 128 clocks when writing to this port. The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

CPU SPEED	AT BUS SPEED	AT BUS MODE	BUS MOD	BRQ DEL	BAK DEL
33.3 MHz	8 MHz	ASYNC	0X	01	11
25.0 MHz	8 MHz	ASYNC	0X	01	00
20.0 MHz	10 MHz	SYNC	10	10	10
20.0 MHz	8 MHz	ASYNC	0X	01	00
16.0 MHz	8 MHz	SYNC	10	10	10

TABLE 5-2. BUS TIMING PARAMETERS

5.4 DMA CONTROL

The System Controller contains two DMA controllers. DMA Controller 1 is in the I/O address space from 000H to 00FH and is used for 8-bit transfers. DMA Controller 2 is in the I/O space from 0C0H to 0DEH and is used for 16-bit transfers. Channel 0 of DMA Controller 2 is used to cascade DMA controller #1. Table 5-4 identifies the Controller/ Channel location and function.

AT Bus DMA Channel	DMA Controller	Transfer Type
0	#1 Channel 0	8-bit
1	#1 Channel 1	8-bit
2	#1 Channel 2	8-bit
3	#1 Channel 3	8-bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16-bit
6	#2 Channel 2	16-bit
7	#2 Channel 3	16-bit

TABLE 5-3. DMA TRANSFER TYPES

5.4.1 Transfer Modes

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode or Cascade Mode.

Refer to Section 5.4.12 - Mode Register, bits 7 and 6 for programming.

Demand Mode - 00

In demand mode, a transfer continues to take place until DRQ is de-asserted or a Terminal Count (TC) is reached. If the DRQ is de-asserted, the bus will be released. If DRQ is re-asserted, the transfer will resume. The address and word count behave as in single mode.

Single Transfer Mode - 01

In single transfer mode, the channel makes one transfer for each request. The word count is decremented and the address is incremented or decremented at the end of each transfer. When the word count goes from 0000H to FFFFH, a Terminal Count (TC) is generated. To start a transfer, the DRQ should be asserted until a DACK is received. If the DRQ is asserted through the cycle, only one transfer will take place. The DRQ must be de-asserted and then re-asserted to start another transfer. The bus is released between transfers.

Block Transfer Mode - 10

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK is asserted. Block mode should be used with caution since refresh is locked out. The address and word count behave as in single mode.

Cascade Mode - 11

Cascade mode is used for bus master transfers and to cascade DMA controller #2 to DMA controller #1. A channel in cascade mode gets the bus when a DRQ is asserted but the word count and address are ignored. The channel holds the bus until DRQ is de-asserted. The $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ and $\overline{MEMW}$ signals must be generated by the bus master device. The addresses from the System Controller are tristated when the MASTER signal is asserted.

5.4.2 Transfer Types

There are three types of transfers: verify, write and read.

Refer to Section 5.4.12 - Mode Register, bits 3 and 2 for programming.

Verify - 00

A verify transfer is a pseudo transfer that does not generate $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ or $\overline{MEMW}$ signals.

Write - 01

A write transfers data from an I/O device to memory.

Read - 10

A read transfers data from memory to an I/O device.

5.4.3 Autoinitialize

A channel may be programmed to autoinitialize for any transfer type. When a TC is reached in this mode the channel is loaded with the original word count and address and is ready to start another transfer.

Refer to Section 5.4.12 - Mode Register, bit 4 for programming.

5.4.4 Priority

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority.

5.4.5 Extended Write

In normal timing, the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ pulse is two clock cycles and the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ is one clock cycle. If extended write is selected, the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ will be the same as the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$.

5.4.6 Base and Current Address

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{REFRESH}}$ is asserted, indicating a refresh cycle. Only address bits A(23:16) (from the page register) and bits A(10:0) (from the refresh counter) are meaningful during refresh. The address counter is incremented on the rising edge of $\overline{\text{REFRESH}}$.

5.4.7 Base and Current Word Count

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current word count is decremented during a transfer.

10-BIT MODE I/O ADDRESS IN HEX	16-BIT MODE I/O ADDRESS IN HEX	READ/WRITE	DMA CONTROLLER	FUNCTION
000	0000	Read/Write	1	Channel 0 Address
001	0001	Read/Write	1	Channel 0 Word Count
002	0002	Read/Write	1	Channel 1 Address
003	0003	Read/Write	1	Channel 1 Word Count
004	0004	Read/Write	1	Channel 2 Address
005	0005	Read/Write	1	Channel 2 Word Count
006	0006	Read/Write	1	Channel 3 Address
007	0007	Read/Write	1	Channel 3 Word Count
008	0008	Read	1	Status
008	0008	Write	1	Command Register
009	0009	Write	1	Request Register
00A	000A	Write	1	Single Mask
00B	000B	Write	1	Mode Register
00C	000C	Write	1	Clear Pointer
00D	000D	Write	1	Master Clear
00E	000E	Write	1	Clear Mask
00F	000F	Write	1	Mask All
080-09F	0080-008F			DMA Page Register
0C0	00C0	Read/Write	2	Channel 0 Address
0C2	00C2	Read/Write	2	Channel 0 Word Count
0C4	00C4	Read/Write	2	Channel 1 Address
0C6	00C6	Read/Write	2	Channel 1 Word Count
0C8	00C8	Read/Write	2	Channel 2 Address
0CA	00CA	Read/Write	2	Channel 2 Word Count
0CC	00CC	Read/Write	2	Channel 3 Address
0CE	00CE	Read/Write	2	Channel 3 Word Count
0D0	00D0	Read	2	Status
0D0	00D0	Write	2	Command Register
0D2	00D2	Write	2	Request Register
0D4	00D4	Write	2	Single Mask
0D6	00D6	Write	2	Mode Register
0D8	00D8	Write	2	Clear Pointer
0DA	00DA	Write	2	Master Clear
0DC	00DC	Write	2	Clear Mask
0DE	00DE	Write	2	Mask All
B872	B872	Read	1, 2	DMA Mode Shadow

TABLE 5-4. DMA CONTROLLER/CHANNEL FUNCTION MAP

5.4.8 Command Register

Port Addresses 008H, 0D0H – Write only

This write only register may be read by the DMA Shadow Register 3 at Port 4C72H (see Section 8.14.3). The Command Register is reset by RSTIN or by writing any data to Port Address 00DH or 0DAH (see Section 5.4.14).

7	6	5	4	3	2	1	0
		EX_ WR	RO_ PRI	0	CO_ DIS		

Signal Name	Default At RSTIN
All signals	0

Bits 7:6 - Not used, state is ignored

Bit 5 - EX_WR, Extended Write

Bit 4 - RO_PRI, Rotating Priority

Bit 3 - Must be set to 0

Bit 2 - CO_DIS, Controller Disabled

Bits 1:0 - Not used, state is ignored

5.4.9 Status Register

Port Addresses 008H, 0D0H – Read only

Bits 3:0 are reset by RSTIN, writing any data to Port Address 00DH or 0DAH (see Section 5.4.14) or when read by a Status Read Command.

Channels 7:5 are accessed at Port Address 0D0H
Channel 4 is not available
Channels 3:0 are accessed at Port Address 008H

7	6	5	4	3	2	1	0
CH3_ DRQ	CH2_ DRQ	CH1_ DRQ	CH0_ DRQ	CH3_ TC	CH2_ TC	CH1_ TC	CH0_ TC

Signal Name	Default At RSTIN
CH3_DRQ - CH0_DRQ	None
CH3_TC - CH0_TC	0

Bit 7 - CH3_DRQ, Channel 3 DRQ active

Bit 6 - CH2_DRQ, Channel 2 DRQ active

Bit 5 - CH1_DRQ, Channel 1 DRQ active

Bit 4 - CH0_DRQ, Channel 0 DRQ active

Bit 3 - CH3_TC, Channel 3 has reached TC

Bit 2 - CH2_TC, Channel 2 has reached TC

Bit 1 - CH1_TC, Channel 1 has reached TC

Bit 0 - CH0_TC, Channel 0 has reached TC

5.4.10 Request Register

Port Addresses 009H, 0D2H – Write only

Each channel may be started by a software request. These requests are not affected by the Mask Register. The Request Register is reset by RSTIN or by writing any data to Port Address 00DH or 0DAH (see Section 5.4.14).

Channels 7:5 are accessed at Port Address 0D2H
Channel 4 is not available
Channels 3:0 are accessed at Port Address 009H

7	6	5	4	3	2	1	0
					CRQ	CH#	

Signal Name	Default At RSTIN
All signals	0

Bits 7:3 - Not used, state is ignored

Bit 2 - CRQ, Channel Requested

Bits 1:0 - CH#, Channel Number Requested

CH#1	0
0	0 - Channel 0
0	1 - Channel 1
1	0 - Channel 2
1	1 - Channel 3

5.4.11 Mask Registers

Each channel has a mask bit associated with it. If it is set, the channel is disabled. The bits may be set or reset by software, or set by a Terminal Count (TC) if the channel is not in autoinitialize mode. All the bits are set by a RSTIN, or by writing any data to Port Address 00DH or 0DAH (see Section 5.4.14).

5.4.11.1 Single Mask Register

Port Addresses 00AH, 0D4H – Write only

Channels 7:5 are accessed at Port Address 0D4H
Channel 4 is not available
Channels 3:0 are accessed at Port Address 00AH

7	6	5	4	3	2	1	0
					SE_ MA	CH#	

Signal Name	Default At RSTIN
All signals	1

Bits 7:3 - Not used, state is ignored

Bit 2 - SE_MA, Set Mask

SE_MA = 0 -
Clear Mask

SE_MA = 1 -
Set Mask

Bits 1:0 - CH#, Channel Number Requested

CH# 1	0	
0	0	- Channel 0
0	1	- Channel 1
1	0	- Channel 2
1	1	- Channel 3

5.4.11.2 Clear Mask Register

Port Addresses 00EH, 0DCH – Write only

Writing any data to this register resets all Masks. The data is ignored.

Channels 7:5 are accessed at Port Address 0DCH
Channel 4 is not available
Channels 3:0 are accessed at Port Address 00EH

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7:0 - Not used, state is ignored

5.4.11.3 Mask Multiple Register

Port Addresses 00FH, 0DEH – Write only

Channels 7:5 are accessed at Port Address 0DEH
Channel 4 is not available
Channels 3:0 are accessed at Port Address 00FH

7	6	5	4	3	2	1	0
				CH3_ MA	CH2_ MA	CH1_ MA	CH0_ MA

Signal Name	Default At RSTIN
All signals	1

Bits 7:4 - Not used, state is ignored

Bit 3 - CH3_MA, Channel 3 Mask

Bit 2 - CH2_MA, Channel 2 Mask

Bit 1 - CH1_MA, Channel 1 Mask

Bit 0 - CH0_MA, Channel 0 Mask

5.4.12 Mode Register

Port Addresses 00BH, 0D6H – Write only

These registers are shadowed and may be read back through DMA Shadow Registers 1:3 at Port Addresses 3C72H, 4472H and 4C72H, described in Sections 8.13.(1:3).

These registers select the mode and type of transfer for each channel. Refer to Sections 5.4.1 through 5.4.1.4 for a description of the Transfer Modes, Sections 5.4.2 through 5.4.2.3 for a description of the Transfer Types and Section 5.4.3 for a description of Autoinitialize.

Channels 7:5 are accessed at Port Address 0D6H
Channel 4 is not available
Channels 3:0 are accessed at Port Address 00BH

7	6	5	4	3	2	1	0
TRA_ MOD		AD_ DEC	AUTO	TRA_ TYP		CHA# SEL	

Signal Name	Default At RSTIN
All signals	None

Bits 7:6 - TRA_MOD, Transfer Mode

TRA_MOD
7 6
0 0 - Demand
0 1 - Single
1 0 - Block
1 1 - Cascade

Bit 5 - AD_DEC, Address Decrement

AD_DEC = 0
Address is incremented.

AD_DEC = 1
Address is decremented after each DMA cycle.

Bit 4 - AUTO, Autoinitialize

AUTO = 0
Autoinitialization is disabled.

AUTO = 1
Autoinitialization is enabled.

Bits 3:2 - TRA_TYP, Transfer Type

TRA_TYP
3 2
0 0 - Verify
0 1 - Write
1 0 - Read
1 1 - Not used

Bits 1:0 - CHA#_SEL, Channel Select

CHA#_SEL
1 0
0 0 - Channel 0
0 1 - Channel 1
1 0 - Channel 2
1 1 - Channel 3

5.4.13 Clear Pointer Register

Port Addresses 00CH, 0D8H – Write only

Each DMA controller has a pointer flip-flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer changes state. When the flip-flop is reset, bits 7:0 are accessed, and when it is set, bits 15:8 are accessed. The pointer is reset by writing any data to the Clear Pointer Register, or to Port Address 00DH or 0DAH (see Section 5.4.14). In either case, the data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7:0 - Not used, state is ignored

5.4.14 Master Clear Register

Port Addresses 00DH, 0DAH – Write only

Writing any data to the Master Clear Register will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip-Flop

All data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7:0 - Not used, state is ignored

5.4.15 DMA Mode Shadow Register

Port Address B872H – Read only

This register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices. Refer to Section 8.14 for more information regarding the DMA Shadow Registers.

15	14	13	12	11	10	09	08
DMA1 MODE							

07	06	05	04	03	02	01	00
DMA2 MODE							

Signal Name	Default At RSTIN
DMA1 MODE	0
DMA 2 MODE	0

Bits 15:08 - DMA 1 MODE

DMA 1 MODE contains a copy of the data written into the DMA1 Mode Register located at I/O address 00BH (see Table 5-4).

Bits 07:00 - DMA 2 MODE

DMA 2 MODE contains a copy of the data written into the DMA2 Mode Register located at I/O address 0D6H (see Table 5-4).

5.5 SYSTEM CONTROLLER 8259 INTERRUPT CONTROLLERS

The System Controller contains two interrupt controllers. Interrupt Controller 1 is in the I/O space of 020H to 021H and Interrupt Controller 2 is in the I/O space of 0A0H to 0A1H. Interrupt 2 of Interrupt Controller 1 is used to cascade Interrupt Controller 2.

5.5.1 Interrupt Sequence

1. When an interrupt arrives from a peripheral device, the interrupt may only be programmed to be edge sensitive. In this mode, the interrupt must go low and high for each interrupt. The interrupt sets the appropriate bit in the Interrupt Request Register (IRR).

SYSTEM INTERRUPT	INTERRUPT CONTROLLER	USE
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3:7	#1 Level 3:7	AT Bus
8	#2 Level 0	RTC
9:12	#2 Level 1:4	AT Bus
13	#2 Level 5	Co-Processor
14:15	#2 Level 6:7	AT Bus

TABLE 5-5. INTERRUPT SEQUENCE

2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

Fixed

In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

Automatic Rotation

In automatic rotation, the last interrupt serviced has the lowest priority.

Specific Rotation

In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example, if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3 and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA, causing the interrupt controller to send a vector to the CPU, set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower are inhibited unless programmed for special mask mode.

6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's, Specific, Non-specific and Automatic.

Specific

An EOI is issued by software for a specific interrupt.

Non-Specific

A non-specific EOI is also issued by software. The hardware generates an EOI for the highest level active interrupt.

Automatic

An automatic EOI is a non-specific EOI that is caused by the second INTA.

The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e., allow higher interrupts to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see whether any other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

5.5.2 Setup - Initialization Command Words (ICW)

The interrupt controllers are set up by writing a series of Initialization Command Words (ICW). The sequence is started by writing a one to bit 4 of ICW1. If ICW4 is to be included in the sequence, a one must also be written to bit 0 of the ICW1.

Interrupt Controller	Address Hex	Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

TABLE 5-6. INTERRUPT CONTROLLER FUNCTION MAP

5.5.2.1 ICW1 - Initialization Command Word 1

Port Addresses 020H, 0A0H – Write only

Bit 4 of this register must be set to 1 or it will be interpreted as OCW2 or OCW3.

7	6	5	4	3	2	1	0
			S_S	L_T		N C_M	ICW 4

Signal Name	Default At RSTIN
All signals	None

Bit 7:5 - Not used, state is ignored

Bit 4 - S_S, Start Sequence

S_S Must be set to 1

Bit 3 - L_T, Level Trigger

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

L_T = 0 -
Edge Triggered Mode is selected.

L_T = 1 -
Level Triggered Mode is selected. EN_LVL (bit 00) in Port A872H must first be set to 1.

Bit 2 - Not Used, state is ignored

Bit 1 - N C_M, Not Cascade Mode

N C_M = 0 -
Cascade Mode selected

N C_M = 1 -
Single Mode selected

Bit 0 - ICW4, Initialization Control Word 4

ICW4 = 0 -
ICW4 not included in sequence

ICW4 = 1 -
ICW4 is included in sequence

5.5.2.2 ICW2 - Initialization Command Word 2

Port Addresses 021H, 0A1H – Write only

For Suspend/Resume or Hibernation operations this register may be read at Port Address D472H. Refer to Section 8.10.

7	6	5	4	3	2	1	0
Interrupt Vector							

Signal Name	Default At RSTIN
All signals	None

Bits 7:3 - Interrupt Vector

Bits 2:0 - Not used, state is ignored

5.5.2.3 ICW3 - Initialization Command Word 3

Port Addresses 021H – Write only

This address accesses only Interrupt Controller 1.

7	6	5	4	3	2	1	0
0	0	0	0	0	I2 H_L	0	0

Signal Name	Default At RSTIN
All signals	None

Bits 7:3 - Not used, must be set to 0

Bit 2 - I2 H_L, Interrupt 2 Has Slave

I2 H_L = 0 -
Interrupt 2 does not have the Slave

I2 H_L = 1 -
Interrupt 2 has the Slave

Bits 1:0 - Not used, must be set to 0

Port Addresses 0A1H – Write only

This address accesses only Interrupt Controller 2.

7	6	5	4	3	2	1	0
0	0	0	0	0	Slave ID		

Signal Name	Default At RSTIN
All signals	None

Bits 7:3 - Not used, must be set to 0

Bits 2:0 - Slave ID

5.5.2.4 ICW4 - Initialization Command Word 4

Port Addresses 021H, 0A1H – Write only

For Suspend/Resume or Hibernation operations this register may be read at Port Address D472H. Refer to Section 8.10.

A Slave does not have ICW4.

7	6	5	4	3	2	1	0
0	0	0	SF NM	0	0	AUT EOI	1

Signal Name	Default At RSTIN
All signals	None

Bits 7:5 - Not used, must be set to 0

Bit 4 - SFNM, Special Fully Nested Mode

SFNM = 0 -
Not Special Fully Nested Mode

SFNM = 1 -
Special Fully Nested Mode

Bits 3:2 - Not used, must be set to 0

Bit 1 - AUT_EOI, Auto End Of Interrupt

AUT_EOI = 0 -
Normal End Of Interrupt

AUT_EOI = 1 -
Automatic End Of Interrupt

Bit 0 - Not used, must be set to 1

5.5.3 Operation

Once the interrupt controllers are set up, they may be programmed by Operation Control Words One through Three (OCW1:3).

5.5.3.1 OCW1 - Operation Control Word 1

Port Addresses 021H, 0A1H – Write only

7	6	5	4	3	2	1	0
INT 7_M	INT 6_M	INT 5_M	INT 4_M	INT 3_M	INT 2_M	INT 1_M	INT 0_M

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Interrupt 7 Mask

Bit 6 - Interrupt 6 Mask

Bit 5 - Interrupt 5 Mask

Bit 4 - Interrupt 4 Mask

Bit 3 - Interrupt 3 Mask

Bit 2 - Interrupt 2 Mask

Bit 1 - Interrupt 1 Mask

Bit 0 - Interrupt 0 Mask

5.5.3.2 OCW2 - Operation Control Word 2

Port Addresses 020H, 0A0H – Write only

For Suspend/Resume or Hibernation operations this register may be read at Port Address D472H. Refer to Section 8.10.

7	6	5	4	3	2	1	0
EOI_CONT			0	0	INT_LEV		

Signal Name	Default At RSTIN
All signals	None

Bits 7:5 - EOI_CONT, End Of Interrupt

EOI_CONT
7 6 5
0 0 0 - Clear Rotate On Automatic EOI
0 0 1 - Non-specific EOI
0 1 0 - Not used
0 1 1 - Specific EOI
1 0 0 - Set Rotate on Automatic EOI
1 0 1 - Rotate on Non-specific EOI
1 1 0 - Set Priority
1 1 1 - Rotate on Specific EOI

Bits 4:3 - Must be set to 0

Bits 2:0 - INT_LEV, Interrupt Level

To enable the setting of the interrupt level (INT_LEV), EOI_CONT must be set to 1 1 0 (Set Priority).

INT_LEV
2 1 0
0 0 0 - Interrupt Level 0
⋮
1 1 1 - Interrupt Level 7

5.5.3.3 OCW3 - Operation Control Word 3

Port Addresses 020H, 0A0H – Write only

For Suspend/Resume or Hibernation operations this register may be read at Port Address D472H. Refer to Section 8.10.

7	6	5	4	3	2	1	0
0	SMM		0	1	P_C	IRR_ISR	

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Must be set to 0

Bits 6:5 - SMM, Special Mask Mode

SMM
6 5
0 0 - Not used
0 1 - Not used
1 0 - Reset Special Mask Mode
1 1 - Set Special Mask Mode

Bit 4 - Must be set to 0

Bit 3 - Must be set to 1

Bit 2 - P_C, Poll Command

P_C = 0 -
No Poll Command

P_C = 1 -
Poll Command

Bits 1:0 - IRR_ISR, Interrupt Request Register and Interrupt Service Register

IRR_ISR
1 0
0 0 - Not used
0 1 - Not used
1 0 - Read Interrupt Request Register
1 1 - Read Interrupt Service Register

5.6 SYSTEM CONTROLLER 8254 TIMER

The System Controller contains an 8254 equivalent timer containing three independent counters. All the timers run off of a 1.19 MHz clock derived from the 14.318 MHz clock input. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61H, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initialize a counter, the Control Word must be written, followed by one or two bytes of count if needed. Refer to Table 5-7 for the correct Control Word Format. Each counter may be programmed to count in BCD or binary.

I/O Address	Use	Read/Write
040H	Timer 0 Count/Status	Read/Write
041H	Timer 1 Count/Status	Read/Write
042H	Timer 2 Count/Status	Read/Write
043H	Control Word	Write

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

5.6.1 Setup

Each counter may be set in one of six modes by writing a Control Word (format 1). The Control Word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

CONTROL WORD (FORMAT 1) - I/O Address 043H - Counter Latch Command			
0	BCD		
1-3	Mode	000	Mode 0
		001	Mode 1
		X10	Mode 2
		X11	Mode 3
		100	Mode 4
		101	Mode 5
4-5	Function	00	Counter Latch Command
		01	Read/Write Low Byte
		10	Read/Write High Byte
		11	Read/Write Low Byte then High Byte
6-7	Counter	00	Counter 0
		01	Counter 1
		10	Counter 2
CONTROL WORD (FORMAT 2) - I/O Address 043H - Read Back Command			
0		0	
1		Select Counter 0	
2		Select Counter 1	
3		Select Counter 2	
4		Latch Status	
5		Latch Count	
6-7		11	

TABLE 5-7. CONTROL WORD FORMAT

5.6.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT goes low when the counter starts. It goes high when the count = 0 and stays high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter is reloaded with the original count and the counter started.

OUT goes low when GATE goes from low to high. It goes high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

5.6.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

OUT is initially high. When the count = 1, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT is high. When the count is half done, OUT goes low. If GATE goes low then OUT will go high.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT is initially high. When the count = 0, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT is high when the counter starts. When count = 0, OUT goes low for one clock. If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.2 Reading The Counter

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to the fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See Control Word format 1). This command latches the count so that it may be read without changing.

3. The count may be read via a Read Back Command. (See Control Word format 2). This command is the equivalent of multiple Counter Latch Commands.

5.6.3 Reading Status

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See Control Word format 2). Bits 0:5 are the same as the command word for the counter. Bit 6 tells whether the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

STATUS WORD	
0	BCD
1-3	Mode
4-5	Function
6	New Count Written
7	Out Status

5.6.4 Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used during refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles and the other is a read/write port for the CPU.

5.6.5 Refresh Address

This block contains an 11-bit counter that is used for the address during a refresh.

5.6.6 Timer Shadow

For both Suspend/Resume and Hibernation the state of the write only registers in the timer may be read. Refer to Section 8.14.5 Timer Count for details.

5.7 SYSTEM CONTROLLER DECODE

The WD8110/LV supports both the 100% IBM-AT compatible I/O decoding (10-bit mode) and the newer IBM PS/2 compatible I/O decoding (16-bit mode). The mode is selected by EN_16 (bit 05) at Port Address 2872H. Refer to Section 7.2.

Page Register Decodes

Address	Decode
0087H	DMA Channel 0
0083H	DMA Channel 1
0081H	DMA Channel 2
0082H	DMA Channel 3
008BH	DMA Channel 5
0089H	DMA Channel 6
008AH	DMA Channel 7
008FH	Refresh

TABLE 5-9. PAGE REGISTER DECODES

NOTE

Page register data appears on address bits A(23:16) during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5:7), the LSB of the page register does not appear.

DEVICE	10-BIT MODE ADDRESS IN HEX	16-BIT MODE ADDRESS IN HEX
DMA Controller 1 (Ch 0:3)	000:01F	0000:000F
Interrupt Controller Master	020:03F	0020:0021
Timer	040:05F	0040:0043
Port B - Parity Error And I/O Channel Check	061:06F (odd)	0061
Real-Time Clock (Address)	070	0070
Real-Time Clock (Data)	071	0071
Page Register (except 092H)	080:091 093:09F	0080:008F
ALT 20 GATE, Hot Reset (Port 92H)	092	0092
Interrupt Controller Slave	0A0:0BF	00A0:00A1

TABLE 5-8. DEVICE ADDESSES

5.8 NMI AND REAL TIME CLOCK

5.8.1 Real-Time Clock Address Register

Port Addresses 070H in 10-bit mode
0070H in 16-bit mode

- Write only

7	6	5	4	3	2	1	0
D_ NMI	RTC A6	RTC A5	RTC A4	RTC A3	RTC A2	RTC A1	RTC A0

Signal Name	Default At RSTIN
D_NMI	1
RTCA(6:0)	None

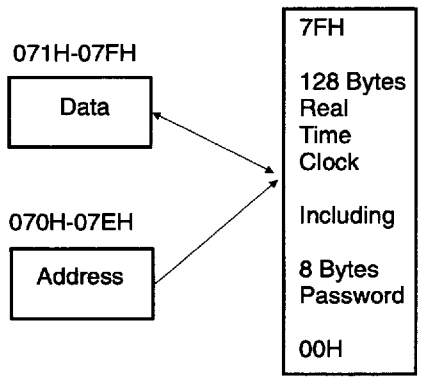
Bit 7 - D_NMI, Disable Non-Maskable Interrupt

D_NMI = 0 -
Non-Maskable Interrupt enabled.

D_NMI = 1 -
Non-Maskable Interrupt disabled.

Bits 6:0 - RTCA(6:0), Real-Time Clock Address

RTCA(6:0) provide the 128 addresses of the Real-Time Clock area. The data selected by one of these addresses is available by reading the RTC Data Register at 071H in 10-bit mode or 0071H in 16-bit mode.



5.8.2 Real-Time Clock Data Register

Port Addresses 071H in 10-bit mode
0071H in 16-bit mode

- Read and Write

Data is transferred between this register and the memory location selected by the RTC Address Register. The data bus used is selected by bit 15 of the register at Port Address 2872H (refer to Section 7.2).

7	6	5	4	3	2	1	0
Real-Time Clock Data							

5.8.3 Lock Pass, Alternate A20G and Hot Reset

Port Address 092H in 10-bit mode
0092H in 16-bit mode

– Read and Write

7	6	5	4	3	2	1	0
				LOCK PASS		ALT_ A20G	HOT_ RST

Signal Name	Default At RSTIN
Bits 7-4, 2	None
LOCK_PASS	0
ALT_A20G	0
HOT_RST	0

Bit 3 - LOCK_PASS

LOCK_PASS is used to prevent access to the eight byte password located in the Real-Time Clock area. The protected addresses are 38H through 3FH. Before LOCK_PASS can be set, bit 2 of the register at Port Address 2872H must be set to 0. Once LOCK_PASS is set, it can only be reset by RSTIN.

LOCK_PASS = 0 -
The eight byte password area is accessible.

LOCK_PASS = 1 -
The eight byte password area is not accessible.

Bit 1 - ALT_A20G, Alternate A20 Gate

Normally, the state of ALT_A20G is ORed with the external A20GT signal. If either ALT_A20G or A20GT is high, the A20 line is ungated. If both ALT_A20G and A20GT are low, A20 will be gated low.

As an option, ALT_A20G may be programmed by the Diagnostic Register at Port Address 9872H to automatically change state to match that of the Keyboard's A20GATE.

Bit 0 - HOT_RST, Hot Reset

A processor reset (CPURES) is generated 128 CPUCLKs after the HOT_RST changes from a 0 to 1. The CPURES is 16 clock pulses wide.

5.9 PORT B - PARITY ERROR AND I/O CHANNEL CHECK

Port B is accessed at any odd numbered Port Address 061H:06FH in 10-bit mode, or 0061H in 16-bit mode. This provides access to parity error and I/O Channel Check of the expansion bus.

- Bits 7:4 – Read only
- Bits 3:0 – Read and Write

7	6	5	4	3	2	1	0
PE	IOCK	OUT 2	REF DT	D_ IOC	D_ PE	ENS PK	TMR 2G

Signal Name	Default At RSTIN
PE	0
IOCK	0
OUT2	NA
REFDT	1
D_IOC	0
D_PE	0
ENSPK	0
TMR2G	0

Bit 7 - PE, Parity Error

PE = 0 -
No Parity Error.

PE = 1 -
Parity Error.

Bit 6 - IOCK, I/O Channel Check from the expansion bus

IOCK = 0 -
No I/O Channel Check Error.

IOCK = 1 -
I/O Channel Check Error.

Bit 5 - OUT2, Out from timer channel 2

OUT2 represents the state of the Timer 2 output.

Bit 4 - REF_DT, Refresh Detect

REF_DT changes state on each refresh.

Bit 3 - D_IOC, Disable I/O Channel Check

D_IOC = 0 -
I/O channel check from the expansion bus is not disabled.

D_IOC = 1 -
I/O channel check from the expansion bus is disabled.

Bit 2 - D_PE, Disable Parity Error Check

D_PE = 0 -
Parity error checking not disabled. This may be overridden by the PAR_CHE bit in ESF Register 1A8H for systems without parity RAM.

D_PE = 1 -
Parity error checking disabled.

Bit 1 - ENSPK, Enable Speaker

ENSPK = 0 -
Speaker is not enabled.

ENSPK = 1 -
Speaker is enabled.

Bit 0 - TMR2G, Gate for Timer Channel 2

TMR2G = 0 -
Timer Channel 2 gated low.

TMR2G = 1 -
Timer Channel 2 output enabled.

6.0 CPU DRAM CONTROLLER

This section describes the programmable Extended Setup Facility (ESF) registers as well as the following DRAM controller modes of operation:

Burst Mode
Interleave Mode
Fast Page Mode
Static Column Mode

The DRAM Controller directly supports a 486 Burst order sequence and always operates in Page Mode. It also supports Double Word Interleave with concurrent access to two banks.

For 80486 CPUs, the DRAM data bus can be connected directly to the CPU and WD8110 data bus, eliminating the need for DRAM data buffers such as 74ACT245. For 80386 CPUs 74ACT245 memory data buffers are required to prevent data contention between the CPU and DRAM data.

The DRAM parameters are programmable and the DRAM controller operates in either Interleave on or off mode. The DRAMs CAS signals are used as output enables for banks. The DRAM controller supports up to five banks of DRAM using 14 signals. $\overline{RAS}(4:0)$ for all banks, $\overline{CAS}(03:00)$ for each byte in Banks 4, 2 and 0, and $\overline{CAS}(13:10)$ for Banks 3 and 1, and one $\overline{WE}$ for all banks.

In 486 Mode, the DRAM controller accesses four 32-bit words, while in 386 Mode, it accesses only one 32-bit word.

6.1 INTERLEAVE MODE ON

Interleave Mode for banks 1 and 0 is enabled by setting ESF Register 198H bit 3 to 1. Interleave Mode for banks 3 and 2 is enabled by setting ESF Register 198H bit 4 to 1. As many as five banks of DRAM may be controlled and there must be two or four banks installed to turn interleave on. Banks 1 and 0 operate as one pair and may be interleaved, and banks 3 and 2 operate as another pair and may be interleaved. Bank 4 is not interleaved.

Each bank has its own dedicated RAS signal, $\overline{RAS4}$ for bank 4 through $\overline{RAS0}$ for bank 0. When Interleave Mode is on, it is necessary that both banks being interleaved are of the same type. When access starts, RAS lines for both banks are asserted simultaneously.

The WD8110/LV generates multiplexed address bits RA(11:4, 2:0), RA3B and RA3A for the DRAMs. RA(11:4, 2:0) go to all five banks, RA3A to banks 4, 2 and 0 and RA3B to banks 3 and 1. The WD8110/LV uses address bit A3 from the CPU to generate RA3A and RA3B.

When access starts, 32 bits from banks 1 and 0 or 3 and 2 are addressed simultaneously (64 bits), but only one set of CAS signals (CAS03:00 or CAS13:10) are asserted at this time, selecting 32 bits from a single bank. When the 32-bit word is received by the CPU, RA3A and RA3B and the CAS sets change state. If the first 32-bit word is being sent to the CPU from bank 1, the next word may be accessed from bank 0 because RA3A and RA3B have already changed state.

This overlapping of access allows Fast Page Mode DRAMs to be used to achieve high performance line fill. Separate CAS lines for bank 0 (CAS03:00) and bank 1 (CAS13:10) are provided and used as output enable of DRAM banks. The CPU address bit A2 decides whether CAS(03:00) (A2 = 0) or CAS(13:10) (A2 = 1) will be turned on first. The CAS pulse width is programmable in units of CPUCLK as defined by ESF Registers 199H, 1A1H:1A5H.

6.2 INTERLEAVE MODE OFF

When Interleave Mode is off, the DRAM controller requires all word accesses from the same bank. The DRAM signals are controlled so that CAS(03:00) is generated for access to banks 2 and 0. For access to banks 3 or 1, CAS(13:10) is generated).

For Static Column DRAMs, CAS(03:00) or CAS(13:10) is set low on the first 32-bit read and remains low for the rest of the cycle and only the DRAM address is changed.

For Page Mode DRAMs, the address is changed and CAS(03:00) or CAS(13:10) is set high for one CLK (or CAS precharge programmed value) and then set low again to clock the new DRAM address and access the next word. The Static

Column access is four CPUCLK times faster since CAS does not have to be set high.

In either Interleave Mode on or off, early write mode of DRAMs is used.

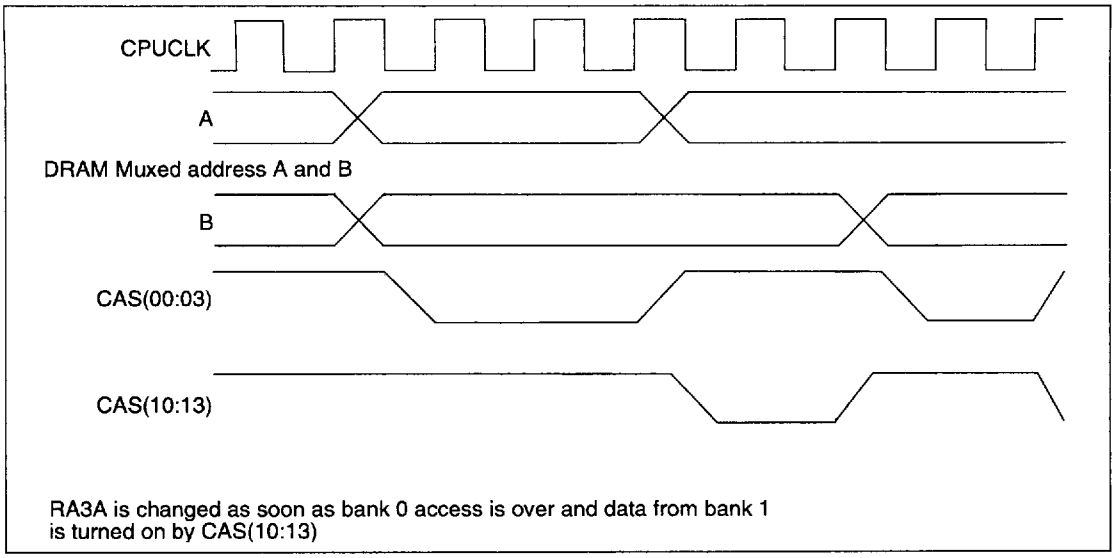


FIGURE 6-1. INTERLEAVE ON - FAST PAGE MODE DRAMs

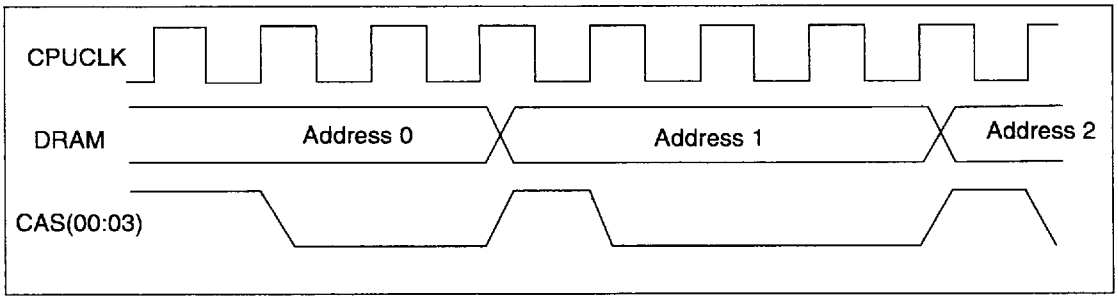


FIGURE 6-2. INTERLEAVE OFF - PAGE MODE DRAM

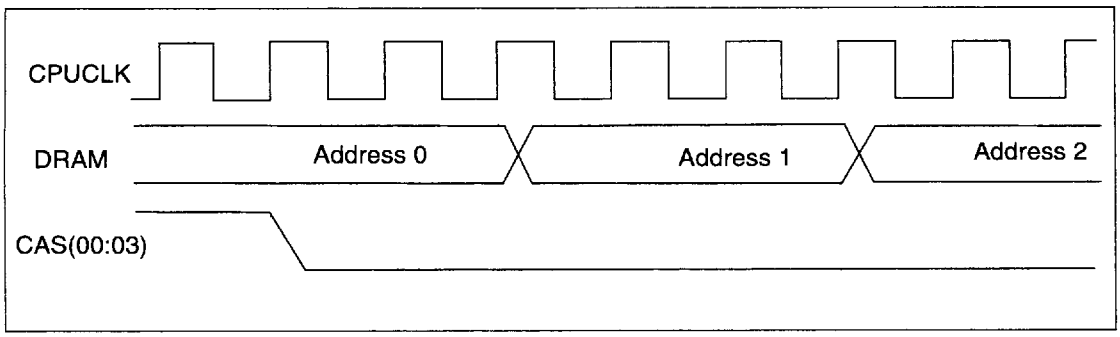


FIGURE 6-3. INTERLEAVE OFF - STATIC COLUMN MODE DRAM

6.3 DRAM ADDRESS MULTIPLEXER

The memory address bus serves three functions.

1. During DRAM cycles, the DRAM row and column address RA(11:4), RA3A, RA3B and RA(2:0) are present as the RA bus.

2. During I/O cycles, chip selects CS(4:0), along with $\overline{\text{CSEN}}$, are output to select up to 16 or 32 possible chip selects.

3. During I/O cycles, the bus serves as an eight bit data bus ED(7:0) to devices such as the keyboard controller or system BIOS.

The address multiplexer is implemented in the WD8110/LV. RA(11:4), RA3A, RA3B and RA(2:0) can drive loads as great as 450 pF, so that additional address buffers are not required for DRAM addresses with a load less than 450 pF. External buffers can be used for loads greater than 450 pF.

The following tables present the address assignment for the different type of DRAM and Interleave bit.

When Interleave is on, banks being interleaved must have the same type DRAMs.

DRAM Address MUX type 9x9, 10x9 - Interleave on

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	10	3	6	7	8	9	11			
RAS	13	14	18	19	20	12	15	16	17	21	22	23
REF	4	5	2	3	6	7	0	1	8	9	10	11

DRAM Address MUX type 9x9, 10x9 - Interleave off

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	2	3	6	7	8	9	10			
RAS	13	14	18	19	11	12	15	16	17	20	21	22
REF	4	5	2	3	6	7	0	1	8	9	10	11

DRAM Address MUX type 10x10, 11x10 - Interleave on

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	10	3	6	7	8	9	11	12		
RAS	13	14	18	19	20	22	15	16	17	21	23	24
REF	4	5	2	3	6	7	0	1	8	9	10	11

DRAM Address MUX type 10x10, 11x10 - Interleave off

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	2	3	6	7	8	9	10	11		
RAS	13	14	18	19	21	12	15	16	17	20	22	23
REF	4	5	2	3	6	7	0	1	8	9	10	11

DRAM Address MUX type 11x11, 12x11 - Interleave on

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	10	3	6	7	8	9	11	12	13	
RAS	24	14	18	19	20	22	15	16	17	21	23	25
REF	4	5	2	3	6	7	0	1	8	9	10	11

DRAM Address MUX type 11x11, 12x11 - Interleave off

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	2	3	6	7	8	9	10	11	12	
RAS	13	14	18	19	21	23	15	16	17	20	22	24
REF	4	5	2	3	6	7	0	1	8	9	10	11

DRAM Address MUX type 12x8 - Interleave on

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	10	3	6	7	8	9				
RAS	13	14	18	19	20	12	15	16	17	21	22	11
REF	4	5	2	3	6	7	0	1	8	9	10	11

DRAM Address MUX type 12x8 - Interleave off

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	2	3	6	7	8	9				
RAS	13	14	18	19	20	12	15	16	17	21	10	11
REF	4	5	2	3	6	7	0	1	8	9	10	11

DRAM Address MUX type 12x12 - Interleave on

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	10	3	6	7	8	9	11	12	13	14
RAS	24	26	18	19	20	22	15	16	17	21	23	25
REF	4	5	2	3	6	7	0	1	8	9	10	11

DRAM Address MUX type 12x12 - Interleave off

RA	0	1	2	3	4	5	6	7	8	9	10	11
CAS	4	5	2	3	6	7	8	9	10	11	12	13
RAS	25	14	18	19	21	23	15	16	17	20	22	24
REF	4	5	2	3	6	7	0	1	8	9	10	11

6.4 EXTENDED SETUP FACILITY (ESF) REGISTERS

The DRAM controller within the WD8110/LV always operates in Page Mode for CPU accesses and controls up to five banks. The ESF registers control the operation of DRAM.

The Extended Setup Facility (ESF) provides a means of programming the I/O registers in the System Controller. The ESF register address is written to Ports 74H and 75H. The data addressed by these ports can be accessed from Data Port 700H (default). The data port address can be changed by unlocking the ESF registers.

Port 74H bits 7:0 = LSB of the ESF address.
Port 75H bits 7:0 = MSB of the ESF address.
Port 700H = Data Port for ESF.

Optionally the ESF address can be written to Port Address 4872H and the data at the ESF register can be read from Port Address 5072H. All ESF I/O ports are accessed as eight bit ports. All System Controller I/O Ports are within ESF:190H to 19FH and 1A0H to 1AFH. All other ESF addresses are reserved for future use.

The following ESF registers are read only when in Virus Protection Mod:
ESF190H:ESF198H ESF19AH:ESF19EH,
ESF1A8H, ESF1ABH

6.4.1 System Configuration Register

ESF Port Address 19FH – Bits 3:1 Read only
Bits 7:4, 0 Read and Write

7	6	5	4	3	2	1	0
Reserved		RAS Timeout		Reserved			WTKEN

Signal Name	Default At RSTIN
Reserved	0
RAS Timeout	0
Reserved	0
WTKEN	0

Bit 7:6 - Reserved

Bit 5:4 - RAS Timeout

If the 10 µs RAS Timeout feature is enabled, these bits are used to control the accuracy. The WD8110/LV approximates the 10 µs RAS timeout timer by counting CPU clock and counts more clock at high speed.

Bit 5 4
0 0 - 25 MHz
0 1 - 33 MHz
1 0 - 50 MHz
1 1 - 20 MHz

Bits 3:1 - Reserved

Bit 0 - WTKEN, Weitek 4167 Enable

WTKEN = 0 -
Weitek 4167 is disabled. WD8110/LV generates one wait state RDY486 for addresses C0000000 through CFFFFFFF.

WTKEN = 1 -
Weitek 4167 is present. Addresses C0000000 through CFFFFFFF are not executed by WD8110/LV and it waits for Weitek 4167 to generate $\overline{\text{RDYIN}}$.

6.4.2 Bank 0:4 Enabling and Address Multiplexing

The following three registers control the enable/disable, and Column and Row address bits, of Banks 0:4

6.4.2.1 Banks 0:1

ESF Port Address 190H – Read and Write

7	6	5	4	3	2	1	0
BK EN 1	BK EN 0	BANK 1 BK 1 AD MU			BANK 0 BK 0 AD MU		

Signal Name	Default At RSTIN
All signals	0

Bit 7 - BK EN 1, Bank Enable 1

BK EN 1 = 0 -
Bank 1 disabled.

BK EN 1 = 1 -
Bank 1 enabled.

Bit 6 - BK EN 0, Bank Enable 0

BK EN 0 = 0 -
Bank 0 disabled.

BK EN 0 = 1 -
Bank 0 enabled.

Bits 5:3 - BK 1 AD MU, Bank 1 Address Mux

BK 1 AD MU

5	4	3		
0	0	0	-	Col Add 9 bits Row Add 9, 10, 11, 12 bits
0	0	1	-	Col Add 12 bits Row Add 12 bits
0	1	0	-	Col Add 10 bits Row Add 10, 11, 12, bits
0	1	1	-	Col Add 11 bits Row Add 11, 12 bits
1	0	0	-	Col Add 8 bits Row Add 12 bits

Bits 2:0 - BK 0 AD MU, Bank 0 Address Mux

BK 0 AD MU

2	1	0		
0	0	0	-	Col Add 9 bits Row Add 9, 10, 11, 12 bits
0	0	1	-	Col Add 12 bits Row Add 12 bits
0	1	0	-	Col Add 10 bits Row Add 10, 11, 12, bits
0	1	1	-	Col Add 11 bits Row Add 11, 12 bits
1	0	0	-	Col Add 8 bits Row Add 12 bits

Bit 6 - BK EN 2, Bank Enable 2

BK EN 2 = 0 -
Bank 2 disabled.

BK EN 2 = 1 -
Bank 2 enabled.

Bits 5:3 - BK 3 AD MU, Bank 3 Address Mux

BK 3 AD MU

5	4	3		
0	0	0	-	Col Add 9 bits Row Add 9, 10, 11, 12 bits
0	0	1	-	Col Add 12 bits Row Add 12 bits
0	1	0	-	Col Add 10 bits Row Add 10, 11, 12, bits
0	1	1	-	Col Add 11 bits Row Add 11, 12 bits
1	0	0	-	Col Add 8 bits Row Add 12 bits

Bits 2:0 - BK 2 AD MU, Bank 2 Address Mux

BK 2 AD MU

2	1	0		
0	0	0	-	Col Add 9 bits. Row Add 9, 10, 11, 12 bits.
0	0	1	-	Col Add 12 bits. Row Add 12 bits.
0	1	0	-	Col Add 10 bits. Row Add 10, 11, 12, bits.
0	1	1	-	Col Add 11 bits. Row Add 11, 12 bits.
1	0	0	-	Col Add 8 bits. Row Add 12 bits.

6.4.2.2 Banks 2:3

ESF Port Address 191H – Read and Write

7	6	5	4	3	2	1	0
BK EN 3	BK EN 2	BANK 3 BK 3 AD MU			BANK 2 BK 2 AD MU		

Signal Name	Default At RSTIN
All signals	0

Bits 7 - BK EN 3, Bank Enable 3

BK EN 3 = 0 -
Bank 3 disabled.

BK EN 3 = 1 -
Bank 3 enabled.

6.4.2.3 Bank 4

ESF Port Address 1A0H – Read and Write

7	6	5	4	3	2	1	0
BK EN 4			BANK 4 WCCPW		BANK 4 BK 4 AD MU		

Signal Name	Default At RSTIN
Bits 7:6	1
Bits 5:0	0

Bit 7 - BK EN 4, Bank Enable 4

BK EN 4 = 0 -
Bank 4 disabled.

BK EN 4 = 1 -
Bank 4 enabled.

Bits 6:5 - Reserved

Bits 4:3 - WCCPW, Bank 4 Write Cycle CAS Pulse Width

WCCPW
4 3
0 0 - CAS is 1 CLK.
0 1 - CAS is 2 CLK.
1 0 - CAS is 3 CLK.
1 1 - CAS is 3 CLK.

Bits 2:0 - BK 4 AD MU, Bank 4 Address Mux

BK 4 AD MU
2 1 0
0 0 0 - Col Add 9 bits.
Row Add 9, 10, 11, 12 bits.
0 0 1 - Col Add 12 bits.
Row Add 12 bits.
0 1 0 - Col Add 10 bits.
Row Add 10, 11, 12, bits.
0 1 1 - Col Add 11 bits.
Row Add 11, 12 bits.
1 0 0 - Col Add 8 bits.
Row Add 12 bits.

6.4.3 Bank 0:4 Size

The Bank Size Control registers in ESF Port Addresses 192H, 19AH, 19BH, 19CH and 19DH are used to program the Row Address bits and control the total DRAM memory size in each of the five Banks. MA(25:20) are used as masking control bits for corresponding address comparison to determine the memory size. The encoding of MA(25:20) is the same for all five registers and is provided in Table 6-1.

6.4.3.1 Bank 0 Size Control

ESF Port Address 192H – Read and Write

7	6	5	4	3	2	1	0
RA01	RA00	Memory Address MA25	MA24	MA23	MA22	MA21	MA20

Signal Name	Default At RSTIN
All signals	0

Bits 7:6 - RA(01:00), Row Address bits 01:00

RA(01:00) are used to detect Page Hit cycles.

RA(01:00)
7 6
0 0 - 9 Row Address bits.
0 1 - 10 Row Address bits.
1 0 - 11 Row Address bits.
1 1 - 12 Row Address bits.

Bits 5:0 - MA(25:20), Memory Address

See Table 6-1.

MA25	MA24	MA23	MA22	MA21	MA20	BANK SIZE INTERLEAVE 0FF	ON
0	0	0	0	0	0	1 MB	N.A.
0	0	0	0	0	1	2 MB	1 MB
0	0	0	0	1	1	4 MB	2 MB
0	0	0	1	1	1	8 MB	4 MB
0	0	1	1	1	1	16 MB	8 MB
0	1	1	1	1	1	32 MB	16 MB
1	1	1	1	1	1	64 MB	32 MB

TABLE 6-1. BITS 5:0 MA(25:20) MEMORY ADDRESS SETTING

6.4.3.2 Bank 1 Size Control

ESF Port Address 19AH – Read and Write

7	6	5	4	3	2	1	0
RA11	RA10	Memory Address MA25	MA24	MA23	MA22	MA21	MA20

Signal Name	Default At RSTIN
All signals	0

Bits 7:6 - RA(11:10), Row Address bits 11:10

RA(11:10) are used to detect Page Hit cycles.

RA(11:10)
7 6
0 0 - 9 Row Address bits.
0 1 - 10 Row Address bits.
1 0 - 11 Row Address bits.
1 1 - 12 Row Address bits.

Bits 5:0 - MA(25:20), Memory Address

See Table 6-1.

6.4.3.3 Bank 2 Size Control

ESF Port Address 19BH – Read and Write

7	6	5	4	3	2	1	0
RA21	RA20	Memory Address MA25	MA24	MA23	MA22	MA21	MA20

Signal Name	Default At RSTIN
All signals	0

Bits 7:6 - RA(21:20), Row Address bits 21:20

RA(21:20) are used to detect Page Hit cycles.

RA(21:20)
7 6
0 0 - 9 Row Address bits.
0 1 - 10 Row Address bits.
1 0 - 11 Row Address bits.
1 1 - 12 Row Address bits.

Bits 5:0 - MA(25:20), Memory Address

See Table 6-1.

6.4.3.4 Bank 3 Size Control

ESF Port Address 19CH – Read and Write

7	6	5	4	3	2	1	0
RA31	RA30	Memory Address MA25	MA24	MA23	MA22	MA21	MA20

Signal Name	Default At RSTIN
All signals	0

Bits 7:6 - RA(31:30), Row Address bits 31:30

RA(31:30) are used to detect Page Hit cycles.

RA(31:30)
7 6
0 0 - 9 Row Address bits.
0 1 - 10 Row Address bits.
1 0 - 11 Row Address bits.
1 1 - 12 Row Address bits.

Bits 5:0 - MA(25:20), Memory Address

See Table 6-1.

6.4.3.5 Bank 4 Size Control

ESF Port Address 19DH – Read and Write

7	6	5	4	3	2	1	0
RA41	RA40	Memory Address MA25	MA24	MA23	MA22	MA21	MA20

Signal Name	Default At RSTIN
All signals	0

Bits 7:6 - RA(41:40), Row Address bits 41:40

RA(41:40) are used to detect Page Hit cycles.

RA(41:40)
7 6
0 0 - 9 Row Address bits.
0 1 - 10 Row Address bits.
1 0 - 11 Row Address bits.
1 1 - 12 Row Address bits.

Bits 5:0 - MA(25:20), Memory Address

See Table 6-1.

6.4.4 Memory Shadow Control

Memory Shadow Control Registers 1 and 2 control whether the memory space between 640 KB and 1 MB is Disabled, Read Only, Write Only or Read and Write. This memory space is divided into seven regions and each region is controlled separately. When a region is disabled and the CPU generates an address in that region, an AT Bus cycle is initiated. Also, when a region is disabled, it may be remapped to the highest memory location by enabling its corresponding Split Enable control bit in ESF:1ABH register.

The seven regions are identified as follows:

A0000 - AFFFF = Region A 64KB of memory
B0000 - BFFFF = Region B 64KB of memory
C0000 - C7FFF = Region C0 32KB of memory
C8000 - CFFFF = Region C8 32KB of memory
D0000 - DFFFF = Region D 64KB of memory
E0000 - EFFFF = Region E 64KB of memory
F0000 - FFFFF = Region F 64KB of memory

6.4.4.1 Memory Shadow Control Register 1

ESF Port Address 1AAH – Read and Write

7	6	5	4	3	2	1	0
REGION C8		REGION C0		REGION B		REGION A	

Signal Name	Default At RSTIN
All Signals	0

Bits 7:6 - C8, Region C8

Region C8
7 6
0 0 - DRAM block disabled. R/W are mapped to AT Bus.
0 1 - Read from DRAM, write to AT Bus.
1 0 - Write to DRAM, read from AT Bus.
1 1 - Read/Write from or to DRAM.

Bits 5:4 - C0, Region C0

Region C0
5 4
0 0 - DRAM block disabled. R/W are mapped to AT Bus.
0 1 - Read from DRAM, write to AT Bus.
1 0 - Write to DRAM, read from AT Bus.
1 1 - Read/Write from/to DRAM.

Bits 3:2 - B, Region B

Region B
3 2
0 0 - DRAM block disabled. R/W are mapped to AT Bus.
0 1 - Read from DRAM, write to AT Bus.
1 0 - Write to DRAM, read from AT Bus.
1 1 - Read/Write from/to DRAM.

Bits 1:0 - A, Region A

Region A
1 0
0 0 - DRAM block disabled. R/W are mapped to AT Bus.
0 1 - Read from DRAM, write to AT Bus.
1 0 - Write to DRAM, read from AT Bus.
1 1 - Read/Write from/to DRAM.

6.4.4.2 Memory Shadow Control Register 2

ESF Port Address 1A9H – Read and Write

7	6	5	4	3	2	1	0
BIOS ROM		REGION F		REGION E		REGION D	

Signal Name	Default At RSTIN
All Signals	0

Bits 7:6 - ROM SP, BIOS ROM Space

ROM SP
7 6
0 0 - BIOS ROM Chip Select for 0E0000 to 0FFFFF
0 1 - BIOS ROM Chip Select for 0F0000 to 0FFFFF
1 0 - BIOS ROM Chip Select for 0D0000 to 0FFFFF
1 1 - BIOS ROM Chip Select for 0C0000 to 0FFFFF

Bits 5:4 - F, Region F

Region F
5 4
0 0 - DRAM block disabled. R/W are mapped to AT Bus.
0 1 - Read from DRAM, write to AT Bus.
1 0 - Write to DRAM, read from AT Bus.
1 1 - Read/Write from/to DRAM.

Bits 3:2 - E, Region E

Region E
3 2
0 0 - DRAM block disabled. R/W are mapped to AT Bus.
0 1 - Read from DRAM, write to AT Bus.
1 0 - Write to DRAM, read from AT Bus.
1 1 - Read/Write from/to DRAM.

Bits 1:0 - D, Region D

Region D
1 0
0 0 - DRAM block disabled. R/W are mapped to AT Bus.
0 1 - Read from DRAM, write to AT Bus.
1 0 - Write to DRAM, read from AT Bus.
1 1 - Read/Write from/to DRAM.

6.4.5 Split Memory and SMI Control

Only regions A, B, C and D can be remapped to the address specified by the Split Memory Start Address Register at ESF:193H. The Split Memory Start Address is on 1 MB boundaries. The SMIBASE(1:0) bits designate the start address of the SMI RAM in the processor memory address range and can be selected as 30000H, 40000H or 60000H.

Bit 8 of Port Address 7472H is an SMI RAM enable bit and, when low, the RAM that is split appears at the Split Memory Start address. For example: If regions A, C and D are to be split and the Split RAM Starting Address is 4 MB, the CPU will detect a 192 KB of memory at address range 4 MB to be 4 MB + 192 KB (three 64 KB blocks). Programming SMISIZE(1:0) to 0 1 (128 KB) programs the last two blocks (C and D) as SMI RAM map. As long as SMI RAM Enable is low, the CPU can detect three 64 KB blocks starting at 4 MB. The CPU can download the SMI software in SMI RAM area. Once the SMI RAM Enable bit is set, any time that the CPU makes an access to 06000 through 6FFFF (or 30000 through 3FFFF etc.) with $\overline{\text{SMIADS}}$ active, the access is translated to 0C0000 through CFFFF and accesses to 70000 through 7FFFF with $\overline{\text{SMIADS}}$ active are translated to D0000 through DFFFF. The CPU can detect only one 64 KB block at 4 MB address, thereby protecting the SMI RAM area from normal CPU operation.

6.4.5.1 Split Memory Control and SMI RAM Start Address

ESF Port Address 1ABH – Read and Write

7	6	5	4	3	2	1	0
Split Memory				SMI RAM Size		SMI Base	
SPLT A	SPLT B	SPLT C	SPLT D	SRS1	SRS0	1	0

Signal Name	Default At RSTIN
SPLT(A:B)	11
SPLT(C:D)	00
SRS1	0
SRS0	1
SMIBASE(1:0)	11

Bit 7 - SPLTA, Split Memory at DRAM Region A

SPLTA = 0 -
Disabled

SPLTA = 1 -
Enabled

Bit 6 - SPLTB, Split Memory at DRAM Region B

SPLTB = 0 -
Disabled

SPLTAB= 1 -
Enabled

Bit 5 - SPLTC, Split Memory at DRAM Region C

SPLTC = 0 -
Disabled

SPLTC = 1 -
Enabled

Bit 4 - SPLTD, Split Memory at DRAM Region D

SPLTD = 0 -
Disabled

SPLTD = 1 -
Enabled

Bits (3:2) - SRS(1:0), SMI RAM Size

SMI RAM size 192 KB supports only the following region groups: A, A B C, A B D, A C D.

SRS(1:0)
1 0
0 0 - 64 KB
0 1 - 128 KB
1 0 - 192 KB
1 1 - 256 KB

Bits (1:0) - SMIBASE(1:0), SMI RAM Base Address

SMIBASE(1:0)
1 0
0 0 - 30000H (Intel SMI)
0 1 - 40000H (Cyrix SMI with 256K SMI RAM)
1 0 - 60000H (AMD SMI)
1 1 - Reserved

6.4.6 Split Start Address Register

ESF Port Address 193H – Read and Write

7	6	5	4	3	2	1	0
SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20

Signal Name	Default At RSTIN
SA(27:20)	0

6.4.7 Memory Banks(0:4) Start Address Registers

Bank 0:
ESF Port Address 194H – Read and Write

This register provides the start address for memory bank 0 as controlled by the WD8110/LV.

7	6	5	4	3	2	1	0
A27	A26	A25	A24	A23	A22	A21	A20

Signal Name	Default At RSTIN
A(27:20)	0

Bank 1:
ESF Port Address 195H – Read and Write

This register provides the start address for memory bank 1 as controlled by the WD8110/LV.

7	6	5	4	3	2	1	0
A27	A26	A25	A24	A23	A22	A21	A20

Signal Name	Default At RSTIN
A(27:21)	0
A20	1

Bank 2:
ESF Port Address 196H – Read and Write

This register provides the start address for memory bank 2 as controlled by the WD8110/LV.

7	6	5	4	3	2	1	0
A27	A26	A25	A24	A23	A22	A21	A20

Signal Name	Default At RSTIN
A(27:22)	0
A21	1
A20	0

Bank 3:
ESF Port Address 197H – Read and Write

This register provides the start address for memory bank 3 as controlled by the WD8110/LV.

7	6	5	4	3	2	1	0
A27	A26	A25	A24	A23	A22	A21	A20

Signal Name	Default At RSTIN
A(27:22)	0
A(21:20)	1

Bank 4:
ESF Port Address 19EH – Read and Write

This register provides the start address for memory bank 4 as controlled by the WD8110/LV.

7	6	5	4	3	2	1	0
A27	A26	A25	A24	A23	A22	A21	A20

Signal Name	Default At RSTIN
A(27:23)	0
A22	1
A(21:20)	0

6.4.8 DRAM Mode Register

ESF Port Address 198H – Read and Write

This register establishes some of the operating modes for all the DRAM banks. See Section 6.4.9 Static Column or Page Mode.

7	6	5	4	3	2	1	0
	RAS_ TO	STBU _REF	Interleave On INTLV 2 3	INTLV 0 1	MCD	FAST _RD	FAST _WR

Signal Name	Default At RSTIN
All Signals	0

Bit 7 - Reserved

Bit 6 - RAS_TO, RAS Timeout

RAS_TO = 0 -
10 µs RAS timeout disabled.

RAS_TO = 1 -
10 µs RAS timeout enabled.

Bit 5 - STBU_REF, Standard Or Burst Refresh

STBU_REF = 0 -
Standard refresh.

STBU_REF = 1 -
Burst of 8 refresh cycles.

Bit 4 - INTLV 2 3, Banks 2 and 3 Interleave

INTLV = 0 -
Interleave off for banks 2 and 3.

INTLV = 1 -
Interleave on for banks 2 and 3.

Bit 3 - INTLV 0 1, Banks 0 and 1 Interleave

INTLV = 0 -
Interleave off for banks 0 and 1.

INTLV = 1 -
Interleave on for banks 0 and 1.

Bit 2 - MCD, MUX To CAS Delay

MCD = 0 -
1 CLK for Page Miss.

MCD = 1 -
2 CLK for Page Miss.

Bit 1 - FAST_RD, Fast Read

FAST_RD = 0 -
Normal read, Page Hit cycle drops CAS at end of T2.

FAST_RD = 1 -
Fast read, Page Hit cycle drops CAS in middle of T2.

Bit 0 - FAST_WR, Fast Write

FAST_WR = 0 -
Normal write, Page Hit cycle drops CAS at end of T2.

FAST_WR = 1 -
Fast write, Page Hit cycle drops CAS in middle of T2.

6.4.9 Static Column or Page Mode

ESF Port Address 1A8H - Read and Write

This register is used to place Banks 4:0 in either Page Mode or Static Column Address Mode.

7	6	5	4	3	2	1	0
PAR_ CHE	SMI_ ADTR	WPC	SCM4	SCM3	SCM2	SCM1	SCM0

Signal Name	Default At RSTIN
PAR_CHE	1
All Other Signals	0

Bit 7 - PAR_CHE, Parity Check

Both this bit and D_PE in Port B (I/O address 061H) must be set to 0 for DRAM parity checking to be performed.

PAR_CHE = 0 -
DRAM parity checking is enabled.

PAR_CHE = 1 -
DRAM parity checking is disabled.

Bit 6 - SMI_ADTR, SMI Address Translation

SMI_ADTR applies to Intel Mode only.

SMI_ADTR = 0 -
SMI translation for RAM data and code accesses is performed.

SMI_ADTR = 1 -
SMI translation for data accesses is not performed. Any access with D/$\overline{C}$ = 1 is not translated for SMI cycles. In an SMI routine data access will go to standard RAM and code accesses go to SMI RAM.

Bit 5 - WPC, Write Parity Control

WPC = 0 -
Odd parity is Written.

WPC = 1 -
Even parity is Written.

Bit 4 - SCM4, Static Column Mode Bank 4

SCM4 = 0 -
Bank 4 in Page Mode.

SCM4 = 1 -
Bank 4 in Static Column Address Mode.

Bit 3 - SCM3, Static Column Mode Bank 3

SCM3 = 0 -
Bank 3 in Page Mode.

SCM3 = 1 -
Bank 3 in Static Column Address Mode.

Bit 2 - SCM2, Static Column Mode Bank 2

SCM2 = 0 -
Bank 2 in Page Mode.

SCM2 = 1 -
Bank 2 in Static Column Address Mode.

Bit 1 - SCM1, Static Column Mode Bank 1

SCM1 = 0 -
Bank 1 in Page Mode.

SCM1 = 1 -
Bank 4 in Static Column Address Mode.

Bit 0 - SCM0, Static Column Mode Bank 0

SCM0 = 0 -
Bank 0 in Page Mode.

SCM0 = 1 -
Bank 0 in Static Column Address Mode.

6.4.10 Banks(0:4) RAS/CAS Pulse Width and Precharge Registers

Bank 0:

ESF Port Address 199H – Read and Write

This register controls the RAS/CAS precharge time and pulse width for DRAM Bank 0.

7	6	5	4	3	2	1	0
CAS_PC	CAS_PW_RD			RAS_PW		RAS_PC	

Signal Name	Default At RSTIN
All Signals	1

Bit 7 - CAS_PC, CAS Precharge

CAS_PC = 0 -
1 CLK

CAS_PC = 1 -
2 CLK

Bits 6:4 - CAS_PW_RD, CAS Pulse Width Read for CAS Pulse Width Write refer to ESF Address 1A4.

CAS_PW_RD

6	5	4		
0	X	X	-	1 CLK
1	0	0	-	2 CLK
1	0	1	-	3 CLK
1	1	0	-	4 CLK
1	1	1	-	5 CLK

Bits 3:2 - RAS_PW, RAS Pulse Width

RAS_PW

3	2		
0	0	-	2 CLK
0	1	-	3 CLK
1	0	-	4 CLK
1	1	-	5 CLK

Bits 1:0 - RAS_PC, RAS Precharge

RAS_PC

1	0		
0	0	-	2 CLK
0	1	-	3 CLK
1	0	-	4 CLK
1	1	-	5 CLK

Bank 1:

ESF Port Address 1A1H – Read and Write

This register controls the RAS/CAS precharge time and pulse width for DRAM Bank 1.

7	6	5	4	3	2	1	0
CAS_ PC	CAS_PW_RD			RAS_PW		RAS_PC	

Signal Name	Default At RSTIN
All Signals	1

Bit 7 - CAS_PC, CAS Precharge

CAS_PC = 0 -
1 CLK

CAS_PC = 1 -
2 CLK

Bits 6:4 - CAS_PW_RD, CAS Pulse Width Read. For CAS Pulse Width Write refer to ESF Address 1A4H.

CAS_PW_RD

6	5	4		
0	X	X	-	1 CLK
1	0	0	-	2 CLK
1	0	1	-	3 CLK
1	1	0	-	4 CLK
1	1	1	-	5 CLK

Bits 3:2 - RAS_PW, RAS Pulse Width

RAS_PW

3	2		
0	0	-	2 CLK
0	1	-	3 CLK
1	0	-	4 CLK
1	1	-	5 CLK

Bits 1:0 - RAS_PC, RAS Precharge

RAS_PC

1	0		
0	0	-	2 CLK
0	1	-	3 CLK
1	0	-	4 CLK
1	1	-	5 CLK

Bank 2:

ESF Port Address 1A2H – Read and Write

This register controls the RAS/CAS precharge time and pulse width for DRAM Bank 2.

7	6	5	4	3	2	1	0
CAS_ PC	CAS_PW_RD			RAS_PW		RAS_PC	

Signal Name	Default At RSTIN
All Signals	1

Bit 7 - CAS_PC, CAS Precharge

CAS_PC = 0 -
1 CLK

CAS_PC = 1 -
2 CLK

Bits 6:4 - CAS_PW_RD, CAS Pulse Width Read. For CAS Pulse Width Write refer to ESF Address 1A4H.

CAS_PW_RD

6	5	4		
0	X	X	-	1 CLK
1	0	0	-	2 CLK
1	0	1	-	3 CLK
1	1	0	-	4 CLK
1	1	1	-	5 CLK

Bits 3:2 - RAS_PW, RAS Pulse Width

RAS_PW

3	2		
0	0	-	2 CLK
0	1	-	3 CLK
1	0	-	4 CLK
1	1	-	5 CLK

Bits 1:0 - RAS_PC, RAS Precharge

RAS_PC

1	0		
0	0	-	2 CLK
0	1	-	3 CLK
1	0	-	4 CLK
1	1	-	5 CLK

Bank 3:

ESF Port Address 1A3H – Read and Write

This register controls the RAS/CAS precharge time and pulse width for DRAM Bank 3.

7	6	5	4	3	2	1	0
CAS_PC	CAS_PW_RD			RAS_PW		RAS_PC	

Signal Name	Default At RSTIN
All Signals	1

Bit 7 - CAS_PC, CAS Precharge

CAS_PC = 0 -
1 CLK

CAS_PC = 1 -
2 CLK

Bits 6:4 - CAS_PW_RD, CAS Pulse Width Read. For CAS Pulse Width Write refer to ESF Address 1A4H.

CAS_PW_RD

6	5	4		
0	X	X	-	1 CLK
1	0	0	-	2 CLK
1	0	1	-	3 CLK
1	1	0	-	4 CLK
1	1	1	-	5 CLK

Bits 3:2 - RAS_PW, RAS Pulse Width

RAS_PW

3	2		
0	0	-	2 CLK
0	1	-	3 CLK
1	0	-	4 CLK
1	1	-	5 CLK

Bits 1:0 - RAS_PC, RAS Precharge

RAS_PC

1	0		
0	0	-	2 CLK
0	1	-	3 CLK
1	0	-	4 CLK
1	1	-	5 CLK

Bank 4:

ESF Port Address 1A5H – Read and Write

This register controls the RAS/CAS precharge time and pulse width for DRAM Bank 4.

7	6	5	4	3	2	1	0
CAS_PC	CAS_PW_RD			RAS_PW		RAS_PC	

Signal Name	Default At RSTIN
All Signals	1

Bit 7 - CAS_PC, CAS Precharge

CAS_PC = 0 -
1 CLK

CAS_PC = 1 -
2 CLK

Bits 6:4 - CAS_PW_RD, CAS Pulse Width Read. For CAS Pulse Width Write refer to ESF Address 1A0H.

CAS_PW_RD

6	5	4		
0	X	X	-	1 CLK
1	0	0	-	2 CLK
1	0	1	-	3 CLK
1	1	0	-	4 CLK
1	1	1	-	5 CLK

Bits 3:2 - RAS_PW, RAS Pulse Width

RAS_PW

3	2		
0	0	=	2 CLK
0	1	=	3 CLK
1	0	=	4 CLK
1	1	=	5 CLK

Bits 1:0 - RAS_PC, RAS Precharge

RAS_PC

1	0		
0	0	=	2 CLK
0	1	=	3 CLK
1	0	=	4 CLK
1	1	=	5 CLK

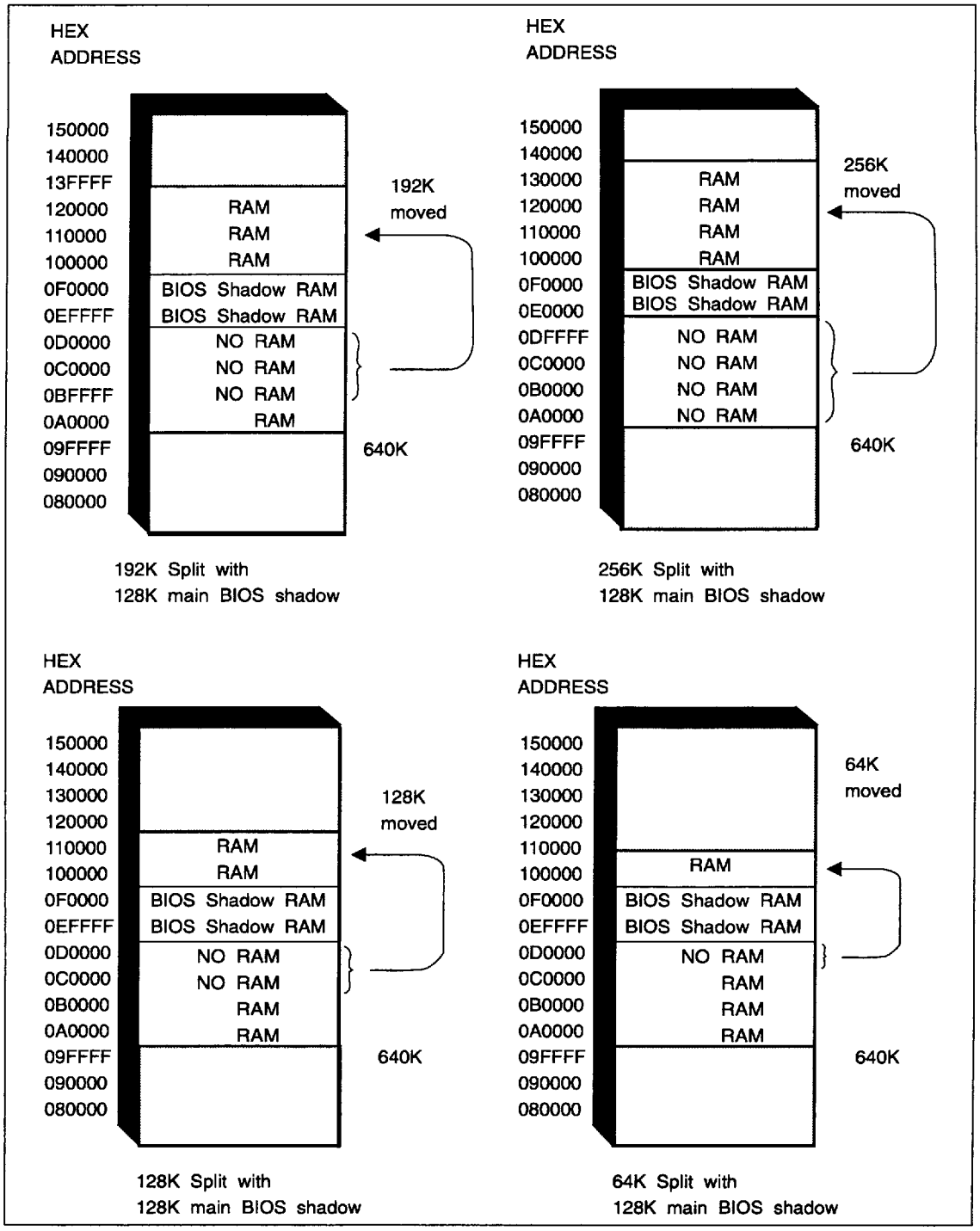


FIGURE 6-4. SPLIT SIZE

Banks 3:0

ESF Port Address 1A4H – Read and Write

This register controls the write cycle CAS Pulse Width for Banks 3:0.

7	6	5	4	3	2	1	0
CAS_PW_WT 3		CAS_PW_WT 2		CAS_PW_WT 1		CAS_PW_WT 0	

Signal Name	Default At RSTIN
All Signals	1

Bits 7:6 - CAS_PW_WT_3, CAS Pulse Width Write, Bank 3

CAS_PW_WT_3
7 6
0 0 = 1 CLK
0 1 = 2 CLK
1 0 = 3 CLK
1 1 = 3 CLK

Bits 5:4 - CAS_PW_WT_2, CAS Pulse Width Write, Bank 2

CAS_PW_WT_2
5 4
0 0 = 1 CLK
0 1 = 2 CLK
1 0 = 3 CLK
1 1 = 3 CLK

Bits 3:2 - CAS_PW_WT_1, CAS Pulse Width Write, Bank 1

CAS_PW_WT_1
3 2
0 0 = 1 CLK
0 1 = 2 CLK
1 0 = 3 CLK
1 1 = 3 CLK

Bits 1:0 - CAS_PW_WT_0, CAS Pulse Width Write, Bank 0

CAS_PW_WT_0
1 0
0 0 = 1 CLK
0 1 = 2 CLK
1 0 = 3 CLK
1 1 = 3 CLK

6.5 BACKLIGHT MOUSE AND SMI CONTROL

Port Address 7472H – Read and Write

15	14	13	12	11	10	09	08
BL_MOU		KC_L	AMWDE	ASMIE	CSUDE	HSRPD	SMI_RENB

07	06	05	04	03	02	01	00

Signal Name	Default At RSTIN
BL_MOU	00
KC_L, AMWDE,	0
ASMIE, CSUDE	0
HSRPD, SMI_RENB	0

Bit 15:14 - BL_MOU, Backlight Mouse Control

Enabling the Backlight Mouse Control increases the CPU speed for one second if Auto Clock Switching is on. The AUT_FST bit is located at Port Address 1072H bit 11. Enabling the Backlight Mouse Control also affects the Backlight and LCD timers in the PMC Timer Register at Port Address 8072H.

BL_MOU
01 00
0 0 - No mouse control
0 1 - INT12 mouse
1 0 - Reserved
1 1 - Reserved

Bit 13 - KC_L, Keyboard Controller Location

KC_L = 0 -
The Keyboard controller (I/O ports 60 and 64) is located on the RAD bus.

KC_L = 1 -
The keyboard controller is located on the expansion bus.

Bit 12 - AMWDE, AutoFast Memory Write Detection Enable

When AutoFast Memory Write Detection is enabled, memory writes to address range 020000-0FFFFF (128K to 1M) are detected as a source of activity and causes a 1 ms speedup. However, the activity will not be

detected during SMI handler execution on an Intel processor.

AMWDE = 0 -
AutoFast Memory Write Detection not enabled.

AMWDE = 1 -
AutoFast Memory Write Detection is enabled.

Bit 11 - ASMIE, AutoFast SMI Enable

Setting ASMIE to 1 enables an SMI to be generated when autofast logic determines it is necessary to assert the STP_REQ output. It also enables automatic clearing of the ASRE bit at Port Address 1072H when autofast logic determines that the STP_REQ output is to be de-asserted.

Note that when ASMIE is set, SMIFST at Port Address 8C72H must be cleared or each SMI to set STP_REQ will cause an immediate autofast speedup, effectively cancelling autofast.

The WD8110/LV must be in the Stop Grant AutoFast mode (SGAE =1 at Port Address 1072H) or ASMIE will be ignored.

ASMIE = 0 -
AutoFast SMI disabled.

ASMIE = 1 -
AutoFast SMI enabled.

Bit 10 - CSUDE, Clock Start-Up Delay Enable

CSUDE is used in conjunction with the SCH and SCHH bits in the register at Port Address 1072H. When CSUDE equals one, a 1 to 2 ms time delay is enforced between the time the CPU clock is restarted and the time STP_REQ is de-asserted. This delay is necessary for clock stop support of Intel 1X clock processors that require 1 ms for the CPU's PLL to stabilize.

CSUDE = 0 -
Clock Start-Up Delay is not enabled.

CSUDE = 1 -
Clock Start-Up Delay is enabled.

Bit 09 - HSRPD, Holdoff SMI When Reset Pending Disable

When HSRPD is set to 0, all SMI sources except I/O traps, are held off whenever a reset-pending condition is detected. The sources remain active internally but do not cause the SMI output to be asserted until the reset-pending condition is cleared.

When HSRPD is set to a 1, the reset pending condition does not gate off the assertion of SMI. Reset pending is defined as: (1) Port 92H reset pending, (2) KB controller Ports 60H or 64H have been written within the last 14 µs or (3) the CPU is in a halt state.

HSRPD = 0 -
SMI is held off when reset is pending

HSRPD = 1 -
SMI is not held off

Bit 08 - SMI_R ENB, SMI RAM Enable

Setting SMI_R ENB enables the SMI RAM remapping and protection. The system BIOS should load the SMI service routine into the SMI RAM before setting this bit.

SMI_R ENB = 0 -
SMI RAM disable

SMI_R ENB = 1 -
SMI RAM enable

Bits 07:00 - Reserved

7.0 PORT CHIP SELECT AND REFRESH

This section describes refresh control logic used by the power down feature. This section also describes the registers used to control the following functions:

- Port chip select and control
- High speed hard disk access
- AT hard disk IDE mode
- Real-Time Clock bus location
- Access to the CMOS RAM password

Table 7-1 identifies the ports, their Chip Select number, I/O address and function.

7.1 REFRESH CONTROL, SERIAL AND PARALLEL CHIP SELECTS

Port Address 2072H – Read and Write

15	14	13	12	11	10	09	08
M_ REF	V_ REF	CBR_ REF	CBR_ SR	SCSI	PAR		PAR_ L

07	06	05	04	03	02	01	00
SER_A			SER_ AL	SER_B			SER_ BL

Signal Name	Default At RSTIN
M_REF	0
V_REF	0
CBR_REF	0
CBR_SR	0
SCSI	0
PAR	00
PAR_L	0
SER_A	000
SER_AL	0
SER_B	000
SER_BL	0

Bit 15 - M_REF, Memory Refresh Power Down Mode

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port Address 1872H, and when M_REF = 1, the on-board DRAM is refreshed with every eighth PDREF. PDREF is a 64 KHz input signal supplied by the WD76C20.

M_REF = 0 -
Normal refresh period for main on-board memory.

M_REF = 1 -
Slow refresh main on-board memory.

Bit 14 - V_REF, Video Refresh Power Down Mode

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, video memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port Address 1872H, and V_REF = 1, the video DRAM is refreshed with every eighth PDREF. PDREF is a 64 KHz input signal supplied by the WD76C20.

V_REF = 0 -
Normal refresh period for video memory.

V_REF = 1 -
Slow refresh video memory.

Bit 13 - CBR_REF, CAS Before RAS Refresh For On-board DRAM

Most standard DRAMs support this type of CAS before RAS refresh, while special DRAMs do not. CBR_REF must always be set to 1 for portable systems that support suspend/resume.

CBR_REF = 0 -
Normal refresh for on-board DRAM.

CBR_REF = 1 -
CAS before RAS refresh.

Bit 12 - CBR_SR, CAS Before RAS Self Refresh

CAS before RAS self refresh is supported only by special DRAMs.

CBR_SR = 0 -
No CAS before RAS self refresh.

CBR_SR = 1 -
CAS before RAS self refresh of DRAM is supported during suspend and resume, when CAS is held low continuously while in suspend.

Bit 11 - SCSI, Small Computer System Interface Chip Select

The SCSI is selected by chip select number 12. See Table 7-3.

SCSI = 0 -
SCSI chip select disabled.

SCSI = 1 -
SCSI chip select at I/O port 353XH.

Bits 10:09 - PAR, Parallel Port Chip Select

The parallel port is selected by chip select number 0FH and may be located at I/O address 278H through 27FH, 378H through 37FH, or 3BCH through 3BFH. Bits 10 and 09 may disable the chip select or locate it at one of three areas. See Table 7-3.

PAR
10 09

0 0 - PAR chip select disabled.
0 1 - PAR chip select at I/O port 3BCH - 3BFH.
1 0 - PAR chip select at I/O port 378H - 37FH.
1 1 - PAR chip select at I/O port 278H - 27FH.

Bit 08 - PAR_L, Parallel Port Bus Location

PAR_L = 0 -
Parallel port is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30A is used.

PAR_L = 1 -
Parallel port is located on the expansion data bus. This is typical when the WD7615 is used.

Bits 07:05 - SER_A, Serial Port A Chip Select

The Serial Port A is selected by chip select number 0EH and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 07:05 may disable the chip select or locate it at one of the four areas. See Table 7-3.

It is possible to select the same I/O port address for Serial Port A and Serial Port B. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_A
07 06 05

0 0 0 - Serial Port A Chip Select disabled.
0 0 1 - Serial Port A Chip Select at I/O Port 3F8H - 3FFH.
0 1 0 - Serial Port A Chip Select at I/O Port 2F8H - 2FFH.
0 1 1 - SeriAl Port A Chip Select at I/O Port 3E8H - 3EFH.
1 0 0 - SeriaL Port A Chip Select at I/O Port 2E8H - 2EFH.

Bit 04 - SER_AL, Serial Port A Bus Location

SER_AL = 0 -
Serial Port A is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30A is used.

SER_AL = 1 -
Serial Port A is located on the expansion data bus.

Bits 03:01 - SER_B Serial Port B Chip Select

The Serial Port B is selected by chip select number 10 and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 03:01 may disable the chip select or locate it at one of the four areas. See Table 7-3.

It is possible to select the same I/O port address for Serial Port B and Serial Port A. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_B
03 02 01

0 0 0 - Serial Port B Chip Select disabled.
0 0 1 - Serial Port B Chip Select at I/O Port 3F8H - 3FFH.
0 1 0 - Serial Port B Chip Select at I/O Port 2F8H - 2FFH.
0 1 1 - SerialL Port B Chip Select at I/O Port 3E8H - 3EFH.
1 0 0 - Serial Port B Chip Select at I/O Port 2E8H - 2EFH.

Bit 00 - SER_BL, Serial Port B Bus Location

SER_BL = 0 -
Serial Port B is located on the RA(0:7)/ED(0:7) bus. This is typical when the WD76C30A is used.

SER_BL = 1 -
Serial Port B is located on the expansion data bus.

7.2 RTC, PVGA AND DISK CHIP SELECTS

Port Address 2872H – Read and Write

Bits 12:07 and Port Address 3072H control the use and location of the Programmable Chip Select #1.

15	14	13	12	11	10	09	08
RTC_ L	FST_ VGA	FST_ SCSI	EN_ PCS1	U_ MSK1	L_MSK1		

07	06	05	04	03	02	01	00
PRG_ L	HS_ HD	EN_ 16	P/S		LK_ PSW	DS_ HD	DS_ FLP

Signal Name	Default At RSTIN
RTC_L	0
FST_VGA	0
FST_SCSI	0
EN_PCS	0
U_MSK1	00
L_MSK1	00
PRG_L	0
HS_HD	000
P/S	000
LK_PSW	0
DS_HD	0
DS_FLP	0

Bit 15 - RTC_L, Real-Time Clock

The Real-Time Clock is normally on the RA0-7/ED0-7 bus but may be placed on the expansion data bus.

RTC_L = 0 -
Real-Time Clock is on the RA(0:7)/ED(0:7) bus.

RTC_L = 1 -
Real-Time Clock is on the expansion data bus. This is the required setting when the WD76C20 is used.

Bit 14 - FST_VGA, Fast VGA Video

The performance of Western Digital PVGA display controllers may be enhanced by reducing wait states for access to video I/O. This feature should only be used with Western Digital PVGA1A, WD90C90, WD90C30, WD90C20, WD90C11 and WD90C10 devices. I/O cycles to eight-bit ports 3C0H - 1H, 3C4H - 5H and 3CEH - FH are made with one wait state cycles.

FST_VGA = 0 -
Normal PVGA control.

FST_VGA = 1 -
One wait state I/O cycle to PVGA.

Bit 13 - FST_SCSI, Fast SCSI

The performance of the WD33C93 SCSI Controller is enhanced by performing eight-bit accesses with one wait state rather than four wait states.

FST_SCSI = 0 -
Four Wait States.

FST_SCSI = 1 -
One Wait State.

Bit 12 - EN_PCS1, Enable Programmable Chip Select 1

The Programmable Chip Select logic is selected with Chip Select 11 and may be disabled or enabled. See Table 7-3.

EN_PCS = 0 -
Disable Programmable Chip Select.

EN_PCS = 1 -
Enable Programmable Chip Select.

Bit 11 - U_MSK1, Upper Address Bits Masked

U_MSKI determines whether or not the upper address bits A(15:10) are to be used as designated in the Programmable Chip Select Address Register at Port Address 3072H.

U_MSKI = 0 -
A(15:10) are ignored.

U_MSKI = 1 -
A(15:10) are included in the address.

Bits 10:08 - L_MSK1, Lower Address Bits Masked

L_MSK1 determines whether the lower four address bits A(03:00) are to be used as designated in the Programmable Chip Select Address Register at Port Address 3072H.

L_MSK1
10 09 08

0 0 0 - A09 through A00 are included in the address.
0 0 1 - A00 is ignored.
0 1 0 - A00, A01 are ignored.
0 1 1 - A00, A01, A02 are ignored.
1 0 0 - A00, A01, A02, A03 are ignored

Bit 07 - PRG_L, Programmable Chip Select Bus Location

PRG_L = 0 -
Programmable Chip Select is on the RA(0:7)/ED(0:7) bus.

PRG_L = 1 -
Programmable Chip Select is on the expansion bus.

Bit 06 - HS_HD, High Speed Hard Disk Data Transfer Rate

Enabling the high speed data transfers results in hard disk, 16-bit data transfers to be performed at a compressed timing rate rather than at the compatible bus rate. When operating in the high speed mode, the first data transfer is made at the compatible bus rate. Subsequent accesses to the hard disk port are made at high speed, with $\overline{IOCS16}$ ignored and the WD76C20 hard disk chip select remaining stable.

NOTE

This feature requires the use of the WD76C20 and should only be used with Western Digital IDE drives.

HS_HD = 0 -
Compatible bus timing enabled.

HS_HD = 1 -
High speed hard disk accesses enabled.

Bit 05 - EN_16, Enable 16-bit I/O Decoding

The WD8110/LV supports both the 100% IBM-AT compatible I/O decoding (10-bit mode) and the newer IBM PS/2 compatible I/O decoding (16-bit mode). The mode is selected by EN_16.

EN_16 = 0 -
AT Compatible 10-bit decode. Address bits A15:10 are ignored. See Table 7-1.

EN_16 = 1 -
Enhanced 16-bit decode. See Table 7-2.

Bit 04 - P/S, Primary Or Secondary Disk

The P/S bit is only used to select the floppy disk chip select address in the IDE mode. See Table 7-3, Chip Select numbers 08H:0BH.

P/S = 0 -
Primary hard disk and Floppy address selected.

P/S = 1 -
Secondary hard disk and Floppy address selected.

Bit 03 - Reserved

Bit 02 - LK_PSW, Prevent Locking Password

Port Address 092H bit 3 (Lock_Pass) is used to prevent access to the CMOS RAM password area located at 38H through 3FH. Setting LK_PSW before attempting to set Lock_Pass, inhibits the setting of Lock_Pass. In this instance, it is possible to access the CMOS RAM password area. If Lock_Pass is set before LK_PSW, LK_PSW will have no effect.

LK_PSW = 0 -
Port Address 092H bit 3, Lock_Pass can be set.

LK_PSW = 1 -
Port Address 092H bit 3, Lock_Pass can not be set.

Bit 01 - DS_HD, Hard Disk Chip Select 0CH, 0DH

DS_HD = 0 -
Hard disk chip select is enabled.

DS_HD = 1 -
Hard disk chip select is not generated.

Bit 00 - DS_FLP, Floppy Disk Chip Select 08H, 09H, 0AH, 0BH

DS_FLP = 0 -
Floppy disk chip select is enabled.

DS_FLP = 1 -
Floppy disk chip select is not generated.

ADDRESS *	DEVICE
000:01F	DMA Controller 1 (Ch 0:3)
020:03F	Interrupt Controller Master
040:05F	Timer
060:06E (even)	Keyboard Port
061:06F (odd)	Port B - Parity Error And I/O Channel Check
070 bit 7	NMI Mask
070	RTC Address
071	RTC Data
080:08F, 090:091 093:09F	DMA Page
092	ALT 20 GATE, Hot Reset Port 92
0A0:0BF	Interrupt Controller Slave
0C0:0DF	DMA Controller 2 (Ch 5:7)
0F0:0F1	Numeric Processor Clear And Reset
1F0:1F7	Hard Disk Chip Select (primary)
170:177	Hard Disk Chip Select (secondary)
278:27F	Parallel Port 3
2E8:2EF	Serial Port 4
2F8:2FF	Serial Port 2
378:37F	Parallel Port 2
3BC:3BF	Parallel Port 1
3E8:3EF	Serial Port 3
3F0:3F7	Floppy and Hard Disk (primary)
370:377	Floppy and Hard Disk (secondary)
3F8:3FF	Serial Port 1
* A15:10 are ignored.	

TABLE 7-1. AT COMPATIBLE 10-BIT MODE

ADDRESS *	DEVICE
0000:000F	DMA Controller 1 (Ch 0:3)
0010:001F	AT Bus
0020:0021	Interrupt Controller Master
0022:003F	AT Bus
0040:0043	Timer
0044:005F	AT Bus
0060, 0064	Keyboard Port
0061	Port B - Parity Error And I/O Channel Check
0062, 0063	AT Bus
0065:006F	
0070 Bit 7	NMI Mask
0070	RTC Address
0071	RTC Data
0072:007F	AT Bus
0080:008F	DMA Page
0090:0091	AT Bus
0092	ALT 20 GATE, Hot Reset Port 92
0093:009F	AT Bus
00A0:00A1	Interrupt Controller Slave
00A2:00BF	AT Bus
00C0:00DE (even)	DMA Controller 2 (Ch 5:7)
00C1:00DF (odd)	AT Bus
00E0:00EF	AT Bus
00F0:00F1	Numeric Processor Clear And Reset
00F2:00FF	AT Bus
01F0:01F7	Hard Disk Chip Select (primary)
0170:0177	Hard Disk Chip Select (secondary)
0278:027F	Parallel Port 3
02E8:02EF	Serial Port 4
02F8:02FF	Serial Port 2
0378:037F	Parallel Port 2
03BC:03BF	Parallel Port 1
03E8:03EF	Serial Port 3
03F0:03F7	Floppy and Hard Disk (primary)
0370:0377	Floppy and Hard Disk (secondary)
03F8:03FF	Serial Port 1
* A15:10 equal 0	

TABLE 7-2. ENHANCED 16-BIT MODE

7.3 PROGRAMMABLE CHIP SELECT #1 ADDRESS

Port Address 3072H – Read and Write

15	14	13	12	11	10	09	08
A15	A14	A13	A12	A11	A10	A09	A08

07	06	05	04	03	02	01	00
A07	A06	A05	A04	A03	A02	A01	A00

Signal Name	Default At RSTIN
All signals	None

7.4 I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

Table 7-1 lists the I/O addresses and chip selects generated for each fixed port type. Address bits A(15:10) are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value.

An I/O to the addresses listed in Table 7-3 automatically causes the System Controller to output $\overline{\text{CSEN}}$ along with the corresponding encoded chip select value on CS4:0 (RA3B, RA3A, RA11:9). This is decoded by either the WD76C20/ALV or discrete logic, which in turn asserts individual chip select signals to the various peripherals. Some of these chip selects can be individually enabled or disabled by way of the registers at Ports 2072H, 2872H and 5C72H.

PORT	I/O ADDRESS 10-BIT MODE (HEX)	I/O ADDRESS 16-BIT MODE (HEX)	CHIP SELECT NUMBER (HEX)	FUNCTION
ROM Chip Select	N/A	N/A	00	Chip select for BIOS ROM
Keyboard Control	060:06E even	0060, 0064	01	Chip select for 8042
Power Control	7072	7072	03	PMC Write Strobe 0
Reserved			04	Reserved
Real-time Clock	070	0070	05	RTC ALE
Real-time Clock	071	0071	06	RTC Write Strobe
Real-time Clock	071	0071	07	RTC Read Strobe
Floppy Operation Chip Select	3F2 372	03F2 0372	08	Primary address Secondary address
Floppy Chip Select	3F4, 3F5 374, 375	03F4, 03F5 0374, 0375	09	Primary address Secondary address
Floppy Control Chip Select	3F7 377	03F7 0377	0A	Primary address Secondary address (Floppy enabled, HD disabled)
Floppy and HD Control Chip Select	3F7 377	03F7 0377	0B	Primary address Secondary address (Floppy enabled, HD enabled)
Hard Disk Chip Select	1F0:1F7 170:177	01F0:01F7 0170:0177	0C	Primary address Secondary address
Hard Disk Chip Select	3F6 3F7 ① 376 377 ①	03F6 03F7 ① 0376 0377 ①	0D	Primary Address Secondary address
Serial Port A Chip Select	2E8:2EF 2F8:2FF 3E8:3EF 3F8:3FF	02E8:02EF 02F8:02FF 03E8:03EF 03F8:03FF	0E ②	
Parallel Port 0 Chip Select	278:27F 378:37F 3BC:3BF	0278:027F 0378:037F 03BC:03BF	0F	

TABLE 7-3. I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

PORT	I/O ADDRESS 10-BIT MODE (HEX)	I/O ADDRESS 16-BIT MODE (HEX)	CHIP SELECT NUMBER (HEX)	FUNCTION
Serial Port B Chip Select	2E8:2EF 2F8:2FF 3E8:3EF 3F8:3FF	02E8:02EF 02F8:02FF 03E8:03EF 03F8:03FF	10 ②	
Program Chip Select 1	PROG 1	PROG 1	11	
SCSI	3530:353X	3530:353X	12	
Cache Flush	F872	F872	13	
Reserved			14	Reserved
	F072	F072	15	48 MHz Clock Disabled
	F472	F472	16	48 MHz Clock Enabled
Power Control	7872	7872	17	PMC Write Strobe 1
Floppy Chip Select	3F0:3F1 370:371	03F0:03F1 0370:0371	18	Primary address Secondary address
Floppy Chip Select	3F3 373	03F3 0373	19	Primary address Secondary address
Program Chip Select 2	PROG 2	PROG 2	1A	
Program Chip Select 3	PROG 3	PROG 3	1B	
Reserved			1E	Reserved
Reserved			1F	Reserved

① IDE Hard disk enabled, floppy disabled

② The Chip Select Number is the decoded value of CS(4:0). If the Programmed Chip Select corresponds to any other decode, the Programmed Chip Select is suppressed. If Serial Port A and B are programmed for the same address, Serial Port B Chip Select is suppressed.

TABLE 7-3. I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS (Continued)

8.0 POWER MANAGEMENT CONTROL

The WD8110/LV supports all PMC inputs, output and interrupt functions.

8.1 SYSTEM ACTIVITY MONITOR (SAM)

The System Activity Monitor (SAM) found in the WD8110/LV is a hardware solution to monitoring system activity. SAM was conceived to solve the problems associated with system activity detection in various operating environments such as DOS, Windows, OS/2, VCPI and Microsoft APM.

With previous System Controllers, such as the WD76C10, a software approach was employed to determine system activity. This software approach was accomplished using a watchdog timer. As a part of the watchdog timer service, the sources of activity are checked and a determination is then made on the state of system activity. This approach does not consider the state of the system activity between watchdog timer interrupts. However, with SAM, the system activity state is continuously monitored through hardware, thus providing a more universal approach to activity detection.

With the help of SAM it is now possible to:

- Provide a trigger when a pre-programmed period of system inactivity time elapses.
- Enable/disable the sources that constitute system activity.
- Select either coarse or fine timeout values for system inactivity period.

System Activity
System activity denotes periods of time in which the system performs useful tasks. The sources of System Activity are:

- Unmasked pending interrupts.
- Unmasked interrupts in service.
- Access to hard disk data port.
- I/O Access to programmable chip select port.
- DMA transfers.
- Coprocessor cycles.
- A programmable PCU input.
- NMI.

SAM allows for excluding the following interrupt sources from contributing to system activity:

- IRQ0, used by DOS to keep track of the system time.
- IRQ7, used for spurious interrupts and parallel port interrupts.
- IRQ8, used by Windows, OS/2 and other multitasking environments to keep the scheduler running.
- A programmable interrupt level used as a power management interrupt.

SAM also takes into account programs such as MOUSE.COM which, in an attempt to locate a mouse on a communication port, generates interrupts on interrupt levels 3 and 4, and leaves them pending. To overcome this problem, SAM allows only the unmasked pending interrupts on 3 and 4 to constitute system activity.

Using SAM for System Power Management:

a) System Timeout Capability

SAM can be programmed to determine coarse periods of inactivity, with the minimum period as one minute, four seconds, up to a maximum period of 16 minutes. It is also possible to extend the maximum limit to any value by reading the Activity Before bit (ACTBEF) in the Activity Monitor Control Register at Port Address B072H.

On reaching the programmed period SAM generates a Local Attention signal. Typically, the Local Attention is tied to a power management interrupt. In response to Local Attention, the power management interrupt handler makes it possible to prepare the system for a Suspend operation. Local Attention may also be programmed to generate an SMI.

b) Responding to a Suspend Request

SAM can be programmed to determine a clean breakpoint for suspending the system upon receiving the Suspend request. At the time the Suspend request is received, it is possible that the system is busy performing an indivisible operation and it is necessary to wait for the system to finish this indivisible operation before initiating suspend. In order to do this, control to the CPU must be relin-

quished for just enough time for the CPU to complete the operation. This is referred as Suspend arbitration.

In addition to performing Suspend arbitration, SAM is also responsible for determining the earliest opportunity to initiate the Suspend sequence. For instance, if a Suspend request is caused by a low battery condition, it is imperative that the system be placed in the suspend state as soon as possible. Here, the fine granularity of SAM may be used to determine brief periods of inactivity from as low as 7.8 milliseconds to as high as 117.2 milliseconds and establish a clean breakpoint for suspending the system.

Advantages of SAM:

1. SAM is a reliable and consistent approach to detecting system activity.

2. SAM is hardware based making it truly non-obtrusive.

3. SAM is independent of the operating environment and the execution mode of the processor.

4. SAM can perform in two modes:

   - Detection of system activity for extended periods of time for the purposes of system timeout.
   - Detection of brief periods of inactivity for initiating Suspend.

5. Programmability allows for the control of sources of system activity and setting up coarse and fine timeout values.

6. SAM generates a signal called Local Attention (LCL_ATN, PMC #4) on reaching programmed periods of timeout. This signal is generally tied to an unused IRQ level to invoke the Power Management program. Optionally, SAM can generate a System Management Interrupt ($\overline{SMI}$ on pin 102) in addition to LCL_ATN.

7. SAM also carries information on DMA activity state. This is used to determine whether it is appropriate to place the processor in the Sleep Mode.

8. SAM makes it possible to read the state of the interrupt controllers and, if needed, reprogram them on Resume. This is provided to handle the spurious interrupts that are generated by devices at power-up time on Resume.

NOTE

SAM cannot be used to determine when the processor should be placed in the Sleep Mode. This determination is intimately tied to the operating environment and is handled either by Western Digital's Power Management drivers DOS/VCPI, Windows and OS/2 or by Microsoft APM.

The System Activity Monitor is controlled by the Activity Monitor Control Register at Port Address B072H, Activity Monitor Mask Register at Port Address D872H and bit 09 of the Test Enable Register at Port Address A872H.

8.2 PROCESSOR POWER DOWN MODE

The Processor Power Down Mode is initiated by setting bit 13 of the register at Port Address 1872H to one. The CPURES signal is asserted, then tristated. An internal 200K pullup resistor holds the CPURES active. The Processor Power Down (PMC #5) signal from the PMC Control Register is used to control the power converter from the processor. The WD8110/LV holds CPUCLK, $\overline{RDY486}$, HOLDR, INTRQ and NMI low to the processor.

The same conditions used to restart a stopped clock also initiate the Power Up Mode. The Power Up Mode is entered by an unmasked DRQ, unmasked IRQ interrupt or a PMC input change, resulting in an unmasked NMI to Port 9072H. A Processor Power Good signal is then input on the PMCIN pin. After 1 ms, PMC Processor Power Good signal is checked for a logic 1 state. At this time, CPURES is driven high and the CPUCLK, $\overline{RDY486}$, HOLDR, INTRQ and NMI signals are driven to their correct states. CPURES remains asserted for 64 additional CPUCLKs.

The PMC unit is composed of either two 74HCT273 chips and one 74HCT151 chip, or a Western Digital WD7625 Buffer Manager. The two 74HCT273 octal latches are used for the 16 PMC outputs from data bus ED(0:7) and the 74HCT151 8:1 multiplexer is used for the PMCIN signal, while the WD7625 internal multiplexers perform both functions. The PMC output latches are cleared at power up (see Figure 5-1).

8.3 LOCAL ACCESS BY KEYBOARD CONTROLLER

The keyboard processor may access the WD8110/LV internal registers by way of the PMC logic. The keyboard processor starts a local access by asserting LCL_REQ, which causes PMCIN 2 to be asserted and written in the PMC input register at Port 8872H (see Figure 5-1 and Table 8-2). The WD8110/LV arbitrates with refresh, DMA and master for a hold cycle from the processor. When the processor returns a hold acknowledge (HOLDA), the WD8110/LV asserts LCL_ACK (PMC output 3 from Port 7072H) on the ED(0:7) data bus. The keyboard processor then passes the opcode/address byte to the WD8110/LV on the data bus and drops the LCL_REQ. The WD8110/LV responds by deasserting LCL_ACK.

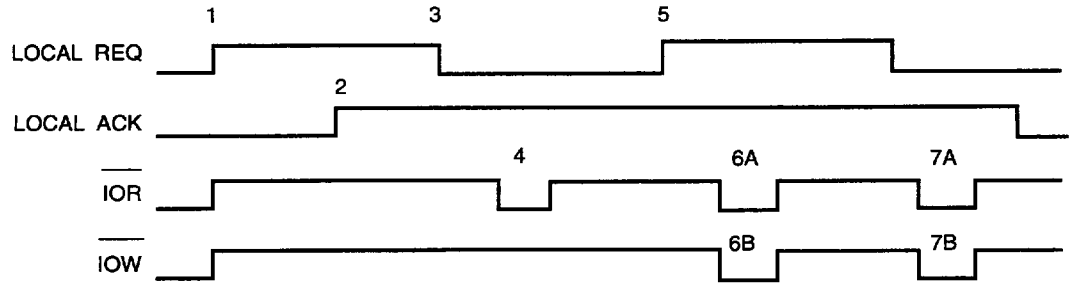
If the opcode specified a register write, data high (D15:08) and data low (D07:00) bytes are passed to the WD8110/LV. If the opcode specified an I/O read, the data high and data low bytes are sent from the WD8110/LV to the keyboard processor.

All special operation registers within the WD8110/LV may be accessed in this manner without first unlocking the register. See Section 2.8.2, Port Address F073H, for Lock/Unlock Register. This method allows the keyboard processor to control speed switching and other parameters without host processor intervention.

If a particular design uses processor-power-down on a non-static CPU and also uses this local access feature, then an additional AND gate is required. Local access during CPU power-down depends on ADDR2 coming from the CPU through the 74ACT373 bus latch. If the CPU is powered down, ADDR2 can be either high or low, depending on the last CPU address. PROC_PWR_GOOD should be ANDed with ADDR2 going to the 8742. This forces ADDR2 low, making local accesses possible during CPU power-down conditions. This also passes ADDR2 during normal operation.

Figure 8-1 shows the handshake procedure, followed by the keyboard controller and the WD8110/LV.

Figures 8-2 and 8-3 represents the power-down (suspend) and power-up (resume) sequence and control.



1 Keyboard Controller requests local data transfer

2 WD8110/LV returns LOCAL_ACK after receiving HOLDA from the host processor

3 Keyboard Controller loads address and OPCODE into data register, then drops LOCAL_REQ

4 WD8110/LV reads address and OPCODE

5 Keyboard Controller reloads data register with high byte, then asserts LOCAL_REQ

6A WD8110/LV reads high byte

7A WD8110/LV reads low byte, writes to internal register

FOR READ CYCLE OF WD8110/LV INTERNAL REGISTER:

6B WD8110/LV writes high byte to Keyboard Controller

7B WD8110/LV writes low byte to Keyboard Controller

OP_CODE FORMAT

7	6	5	4	3	2	1	0
DIR	RSV	A 15	A 14	A 13	A 12	A 11	A 10

DIR = 1 - Read register (generates IOW to Keyboard Controller)

DIR = 0 - Write register (generates IOR to Keyboard Controller)

FIGURE 8-1. REGISTER ACCESS BY KEYBOARD CONTROLLER

8.4 PMC OUTPUT CONTROL REGISTERS

Port Address 7072H - Bits 07:00 are Read only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

Signal Name	Default At RSTIN
All signals	None

PMC Output Control Bits 7:0

Port Address 7872H - Bits 07:00 are Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT F	OUT E	OUT D	OUT C	OUT B	OUT A	OUT 9	OUT 8

Signal Name	Default At RSTIN
All signals	None

PMC Output Control Bits 15:08

PMC NO.	PMC OUTPUT SIGNAL PORT 7072H	SOURCE
0H	Not Used	
1H	LCD Enable	Port 8072H - Bits 7:0
2H	Backlight Enabled	Port 8072H - Bits 15:8
3H	LCL_ACK	Port 8872H - Bit 2
4H	LCL_ATN	Port 8872H - Bit 15
5H	Processor power Down	Port 1872H - Bit 13
6H	Gate A20	
7H	Full Power Down	Port 1872H - Bit 14
	PMC OUTPUT SIGNAL PORT 7872H	**SOURCE**
8H	User Defined	Port 7872H
9H	User Defined	Port 7872H
AH	User Defined	Port 7872H
BH	User Defined	Port 7872H
CH	User Defined	Port 7872H
DH	User Defined	Port 7872H
EH	User Defined	Port 7872H
FH	User Defined	Port 7872H

TABLE 8-1. PMC OUTPUT SIGNALS

8.5 PMC TIMERS

Port Address 8072H - Read and Write

When no Keyboard or Mouse interrupts have occurred for the time specified by BL_TIMEOUT or LCD_TIMEOUT, PMC Output 1 or 2 is written to the PMC OUTPUT CONTROL 7:0 register at Port Address 7072H (see Table 8-1) to disable the LCD or Backlight. The timer is reset and the Backlight and LCD control re-enabled at the refresh cycle following a Keyboard or Mouse interrupt. The Mouse Interrupts are programmed by bits 15 and 14 (BL_MOU) in the Backlight Mouse Control Register at Port Address 7472H. The same timer is used for the Backlight and LCD timeout.

The timeout delay may be programmed in increments of five seconds, to a maximum of 1,270 seconds, or 21 minutes and 10 seconds.

15	14	13	12	11	10	09	08
BL_TIMEOUT							

07	06	05	04	03	02	01	00
LCD_TIMEOUT							

Signal Name	Default At RSTIN
BL_TIMEOUT	0
LCD_TIMEOUT	0

Bits 15:08 - BL_TIMEOUT, Backlight Time Out

00H - Backlight always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds
↕
FEH - Enabled for 254 x 5 seconds
FFH - Backlight enabled

Bits 07:00 - LCD_TIMEOUT, LCD Time Out

00H - LCD always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds
↕
FEH - Enabled for 254 x 5 seconds
FFH - LCD enabled

8.6 PMC INPUTS

Port Address 8872H - Bits 15:08 Read and Write
Bits 07:00 Read only

15	14	13	12	11	10	09	08
PMC_ UPD	EN_ LCL	AF 7	AF 6	AF 5	AF 4	AF 3	AF 2

07	06	05	04	03	02	01	00
IN 7	IN 6	IN 5	IN 4	IN 3	IN 2	IN 1	IN 0

Signal Name	Default At RSTIN
PMC_UPD	0
EN_LCL	0
AF7:AF2	0
IN7:IN0	None

Bit 15 - PMC_UPD, Enable PMC Update

PMC_UPD = 0 -
No update cycles occur.

PMC_UPD = 1 -
A change of state of the PMC outputs 15 through 0 (Port Address 7072H and 7872H) or the internal A20 GATE causes an update cycle of the PMC 15:0 output latch.

Bit 14 - EN_LCL, Enable Local Request

EN_LCL either enables the PMCIN 2 to be defined by the user or to initiate a local access of the WD8110/LV internal registers from the keyboard controller.

EN_LCL = 0 -
PMCIN 2 is user defined.

EN_LCL = 1 -
PMCIN 2 is LOCAL_REQ.

Bits 13:08 - AF7:AF2, Local Attention Flags

Local attention flags AF7 through AF2 are set to indicate which PMC input(s) have caused LCL_ATN in PMC Interrupt Enable Register at Port Address C872H to be asserted. To clear the flag and corresponding IN bit in the PMC Inputs Register, it is necessary to clear the corresponding EA bit in PMC Interrupt Enable Register. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and AF flag.

AF7 - AF2 = 0 -
This PMC input did not cause LCL_ATN to be asserted.

AF7 - AF2 = 1 -
This PMC input caused LCL_ATN to be asserted.

Bits 07:00 - IN7:IN0, PMC Inputs 7:0

The Activity Monitor Mask Register at Port Address D872H may be used to select one of the PMC inputs IN7 through IN2 as a source of activity for power management purposes.

IN7:0 are status flags which provide information about the corresponding PMC input IN7 through IN0. IN1 and IN0 represent the current state of the input, while IN7 through IN2 represent either the current state or a latched transition. An IN7 through IN2 status is unlatched when both the corresponding EI and EA bits in the PMC Interrupt Enable Register at Port Address C872H are reset. It becomes a latched status when either the corresponding EI or EA bit is set. See Table 8-2.

8.7 PMC INTERRUPT ENABLE

Port Address C872H - Read and Write

15	14	13	12	11	10	09	08
Non-maskable Interrupt Enable EI7 EI6 EI5 EI4 EI3 EI2							

07	06	05	04	03	02	01	00
Local Attention Enable EA7 EA6 EA5 EA4 EA3 EA2							

Signal Name	Default At RSTIN
EI7-EI2	0
EA7-EA2	0

Bits 15:10 - EI7:EI2, Non-maskable Interrupt Enable 7 through 2

EI7:EI2 enable the generation of an NMI when the corresponding PMC inputs IN_7:IN_2 at Port Address 8872H change state. For example, when EI7 is a 1 and IN_7 changes from a 0 to 1 an NMI will be generated.

EI7:EI2 = 0 -
Non-maskable Interrupt not enabled

EI7:EI2 = 1 -
Non-maskable Interrupt is enabled

Bits 09:08 - Not used, state is ignored

Bits 07:02 - EA7:EA2, Local Attention Enable

EA7 through EA2 enable the assertion of LCL_ATN by the corresponding IN_7 through IN_2. LCL_ATN is PMC output number 4.

EA7-EA2 = 0 -
LCL_ATN is not enabled

EA7-EA2 = 1 -
LCL_ATN is enabled. If LAEN at Port Address 7C72H is set, SMI will occur. Refer to Section 9.2.

Bits 01:00 - Not used, state is ignored

PMC INPUT NUMBER ①	PMC INPUT NAME	INTERRUPT ON	SETS FLAG NUMBER ②
00H	$\overline{\text{TURBO}}$		
01H	PROC_PWR_GOOD		
02H	LCL_REQ or User Defined	Transition	IF2 or AF2
03H	User Defined	Transition	IF3 or AF3
04H	User Defined	Transition	IF4 or AF4
05H	User Defined	Transition	IF5 or AF5
06H	User Defined	Transition	IF6 or AF6
07H	User Defined	Active Edge	IF7 or AF7

① Port Address 8872H, Section 8.6
② Port Address 9072H, Section 8.8
Port Address 8872H, Section 8.6

TABLE 8-2. PMCIN INPUTS

8.8 NMI STATUS

Port Address 9072H - Read and Write

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
Non-maskable Interrupt Flags IF7 IF6 IF5 IF4 IF3 IF2						0	0

Signal Name	Default At RSTIN
IF7:IF2	0

Bits 15:08 - Not used, must be 0

Bits 07:02 - IF7:IF2, Non-maskable Interrupt Flags 7 through 2

NMI interrupt flags IF7:IF2 are set to indicate which PMC input(s), if any, have caused NMI to be asserted. To reset the flag and corresponding IN status bit in the PMC Input Register at Port Address 8872H, it is necessary to reset the corresponding bit in the PMC Interrupt Enable Register at Port Address C872H. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and IF flag.

Bits 01:00 - Not used, must be 0

8.9 SERIAL/PARALLEL SHADOW REGISTER

Port Address D072H - Read only

The Shadow Register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board serial and parallel devices.

15	14	13	12	11	10	09	08
Serial Port A SP_A		Serial Port B SP_B		Parallel Port 2 PP_2			

07	06	05	04	03	02	01	00
Parallel Port 0 PP_0							

Signal Name	Default At RSTIN
All signals	None

Bits 15:14 - SP_A, Serial Port A Register 2

This field represents bits 7 and 6 of Serial Port A Register 2.

Bits 13:12 - SP_B, Serial Port B Register 2

This field represents bits 7 and 6 of Serial Port B Register 2.

Bits 11:08 - PP_2, Parallel Port Register 2

This field represents bits 3:0 of Parallel Port Register 2.

Bits 07:00 - PP_0, Parallel Port Register 0

This field represents bits 7:0 of Parallel Port Register 0.

8.10 INTERRUPT CONTROLLER SHADOW REGISTER

Port Address D472H - Read only

When performing a resume operation, it may be advantageous to reset and reinitialize the interrupt controllers in the System Controller. Since many of the interrupt control registers are write only, it is impossible to determine the state of the interrupt controllers at suspend time. This register makes it possible to determine the state of selected signals internal to the master and slave interrupt controllers. With this information, when the interrupt control registers are reinitialized during resume, they can be returned to the state in which they were before suspend.

ICW2, ICW4, OCW2 and OCW3 referred to in this text is further defined in Sections 5.5.2.2, 5.5.2.4, 5.5.3.2 and 5.5.3.3.

15	14	13	12	11	10	09	08
AMT OUT	DEV		TM7	TS7	SF NM	AUT_ EOI	RA_ EOI

07	06	05	04	03	02	01	00
Priority Level Master PLM2	PLM1	PLM0	Priority Level Slave PLS2	PLS1	PLS0	SMM M	SMM S

Signal Name	Default At RSTIN
DEV	10
All other signals	None

Bit 15 - AMTOUT, Activity Monitor Timeout

AMTOUT represents the current state of the timeout comparator in the activity monitor. It is for test purposes only

Bits 14:13 - DEV, Device

DEV = 10 and identifies the device as WD8110.

This field is reserved for future device identifiers of the WD8110 family parts.

Bit 12 - TM7, Master Interrupt Vector Bit 7

TM7 represents bit 7 of the Interrupt Vector in the Master Interrupt Controller as set by ICW2. Bits 6:3 of the Interrupt Vector may be read from D6:3 by a Poll Command to the Master Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 11 - TS7, Slave Interrupt Vector Bit 7

TS7 represents bit 7 of the Interrupt Vector in the Slave Interrupt Controller as set by ICW2. Bits 6:3 of the Interrupt Vector may be read from D6:3 by a Poll Command to the Slave Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 10 - SFNM, Special Fully Nested Mode

SFNM represents the state of ICW4 - bit 4 in the Master Interrupt Controller. The WD8110/LV does not require SFNM for the slave interrupt controller and ignores its state.

Bit 09 - AUT_EOI, Auto End Of Interrupt

AUT_EOI represents the state of ICW4 - bit 1 in the Master Interrupt Controller. The WD8110/LV does not require AUT_EOI for the slave interrupt controller and ignores its state.

Bit 08 - RA_EOI, Rotate Auto End Of Interrupt

RA_EOI indicates whether or not Rotate On Automatic End Of Interrupt has been selected in the Master Interrupt Controller by EOI_CONT (bits 7:5 of OCW2). The WD8110/LV does not require Rotate On End Of Interrupt for the slave interrupt controller and ignores its state.

RA_EOI = 0 -
Rotate On Auto End Of Interrupt has not been selected.

RA_EOI = 1-
Rotate On Auto End Of Interrupt has been selected.

Bits 07:05 - PLM2:PLM0, Priority Level Master

PLM2:PLM0 represent the bottom priority level programmed into the Master Interrupt Controller by INT_LEV (OCW2 bits 2:0).

Bits 04:02 - PLS2:PLS0, Priority Level Slave

PLS2:PLS0 represent the bottom priority level programmed into the Slave Interrupt Controller by INT_LEV (OCW2 bits 2:0).

Bit 01 - SMMM, Special Mask Mode Master

SMMM indicates whether Special Mask Mode has been set in the Master Interrupt Controller by a write to SMM in OCW3.

SMMM = 0 -
Special Mask Mode is not enabled.

SMMM = 1 -
Special Mask Mode is enabled.

Bit 00 - SMMS, Special Mask Mode Slave

SMMS indicates whether Special Mask Mode has been set in the Slave Interrupt Controller by a write to SMM in OCW3.

SMMS = 0 -
Special Mask Mode is not enabled.

SMMS = 1 -
Special Mask Mode is enabled.

8.11 PORT 70H SHADOW REGISTER

Port Address E472H - Bits 15:12, 10:00 Read only
Bit 11 Read and Write

This register provides information on the status of interrupts and DMA which is useful for determining when the processor may be placed in the sleep mode. Two bits are also provided for generating software delays without incurring the operating system traps that would result from accessing I/O Port Address 0061H in virtual 86 mode. This register also contains a shadow of the Real Time Clock Address Register, a write only I/O port. It is necessary to access the Real Time Clock CMOS RAM during Suspend/Resume operations. This shadow of Port Address 0070H allows it to be restored to the same state it was in at suspend time.

This register can be read without first unlocking the WD8110/LV. This is important since the CLK32K, REFDET, and TODUN bits may need to be read frequently.

15	14	13	12	11	10	09	08
CLK 32K	REF_ DET	INTRQ	NO_ DMA	TOD UN	Reserved		

07	06	05	04	03	02	01	00
D NMI	RTC A6	RTC A5	RTC A4	RTC A3	RTC A2	RTC A1	RTC A0

Signal Name	Default At RSTIN
D_NMI	1
Reserved	0
All other signals	None

Bit 15 - CLK32K

CLK32K is PDREF at input pin 129 divided by two. CLK32K may be read to provide a stable timing reference, not subject to reprogramming of the refresh rate. CLK32K has a 30.5 µs period and 50% duty cycle.

Bit 14 - REF_DET, Refresh Detect

REF_DET is a copy of the REF_DET bit available from I/O Port Address 0061H, Bit 4 described in Section 5.9.

Bit 13 - INTRQ, Interrupt Request

INTRQ represents the state of the INTRQ output pin 54 to the CPU.

Bit 12 - NO_DMA, No DMA

NO_DMA = 0
A DMA or Bus Master Cycle has occurred within the last 61 µs

NO_DMA = 1
A DMA or Bus Master Cycle has not occurred within the last 30.5 µs

Bit 11 - TODUN, Time of Day Update Needed

This is a general purpose storage bit which can be written and read but has no effect on internal logic. Its purpose is to allow an SMI handler to signal the operating system that the time of day has been corrupted. This bit is checked by the Timer 0 Interrupt Handler. Note that although this bit is readable without unlocking the WD8110/LV, it cannot be written unless the WD8110/LV is unlocked.

Bits 10:08 - Reserved

Bit 07 - D_NMI, Disable Non-Maskable Interrupt Shadow

D_NMI represents the state of the D_NMI bit as it was set the last time I/O Port Address 0070H described in Section 5.8.1 was written.

Bits 06:00 - RTC_A6:RTC_A0, Real Time Clock Address Shadow

RTC_A(6:0) represents the state of the Real Time Clock Address Register as it was set the last time I/O Port Address 0070H was written.

8.12 ACTIVITY MONITOR CONTROL REGISTER

Port Address B072H - Bits 15, 13:11, 08:00 Read and Write
Bits 14, 10, 09 Read only

For an overview of the Activity Monitor Register, see the general description of the Activity Monitor Mask Register in Section 8.13.

15	14	13	12	11	10	09	08
IRR_ AE	CB12	AM TM	ACT LCH	IND ET	ACT AFT	ACT BEF	AM EN

07	06	05	04	03	02	01	00
Coarse Timeout Count AMC7 AMC6 AMC5 AMC4				Fine Timeout Count AMC3 AMC2 AMC1 AMC0			

Signal Name	Default At RSTIN
IRRAE	0
CB12	None
AMTM	0
ACTLCH	None
INDET	None
ACTAFT	None
ACTBEF	None
AMEN	0
AMC7:AMC0	0

Bit 15 - IRRAE, Interrupt Request Register Activity Enable

IRRAE controls whether or not the IRR (Interrupt Request Register) bits from the Interrupt Controller at Port Address 020H, 0A0H may be a source of activity (refer to Section 5.5).

IRRAE = 0 -
No IRR bits can be used as an activity source.

IRRAE = 1 -
IRR bits can be a source of activity. IRR8, IRR7 and IRR0 may still be masked by Port Address D872H.

Bit 14 - CB12, Counter Bit 12

For factory use only.

The activity monitor circuitry contains a 17-bit timeout counter for generating long timeouts. For test purposes, CB12 represents the twelfth bit of that counter.

Bit 13 - AMTM, Activity Monitor Test Mode

AMTM = 0 -
Activity Monitor functions normally.

AMTM = 1 -
Activity Monitor is in Test Mode. Activity Monitor State Machine is clocked faster than normal and nine stages of the 17-bit timeout counter are bypassed.

Bit 12 - ACTLCH, Activity Latch

This latch is always enabled regardless of other enable bit settings. Writing a 1 to ACTLCH has no effect.

ACTLCH = 0 -
The Activity Latch is reset by writing 0 to ACTLCH.

ACTLCH = 1 -
Activity by an unmasked source has occurred.

Bit 11 - INDET, Inactivity Detect

Writing a 1 to INDET has no effect.

INDET = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

INDET = 1 -
System is idle and the Activity Monitor has requested the local attention output be set. This occurs when there has been no unmasked activity, allowing the predetermined timeout (bits 07:00) to be reached.

NOTE

PMCIN transitions may also cause the local attention (LCL_ATN PMC 4) output to be set.

Bit 10 - ACTAFT, Activity After INDET

ACTAFT is a read only bit and its state is ignored during writes.

ACTAFT = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTAFT = 1 -
Activity has occurred after INDET had been set. This would happen when activity occurs during the time it takes to reach the interrupt service routine invoked by the local attention output request.

Bit 09 - ACTBEF, Activity Before INDET

ACTBEF is a read only bit and its state is ignored during writes.

ACTBEF = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTBEF = 1 -
Activity did occur and reset the timeout counter before INDET was set. This is important if consecutive timeout periods are being counted in a service routine to obtain a system timeout period other than that available using AMC(7:0) (bits 07:00). It would be necessary for the routine to clear the software counter if ACTBEF were set since there would have been no activity only for the period of time programmed in AMC(7:0).

Bit 08 - AMEN, Activity Monitor Enable

This is the master enable for the Activity Monitor.

AMEN = 0 -
Writing 0 to AMEN places the Activity Monitor in the idle state.

AMEN = 1 -
Writing 1 to AMEN causes the Activity Monitor to start clocking the timeout counter. Each time an unmasked source of activity is detected the counter is cleared. If no unmasked source of activity is detected before the timeout counter reaches the value programmed by ACM(7:0), INDET and the local attention output are set. The timeout counter is then cleared and a new timeout sequence begins.

Bits 07:04 - AMC7:AMC4, Activity Monitor Counter Coarse

AMC(7:4) establish the timeout values from 64 seconds to 16 minutes in 64-second increments. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

AMC 7	6	5	4		
0	0	0	0	-	0 seconds
0	0	0	1	-	1 minute, 4 seconds
0	0	1	0	-	2 minutes, 8 seconds
0	0	1	1	-	3 minutes, 12 seconds
0	1	0	0	-	4 minutes, 16 seconds
0	1	0	1	-	5 minutes, 20 seconds
0	1	1	0	-	6 minutes, 24 seconds
0	1	1	1	-	7 minutes, 28 seconds
1	0	0	0	-	8 minutes, 32 seconds
1	0	0	1	-	9 minutes, 36 seconds
1	0	1	0	-	10 minutes, 40 seconds
1	0	1	1	-	11 minutes, 44 seconds
1	1	0	0	-	12 minutes, 48 seconds
1	1	0	1	-	13 minutes, 52 seconds
1	1	1	0	-	14 minutes, 56 seconds
1	1	1	1	-	16 minutes, 0 seconds

Bits 03:00 - AMC3:AMC0, Activity Monitor Counter Fine

AMC(3:0) establish the timeout values from 7.8 milliseconds to 117.2 milliseconds in 7.8 millisecond increments. Tolerance on time delays is -0, +3.9 milliseconds. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

AMC 3	2	1	0	
0	0	0	0	- 0 milliseconds
0	0	0	1	- 7.8 milliseconds
0	0	1	0	- 15.6 milliseconds
0	0	1	1	- 23.4 milliseconds
0	1	0	0	- 31.3 milliseconds
0	1	0	1	- 39.1 milliseconds
0	1	1	0	- 46.9 milliseconds
0	1	1	1	- 54.7 milliseconds
1	0	0	0	- 62.5 milliseconds
1	0	0	1	- 70.3 milliseconds
1	0	1	0	- 78.1 milliseconds
1	0	1	1	- 85.9 milliseconds
1	1	0	0	- 93.8 milliseconds
1	1	0	1	- 101.6 milliseconds
1	1	1	0	- 109.4 milliseconds
1	1	1	1	- 117.2 milliseconds

NOTE

The fine timeout delay (AMC3 through AMC0) is added to the coarse timeout delay (AMC7 through AMC4) to obtain the total timeout delay.

8.13 ACTIVITY MONITOR MASK REGISTER

Port Address D872H - Read and Write

The activity monitor provides a hardware solution for determining inactivity in a system. Knowing when a system is inactive is key to performing such power reduction activities as suspend. When the Activity Monitor is enabled by the Activity Monitor Control Register at Port Address B072H, the Activity Monitor clocks a counter and invokes a service routine using local attention when the counter reaches a programmed timeout value. However, while the counter is being clocked, the Activity Monitor continuously monitors for any of several events that would indicate that the system is active. If any of these events occur, the counter is reset and the timeout starts over. Thus the service routine is only invoked when the system has been inactive for a programmed period of time.

To provide a high degree of flexibility in determining what is active and what is not, many sources are routed to the Activity Monitor. These include the IRR (Interrupt Request Register) and ISR (In Service Register) bits from the Interrupt Controller, the PMC inputs, NMI output, DMA (or AT Master) cycles and I/O accesses to either the numeric coprocessor, hard disk data port or programmable chip select. All of these sources are considered activity unless masked.

The interrupt input masks are controlled in the lower byte. All ISR and IRR bits are detected as activity except those specifically masked. Note, however, that ISR2 and IRR2 are not examined since they are cascade interrupts only. Also, IRR3 and IRR4 are qualified by the Mask Register in the Interrupt Controller before being passed to the Activity Monitor. The master mask for all IRR bits is the IRRAE bit in the register at Port Address B072H.

15	14	13	12	11	10	09	08
PCS_1M	PMCILS	PMCIS2	PMCIS1	PMCIS0	NMIM	HDDM	COPM

07	06	05	04	03	02	01	00
IMS1	IMS0	IRR8M	IRR7M	IRR0M	IRS8M	IRS7M	IRS0M

Signal Name	Default At RSTIN
All signals	0

Bit 15 - PCS_1M, Programmable Chip Select 1 Mask

PCS1M = 0 -
Read or write I/O accesses to the ports defined by the programmable chip select 1 in the WD8110/LV are considered activity.

PCS1M = 1 -
Read or write I/O accesses to the ports defined by the programmable chip select 1 in the WD8110/LV are ignored.

Bit 14 - PMCILS, Power Management Control Input Level Select

PMCILS determines which logic level on the selected PMC input is to be considered active. (See bits 13:11, PMCIS2:0.)

PMCILS = 0 -
PMCIN is active low.

PMCILS = 1 -
PMCIN is active high.

Bits 13:11 - PMCIS(2:0), Power Management Control Input Select

One of the PMC inputs IN7 through IN2 at Port Address 8872H may be selected for detection as a source of activity.

NOTE

The EI and EA bits at Port Address C872H, corresponding to the selected IN signal, should be cleared to prevent the IN signal from being latched internally.

PMCIS 2	1	0		
0	0	0	-	PMC input 2 selected
0	0	1	-	PMC input 3 selected
0	1	0	-	PMC input 4 selected
0	1	1	-	PMC input 5 selected
1	0	0	-	PMC input 6 selected
1	0	1	-	PMC input 7 selected
1	1	0	-	Reserved
1	1	1	-	Disabled, no PMC inputs checked

Bit 10 - NMIM, Non-maskable Interrupt Mask

NMIM = 0 -
The NMI output is used as a source of activity.

NMIM = 1 -
The NMI output is ignored.

Bit 09 - HDDM, Hard Disk Data Port Mask

HDDM = 0 -
If the hard disk chip select has been enabled by bit 01 at Port Address 2872H, I/O read and write operations to the 16-bit hard disk data port are allowed as a source of activity.

HDDM = 1 -
The hard disk data port I/O is ignored.

Bit 08 - COPM, Coprocessor Mask

COPM = 0 -
I/O cycles to the coprocessor are treated as a source of activity. Coprocessor cycles are detectable in 80386SX systems when A23 is high and M/$\overline{IO}$ is low and 80386DX systems when A31 is high and M/$\overline{IO}$ is low.

COPM = 1 -
I/O to the coprocessor is ignored.

Bits 07:06 - IMS1:0, Interrupt Mask Select

The local attention generated by the Activity Monitor will be routed to an available interrupt input to invoke a service routine. That interrupt is not to be detected as a source of activity. IMS(1:0) provide a selection of four possible inputs to be used for this function and masks the corresponding IRR and ISR bits as sources of activity.

IMS 1	0		
0	0	-	IRQ5 masked
0	1	-	IRQ10 masked
1	0	-	IRQ11 masked
1	1	-	IRQ15 masked

Bit 05 - IRR8M, Interrupt Request Register 8 Mask

IRR8M = 0 -
Real-Time Clock Interrupt (IRR8) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR8M = 1 -
Real-Time Clock Interrupt (IRR8) is ignored.

NOTE

See Test Enable Register (A872H), Section 10.3 for information about IRQ9 enable control.

See SMI Auxiliary Control Register (5472H), Section 9.3, for a definition of the activity masks for PCS2M and PCS3M.

Bit 04 - IRR7M, Interrupt Request Register 7 Mask

IRR7M = 0 -
Parallel Port or Spurious Interrupt (IRR7) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR7M = 1 -
Parallel Port or Spurious Interrupt (IRR7) is ignored.

Bit 03 - IRR0M, Interrupt Request Register 0 Mask

IRR0M = 0 -
Time Of Day Interrupt (IRR0) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR0M = 1 -
Time Of Day Interrupt (IRR0) is ignored.

Bit 02 - ISR8M, Interrupt Service Register 8 Mask

ISR8M = 0 -
Real-Time Clock Interrupt (ISR8) may be detected as a source of activity.

ISR8M = 1 -
Real-Time Clock Interrupt (ISR8) is ignored.

Bit 01 - ISR7M, Interrupt Service Register 7 Mask

ISR7M = 0 -
Parallel Port or Spurious Interrupt (ISR7) may be detected as a source of activity.

ISR7M = 1 -
Parallel Port or Spurious Interrupt (ISR7) is ignored.

Bit 00 - ISR0M, Interrupt Service Register 0 Mask

ISR0M = 0 -
Time of Day Interrupt (ISR0) may be detected as a source of activity.

ISR0M = 1 -
Time Of Day Interrupt (ISR0) is ignored.

8.14 3V SUSPEND (HIBERNATION) SHADOW REGISTERS

The 3V suspend mode provides maximum power savings for the system. The contents of the DRAM, Chip Set Registers, CPU Registers and Video RAM are all written to the hard disk and then all voltages are shut down, including the power supply. The only logic left on in this mode is the real-time clock and a 3 volt suspend controller. The real-time clock and the 3 volt suspend controller run off of the real-time clock battery. When the resume request is sampled by the suspend controller, the suspend controller enables the power supply and resumes the system.

To maintain compatibility with the IBM AT, the timer and DMA registers cannot be read back. To overcome this, these registers are shadowed and read back through other registers. (See the descriptions for register B872H in Section 5.4.15, register D072H in Section 8.9, register D472H in Section 8.10, registers 3C72H, 4472H and 4C72H in Section 8.14.1, 8.14.2 and 8.14.3.)

8.14.1 DMA Shadow Register 1

Port Address 3C72H - Read only

15	14	13	12	11	10	09	08
AD_ DEC2	AUTO 2	TRA_TYP2		TRA_MOD1		AD_ DEC1	AUTO 1

07	06	05	04	03	02	01	00
TRA_TYP1		TRA_MOD0		AD_ DEC0	AUTO 0	TRA_TYP0	

Signal Name	Default At RSTIN
All Signals	0

Bit 15 - AD_DEC2, Address Decrement 2

AD_DEC bit of register at Port Address 00BH for DMA channel 2.

Bit 14 - AUTO2, Autoinitialize 2

AUTO bit of register 00BH for DMA channel 2.

Bits 13:12 - TRA_TYP2, Transfer Type 2

TRA_TYP bits of register at Port Address 00BH for DMA channel 2.

Bits 11:10 - TRA_MOD1, Transfer Mode 1

TRA_MOD bits of register at Port Address 00BH for DMA channel 1.

Bit 09 - AD_DEC1, Address Decrement 1

AD_DEC bit of register at Port Address 00BH for DMA channel 1.

Bit 08 - AUTO1, Autoinitialize 1

AUTO bit of register at Port Address 00BH for DMA channel 1.

Bits 07:06 - TRA_TYP1, Transfer Type 1

TRA_TYP bits of register at Port Address 00BH for DMA channel 1.

Bits 05:04 - TRA_MOD0, Transfer Mode 0

TRA_MOD bits of register at Port Address 00BH for DMA channel 0.

Bit 03 - AD_DEC0, Address Decrement 0

AD_DEC bit of register at Port Address 00BH for DMA channel 0.

Bit 02 - AUTO0, Autoinitialize 0

AUTO bit of register at Port Address 00BH for DMA channel 0.

Bits 01:00 - TRA_TYP0, Transfer Type 0

TRA_TYP bits of register at Port Address 00BH for DMA channel 0.

8.14.2 DMA Shadow Register 2

Port Address 4472H - Read only

15	14	13	12	11	10	09	08
TRA_TYP6		TRA_MOD5		AD_ DEC5	AUTO 5	TRA_TYP5	

07	06	05	04	03	02	01	00
TRA_MOD3		AD_ DEC3	AUTO 3	TRA_TYP3		TRA_MOD2	

Signal Name	Default At RSTIN
All signals	0

Bits 15:14 - TRA_TYP6, Transfer Type 6

TRA_TYP bits of register at Port Address 0D6H for DMA channel 6.

Bits 13:12 - TRA_MOD5, Transfer Mode 5

TRA_MOD bits of register at Port Address 0D6H for DMA channel 5.

Bit 11 - AD_DEC5, Address Decrement 5

AD_DEC bit of register at Port Address 0D6H for DMA channel 5.

Bit 10 - AUTO5, Autoinitialize 5

AUTO bit of register at Port Address 0D6H for DMA channel 5.

Bits 09:08 - TRA_TYP5, Transfer Type 5

TRA_TYP bits of register at Port Address 0D6H for DMA channel 5.

Bits 07:06 - TRA_MOD3, Transfer Mode 3

TRA_MOD bits of register at Port Address 00BH for DMA channel 3.

Bit 05 - AD_DEC3, Address Decrement 3

AD_DEC bit of register at Port Address 00BH for DMA channel 3.

Bit 04 - AUTO3, Autoinitialize 3

AUTO bit of register at Port Address 00BH for DMA channel 3.

Bits 03:02 - TRA_TYP3, Transfer Type 3

TRA_TYP bits of register at Port Address 00BH for DMA channel 3.

Bits 01:00 - TRA_MOD2, Transfer Mode 2

TRA_MOD bits of register at Port Address 00BH for DMA channel 2.

8.14.3 DMA Shadow Register 3

Port Address 4C72H - Bit 15 Read and Write
Bits14:0 Read only

15	14	13	12	11	10	09	08
SCB		EX_ WR	RO_ PRI		CO_ DIS	TRA_MOD7	

07	06	05	04	03	02	01	00
AD_ DEC7	AUTO 7	TRA_ TYP7		TRA_ MOD6		AD_ DEC6	AUTO 6

Signal Name	Default At RSTIN
All signals	0

Bit 15 - SCB, Shadow Control Bit

For more information regarding SCB see Sections 8.14.4 and 8.14.5)

SCB = 0 -
EX_WR, RO_PRI and CO_DIS from the Command Register at Port Address 0D0H is presented on bits 13, 12 and 10.

SCB = 1 -
EX_WR, RO_PRI and CO_DIS from the Command Register at Port Address 008H is presented on bits 13, 12 and 10.

Bit 14, Reserved

Bit 13 - EX_WR, Extended Write

If SCB = 0, this is EX_WR of Port Address 008H.

If SCB = 1, this is EX_WR of Port Address 0D0H.

Bit 12 - RO_PRI, Rotating Priority

If SCB = 0, this is RO_PRI of Port Address 008H.

If SCB = 1, this is RO_PRI of Port Address 0D0H.

Bit 11, Reserved

Bit 10 - CO_DIS, Controller Disabled

If SCB = 0, this is CO_DIS of Port Address 008H.

If SCB = 1, this is CO_DIS of Port Address 0D0H.

Bits 09:08 - TRA_MOD7, Transfer Mode 7

TRA_MOD bits of register at Port Address 0D6H for DMA channel 7.

Bit 07 - AD_DEC7, Address Decrement 7

AD_DEC bit of register at Port Address 0D6H for DMA channel 7.

Bit 06 - AUTO7, Autoinitialize 7

AUTO bit of register at Port Address 0D6H for DMA channel 7.

Bits 05:04 - TRA_TYP7, Transfer Type 7

TRA_TYP bits of register at Port Address 0D6H for DMA channel 7.

Bits 03:02 - TRA_MOD6, Transfer Mode 6

TRA_MOD bits of register at Port Address 0D6H for DMA channel 6.

Bit 01 - AD_DEC6, Address Decrement 6

AD_DEC bit of register at Port Address 0D6H for DMA channel 6.

Bit 00 - AUTO6, Autoinitialize 6

AUTO bit of register at Port Address 0D6H for DMA channel 6.

8.14.4 DMA Base Address and Count Register

When the SCB (bit 15 of DMA Shadow Register 3) is high, the DMA base address and base count can be read back from channels 0 through 7. When SCB is low, channels 0 through 7 represents the current address and current count.

8.14.5 Timer Count

When SCB (bit 15 of DMA Shadow Register 3) is high, the timer base count can be read back from registers at Port Addresses 040H:043H. When SCB is low, the registers at Port Addresses 040H:043H represents the timer current count. Refer to Sections 5.6 through 5.6.6

8.15 SUSPEND AND RESUME

When the WD8110/LV is in the Suspend Mode, it typically draws less than 500 µA. Figures 8-2 and 8-3 illustrate the steps that the WD8110/LV goes through during suspend and resume.

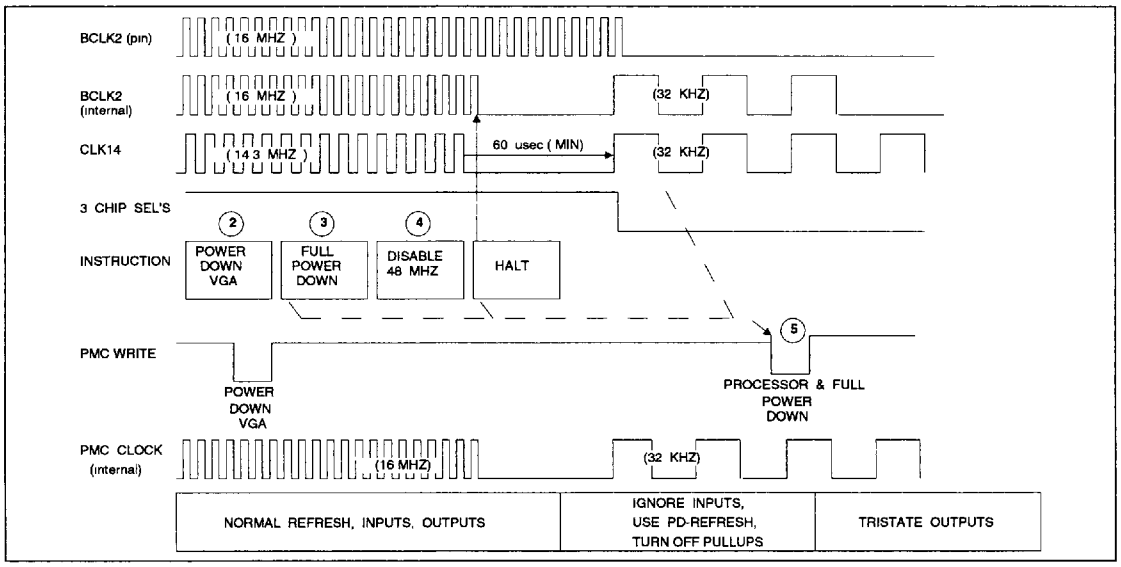


FIGURE 8-2. SUSPEND

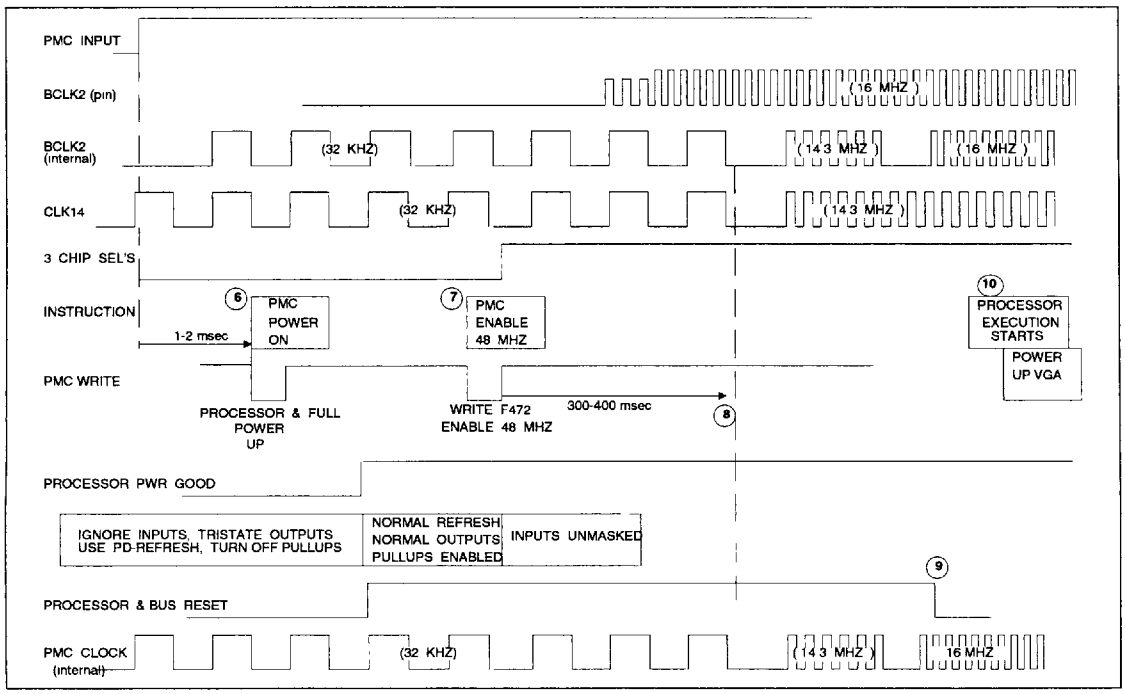


FIGURE 8-3. RESUME

This section describes the suspend/resume sequence shown in Figures 8-2 and 8-3. It is an approach for a low power mode for the WD8110/LV chip set that offers the lowest power drain possible but still allows the main system DRAM and video DRAM to be kept alive. This power-down mode requires specialized suspend/resume SMI Code software to control the operation. Figure 8-4 highlights the inter-connection within the chip set.

8.15.1 Going Into Suspend Mode

1. A change in the PMC input signals the WD8110/LV to generate either SMI or LCL_ATN. The processor vectors to the power-down routine and the processor saves its internal states and the states of the peripherals that are to be powered down. The processor saves the states into a protected area of the system DRAM.

2. The power-down routine writes to the full-power-down bit (FPD bit 13 at Port Address 1872H) which enables the power-down sequence. The WD8110/LV switches to sampling of the PMC inputs with the 14.318 MHz clock instead of the AT Bus clock.

3. The processor then writes to an I/O register in the WD8110/LV that switches a PMC output that is connected to the PWRDN input pin of the WD90C2X. Upon assertion of the PWRDN signal, the VGA controller enters the power-down mode which refreshes the video DRAM via the AT Bus REFRESH signal. CAS before RAS refresh is the preferred way of refreshing the DRAMs because it allows lower power operation without the generation of a DRAM refresh address.

4. The processor then writes to the Disable 48 MHz register (Port F072H) which causes the WD8110/LV to put a code of 15 on the encoded chip select bus. The WD76C20 decodes this write and disables its 48 MHz oscillator, glitchlessly switches the 14.318 MHz oscillator signal to a 32 KHz, 50% duty cycle signal and then disables the 14.318 MHz oscillator. The WD76C20 also asserts the CSSERA, CSSERB and CSPAR signals simultaneously which signals the WD76C30A to disable its 48 MHz oscillator. When this oscillator is disabled, the AT Bus Clock, Keyboard Clock and 80287 Clock are disabled. The processor executes a halt instruction and the WD8110/LV detects the halt status from the processor and switches from the AT compatible refresh to the PDREF controlled refresh. The WD8110/LV then switches the AT Bus compatible REFRESH output signal to reflect that of the PDREF input signal.

   The PDREF input is a CMOS level clock signal that has a 124 µs period and a low going pulse of 200 ns to 1 µs. This signal is always active and is adequate for refreshing low power DRAMs. This signal is generated by the WD76C20.

5. Upon detecting that the 14.318 MHz clock has been changed to 32 KHz, the WD8110/LV tristates all outputs except the PMC controls, DRAM controls, RA bus and AT Bus REFRESH signal. The CPURES signal is asserted and then tristated and is pulled high through a 200K pull-up resistor. All inputs except RSTIN, CLK14 and the PMC are ignored and all circuitry except the PMC and refresh logic is stopped.

   The power is now turned off to the CPU, BUS, etc., by the assertion of the FULLPWDN PMC output from the WD8110/LV.

6. The processor-power-good PMC input must now go low in order for this state machine to start monitoring a resume condition as described in Section 8.15.2

8.15.2 Coming Out of Suspend Mode (Resume)

1. The WD8110/LV is now sampling the PMC inputs at 32 KHz. At this time, the change of any enabled PMC input causes the FULLPWDN PMC output described in step 5 to switch, which powers up the processor, bus, etc. After 1 ms (timed from the 32 KHz clock input), the WD8110/LV samples the processor-power-good PMC input. When active the CPURES is driven high and the rest of the WD8110/LV control outputs are driven to their correct states, a BUS RESET is issued also.

2. Upon detecting the power-good signal, the WD8110/LV state machine performs a write to the ENABLE 48 MHz register which sends a code of 16 on the encoded chip select lines.

3. The WD76C20 receives the code, enables the 48 MHz and 14.318 MHz oscillators and de-asserts the CSSERA, CSSERB and CSPAR signals. After approximately 100 ms (enable time for the oscillators), the WD76C20 glitchlessly switches the 32 KHz signal to 14.318 MHz.

4. The WD76C30A enables its 48 MHz oscillator upon the de-assertion of its CSSERA, CSSERB and CSPAR input signals.

5. When the WD8110/LV detects that the 32 KHz has been switched to 14.318 MHz, it switches the PMC sampling to the AT Bus Clock. The WD8110/LV then switches from the PDREF controlled refresh to the AT compatible refresh. The WD8110/LV also switches the AT bus $\overline{\text{REFRESH}}$ signal from the PDREF input to the AT compatible refresh rate. The WD8110/LV de-asserts the CPURES signal and the processor comes out of reset and checks the shutdown status in the RTC RAM. This tells the processor that it is coming out of full-power-down mode as opposed to a warm or cold boot. The processor then restores the states of the machine.

6. The processor writes to the WD8110/LV register that causes the WD8110/LV to de-assert its PMC output. This output is connected to PWRDN input of the WD90C2X signaling the WD90C2X to come out of the power-down mode.

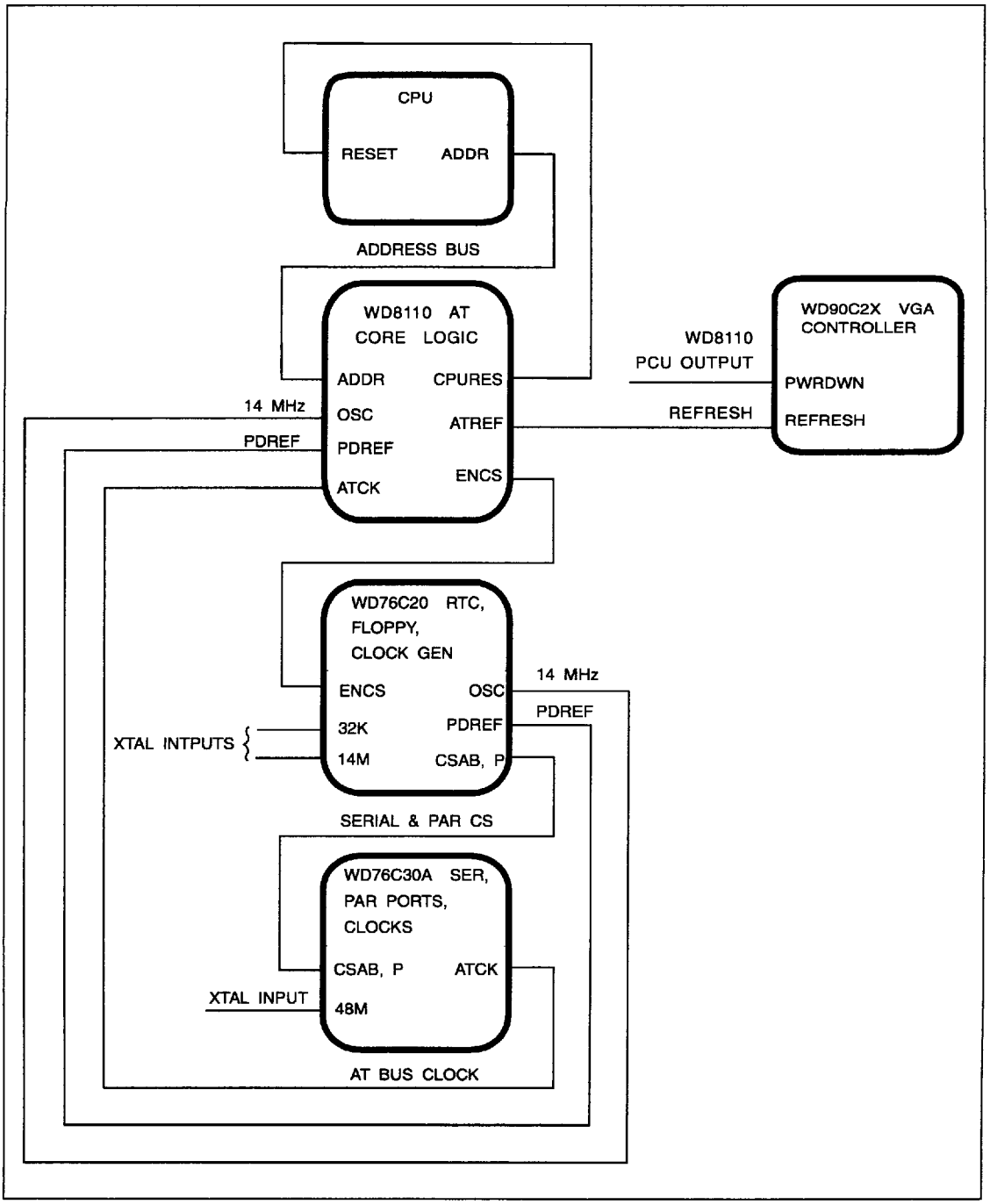


FIGURE 8-4. FULL POWER-DOWN MODE SYSTEM BLOCK DIAGRAM

9.0 SYSTEM MANAGEMENT INTERRUPT (SMI)

9.1 I/O TRAPS

In order to conserve power, certain I/O peripherals can be put to sleep when they are not in use. To accomplish this in a transparent manner, hardware must intercept (trap) any accesses made to the sleeping device and wake it up before allowing the access to proceed. The System Controller can trap accesses to I/O devices controlled by the following chip selects:

- Programmable Chip Select 1
- Programmable Chip Select 2
- Programmable Chip Select 3
- Serial Port A Chip Select
- Serial Port B Chip Select
- Parallel Port Chip Select

When access to an I/O device is trapped, the System Controller asserts the $\overline{SMI}$ pin 102 to the CPU. Control is transferred to the SMI handler routine which determines which I/O access caused the SMI handler to be invoked. The handler looks at the register at Port 7C72H to determine the I/O address accessed.

The SMI handler is located in SMI RAM. SMI RAM consists of from 64K to 256 Kbytes of DRAM space taken from split memory. Once the SMI service routine is loaded into SMI RAM space, the SMI RAM space can be hidden from system access and remapped to SMI address space. The only way to access the SMI address space after remap is to put the CPU in SMI mode.

9.1.1 IBM I/O Trap Register

Port Address 8472H - Read only when in Virus Protection mode.

15	14	13	12	11	10	09	08
IBM IOT	Reserved						

15	14	13	12	11	10	09	08
Reserved							

Signal Name	Default At RSTIN
All signals	0

Bit 15 - IBMIOT, IBM Trap Mode

When IBMIOT is set, a minimum of 12 CLKs between the assertion of SMI for an I/O trap and the end of the I/O instruction is ensured. This is required by IBM CPUs.

Bits 14:00 - Reserved

9.1.2 SMI I/O Trap Control Register

Port Address 7C72H - Bits 15:08 Read and Write
Bit 07 Read and Clear
Bits 06:00 Read only

15	14	13	12	11	10	09	08
LAEN	PH2_ SEL	INT_ SMI	I/O Trap Enable PC1_ TPE	PC2_ TPE	SPA_ TPE	SPB_ TPE	PAR_ TPE

07	06	05	04	03	02	01	00
TRPS	IOWS	I/O Trap Status PC3_ TPS	PC2_ TPS	PC1_ TPS	PAR_ TPS	SPA_ TPS	SPB_ TPS

Signal Name	Default At RSTIN
All signals	0

Bit 15 - LAEN, Local Attention Enable

There are three sources that can cause the Local Attention PMC output to be asserted. One is a transition on an unmasked PMC input pin (see description for registers at Port 8872H and C872H). The second is a signal from the System Activity Monitor (see description for registers at Port B072H and D872H). The third is a Watchdog Timer. These sources will also cause an SMI if LAEN is set high. The SMI is based on an internal version of Local Attention and occurs even if PMC updates are disabled.

LAEN = 0 -
Disables generation of $\overline{SMI}$ by a Local Attention

LAEN = 1 -
Enables $\overline{SMI}$ to be caused by a Local Attention

Bit 14 - PH2_SEL, Phase 2 SMI Select

PH2_SEL cannot be written to while in VPMODE.

PH2_SEL = 0 -
SMI on pin 102 is asserted as an output during phase 1 of the processor clock. This is the appropriate setting for AMD and Cyrix CPUs.

PH2_SEL = 1 -
SMI on pin 102 is asserted as an output during phase 2 of the processor clock. This is the appropriate setting for an Intel CPU.

Bit 13 - INT_SMI, Intel SMI

INT_SMI cannot be written to while in VPMODE.

INT_SMI = 0 -
The SMI handshake logic is configured for AMD, IBM and Cyrix CPUs. Pin 101 is SMIRDY.

INT_SMI = 1 -
The SMI handshake is configured for an Intel CPU. Pin 101 is FLUSH.

Bit 12 - PC1_TPE, Programmable Chip Select 1 Trap Enable

When set to 1, PC1_TPE enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Programmable Chip Select (See registers at Port 2872H and 3072H).

PC1_TPE = 0 -
Disable Trap

PC1_TPE = 1 -
Enable Trap

Bit 11 - PC2_TPE, Programmable Chip Select 2 Trap Enable

When set to 1, PC2_TPE enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the second programmable chip select (see registers at Port 5C72H and 6472H). This trap occurs even if the ENPCS2 bit at Port 5C72H is not set.

PC2_TPE = 0 -
Disable Trap

PC2_TPE = 1 -
Enable Trap

Bit 10 - SPA_TPE, Serial Port A Chip Select Trap Enable

When set to 1, SPA_TPE enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Serial Port A Chip Select (see register at Port 2072H).

SPA_TPE = 0 -
Disable Trap

SPA_TPE = 1 -
Enable Trap

Bit 09 - SPB_TPE, Serial Port B Chip Select Trap Enable

When set to 1, SPB_TPE enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Serial Port B Chip Select (see register at Port 2072H).

SPB_TPE = 0 -
Disable Trap

SPB_TPE = 1 -
Enable Trap

Bit 08 - PAR_TPE, Parallel Port Chip Select Trap Enable

When set to 1, PAR_TPE enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Parallel Port Chip Select (see register at Port 2072H).

PAR_TPE = 0 -
Disable Trap

PAR_TPE = 1 -
Enable Trap

Bit 07 - TRPS, Trap Status

The SMI handler polls TRPS to determine if an I/O trap caused the SMI. The source of the I/O Trap may be determined by reading bits 5:0. When TRPS is set to 0, all status bits (7:0) are reset to 0, preparing the I/O trap state machine to capture future I/O cycles. The SMI handler should do this each time it services an I/O trap. Writing a 1 to TRPS has no effect.

TRPS = 0 -
No I/O trap has occurred.

TRPS = 1 -
An I/O trap has occurred.

Bit 06 - IOWS, I/O Write Status

IOWS is set when the I/O cycle that caused a trap is a write operation. IOWS is cleared when a 0 is written to TRPS.

Bit 05 - PC3_TPS, Programmable Chip Select 3 Trap Status

PC3_TPS = 0 -
I/O trap did not occur on Programmable Chip Select 3.

PC3_TPS = 1 -
I/O trap did occur on Programmable Chip Select 3.

PC3_TPS is cleared during reset or when a 0 is written to TRPS.

Bit 04 - PC2_TPS, Programmable Chip Select 2 Trap Status

PC2_TPS = 0 -
I/O trap did not occur on Programmable Chip Select 2.

PC2_TPS = 1 -
I/O trap did occur on Programmable Chip Select 2.

PC2_TPS is cleared during reset or when a 0 is written to TRPS.

Bit 03 - PC1_TPS, Programmable Chip Select 1 Trap Status

PC1_TPS = 0 -
I/O trap did not occur on Programmable Chip Select 1.

PC1_TPS = 1 -
I/O trap did occur on Programmable Chip Select 1.

PC1_TPS is cleared during reset or when a 0 is written to TRPS.

Bit 02 - PAR_TPS, Parallel Port Trap Status

PAR_TPS = 0 -
I/O trap did not occur on Parallel Port Chip Select.

PAR_TPS = 1 -
I/O trap did occur on Parallel Port Chip Select.

PAR_TPS is cleared during reset or when a 0 is written to TRPS.

Bit 01 - SPA_TPS, Serial Port A Trap Status

SPA_TPS = 0 -
I/O trap did not occur on Serial Port A Chip Select.

SPA_TPS = 1 -
I/O trap did occur on Serial Port A Chip Select.

SPA_TPS is cleared during reset or when a 0 is written to TRPS.

Bit 00 - SPB_TPS, Serial Port B Trap Status

SPB_TPS = 0 -
I/O trap did not occur on Serial Port B Chip Select.

SPB_TPS = 1 -
I/O trap did occur on Serial Port B Chip Select.

SPB_TPS is cleared during reset or when a 0 is written to TRPS.

9.2 SMI I/O TIMEOUT

As a power conservation measure, it is desirable to put some I/O peripherals in the Sleep Mode when they are not in use. This may involve shutting off clocks or removing power. In order to do this, there must be a mechanism for determining that a device is not in use. In the System Controller, timers are included for each I/O device that is a candidate for power reduction measures. Each timer causes an $\overline{SMI}$ when no access is made to an I/O device for a programmable amount of time. The timers are reset by I/O read or write operations to any address which falls within the range of its chip select.

When an $\overline{SMI}$ is generated, the SMI handler takes whatever action is appropriate to power down the I/O peripheral. The handler then enables the I/O trap for that device so that it can be awakened the next time it is accessed.

9.2.1 SMI I/O Timeout Control Register

Port Address 9C72H - Bits 15, 04:00 Read and Write
Bits 14:05 Read only

15	14	13	12	11	10	09	08
F_SMI	PC1_ADS	PC2_ADS	SPA_ADS	SPB_ADS	PAR_ADS	PC1_TOS	PC2_TOS

07	06	05	04	03	02	01	00
SPA_TOS	SPB_TOS	PAR_TOS	PC1 TOE	PC2 TOE	SPA TOE	SPB TOE	PAR TOE

Signal Name	Default At RSTIN
All signals	0

Bit 15 - F_SMI, Force $\overline{SMI}$

F_SMI provides a means to invoke the SMI handler through software. When this bit is set to 1, the $\overline{SMI}$ pin 102 is asserted. F_SMI should be cleared by the $\overline{SMI}$ handler before it exits to prevent another $\overline{SMI}$.

F_SMI = 0 - Force $\overline{SMI}$ Disable

F_SMI = 1 - Force $\overline{SMI}$ Enable

Bit 14 - PC1_ADS, Programmable Chip Select 1 Activity Detect Status

PC1_ADS can be polled by the SMI handler to determine whether the programmable chip select I/O address range has been accessed since PC1_TOS was set. If PC1_ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PC1_ADS is cleared by reset or when PC1_TOE is cleared.

Bit 13 - PC2_ADS, Programmable Chip Select 2 Activity Detect Status

PC2_ADS can be polled by the SMI handler to determine if the second Programmable Chip Select's I/O address range has been accessed since PC2_TOS was set. If PC2_ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PC2_ADS is cleared by reset or when PC2_TOE is cleared.

Bit 12 - SPA_ADS, Serial Port A Chip Select Activity Detect Status

SPA_ADS can be polled by the SMI handler to determine if the Programmable Chip Select's I/O address range has been accessed since SPA_TOS was set. If SPA_ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. SPA_ADS is cleared by reset or when SPA_TOE is cleared.

Bit 11 - SPB_ADS, Serial Port B Chip Select Activity Detect Status

SPB_ADS can be polled by the SMI handler to determine if the Programmable Chip Select's I/O address range has been accessed since SPB_TOS was set. If SPB_ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. SPB_ADS is cleared by reset or when SPB_TOE is cleared.

Bit 10 - PAR_ADS, Parallel Port Chip Select Activity Detect Status

PAR_ADS can be polled by the SMI handler to determine if the programmable chip select I/O address range has been accessed since PAR_TOS was set. If PAR_ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PAR_ADS is cleared by reset or when PAR_TOE is cleared.

Bit 09 - PC1_TOS, Programmable Chip Select 1 Timeout Status

PC1_TOS can be polled by the SMI handler to determine the source of the SMI. PC1_TOS is set when an I/O access timeout has occurred for the Programmable Chip Select I/O address range. PC1_TOS is cleared by reset or when PC1_TOE is cleared.

Bit 08 - PC2_TOS, Programmable Chip Select 2 Timeout Status

PC2_TOS can be polled by the SMI handler to determine the source of the SMI. PC2_TOS is set when an I/O access timeout has occurred for the second Programmable Chip Select I/O address range. PC2_TOS is cleared by reset or when PC2_TOE is cleared.

Bit 07 - SPA_TOS, Serial Port A Chip Select Timeout Status

SPATOS can be polled by the SMI handler to determine the source of the SMI. SPA_TOS is set when an I/O access timeout has occurred for the Serial Port A Chip Select I/O address range. SPA_TOS is cleared by reset or when SPA_TOE is cleared.

Bit 06 - SPB_TOS, Serial Port B Chip Select Timeout Status

SPB_TOS can be polled by the SMI handler to determine the source of the SMI. SPB_TOS is set when an I/O access timeout has occurred for the Serial Port B Chip Select's I/O address range. SPB_TOS is cleared by reset or when SPB_TOE is cleared.

Bit 05 - PAR_TOS, Parallel Port Chip Select Timeout Status

PAR_TOS can be polled by the SMI handler to determine the source of the SMI. PAR_TOS is set when an I/O access timeout has occurred for the Parallel Port Chip Select I/O address range. PAR_TOS is cleared by reset or when PAR_TOE is cleared.

Bit 04 - PC1_TOE, Programmable Chip Select 1 Timeout Enable

PC1_TOE = 0 -
Programmable Chip Select 1 Timeouts disabled and PC1_TOS cleared.

PC1_TOE = 1 -
I/O access timeout for the Programmable Chip Select 1 I/O address range enabled.

Bit 03 - PC2_TOE, Programmable Chip Select 2 Timeout Enable

PC2_TOE = 0 -
Programmable Chip Select 2 timeouts disabled and PC2_TOS cleared.

PC2_TOE = 1 -
I/O access timeout for the Programmable Chip Select 2 I/O address range enabled.

Bit 02 - SPA_TOE, Serial Port A Chip Select Timeout Enable

SPA_TOE = 0 -
Serial Port A Chip Select timeouts disabled and SPA_TOS cleared.

SPA_TOE = 1 -
I/O access timeout for the Serial Port A Chip Select I/O address range enabled.

Bit 01 - SPB_TOE, Serial Port B Chip Select Timeout Enable

SPB_TOE = 0 -
Serial Port B Chip Select timeouts disabled and SPB_TOS cleared.

SPB_TOE = 1 -
I/O access timeout for the Serial Port B Chip Select I/O address range enabled.

Bit 00 - PAR_TOE, Parallel Port Chip Select Timeout Enable

PAR_TOE = 0 -
Parallel Port Chip Select timeouts disabled and PAR_TOS cleared.

PAR_TOE = 1 -
I/O access timeout for the Parallel Port Chip Select I/O address range enabled.

9.2.2 SMI I/O Timeout Count Register 1

Port Address A472H - Read and Write

15	14	13	12	11	10	09	08
SMI_ WUE	Pro. Chip Select Timeout Count 1 PC1_ TC4	PC1_ TC3	PC1_ TC2	PC1_ TC1	PC1_ TC0	Pro. Chip Sel PC2_ TC4	PC2_ TC3

07	06	05	04	03	02	01	00
ect Timeout Count 2 PC2_ TC2	PC2_ TC1	PC2_ TC0	Ser. Port A Chip Select Timeout Count SPA_ TC4	SPA_ TC3	SPA_ TC2	SPA_ TC1	SPA_ TC0

Signal Name	Default At RSTIN
All signals	0

Bit 15 - SMI_WUE, SMI Wake Up Enable

SMI_WUE, when set to 1, causes the assertion of SMI to wake up the processor from a power-down or stop clock state. An INTR, NMI, or DMA request wakes up the processor, regardless of the state of this bit. Note that setting SMI_WUE does not enable SMI to initiate a resume from suspend.

SMI_WUE = 0 -
Disable SMI Wakeup

SMI_WUE = 1 -
Enable SMI Wakeup

Bits 14:10 - PC1_TC 4:0, Programmable Chip Select 1 Timeout Count

PC1_TC 4:0, along with the timeout clock select PC1_TCS (Port AC72H bit 4), determine the time period during which an I/O peripheral, selected by the Programmable Chip Select, must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

PC1_TCS = 0 -
(Count in **PC1_TC4:0**) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PC1_TCS = 1 -
(Count in **PC1_TC4:0**) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Bits 09:05 - PC2_TC 4:0, Programmable Chip Select 2 Timeout Count

PC2_TC 4:0, along with the timeout clock select PC2_TCS (Port AC72H bit 3), determine the time period during which an I/O peripheral, selected by Programmable Chip Select 2, must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

PC2_TCS = 0 -
(Count in **PC2_TC4:0**) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PC2_TCS = 1 -
(Count in **PC2_TC4:0**) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Bits 4:0 - SPA_TC4:0, Serial Port A Chip Select Timeout Count

SPA_TC4:0, along with the timeout clock select SPA_TCS (Port AC72H bit 2), determine the time period during which Serial Port A must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

SPA_TCS = 0 -
(Count in **SPA_TC4:0**) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

SPA_TCS = 1 -
(Count in **SPA_TC4:0**) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

9.2.3 SMI I/O Timeout Count Register 2

Port Address AC72H - Read and Write

15	14	13	12	11	10	09	08
IOT CTM	Ser. Port B Chip Select Timeout Count SPB_ TC4	SPB_ TC3	SPB_ TC2	SPB_ TC1	SPB_ TC0	Par. Port Chip PAR_ TC4	PAR_ TC3

07	06	05	04	03	02	01	00
Select Timeout Count PAR_ TC2	PAR_ TC1	PAR_ TC0	Timeout Clock Select PC1_ TCS	PC2_ TCS	SPA_ TCS	SPB_ TCS	PAR_ TCS

Signal Name	Default At RSTIN
All signals	0

Bit 15 - IOTCTM, I/O Timeout Counter Test Mode

IOTCTM is for factory use only. When = 1, the timeout counters are placed into test mode.

Bits 14:10 - SPB_TC4:0, Serial Port B Chip Select Timeout Count

SPB_TC4:0, along with the timeout clock select SPB_TCS (this register bit 1), determine the time period during which Serial Port B must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

SPB_TCS = 0 -
(Count in **SPB_TC4:0**) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

SPB_TCS = 1 -
(Count in **SPB_TC4:0**) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Bits 09:05 - PAR_TC4:0, Parallel Port Chip Select Timeout Count

PAR_TC4:0, along with the timeout clock select PAR_TCS (this register bit 0), determine the time period during which the parallel port must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

PAR_TCS = 0 -
(Count in **PAR_TC4:0**) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PAR_TCS = 1 -
(Count in **PAR_TC4:0**) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Bit 04 - PC1_TCS, Programmable Chip Select 1 Timeout Clock Select

PC1_TCS selects the clock to be used for the Programmable Chip Select Timeout Counter.

PC1_TCS = 0 -
A high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less.

PC1_TCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution but a longer timeout period of over 20 minutes. See the description of PC1_TC4:0 (register at Port A472H bits 14:10) for more details.

Bit 03 - PC2_TCS, Programmable Chip Select 2 Timeout Clock Select

PC2_TCS selects the clock to be used for the second Programmable Chip Select Timeout Counter.

PC2_TCS = 0 -
A high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less.

PC2_TCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of PC2_TC4:0 (register at Port A472H bits 09:05) for more details.

Bit 02 - SPA_TCS, Serial Port A Chip Select Timeout Clock Select

SPA_TCS selects the clock to be used for the Serial Port A Timeout Counter.

SPA_TCS = 0 -
A high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less.

SPA_TCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of SPA_TC4:0 (register at Port A472H bits 04:00) for more details.

Bit 01 - SPB_TCS, Serial Port B Chip Select Timeout Clock Select

SPB_TCS selects the clock to be used for the Serial Port B Timeout Counter.

SPB_TCS = 0 -
A high-speed clock is used to obtain 4-second timing resolution for timeout periods of 2 minutes or less.

SPB_TCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of SPB_TC4:0 (this register bits 14:10) for more details.

Bit 00 - PAR_TCS, Parallel Port Chip Select Timeout Clock Select

PAR_TCS selects the clock to be used for the Parallel Port Timeout Counter.

PAR_TCS = 0 -
A high-speed clock is used to obtain 4-second timing resolution for timeout periods of 2 minutes or less.

PAR_TCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of PAR_TC4:0 (this register bits 09:05) for more details.

9.3 SMI AUXILIARY CONTROL REGISTER

Port Address 5472H - Bits 15, 13, 11:08, 05:00 Read and Write
Bits 07:06 Read only
Bit 12 Read and clear

15	14	13	12	11	10	09	08
TO_ MSK		WDO GEN	WDO GST	PCS 3M	PCS 2M	PC3 TPE	PC3 TOE

07	06	05	04	03	02	01	00
PC3 TOS	PC3 ADS	PC3 TC4	PC3 TC3	PC3 TC2	PC3 TC1	PC3 TC0	PC3 TCS

Signal Name	Default At RSTIN
All signals	0

Bit 15 - TO_MSK, Timeout Mask

When set to one, TO_MSK masks I/O device timeouts from causing assertion of the SMI output. If enabled, the I/O device timers continue to count down. If a timeout occurs, the SMI output is asserted after TO_MSK is cleared. Also, when TO_MSK is set, the I/O device timers will not detect I/O activity, thus preventing the timer from being reset.

Bit 14 - Reserved

Bit 13 - WDOGEN, Watchdog Timer Interrupt Enable

The interrupt is cleared either by writing a zero to WDOGST or WDOGEN to disable further watchdog interrupts. Note that the first interrupt after the Watchdog Timer is enabled can occur anytime from 62.5 ms to 125 ms later. Each interrupt causes LCL_ATN to be set, so that it is useful both with or without SMI support.

WDOGEN = 0 -
Disable periodic interrupt.

WDOGEN = 1 -
Enables a periodic interrupt to be generated every 125 ms.

Bit 12 - WDOGST, Watchdog Timer Interrupt Status

When WDOGST equals 1, LCL_ATN has been set due to a Watchdog Timer Interrupt Request. WDOGST is cleared by writing a zero to it. The Watchdog Timer continues to run and will set WDOGST at 125 ms intervals. WDOGST is also cleared when WDOGEN is set to a zero. Writing a 1 to WDOGST has no effect.

Bit 11 - PCS_3M, Programmable Chip Select 3 Mask

PCS_3M is an extension to the register at Port Address D872H.

PCS_3M = 0 -
I/O accesses to the Programmable Chip Select 3 address range (see registers at Port Address 5C72H and 6C72H) may be observed as a source of activity by the system activity monitor.

PCS_3M = 1 -
I/O accesses to the Programmable Chip Select 3 are masked from being seen by the system activity monitor. Note that the setting of ENP_CS3 in the register at Port Address 5C72H has no effect on I/O activity detection.

Bit 10 - PCS_2M, Programmable Chip Select 2 Mask

PCS_2M is an extension to the register at Port Address D872H.

PCS_2M = 0 -
I/O accesses to the Programmable Chip Select 2 address range (see registers at Port Address 5C72H and 6472H) are allowed to be observed as a source of activity by the system activity monitor.

PCS_2M = 1 -
I/O accesses to the Programmable Chip 2 Select are masked from being seen by the system activity monitor. Note that the setting of ENP_CS2 in the register at Port Address 5C72H has no effect on I/O activity detection.

Bit 09 - PC3_TPE, Programmable Chip Select 3 Trap Enable

PC3_TPE = 0 -
Trap not enabled

PC3_TPE = 1 -
An I/O trap will occur whenever an I/O read or write occurs at an address within the range covered by the third Programmable Chip Select (see registers at Port Address 5C72H and 6C72H). This trap occurs even if the ENP_CS3 bit in the register at Port Address 5C72H is not set.

Bit 08 - PC3_TOE, Programmable Chip Select 3 Timeout Enable

PC3_TOE = 0 -
Programmable Chip Select 3 timeouts are disabled and PC3_TOS and PC3_ADS are cleared.

PC3_TOE = 1 -
I/O access timeout for the third Programmable Chip Select I/O address range are enabled. The timeout count will be reset by I/O to the Programmable Chip Select 3 address range even if the ENP_CS3 bit in the register at Port 5C72H is not set.

Bit 07 - PC3_TOS, Programmable Chip Select 3 Timeout Status

PC3_TOS is set to 1 when an I/O access timeout has occurred for the Programmable Chip Select 3 I/O address range. It can be polled by the SMI handler in determining the source of the SMI. PC3_TOS is cleard when PC3_TOE is cleared.

Bit 06 - PC3_ADS, Programmable Chip Select 3 Activity Detect Status

PC3_ADS can be polled by the SMI Handler to see if the Programmable Chip Select 3 I/O address range has been accessed since PC3_TOS was set.

If PC3_ADS is set, an I/O access has occurred since the inactivity timeout was triggered. The SMI Handler will ignore the timeout and restart the timeout counter.

PC3_ADS is cleared when PC3_TOE is cleared.

Bits 05:01 - PC3_TC4:0, Programmable Chip Select 3 Timeout Count

PC3_TC4:0, along with the timeout clock select PC3_TCS (this register bit 0), determine the time period during which an I/O peripheral (selected by Programmable Chip Select 3) must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

PC3_TCS = 0 -
(Count in **PC3_TC4-0**) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PC3_TCS = 1 -
(Count in **PC3_TC4-0**) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Bit 00 - PC3_TCS, Programmable Chip Select 3 Timeout Clock Select

PC3_TCS selects the clock to be used for the Programmable Chip Select 3 timeout counter.

PC3_TCS = 0 -
A high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less.

PC3_TCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution but a longer timeout period of over 20 minutes. See the description of PC3_TC4:0 (this register bits 05:01) for more details.

9.4 PROGRAMMABLE CS2 AND CS3 CONTROL REGISTER

Port Address 5C72H - Read and Write

15	14	13	12	11	10	09	08
PCS 2L	ENP CS2	UMS K2	Prog. CS2 Lower Address Bits MASK 2LM SK4	2LM SK3	2LM SK2	2LM SK1	2LM SK0

07	06	05	04	03	02	01	00
PCS 3L	ENP CS3	UMS K3	Prog. CS3 Lower Address Bits MASK 3LM SK4	3LM SK3	3LM SK2	3LM SK1	3LM SK0

Signal Name	Default At RSTIN
All signals	0

Bit 15 - PCS_2L, Programmable Chip Select 2 Location

PCS_2L = 0 -
The I/O device selected by Programmable Chip Select 2 is located on the expansion bus.

PCS_2L = 1 -
The I/O device selected by Programmable Chip Select 2 is located on the RA0:7/ED0:7 bus.

Bit 14 - ENP_CS2, Enable Programmable Chip Select 2

ENP_CS2 = 0 -
The Programmable Chip Select 2 is not enabled.

ENP_CS2 = 1 -
The Programmable Chip Select 2 is enabled.

Bit 13 - UMSK2, Upper Address Bits Mask 2

UMSK2 = 0 -
Bits A15:10 from the register at Port Address 6472H are ignored.

UMSK2 = 1 -
A15:10 from the register at Port Address 6472H are compared against CPU address Bits 15:10 when qualifying the Programmable Chip Select 2.

Bits 12:08 - 2LMSK4:0, Programmable CS2 Lower Address Bits MASK4:0

2LMSK4:0 bits allow individual qualification of the lower five address bits in the register at Port Address 6472H.

2LMSK4:0 = 0 -
The corresponding bit in the register at Port Address 6472H is ignored in the comparison. This allows address ranges of up to 32 bytes to be supported (2LMSK4:0 would all be zeroes), as well as unusual requirements such as odd addresses only.

2LMSK4:0 = 1 -
The corresponding bit in the register at Port Address 6472H is compared against that CPU address bit.

Bit 07 - PCS_3L, Programmable Chip Select 3 Location

PCS_3L = 0 -
The I/O device selected by Programmable Chip Select 3 is located on the expansion bus.

PCS_3L = 1 -
The I/O device selected by Programmable Chip Select 3 is located on the RA0:7/ED0:7 bus.

Bit 06 - ENPCS3, Enable Programmable Chip Select 3

ENPCS3 = 0 -
The Programmable Chip Select 3 is not enabled.

ENPCS3 = 1 -
The Programmable Chip Select 3 is enabled.

Bit 05 - UMSK3, Upper Address Bits Mask 3

UMSK3 = 0 -
Bits A15:10 are ignored.

UMSK3 = 1 -
A15:10 in the register at Port Address 6C72H are compared with CPU address bits 15:10 when selecting Programmable Chip Select 3.

Bits 04:00 - 3LMSK4:0, Programmable CS3 Lower Address Bits Mask

3LMSK4:0 allow individual qualification of the lower five address bits in the register at Port Address 6C72H.

3LMSK4:0 = 0 -
The corresponding bit in the register at Port Address 6C72H is ignored in the comparison. This allows address ranges of up to 32 bytes to be supported (3LMSK4:0 would all be zeroes), as well as unusual requirements such as odd addresses only.

3LMSK4:0 = 1 -
The corresponding bit in the register at Port Address 6C72H is compared with that CPU address bit.

9.5 PROGRAMMABLE CS2 ADDRESS REGISTER

Port Address 6472H - Read and Write

15	14	13	12	11	10	09	08
PC2 A15	PC2 A14	PC2 A13	PC2 A12	PC2 A11	PC2 A10	PC2 A9	PC2 A8

07	06	05	04	03	02	01	00
PC2 A7	PC2 A6	PC2 A5	PC2 A4	PC2 A3	PC2 A2	PC2 A1	PC2 A0

Signal Name	Default At RSTIN
All signals	0

Bits 15:00 - PC2A15:00, Programmable Chip Select 2 Address

PC2A15:00 determine the base address of the I/O device corresponding to Programmable Chip Select 2. The register at Port Address 5C72H provides the enable for Programmable Chip Select 2 and allows selective masking of some of the address bits.

9.6 PROGRAMMABLE CS3 ADDRESS REGISTER

Port Address 6C72H - Read and Write

15	14	13	12	11	10	09	08
PC3 A15	PC3 A14	PC3 A13	PC3 A12	PC3 A11	PC3 A10	PC3 A9	PC3 A8

07	06	05	04	03	02	01	00
PC3 A7	PC3 A6	PC3 A5	PC3 A4	PC3 A3	PC3 A2	PC3 A1	PC3 A0

Signal Name	Default At RSTIN
All signals	0

Bits 15:00 - PC3A15:00, Programmable Chip Select 3 Address

PC3A15:00 determine the base address of the I/O device corresponding to the third Programmable Chip Select. The register at Port Address 5C72H provides the enable for Programmable Chip Select 3 and allows selective masking of some of the address bits.

10.0 DIAGNOSTIC MODE

Two testing modes are provided for board testing. Three chip test modes are provided for chip testing.

I/O Pin Mapping Mode

The I/O Pin Mapping Mode provides the in-circuit tester for evaluating the connectivity of the WD8110/LV to the printed circuit board. Simultaneously asserting MASTER, MEMR, MEMW when A3 is low, A2 is high and RSTIN is asserted, causes the WD8110/LV to switch to I/O Mapping Mode. The WD8110/LV stays in this mode if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The WD8110/LV exits this mode when RSTIN is asserted while either MEMR, MEMW or MASTER is de-asserted, see Section 16.0.

Full Tristate Mode

Simultaneously asserting MASTER, MEMR and MEMW with A2 low and A3 high while RSTIN is asserted, causes all the output pins of the WD8110/LV to tristate and disables all the pullup and pulldown resistors. The WD8110/LV stays in this mode if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted with either MASTER, MEMR or MEMW de-asserted. This allows the tester to test for leakage current of the device.

Pullup and Pulldown Test Mode

Simultaneously asserting MASTER, MEMR, MEMW with A2 and A3 high while RSTIN is asserted, causes all the output pins of the WD8110/LV to become tristated and enables all the pullup and pulldown resistors. The WD8110/LV stays in this mode if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted while either MASTER, MEMR or MEMW is de-asserted. This allows the tester to test the pullup and pulldown resistors of the device.

VOH, VOL Test Mode

Simultaneously asserting MASTER, MEMR and MEMW with A2 and A3 low, and SMIRDY, EADS, and REFRESH high while RSTIN is asserted, causes all bidirectional pins to become outputs. The WD8110/LV stays in this mode if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted.

10.1 DIAGNOSTIC REGISTER

Port Address 9872H - Read and Write

15	14	13	12	11	10	09	08
CSC 1	0	IBM _2X	CLK_ TST	REF_ MAS	AUT_ 20	RSVD	CLK SW

07	06	05	04	03	02	01	00
LP	DS	DIAG					

Signal Name	Default At RSTIN
CSC(1:0)	00
IBM_2X	0
CLK_TST	0
REF_MAS	0
AUT_A20	0
Bit 09	None
CLK_SW	0
LP	None
DS	0
DIAG	0

Bits 15:14 - CSC(1:0), Core Strength Control

CSC 1	0	
0	0	Full strength 3V drivers
0	1	Medium strength 3V drivers
1	0	Illegal
1	1	Low strength 3V drivers

Bit 13 - IBM_2X,

IBM_2X = 0 -
IBM triple clock protocol is used for speed change.

IBM_2X = 1
IBM double clock protocol is used for speed change.

Bit 12 - CLK_TST, Clock Test

Diagnostics for factory use only.

Bit 11 - REF_MAS, Bus Master Refresh

Additional external logic may be required to support the bus master initiated refresh.

REF_MAS = 0 -
Does not support bus master initiated refresh.

REF_MAS = 1 -
Supports bus master initiated refresh.

Bit 10 - AUT_A20, Automatic Gate A20

Normally, the Alternate Gate A20 signal from Port 092H is OR'ed with the 8042 Gate A20.

When the AUT_A20 bit is set, the Alternate Gate A20 control bit automatically changes state to match the keyboard's Gate A20. Bit 1 (ALT_A20G) of Port 092H is set or reset according to the way 8042 is programmed. When the keyboard data port is read using the D1 keyboard controller command, the state of the Gate A20 status bit is replaced by that of AUT_A20.

The state of the A20 gating signal is available on PMC output 6 by reading Port 7072H (see Table 8-1).

AUT_A20 = 0 -
Normal Alternate Gate A20

AUT_A20 = 1 -
Automatic Gate A20

Bit 09 - Reserved

Bit 08 - CLK_SW, Clock Switch

The short clock switch reset pulse width is 1 µs plus 16 CPUCLKs. The 80486 processor requires a 1 ms clock switch. (See Section 4.2.3)

CLK_SW = 0 -
Short clock switch reset width.

CLK_SW = 1 -
1 ms clock switch reset width.

Bit 07 - LP, Low Power Mode

LP = 0 -
Low power features disabled.

LP = 1 -
Low power features enabled.

Bit 06 - DS, Diagnostic Signal

DS represents the state of the diagnostic signal selected by DIAG.

Bits 05:00 - DIAG, Diagnostic Function/Speaker Disable

DIAG selects the diagnostic function to be performed. The DS bit represents the state of the signal selected.

DIAG = 000000 - Diagnostic output disabled, speaker normal.

DIAG = 000001 - Diagnostic output disabled, speaker disabled. This is a method of disabling the speaker without hardware gates.

DIAG = 000010:111111 - Reserved

10.2 DELAY LINE DIAGNOSTIC REGISTER

Port Address A072H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
LAT	DL	DELAY					

Signal Name	Default At RSTIN
Bits 15:08	None
LAT	0
DL	0
DELAY	None

Bit 07 - LAT, Latch Output Strength

The delay line count value (bits 05:00) is used to control the output buffer strength

The output buffer strength is normally adjusted every time the delay count changes. LAT may be used to lock the buffer strength at its present value.

LAT = 0 -
The output buffer strength is adjusted when the delay count changes.

LAT = 1 -
The output buffer strength is locked at its present value.

Bit 06 - DL, Delay Freeze

The internal self tuning delay line normally is updated by one delay element during every refresh cycle. For test purposes, the delay may be forced to stop generating calibration cycles. When delay line updates are frozen, the tester may write different delay line counter values in bits 05:00.

DL = 0 -
Normal delay line operation

DL = 1 -
Freeze delay line

Bits 05:00 - DELAY, Delay Counter Value

The delay line counter value is used to control the output buffer strength.

This register may be written to when DL (bit 06) is set to one.

10.3 TEST ENABLE REGISTER

Port Address A872H - Bits 15:10 Read only
Bits 09:00 Read and Write

The test function bits 07:05 are for factory use only.

15	14	13	12	11	10	09	08
Version				Reserved		IRQ9_EN	TDL

07	06	05	04	03	02	01	00
OLD_HLDA	BFC 3	BIST 3	DRAM_DRV		EN_PLD	RSVD	EN_LVL

Signal Name	Default At RSTIN
15, 14, 11:00	0
13, 12	1

Bits 15:12 - VERSION NUMBER

0000 - Version A
0001 - Version B
0011 - Version C

Bits 11:10 - Reserved

Bit 09 - IRQ9EN, IRQ9 Enable

IRQ9EN is used to mask IRR9 and ISR9 so that the System Activity Monitor does not detect these signals. This prevents vertical retrace from being a source of activity for SAM.

IRQ9EN = 0 -
Masking of IRR9 and ISR9 enabled

IRQ9EN = 1
Masking disabled

Bit 08 - TDL, Test Delay Line.

Bit 07 - OLD_HLDA,

Test bit for factory use only. Must be set to 0.

Bit 06 - BFC3,

DMA Register file test bit, for factory use only. Must be set to 0.

Bit 05 - BIST3,

DMA Register file test bit, for factory use only. Must be set to 0.

Bits 04:03 - DRAM_DRV, DRAM Driver Strength

The DRAM address driver strength may be adjusted for capacitive load. When adjusted properly, output overshoot and undershoot is minimized while still meeting worst case DRAM timing. The DRAM RAS, CAS and address buffers also automatically compensate for variations in temperature, voltage and manufacturing process.

DRAM_DRV
04 03
0 0- Full strength DRAM address drive, up to 450 pF.
0 1- Low strength DRAM address drive, up to 100 pF.
1 0- Medium strength DRAM address drive, up to 180 pF.
1 1- High strength DRAM address drive, up to 260 pF.

Bit 02 - EN_PLD, Enable Pulldown

EN_PLD = 0 -
Pulldown resistors are not enabled.

EN_PLD = 1 -
40K to 100K internal pulldown resistors will be enabled during processor power down or full power down on processor address lines A23:00, and on processor data lines D15:00.

Bit 01 - RSVD, Reserved

Bit 00 - EN_LVL, Enable Level

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability. See Section 5.5.2.1.

EN_LVL = 0 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is not supported. L_T (bit 3) at Port 020H has no effect.

EN_LVL = 1 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is supported. L_T (BIT 3) at Port 020H now controls the selection of edge-sensed or level-sensed interrupts.

10.4 TEST STATUS REGISTER

Port Address DC72H - Read only
For factory use only.

15	14	13	12	11	10	09	08
Delay Line Status CAL		MED SLOW	DLT6	DLT5	DLT4	DLT3	DLT2

07	06	05	04	03	02	01	00
DLT1	DLR0	BF34	BF33	BF32	BF31	BF30	BC

Signal Name	Default At RSTIN
All signals	None

Bit 15 - CAL, Calibration

CAL = 0 -
Internal delay line has not completed initial calibration.

CAL = 1 -
Internal delay line has completed initial calibration.

Bits 14:13 - MED, SLOW, Medium and Slow

These bits provide information regarding the output buffer strength.

MED	SLOW	
0	0	Output buffers are set to low strength (fast WD8110/LV).
0	1	Invalid
1	0	Output buffers are set to medium strength (medium speed WD8110/LV).
1	1	Output buffers are set to full strength (slow WD8110/LV).

Bits 12:06 - DLT6:DLT0,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD8110/LV.

Bits 05:01 - BF34:BF30,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD8110/LV.

Bit 00 - BC

This bit provides information about internal nodes and is for test purposes only. Its state is dependent upon the test mode selected and the speed of the WD8110/LV.

11.0 MISCELLANEOUS REGISTERS

This section describes the two General Purpose registers and two Scratch Pad registers.

11.1 GENERAL PURPOSE I/O EXPANSION REGISTERS

In systems using a CPU with a built in numeric processor, or where real estate constraints are limited, support for a numeric processor by the WD8110 is not required. For these systems, the WD8110 provides the addition of up to 16 extra general purpose inputs and outputs on the system board by multiplexing the strobes GPREGWR with NPBUSY and GPREGRD with EXBUSY on pins 94 and 206.

GPREGWR and GPREGRD are similar to the AT Bus write and read strobes qualified by a programmable I/O location. Transfers using GPREGWR or GPREGRD are 16-bits wide and use 16-bit timing. GPREGRD should be connected directly to the enable input of one or two 74X244 type devices, making it possible to read status from the AT Bus SD15:0. GPREGWR should be connected directly to the clock input of one or two 74X374 type devices so that control bits can be clocked in from the AT Bus SD15:0.

To support hibernation, the last value written using GPREGWR is shadowed in the register at Port Address 3872H.

11.1.1 General Purpose I/O Control Register

Port Address 9472H - Read and Write

This register provides the four byte address range where the General Purpose Register will reside, as well as two control bits for enabling the General Purpose register and pullup resistors for GPREGWR and GPREGRD.

15	14	13	12	11	10	09	08
General Purpose Register Address							
GPR_ A15	GPR_ A14	GPR_ A13	GPR_ A12	GPR_ A11	GPR_ A10	GPR_ A9	GPR_ A8

07	06	05	04	03	02	01	00
General Purpose Register Address							
GPR_ A7	GPR_ A6	GPR_ A5	GPR_ A4	GPR_ A3	GPR_ A2	GPR_ EN	GPR_ PUR

Signal Name	Default At RSTIN
All signals	0

Bits 15:02 - GPR_A(15:2), General Purpose Register I/O Address

These bits provide the four byte address range where GPREGWR and GPREGRD will go active.

Bit 01 - GPR_EN, General Purpose Register Enable

GPR_EN = 0 -
GPREGWR and GPREGRD will not be asserted.

GPR_EN = 1 -
GPREGWR and GPREGRD will be asserted for I/O cycles where the I/O address matches that programmed in GPR_A(15:2).

Bit 00 - GPR_PUR, General Purpose Register Pullup Resistor

GPR_PUR = 0 -
A high value pullup resistor is enabled on pins 94 and 206 for GPREGWR and GPREGRD.

GPR_PUR = 1 -
The high value pullup resistors are not enabled on pins 94 and 206 for GPREGWR and GPREGRD.

11.1.2 General Purpose I/O Write Shadow Register

Port Address 3872H - Read only

This register is used to support hibernation. The last data written to external latches by GPREGWR is written to this register also. This data can be read back to assist in restoring the state of the system before hibernation.

15	14	13	12	11	10	09	08
General Purpose Register Write Data Shadow							
GPW D15	GPW D14	GPW D13	GPW D12	GPW D11	GPW D10	GPW D9	GPW D8

07	06	05	04	03	02	01	00
General Purpose Register Write Data Shadow							
GPW D7	GPW D6	GPW D55	GPW D4	GPW D3	GPW D2	GPW D1	GPW D0

Signal Name	Default At RSTIN
All signals	0

Bits 15:00 - GPW_D(15:0), General Purpose Register Write Data Shadow

The last data written to external latches by GPREGWR.

11.2 SCRATCH PAD REGISTERS

The two Scratch Pad Registers provide a means of communicating status or requests between software routines. The primary intent is for communication between the SMI handler code and the routine that invokes it. The registers perform no function other than to hold the last value written to them.

Port Address C472H - Read and Write

15	14	13	12	11	10	09	08
Scratch Pad A							
SPA_ 15	SPA_ 14	SPA_ 13	SPA_ 12	SPA_ 11	SPA_ 10	SPA_ 09	SPA_ 08

07	06	05	04	03	02	01	00
Scratch Pad A							
SPA_ 07	SPA_ 06	SPA_ 05	SPA_ 04	SPA_ 03	SPA_ 02	SPA_ 01	SPA_ 00

Signal Name	Default At RSTIN
All signals	0

Bits 15:00 - SPA(15:00), Scratch Pad A (15:00)

These bits contain the last value written to them. They perform no other function.

Port Address CC72H - Read and Write

15	14	13	12	11	10	09	08
Scratch Pad B							
SPB 15	SPB_ 14	SPB_ 13	SPB_ 12	SPB_ 11	SPB_ 10	SPB_ 09	SPB_ 08

07	06	05	04	03	02	01	00
Scratch Pad B							
SPB_ 07	SPB_ 06	SPB_ 05	SPB_ 04	SPB_ 03	SPB_ 02	SPB_ 01	SPB_ 00

Signal Name	Default At RSTIN
All signals	0

Bits 15:00 - SPB(15:00), Scratch Pad B (15:00)

These bits contain the last value written to them. They perform no other function.

12.0 VIRUS PROTECTION

This section provides only an overview of the benefits of Western Digital's Immunizer feature and is not intended to describe complete control of the virus protection offered by the Immunizer.

12.1 INTRODUCTION

Intel introduced the concept of System Management Mode (SMM) and it is now offered by their latest processors as well as AMD and Cyrix. SMM is designed to aid the design of Power Managed Laptop Systems. A System Management Interrupt (SMI) causes the complete state of the processor to be saved in a reserved area of memory called SMM-RAM. The processor can then be powered off to save power and, upon receipt of a wakeup command, the complete state of the processor is restored and the system resumes operation where it left off. The SMM-RAM is allocated out of main memory and is inaccessible to application programs. When an SMI occurs, the SMM-RAM is mapped into some range of Real Mode address space and the system begins executing out of SMM-RAM. Typical sources of SMI interrupts are the System Activity Monitors (SAM) offered by Western Digital's line of laptop System Controllers, WD76C10A, WD7855, and for 32 bit systems, the WD8110/LV.

IO Trapping - IO Trapping is a feature of Western Digital System Controllers that allows peripherals to remain in the powered down state until they are called into use. When an IO is accessed, the System Controller catches the IO address and data, powers up the device to be accessed and completes the IO cycle. The WD8110/LV has three programmable Chip Selects which use the IO Trapping feature, as well as dedicated I/O traps for the ATA/IDE hard drive interface for virus protection.

ATA/IDE Hard Disk Interface - This specification defines the IO instructions for data transfers between the hard disk and the System Controller. The Command Port is at 1F7H. The write commands are: 30H, Write Sector; C5H, Write Multiple; and E8H, Write Buffer.

12.2 BENEFITS OF THE IMMUNIZER

Immunizer can detect and protect against unknown viruses and Trojan Horse attacks. Scanners can only find known viruses that have already attacked other systems. Unlike Terminate and Stay Resident (TSR) type solutions, Immunizer does not require any resident memory. Some products are being marketed that operate similar to Immunizer but reside in conventional memory and therefore reduce system resources. SMM-RAM is located at the very top of Extended Memory and requires only 64K of memory so that a system with 8M of memory is virtually unimpacted. Also, these TSR solutions are easily defeated and can be removed or disabled without the users knowledge.

There is no performance degradation. Immunizer determines protection violations in parallel with the disk seek operations and no real time is required to detect virus attacks. Immunizer does not require any additional hardware. Some disk controller cards are being marketed that are similar to the Immunizer, but these solutions require the user to purchase additional hardware and dedicates a card slot to this new controller.

12.3 USING IMMUNIZER

When Immunizer is enabled it is completely transparent until the system performs an IO write to the Integrated Drive Electronics (IDE) disk. IDE disk writes are detected by the IO Trapping facility of the WD8110 System Controller. The following commands to the IDE Control Port, IF7H causes an SMI to occur; 30:33H, 3CH, 50H, C5:C6H, CA:CBH, C7H and CD:CFH.

Once the SMI Interrupt has occurred, the CPU switches to the SMM Mode. The Immunizer code, located in SMM-RAM, compares the contents of locations 1F4H (cylinder low), 1F3H (sector number) and 1F2H (sector count) with Protected File Bit Map. If the contents of IDE Registers indicate that the current write command will cause data in one of the protected clusters to be altered, an Immunizer Alert is issued.

13.0 DC ELECTRICAL SPECIFICATIONS

This section provides the DC Operating Characteristics for the WD8110/LV. The parameters for the WD8110LV at 3.3 volts are marked with an *.

13.1 MAXIMUM RATINGS

Supply Voltage (V_{DD}) with respect to Vss (ground) . . . . . V_{DD} - Vss ≤ 7.0 Volts
Voltage on any pin with respect to Vss (ground) . . . . . Vss -0.3 Volts to V_{DD} +0.3 Volts
Operating Temperature . . . . . 0°C (32°F) to 70°C (158°F)
Storage Temperature . . . . . -40°C (-40°F) to 125°C (257°F)
Power Dissipation . . . . . 600 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

13.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)
V_{DD}AT = +5V ±.25V (5%) for WD8110
V_{DD} = +5V ±.25V (5%)
V_{DD} = 3.3V ±..3V for WD8110LV

Values marked with an * are for 3.3 volt operations.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Leakage		± 10	µA	Vin = .4 to V_{DD}
IOZ	Tristate and Open Drain Output Leakage		± 10	mA	Vout = .4 to V_{DD}
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		.8	V	
VIH	$\overline{RSTIN}$ Input High Voltage	V_{DD} -0.5 -0.3*		V	
VIL	$\overline{RSTIN}$ Input Low Voltage		0.5 0.3*	V	
ICC	Supply Current		200	mA	Inputs at 2.0V
			140	mA	Inputs at 5.0V Outputs Open, CPUCLK = 25 MHz
			240	mA	Inputs at 2.0V
			180	mA	Inputs at 5.0V Outputs Open, CPUCLK = 33 MHz
ICCAT	Supply Current		12	mA	Inputs at 2.0V
			8	mA	Inputs at 5.0V
ICCSB	Typical Supply Current, Power Down Mode for WD8110/LV	.5		mA	Typical, CPUCLK Off, CLK14 = 32 KHz

TABLE 13-1. DC OPERATING CHARACTERISTICS

FOR PINS WITH INTERNAL PULLUPS:

MASTER, IOCK, IOCS16, MEMCS16, ZEROWS, IOCHRDY, PDREF

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-39 -13*	-130 -52*	µA	Not suspend and resume mode

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

M/IO, NPERR, NPBUSY, NPRST, CPURES, ADS, D/C, W/R

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-39 -13*	-130 -52*	µA	Not processor power down or suspend mode

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

IOCHRDY, ZEROWS, IOCS16, MEMCS16, MASTER, PDREF, REFRESH, SBHE, IOR, IOW, MEMR, MEMW

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-39 -13*	-130 -52*	µA	Not suspend mode

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

FOR PINS WITH INTERNAL PULLDOWNS:

A31, A29, A(27:2), D(31:0)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pulldown Current	-39 -13*	-130 -52*	µA	Processor power down or suspend mode

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

FOR OUTPUTS:

DACKEN, D(15:00), READY, CPURES, HOLDR, INTRQ, A(23:00), NMI, RAS(4:0), CAS(3:0), W/R, CSEN, LOWMEG, A20GATE, KEN, FLUSH, SMI,

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	V_{DD} -.8		V	IOUT = -100 µA
VOH	Output High Voltage	2.4		V	IOUT = -2 mA / -1mA*
VOL	Output Low Voltage		.4	V	IOUT = 2 mA / 1.5 mA*

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

FOR OUTPUTS:

MXCTL2:0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	V_{DD} -.8		V	IOUT = -100 µA
VOH	Output High Voltage	2.4		V	IOUT = -3 mA / -2 mA*
VOL	Output Low Voltage		.4	V	IOUT = 3 mA / -2 mA*

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

FOR OUTPUTS:

$\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, AEN, SYSCLK, BALE, LA20, SA0, SA1, $\overline{SBHE}$

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA / -2 mA*
VOL	Output Low Voltage		.5	V	IOUT = 24 mA / -12 mA*

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

FOR OUTPUTS:

SD(15:0)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA / -2 mA*
VOL	Output Low Voltage		.5	V	IOUT = 17 mA / -12 mA*

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

FOR OUTPUTS:

$\overline{REFRESH}$, IOCHRDY

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

FOR OUTPUTS:

RA(11:4), RA3A, RA3B, RA(2:0)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -35 mA / -14 mA*
VOL	Output Low Voltage		0.5	V	IOUT = 35 mA / 27 mA*

TABLE 13-1. DC OPERATING CHARACTERISTICS (Continued)

14.0 AC OPERATING CHARACTERISTICS

This section provides the AC Operating Characteristics for the WD8110/LV. The AC Operating Characteristics are divided into three major categories: Memory Timing (Section 14.1), AT Bus Timing (Section 14.2) and Processor Timing (Section 14.3).

Table 14-1 lists the timing tables and figures, and their section location.

TABLE NUMBER	FIGURE NUMBER	TITLE	SECTION
14-3		5 Volt WD8110/LV Timing	14.1
	14-1 ↕ 14-6	33 MHz, 3-2-2-2 DRAM Read Cycle Static Column Mode, 3-1-1-1 DRAM Read Cycle	
	14-7 ↕ 14-16	Page Mis, DRAM Write Cycle Static Column Mode, 4-2-2-2 Page Hit Cycle	
14-4		CPU Initiated AT Bus Cycles	14.2.1
	14-17 ↕ 14-26	AT Bus I/O or Memory Read: 8-Bit, Default Timing AT Bus I/O or Memory Write: 16-Bit, Default Timing	
14-5		DMA Cycles	14.2.2
	14-27 14-28 14-29	Basic DMA Cycle, Default Timig DMA Cycle, 8-Bit I/O to On-board Memory DMA Cycle, On-board Memory to 8-Bit I/O	
14-6		AT Bus Master Cycle	14.2.3
	14-30 14-31 14-32	AT Bus Master, Bus Acquisition/Release AT Bus Master, Write to On-board Memory AT Bus Master, Read from On-board Memory	
14-7		AT Bus Refresh Cycle, Default Timing	14.2.4
	14-33 14-34 14-35	AT Bus Refresh Cycle, Default Timing Multiple Bus Master Write Cycle, Cache Invalidation Multiple Bus Master Read Cycles, Interleave On	
14-8		80386SX CPU Timing	14.3
	14-36 ↕ 14-40	CPURES And NPRST During Power Up - 2X CPU Mode Latching $\overline{\text{BUSYCPU}}$ When An Error Occurs And Clearing It With A Write To Port F0	
14-9		WD8110/LV SMI Timing	14.3
	14-41	I/O Trap Cycle With 386DXLV	

TABLE 14-1. TIMING FIGURE/TABLE NUMBERS

SIGNAL	LOAD	SIGNAL	LOAD	SIGNAL	LOAD
SMI	50 pF	REFRESH	200 pF	SMIRDY	50 pF
KEN	50 pF	A20GATE	50 pF	MDEN	50 pF
CPURES	50 pF	NPRST	50 pF	MDIR	50 pF
W/R	50 pF	NMI	50 pF	DRMWR	400 pF
MXCTL(2:0)	50 pF	DACKEN	50 pF	CSEN	50 pF
LOWMEG	50 pF	SPKR	50 pF	READY486	50 pF
HOLDR	50 pF	INTRQ	50 pF	BRDY486	50 pF
BUSYCPU	50 pF	EPEREQ	50 pF	BS16	50 pF
CPUCLK	70 pF	SYSCLK	75 pF	ROMBA(18:16)	50 pF
SD(15:0)	200 pF	D(15:00)	100 pF	IOW	200 pF
LBCLK	50 pF	MEMW	200 pF	IOR	200 pF
LA20	200 pF	MEMR	200 pF	AEN	200 pF
BALE	200 pF	SA0, SA1	200 pF	RA(11:00)	450 pF
RAS(4:0)	150 pF	SBHE	200 pF	EADS	50 pF
CAS0(3:0)	200 pF	A31, A29	100 pF		
CAS1(3:0)	200 pF	A(27:2)	100 pF		

TABLE 14-2. SIGNAL LOADING

14.1 MEMORY TIMING

This section provides the WD8110/LV 5 volt and 3.3 volt timing parameters.

SYMBOL	CHARACTERISTIC	MAX 25 MHz	MAX 33 MHz
T200	CPU Address A(31:2) to DRAM Address RA(11:0)		
	@ 450 pF	33 ns	28 ns
	@ 350 pF	30 ns	25 ns
	@ 180 pF	26 ns	21 ns
T201	CPUCLK edge to CAS falling edge		
	@ 75 pF	22 ns	17 ns
	@150 pF	24 ns	19 ns
	@ 200 pF	25 ns	20 ns
T202	CPUCLK rising edge to Cas rising edge		
	@ 75 pF	23 ns	18 ns
	@ 150 pF	25 ns	20 ns
	@ 200 pF	26 ns	21 ns
T203	CPU Data D31:1 to Parity		
	Data DP3:0 valid for 386 mode only	25 ns	20 ns
T204	CPUCLK rising edge to RA3A, RA3B RAM address		
	@ 260 pF	33 ns	28 ns
	@ 108 pF	29 ns	24 ns
	@ 100 pF	27 ns	22 ns
T205	CPUCLK rising edge to RAS(4:0) falling edge		
	@ 150 pF	22 ns	18 ns
	@ 75 pF	20 ns	16 ns
T206	CPUCLK rising edge to $\overline{\text{DRMWR}}$ falling edge		
	@ 450 pF	29 ns	25 ns
	@ 350 pF	27 ns	23 ns
T207	CPUCLK rising edge to BRDY486 valid delay	23 ns	18 ns
T208	CPUCLK rising edge to RDY486 valid time	23 ns	18 ns

TABLE 14-3. 5 VOLT AND 3.3 VOLT WD8110/LV TIMING

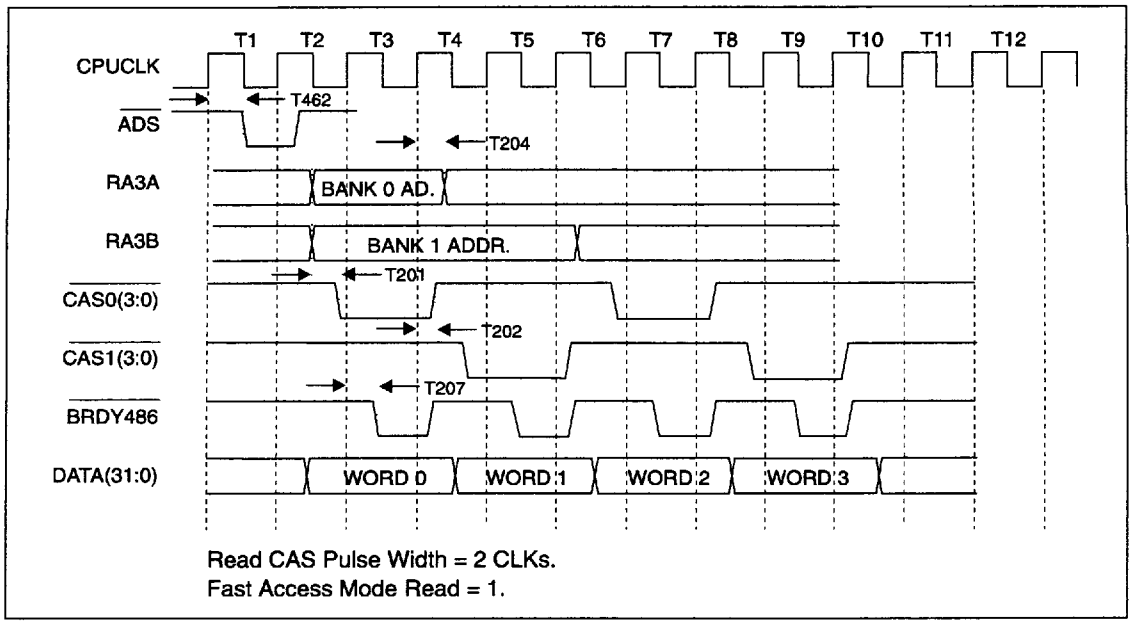


FIGURE 14-1. 33 MHz, 3-2-2-2 DRAM READ CYCLE - INTERLEAVED

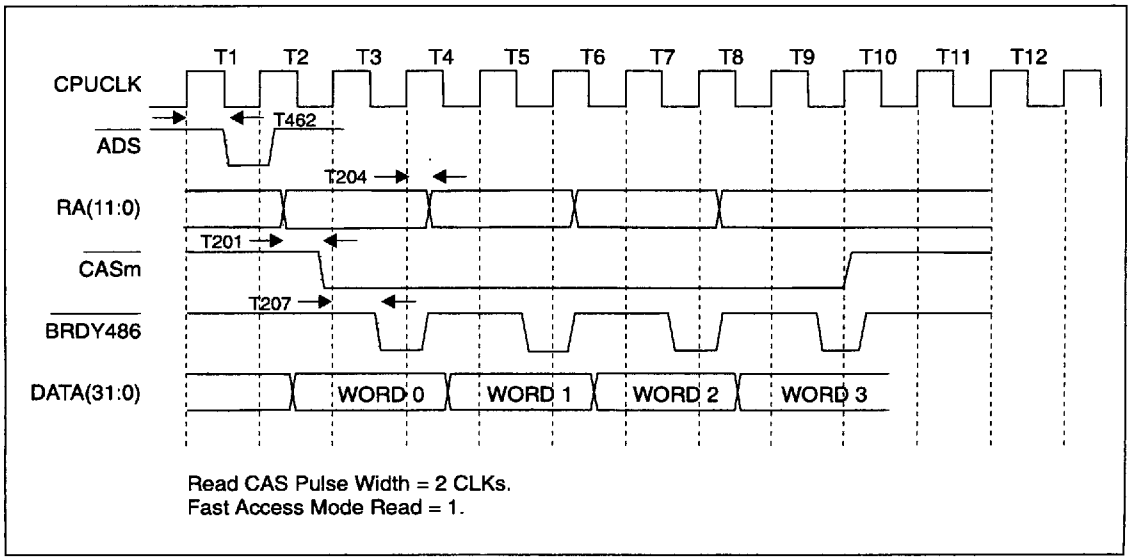


FIGURE 14-2. STATIC COLUMN MODE, 3-2-2-2 DRAM READ CYCLE

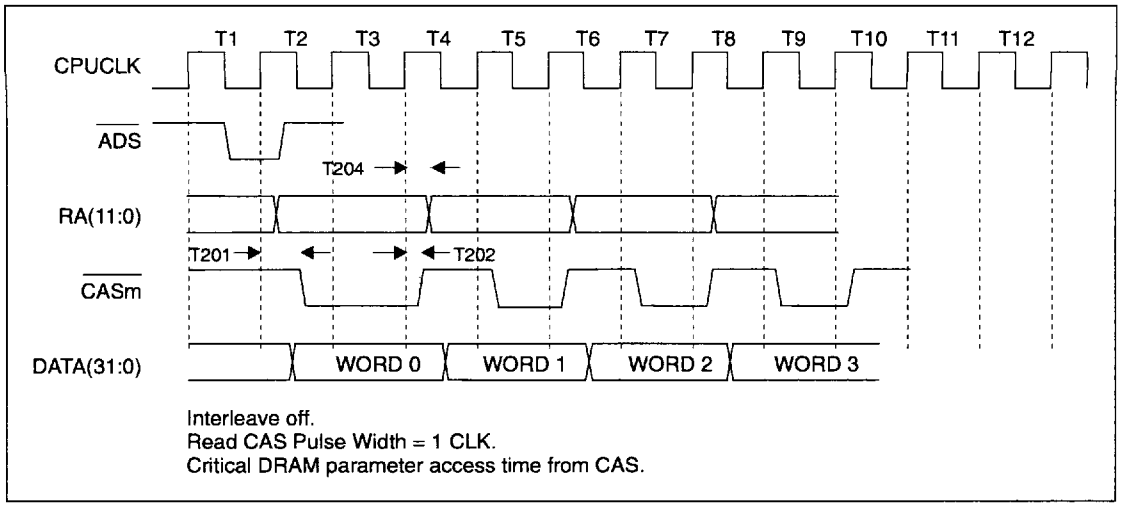


FIGURE 14-3. PAGE MODE, 3-2-2-2 DRAM READ CYCLE - NON-INTERLEAVED

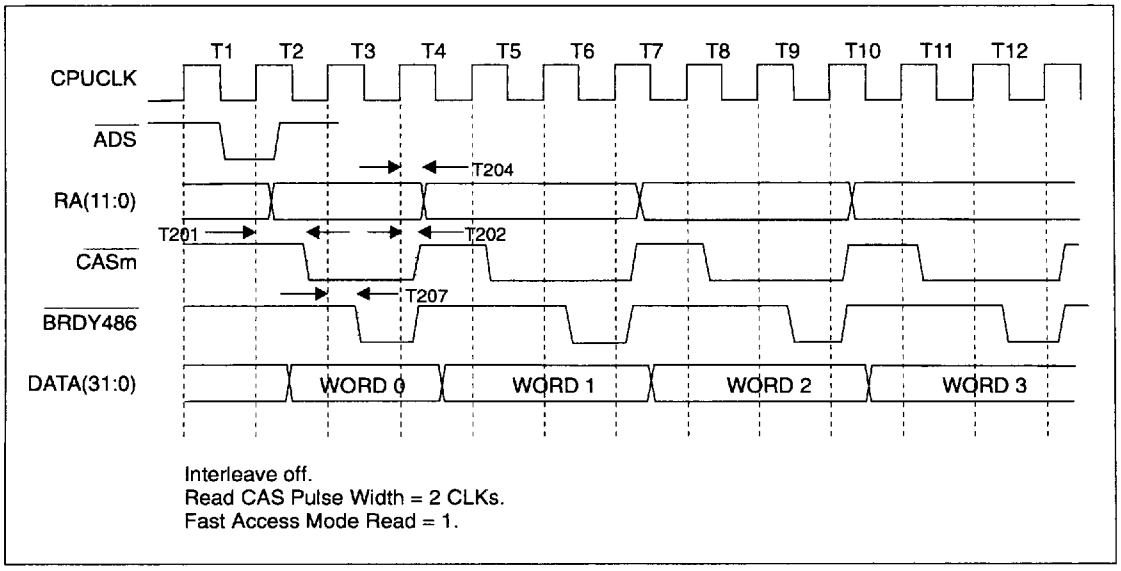


FIGURE 14-4. PAGE MODE, 3-3-3-3 DRAM READ CYCLE - NON-INTERLEAVED

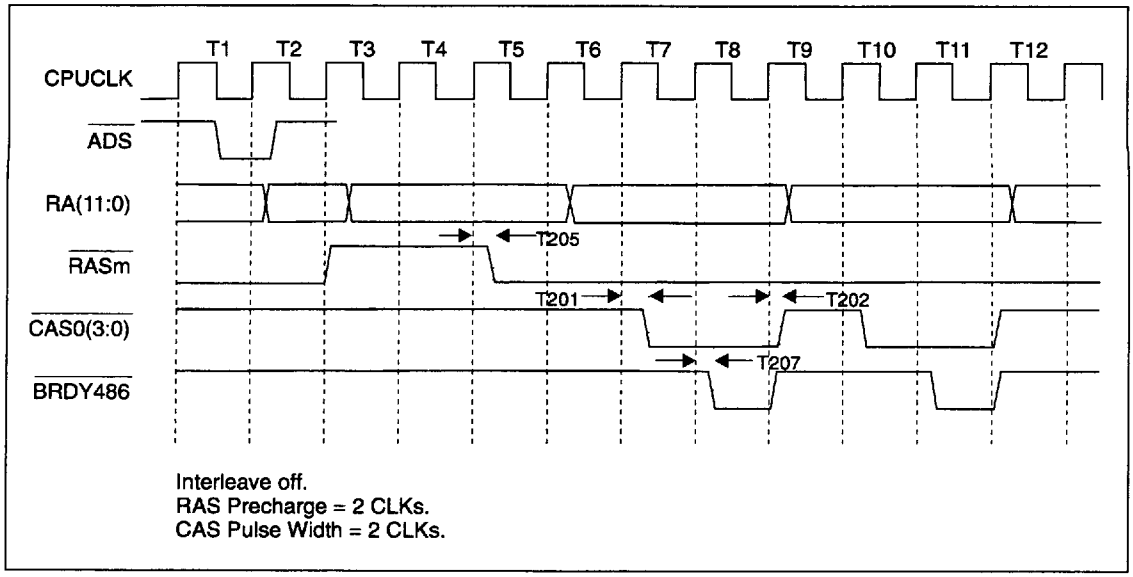


FIGURE 14-5. PAGE MISS, 8-3-3-3 DRAM READ CYCLE

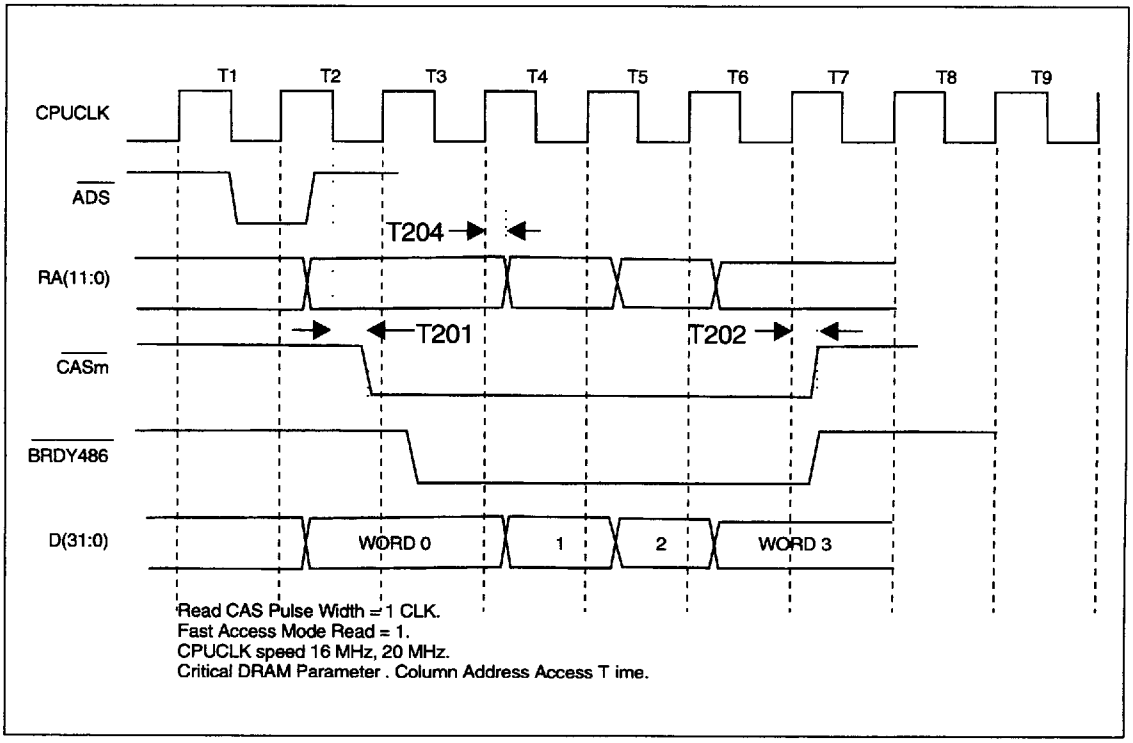


FIGURE 14-6. STATIC COLUMN MODE, 3-1-1-1 DRAM READ CYCLE

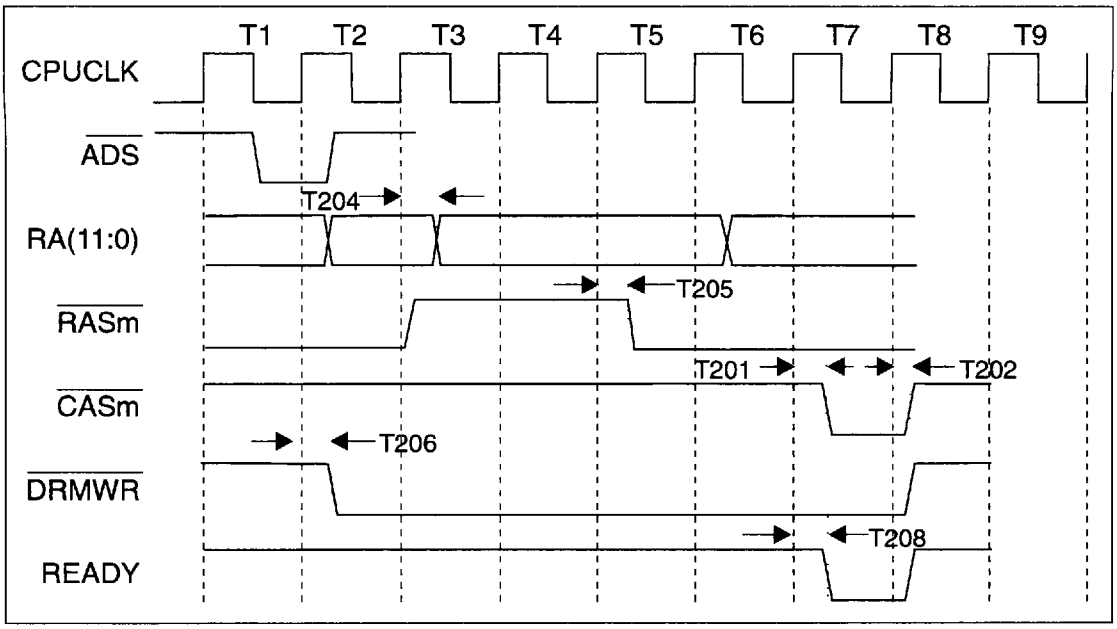


FIGURE 14-7. PAGE MISS, DRAM WRITE CYCLE

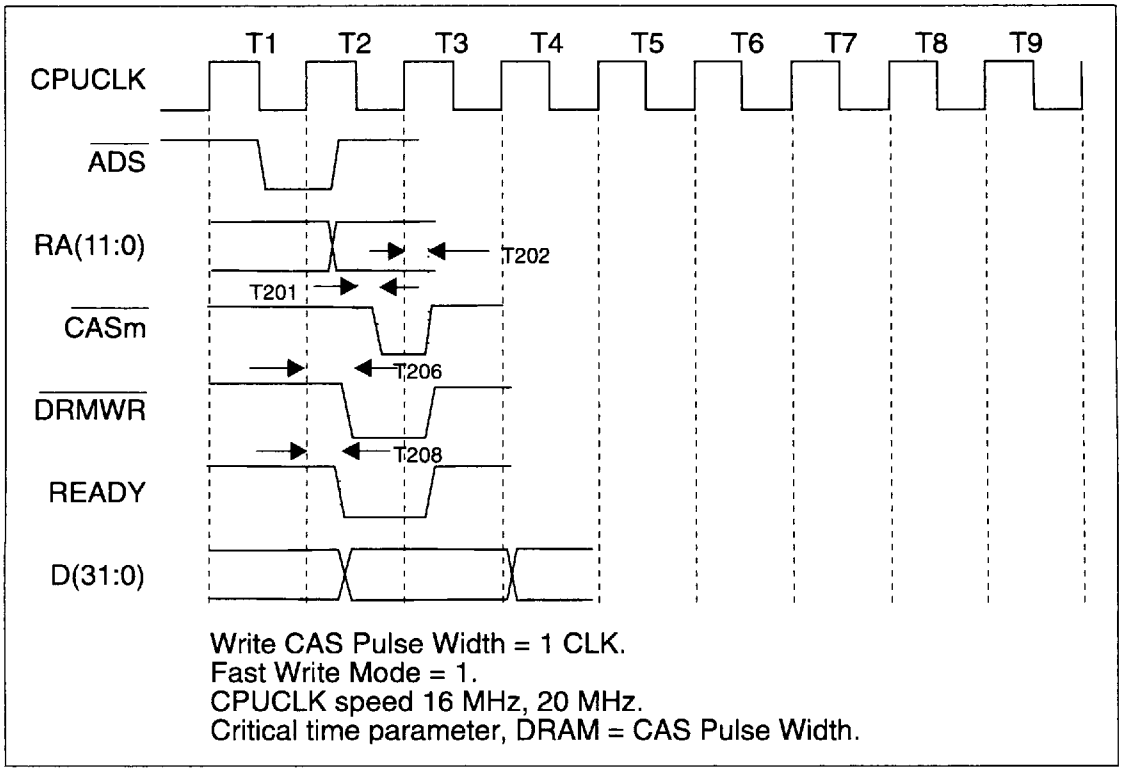


FIGURE 14-8. PAGE HIT, DRAM WRITE CYCLE, 0 WAIT STATE

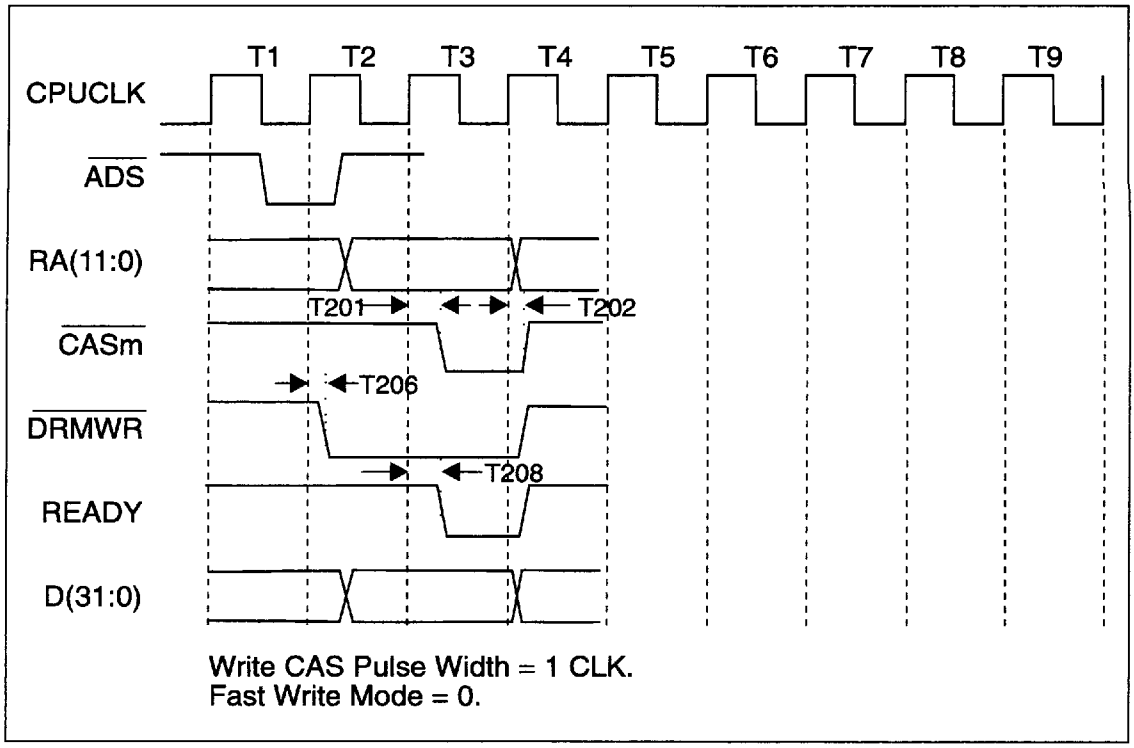


FIGURE 14-9. PAGE HIT, DRAM WRITE CYCLE, 1 WAIT STATE

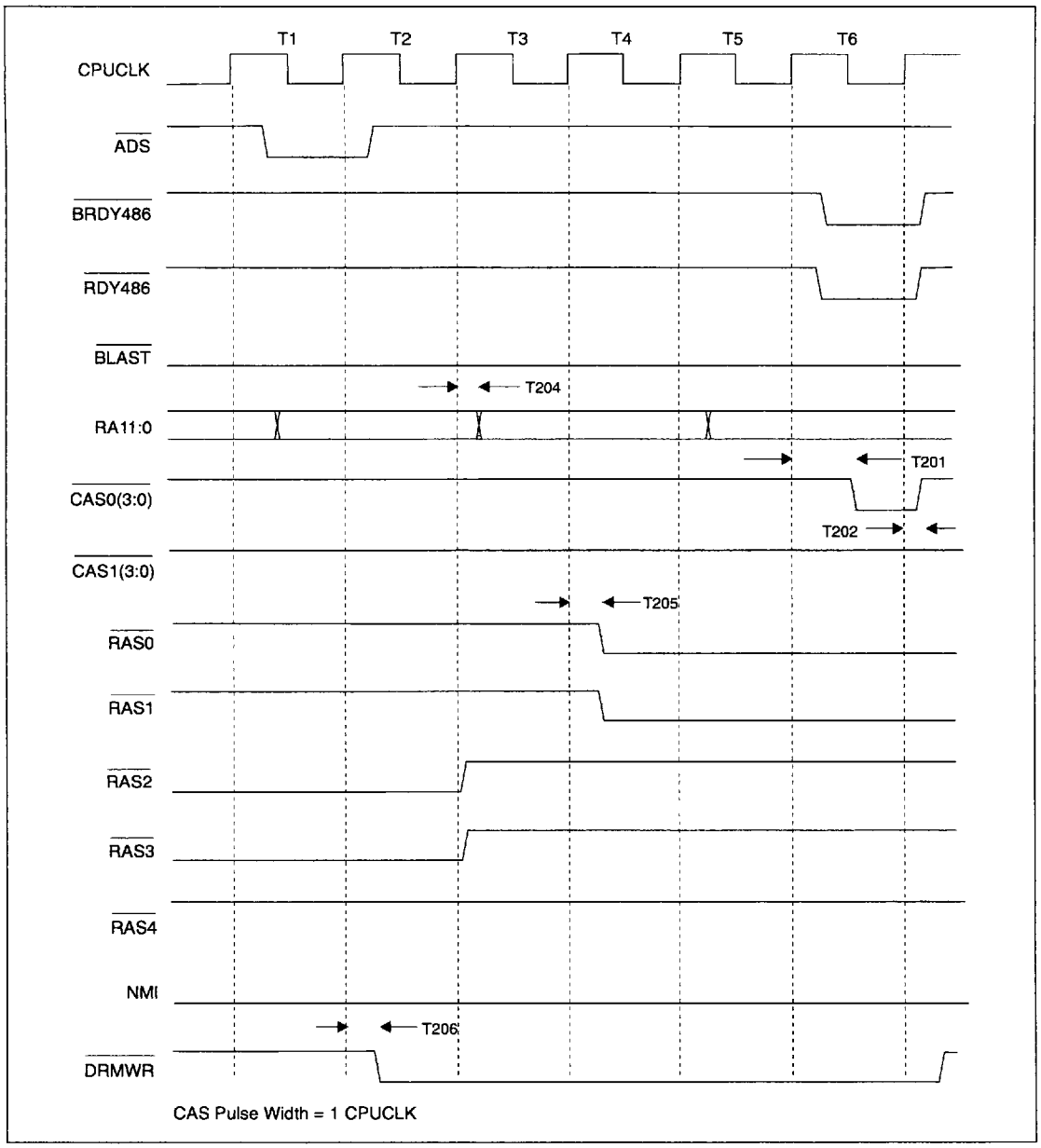


FIGURE 14-10. PAGE MISS, BANK MISS, DRAM WRITE CYCLE 6 CLOCKS

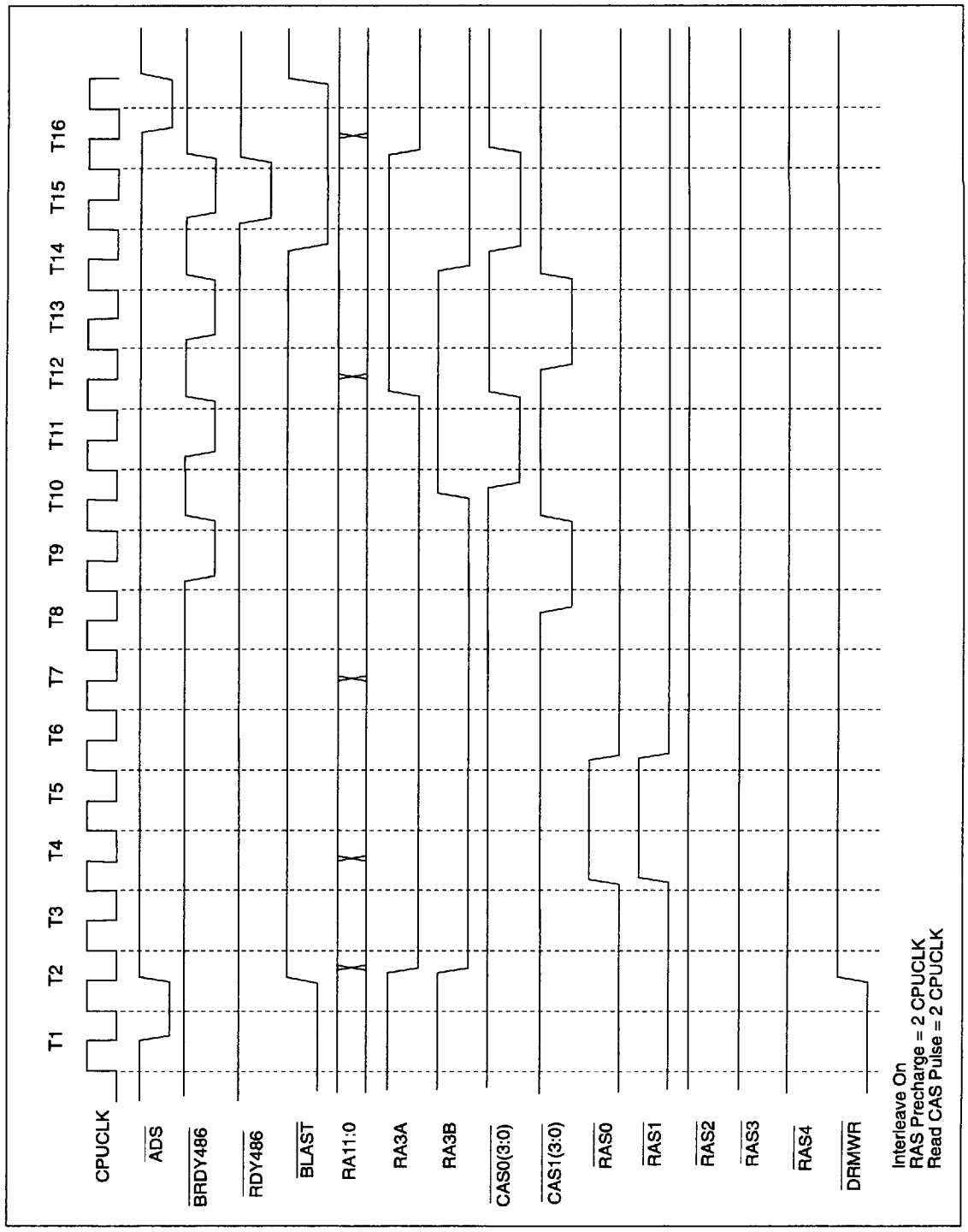


FIGURE 14-11. PAGE MISS, 8-2-2-2 DRAM READ CYCLE

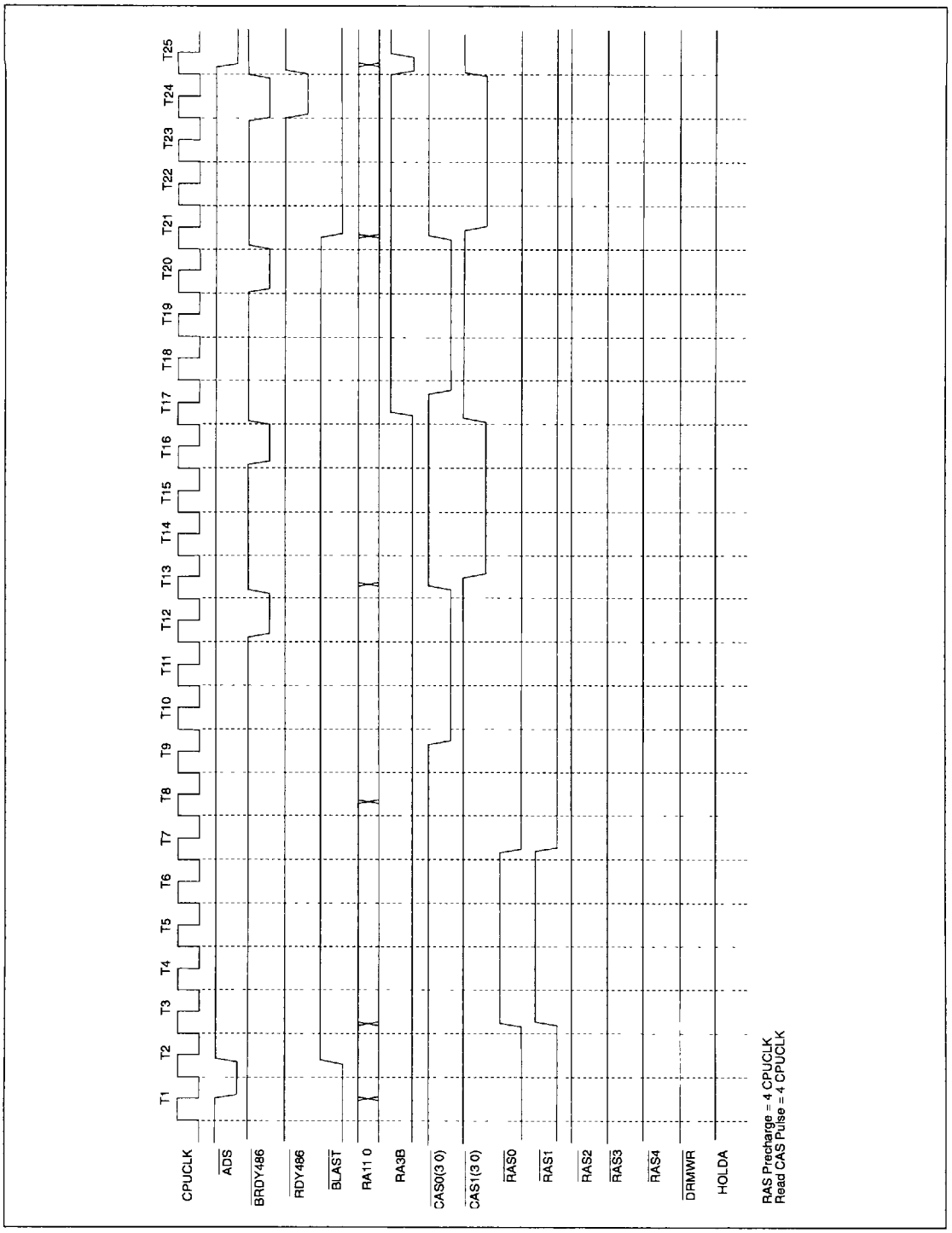


FIGURE 14-12. PAGE MISS, 12-4-4-4 DRAM READ CYCLE

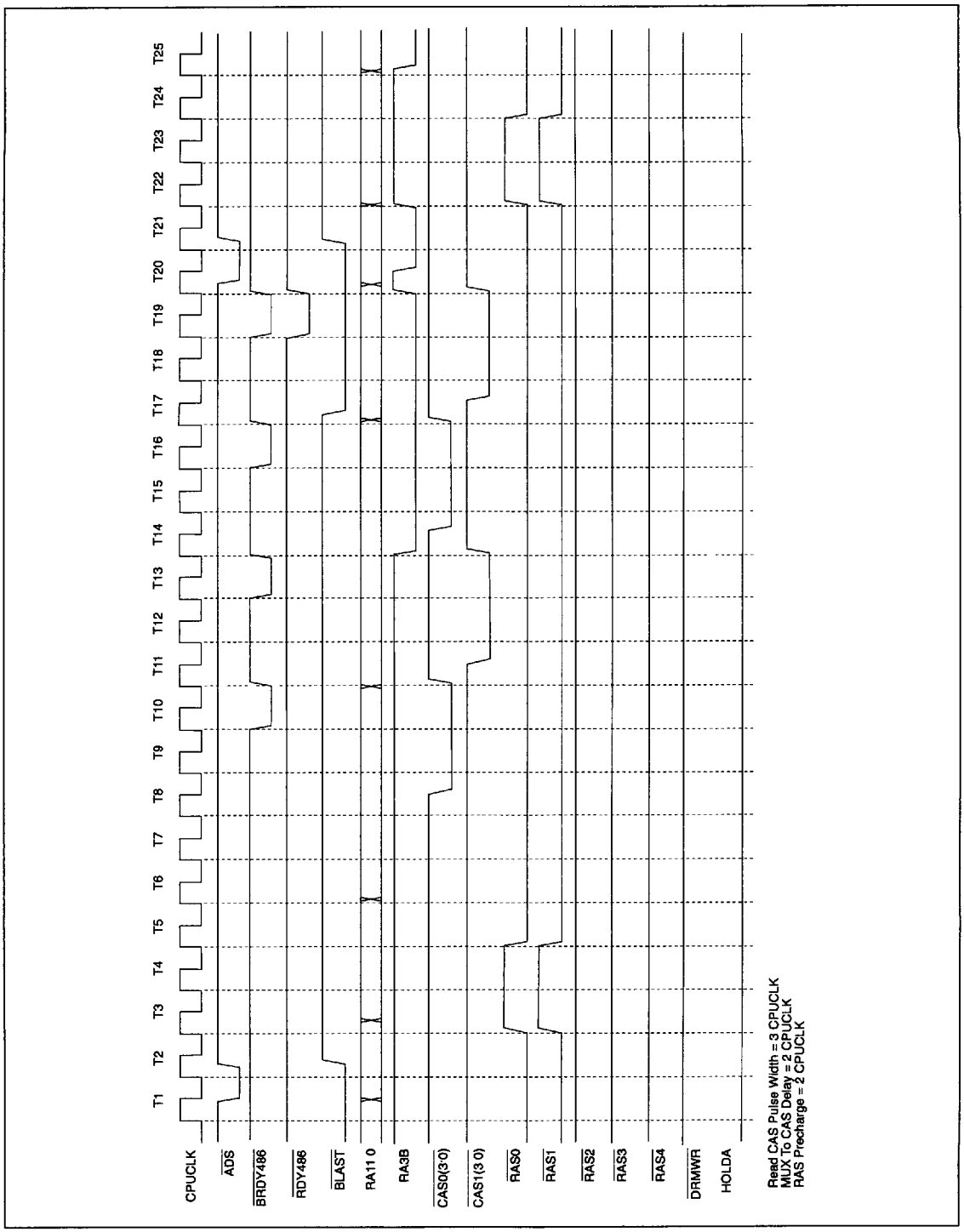


FIGURE 14-13. PAGE MISS, 10-3-3-3 DRAM READ CYCLE

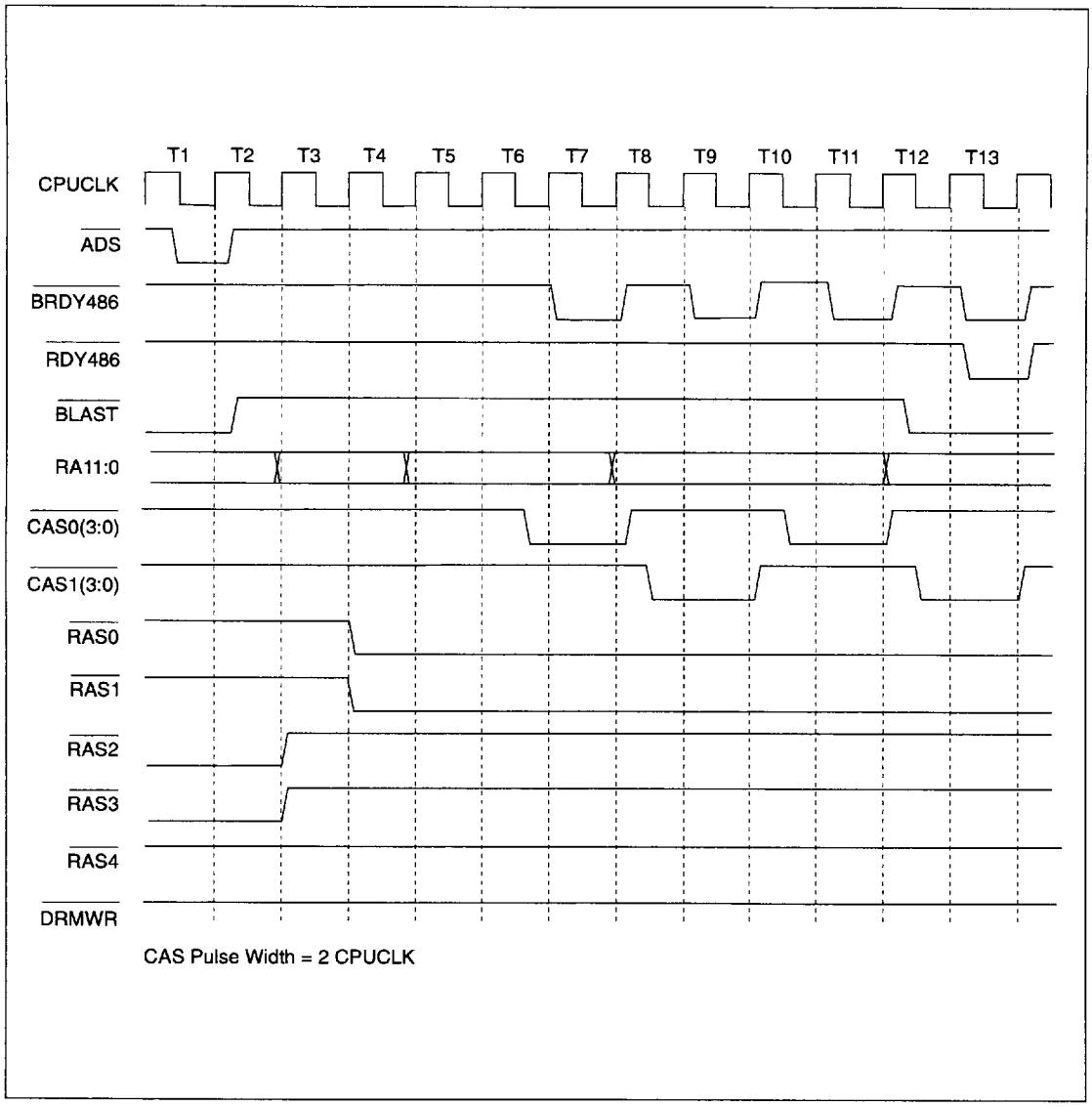


FIGURE 14-14. PAGE MISS, 7-2-2-2 DRAM READ CYCLE

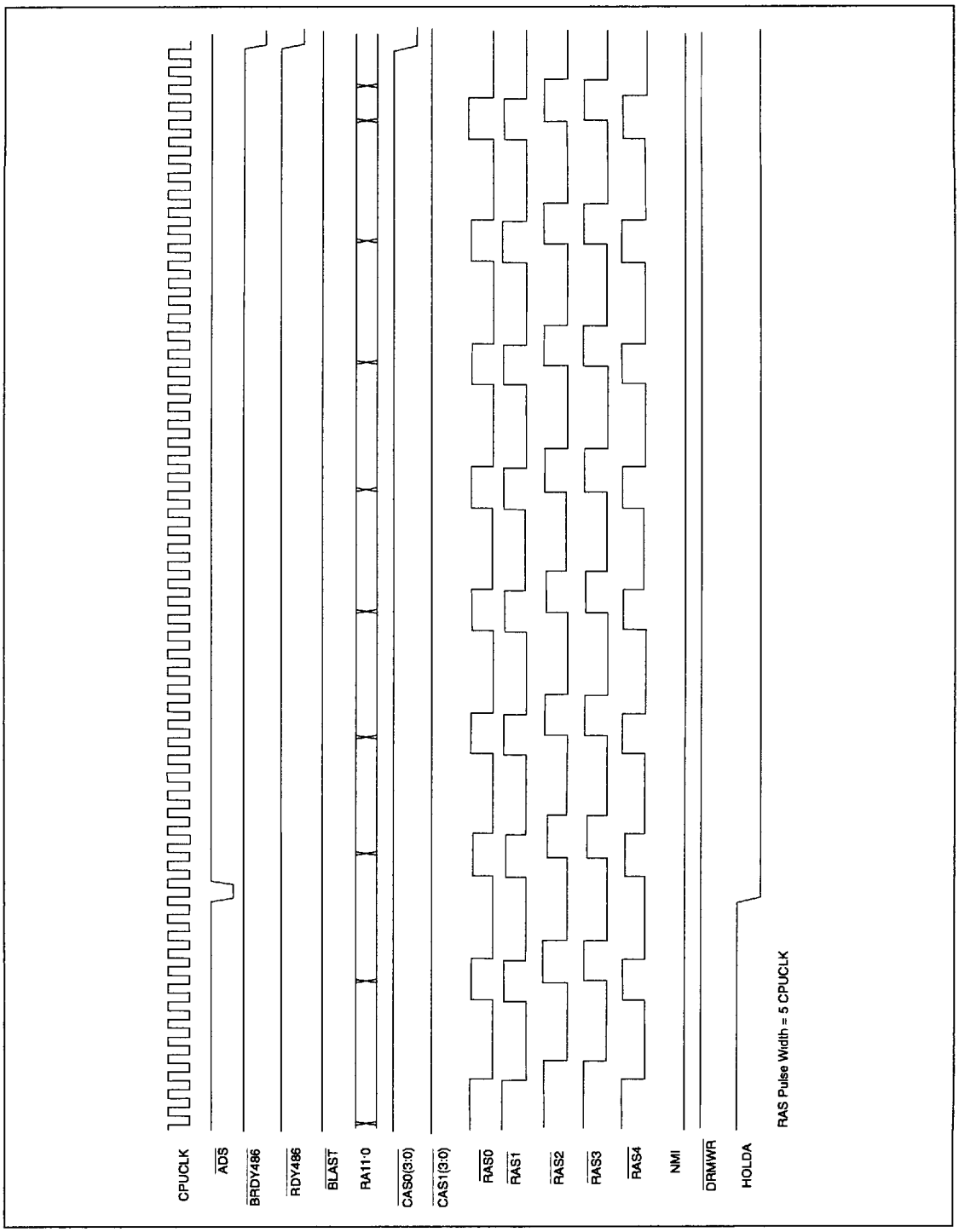


FIGURE 14-15. BURST REFRESH CYCLES

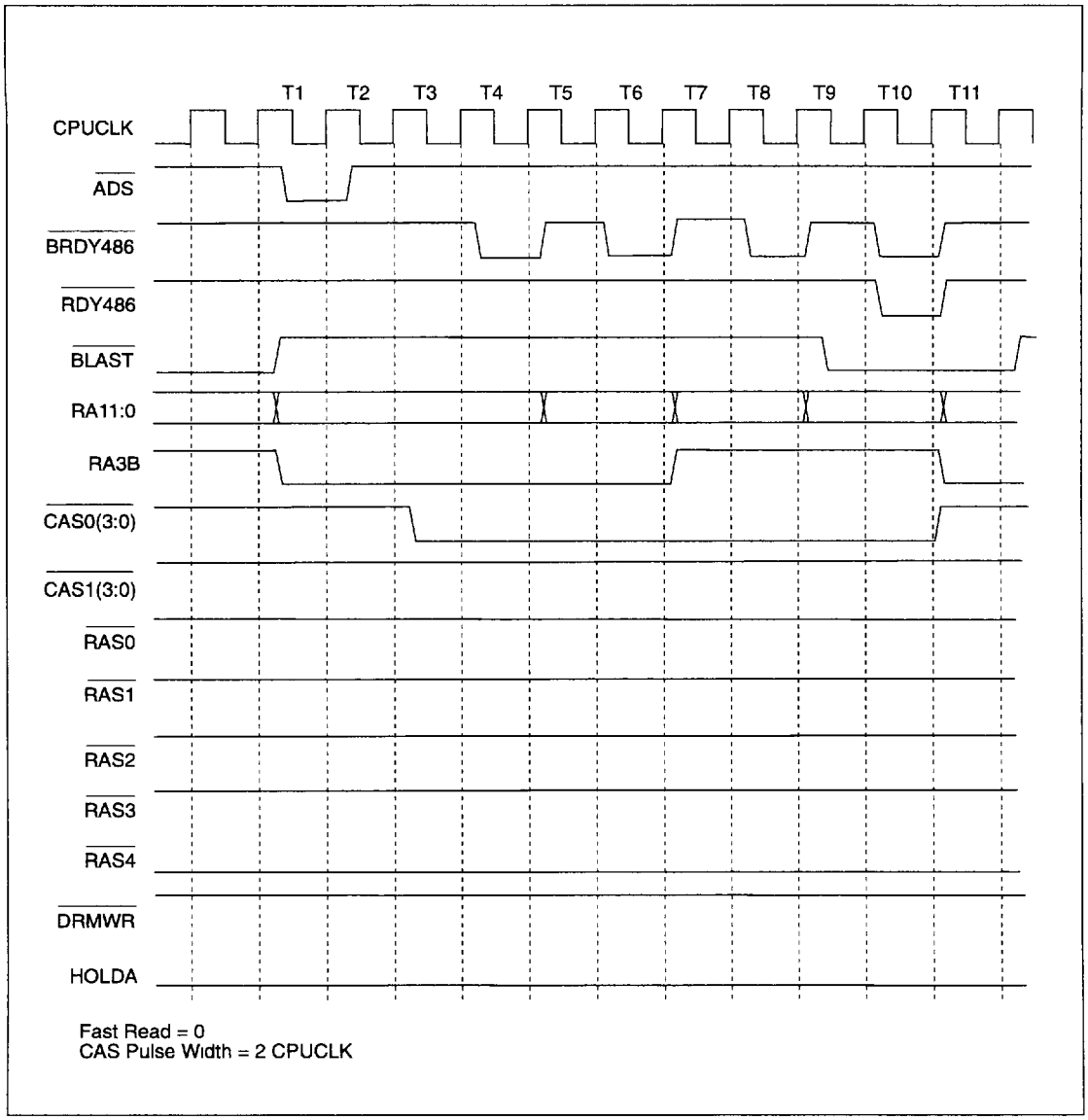


FIGURE 14-16. STATIC COLUMN MODE, 4-2-2-2 PAGE HIT CYCLE

14.2 AT BUS TIMING

The AT Bus timing is divided into six major categories:

1. CPU initiated AT Bus cycles.
2. Entering the AT Bus.
3. Exiting the AT Bus.
4. DMA cycles.
5. AT Bus Master cycles.
6. AT Bus Refresh cycle.

Some figures in this section are included only to show the sequence of the signals during certain operations. In these figures, no timing parameters are provided.

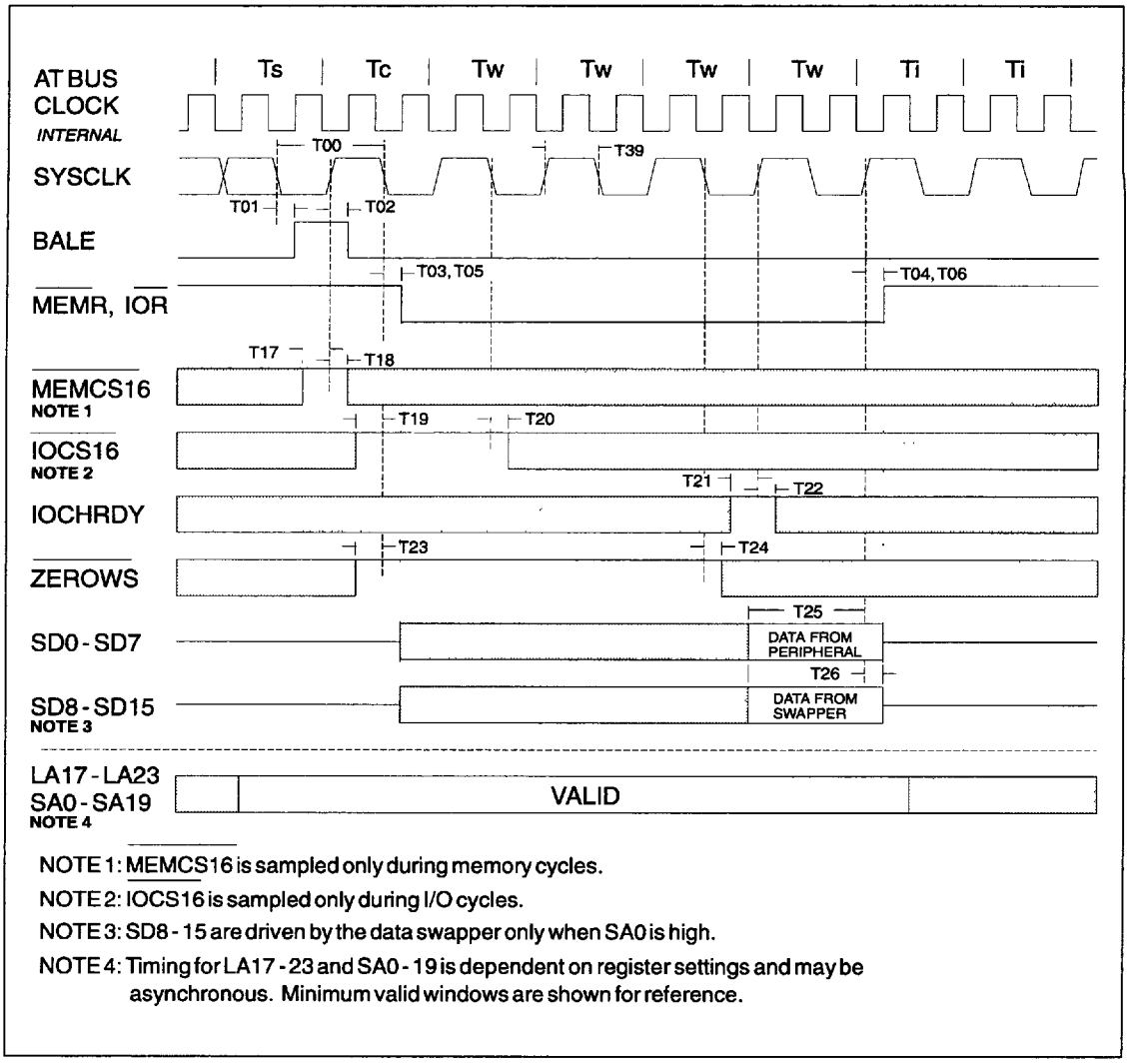
14.2.1 CPU Initiated AT Bus Cycles

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T00	SYSCLK Cycle Time	100		ns	
T01	SYSCLK fall to BALE rise		12	ns	
T02	SYSCLK rise to BALE fall		9	ns	
T03	SYSCLK fall to $\overline{\text{MEMR}}$ fall		9	ns	8-bit cycle
T04	SYSCLK rise to $\overline{\text{MEMR}}$ rise		6	ns	
T05	SYSCLK fall to $\overline{\text{IOR}}$ fall		10	ns	
T06	SYSCLK rise to $\overline{\text{IOR}}$ rise		7	ns	
T17	$\overline{\text{MEMCS16}}$ setup time to SYSCLK rise	25		ns ns	
T18	$\overline{\text{MEMCS16}}$ hold time from SYSCLK rise	0		ns ns	
T19	$\overline{\text{IOCS16}}$ setup time to SYSCLK fall	23		ns	
T20	$\overline{\text{IOCS16}}$ hold time from SYSCLK fall	0		ns	8-bit cycle
T21	IOCHRDY setup time to SYSCLK rise	22		ns	
T22	IOCHRDY hold time from SYSCLK rise	0		ns	
T23	$\overline{\text{ZEROWS}}$ setup time to SYSCLK fall	24		ns	
T24	$\overline{\text{ZEROWS}}$ hold time from SYSCLK fall	0		ns	
T25	AT Bus data setup time to SYSCLK rise	22		ns	
T26	AT Bus data hold time from SYSCLK rise	0	9	ns	
T27	SYSCLK fall to $\overline{\text{MEMW}}$ fall		5	ns	
T28	SYSCLK rise to $\overline{\text{MEMW}}$ rise		10	ns	
T29	SYSCLK fall to $\overline{\text{IOW}}$ fall		8	ns	
T30	SYSCLK rise to $\overline{\text{IOW}}$ rise			ns	

TABLE 14-4. CPU INITIATED AT BUS CYCLES

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T36	SYSCLK fall to SA0 rise		16	ns	Word to byte conversion cycle
T37	SYSCLK rise to MEMR fall		6	ns	16-bit cycle
T38	IOCS16 hold time from SYSCLK rise	0		ns	16-bit cycle
T39	SYSCLK high time	-4	0	ns	(T00 ÷ 2) plus number given

TABLE 14-4. CPU INITIATED AT BUS CYCLES (Continued)



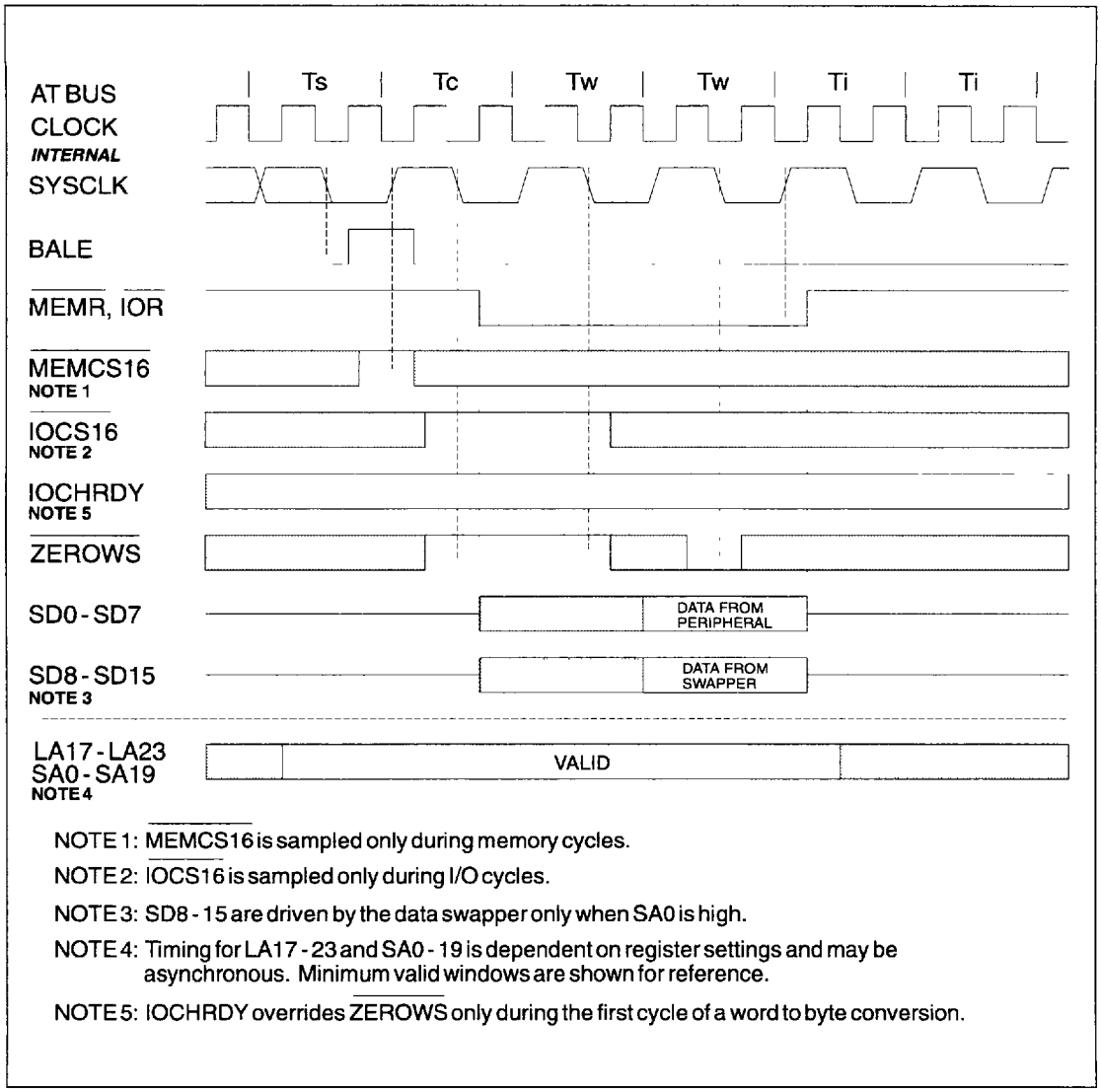
NOTE 1: MEMCS16 is sampled only during memory cycles.

NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: SD8 - 15 are driven by the data swapper only when SA0 is high.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 14-17. AT BUS I/O OR MEMORY READ: 8-BIT, DEFAULT TIMING



NOTE 1: MEMCS16 is sampled only during memory cycles.

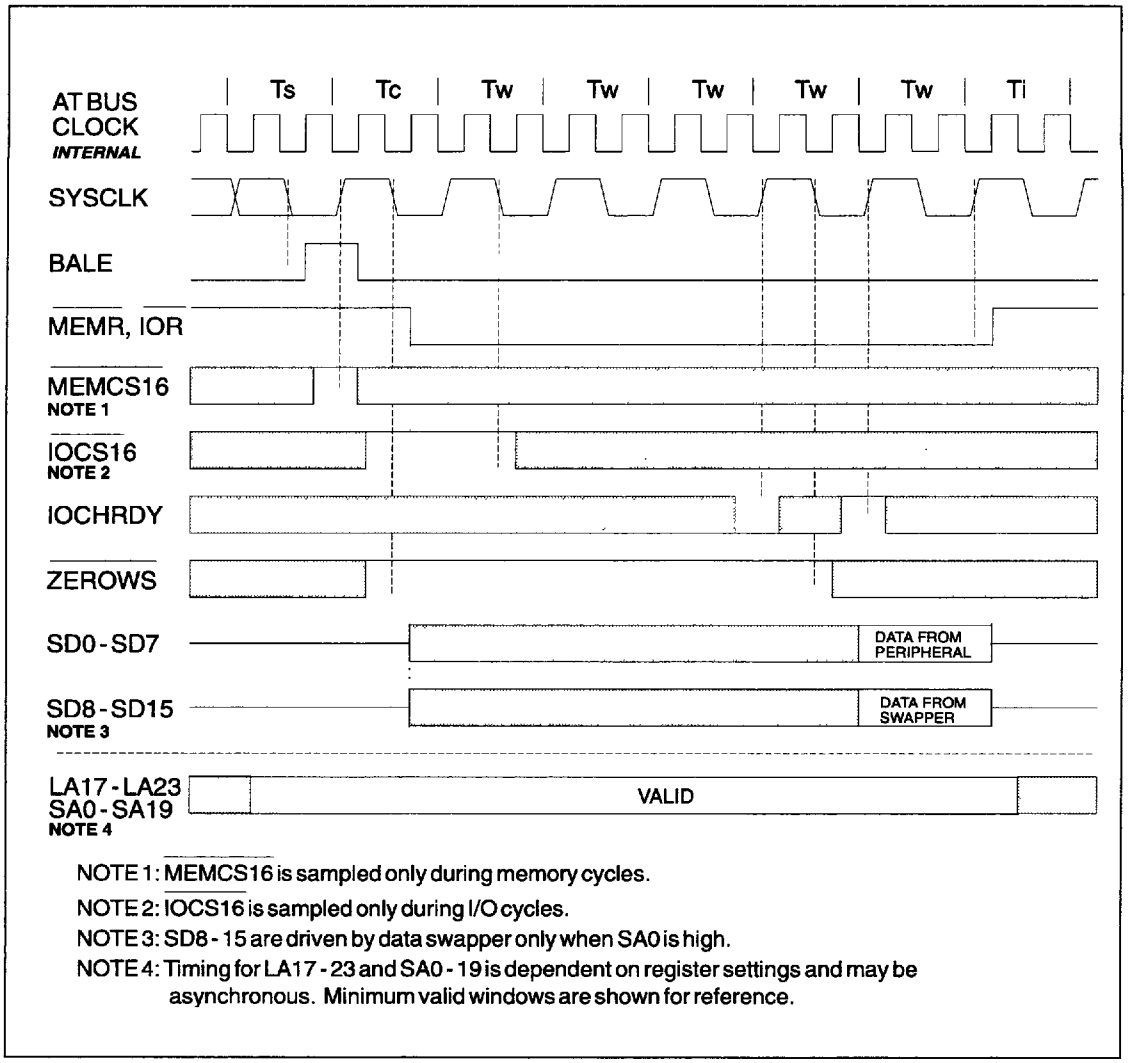
NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: SD8 - 15 are driven by the data swapper only when SA0 is high.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

NOTE 5: IOCHRDY overrides ZEROWS only during the first cycle of a word to byte conversion.

FIGURE 14-18. AT BUS I/O OR MEMORY READ: 8-BIT, ZEROWS ASSERTED



NOTE 1: MEMCS16 is sampled only during memory cycles.
NOTE 2: IOCS16 is sampled only during I/O cycles.
NOTE 3: SD8-15 are driven by data swapper only when SA0 is high.
NOTE 4: Timing for LA17-23 and SA0-19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 14-19. AT BUS I/O OR MEMORY READ: 8-BIT, EXTRA WAIT STATE ADDED

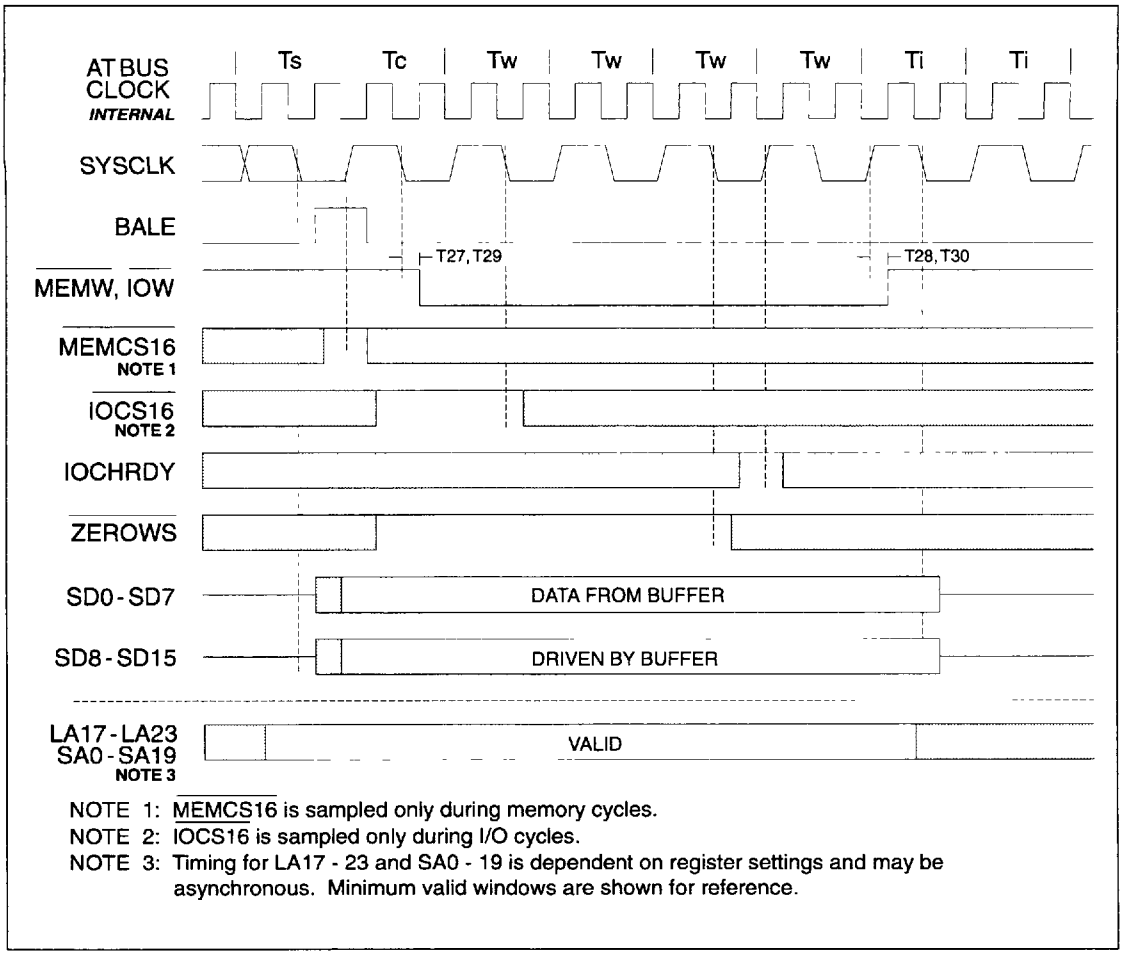


FIGURE 14-20. AT BUS I/O OR MEMORY WRITE: 8-BIT, EVEN BYTE, DEFAULT TIMING

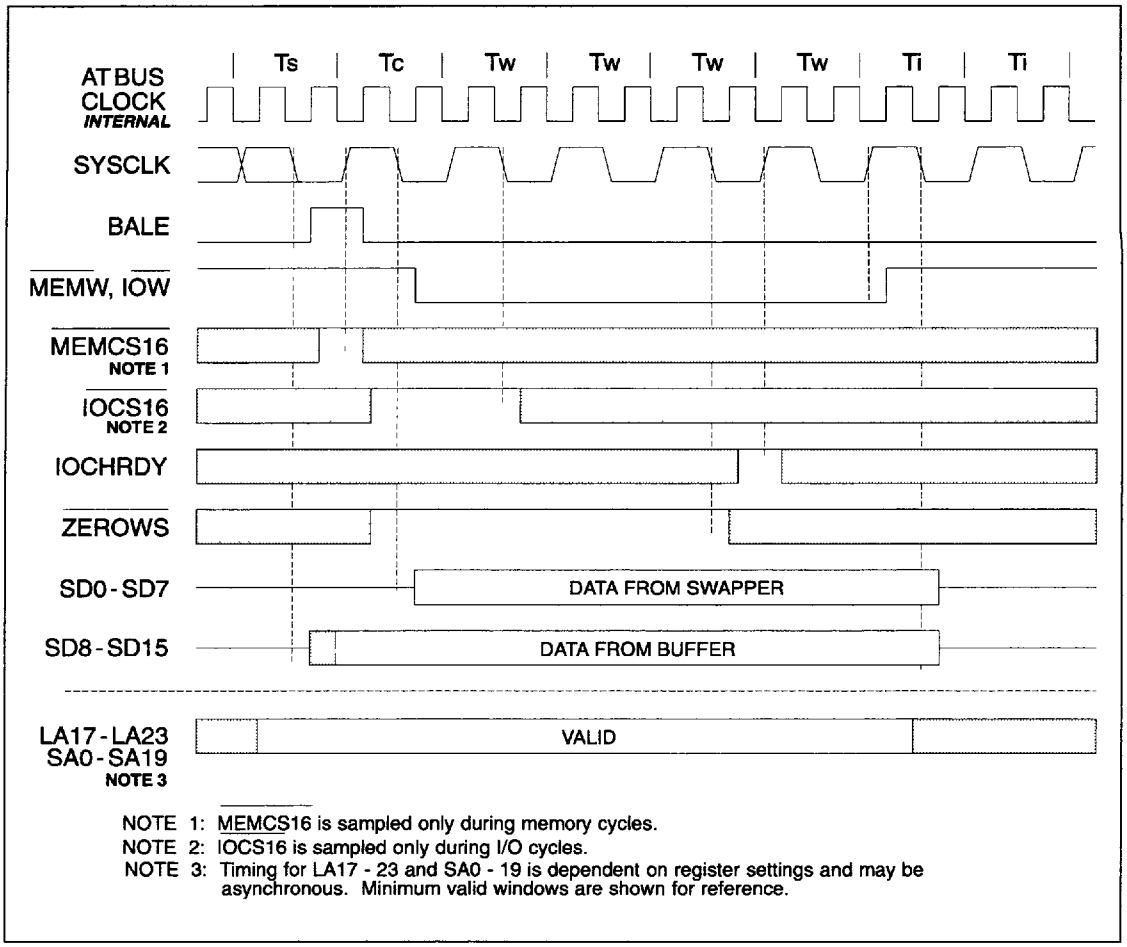


FIGURE 14-21. AT BUS I/O OR MEMORY WRITE: 8-BIT, ODD BYTE, DEFAULT TIMING

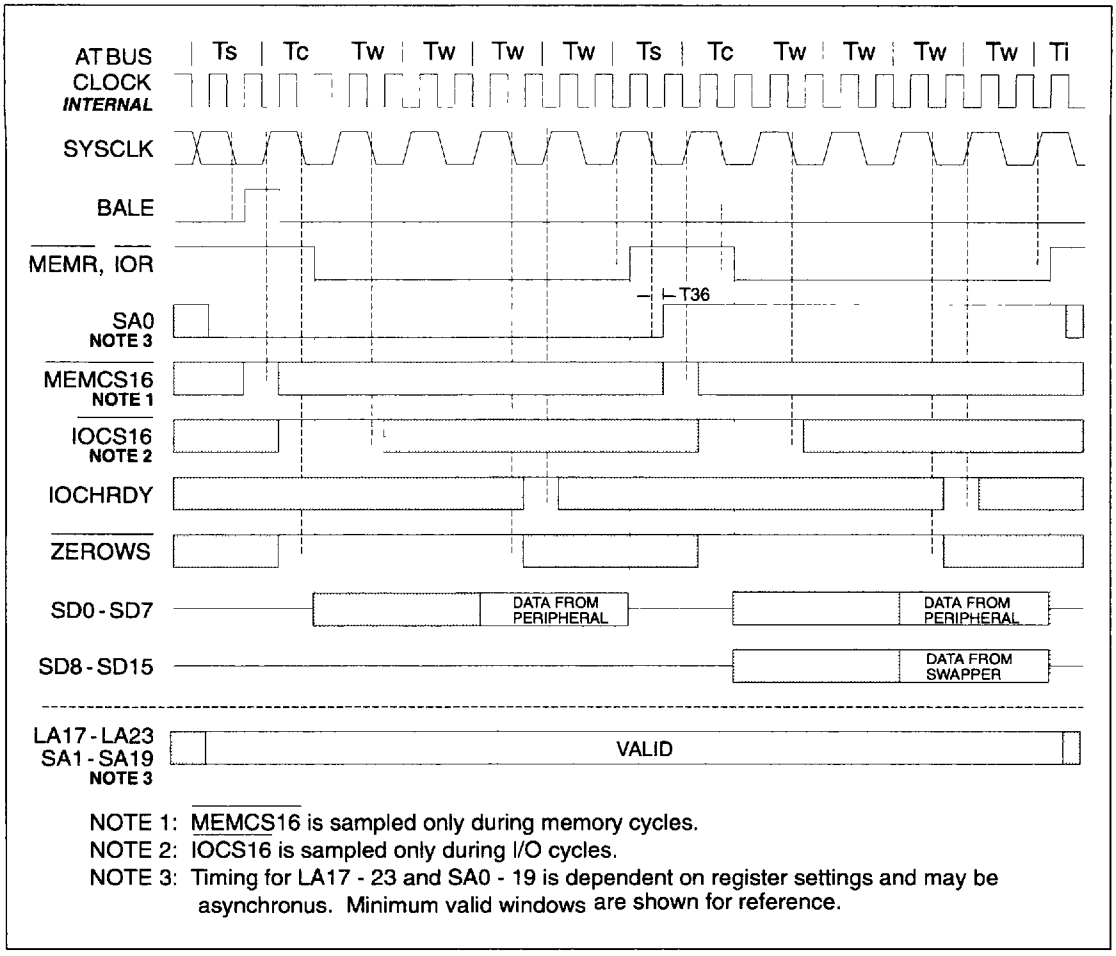
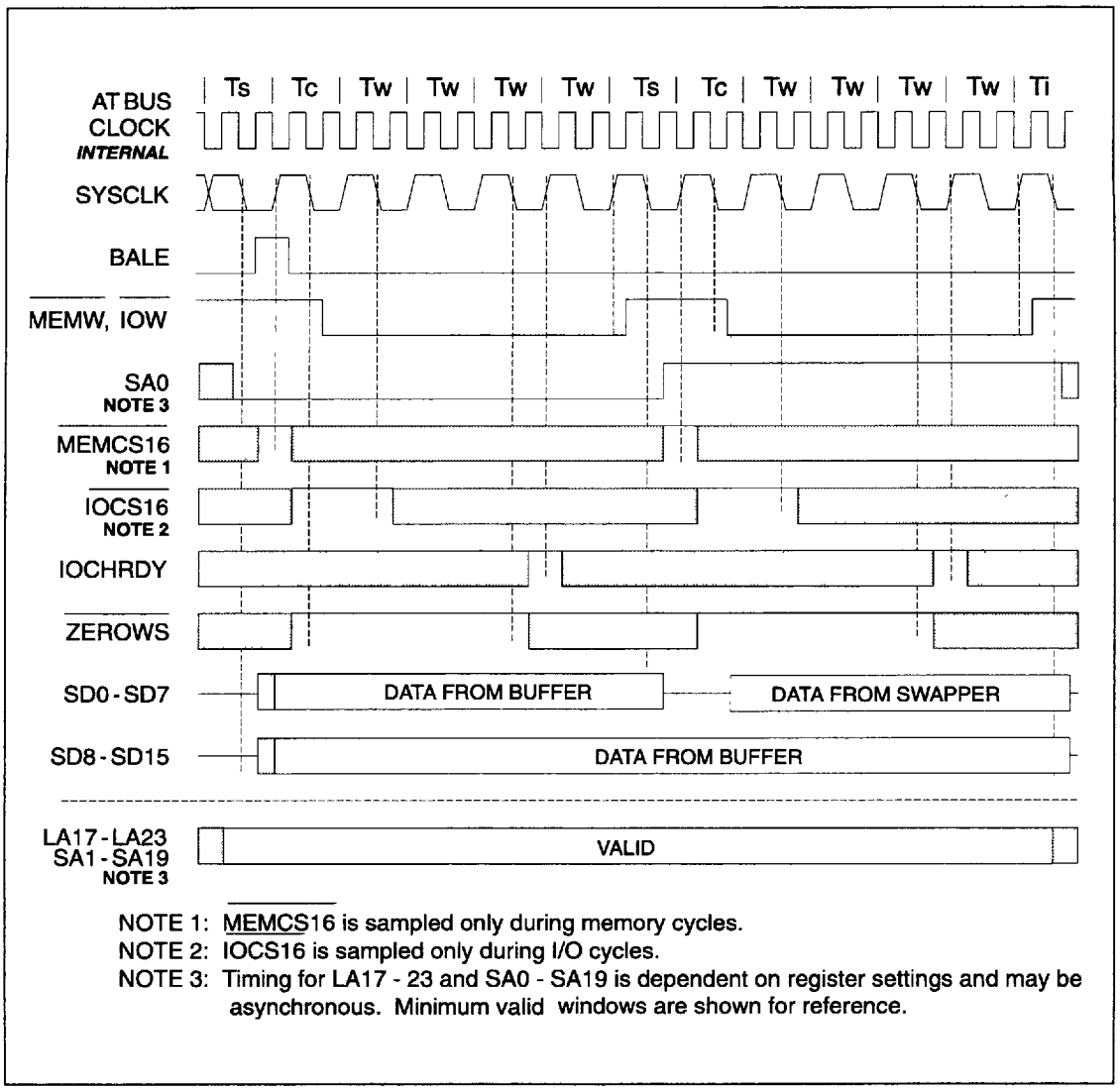
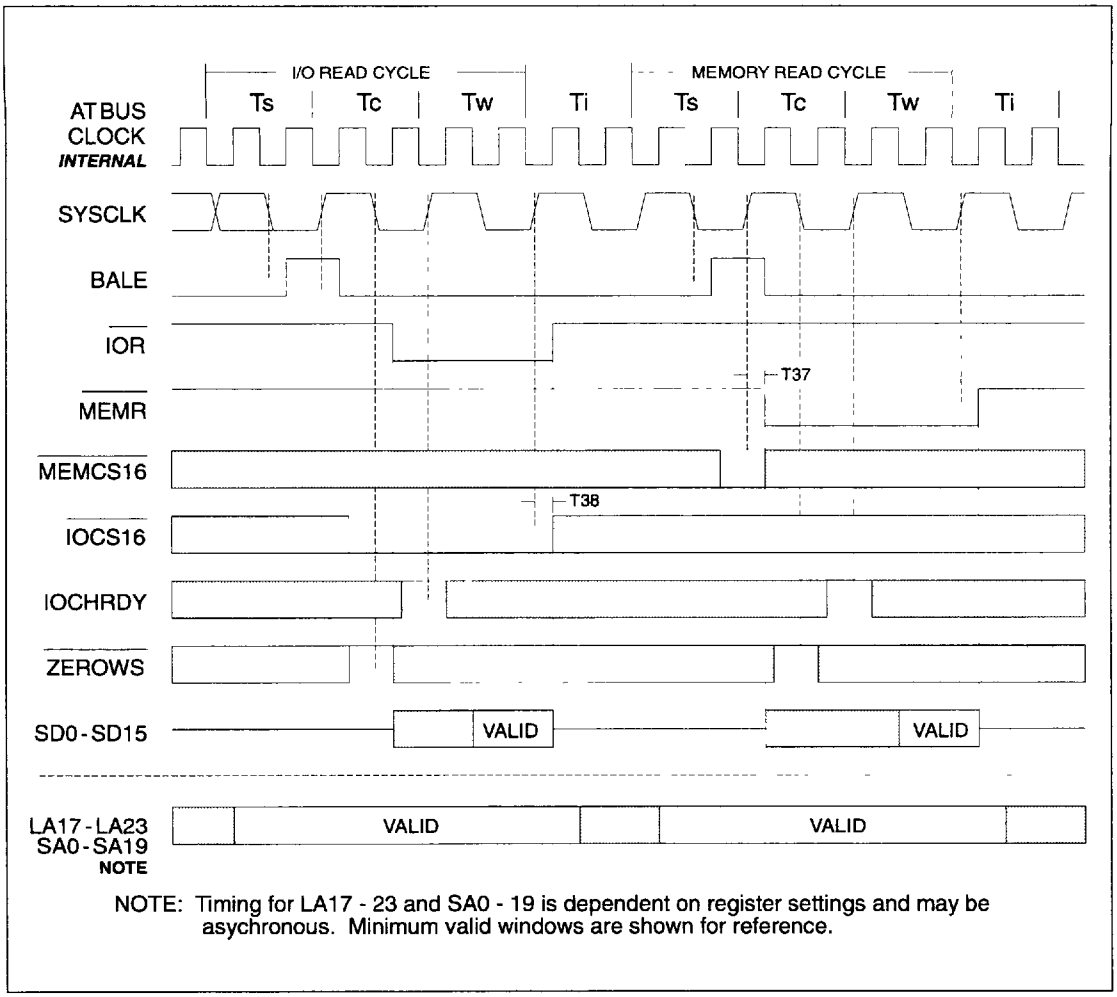


FIGURE 14-22. AT BUS I/O OR MEMORY READ: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING



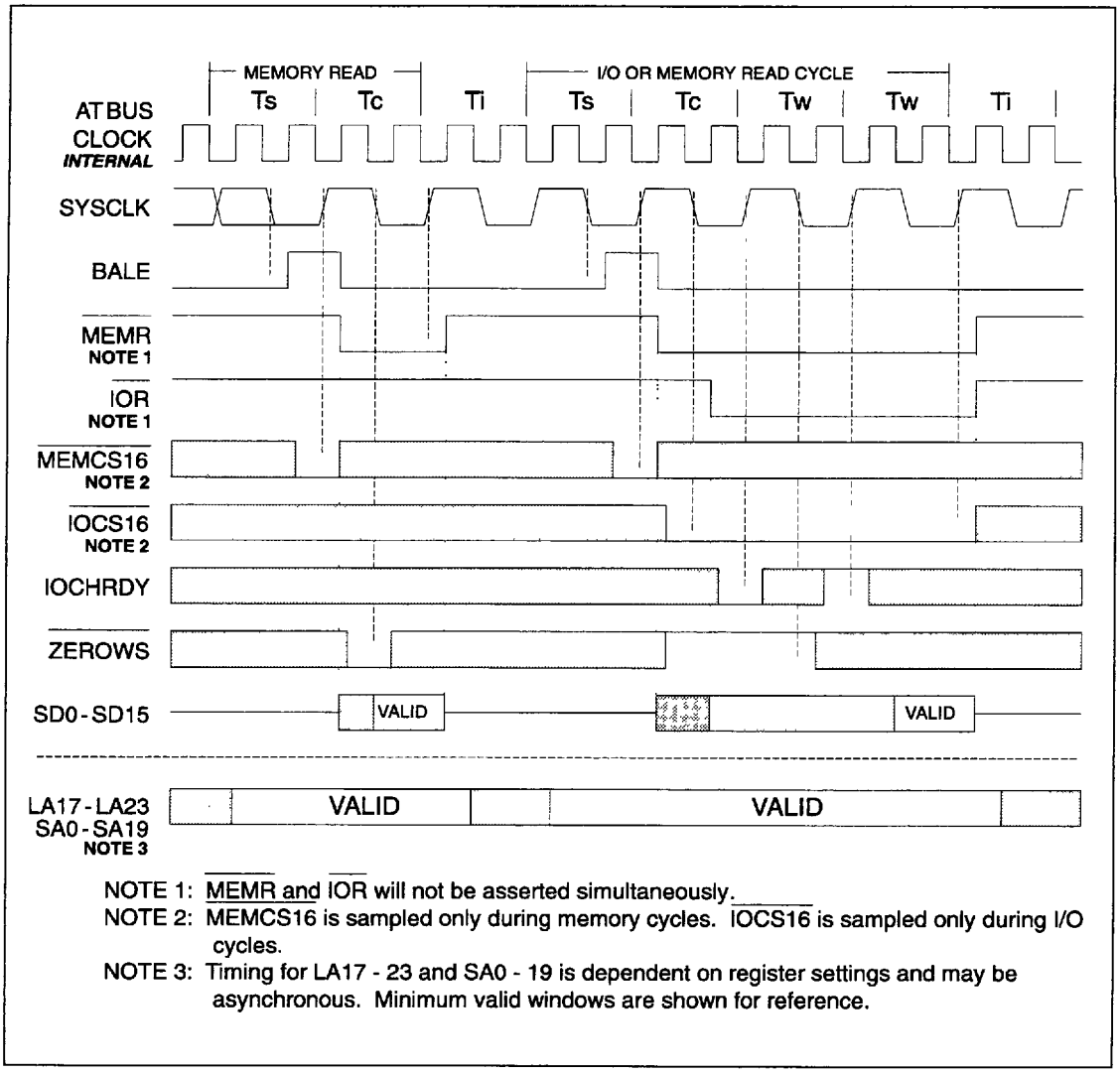
NOTE 1: MEMCS16 is sampled only during memory cycles.
NOTE 2: IOCS16 is sampled only during I/O cycles.
NOTE 3: Timing for LA17 - 23 and SA0 - SA19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 14-23. AT BUS I/O OR MEMORY WRITE: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING



NOTE: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asychronous. Minimum valid windows are shown for reference.

FIGURE 14-24. AT BUS I/O OR MEMORY READ: 16-BIT, DEFAULT TIMING



NOTE 1: MEMR and IOR will not be asserted simultaneously.

NOTE 2: MEMCS16 is sampled only during memory cycles. IOCS16 is sampled only during I/O cycles.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 14-25. AT BUS I/O OR MEMORY READ: 16-BIT, 0WS ASSERTED AND EXTRA WAIT STATE ADDED

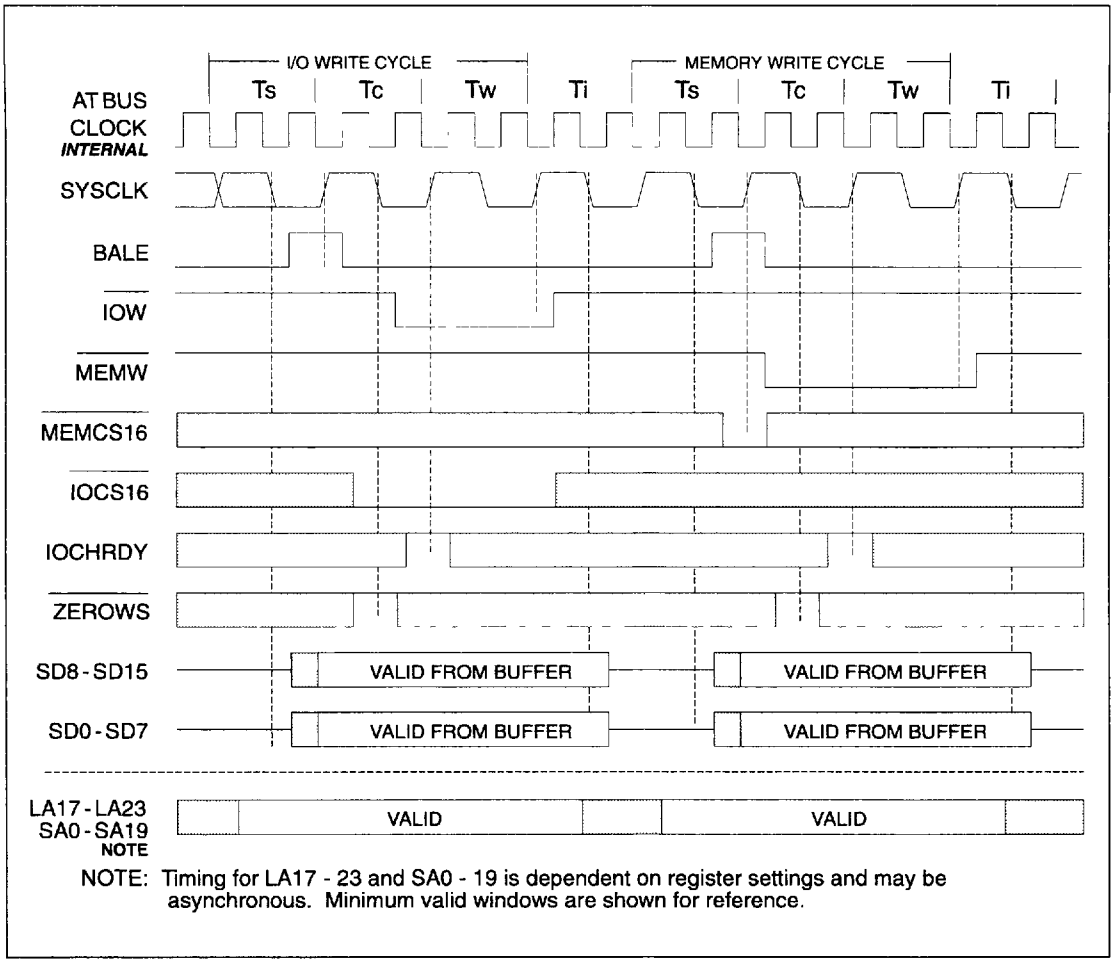


FIGURE 14-26. AT BUS I/O OR MEMORY WRITE: 16-BIT, DEFAULT TIMING

14.2.2 DMA Cycles

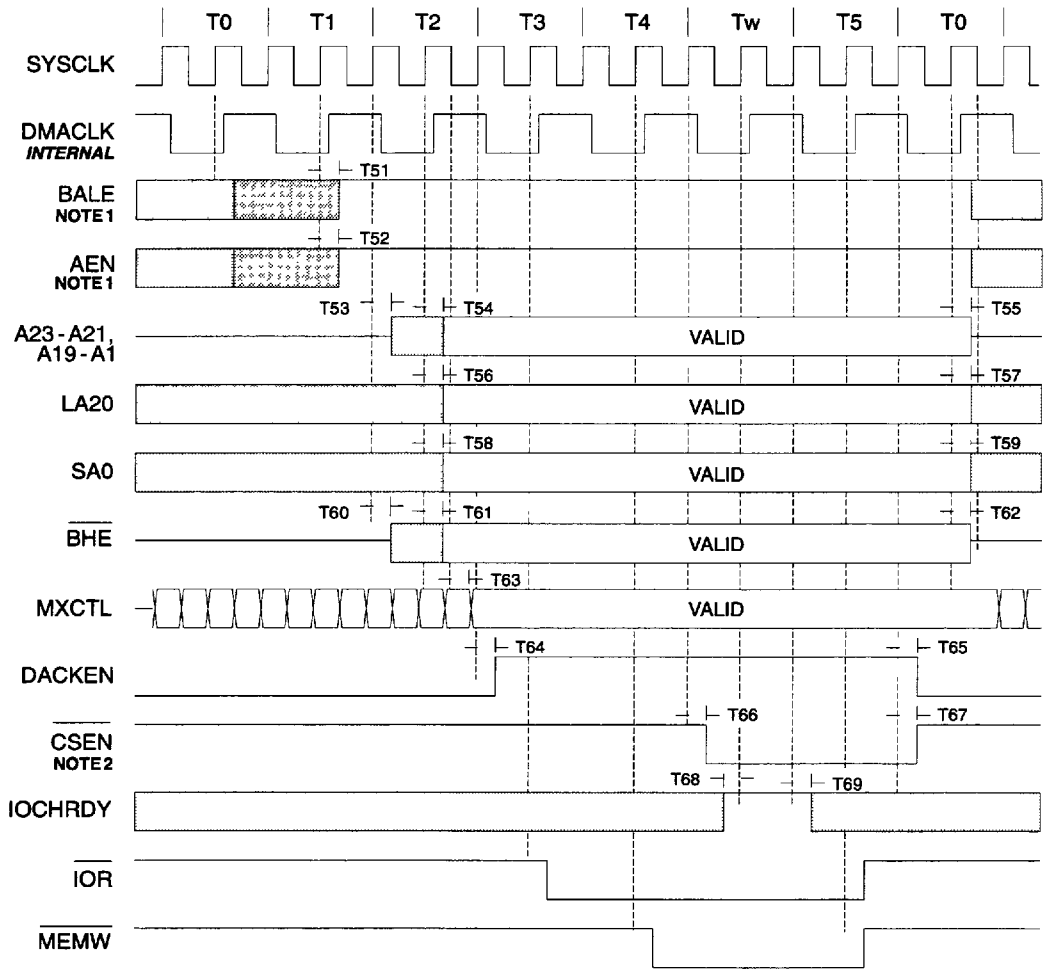
Basic default timing is covered first, followed by 8-bit I/O to onboard memory, then onboard memory to 8-bit I/O.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T54	SYSCLK rise to Address valid		60	ns	
T55	Address hold from SYSCLK rise	0		ns	
T56	SYSCLK rise to LA20 valid		49	ns	
T57	LA20 hold from SYSCLK rise	0		ns	
T58	SYSCLK rise to SA0 valid		40	ns	
T59	SA0 hold from SYSCLK rise	0		ns	
T60	SYSCLK rise to $\overline{BHE}$ driven	0		ns	
T61	SYSCLK rise to $\overline{BHE}$ valid		36	ns	
T62	$\overline{BHE}$ hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T66	SYSCLK rise to $\overline{CSEN}$ fall		32	ns	
T67	SYSCLK rise to $\overline{CSEN}$ rise		33	ns	
T68	IOCHRDY setup to SYSCLK rise	12		ns	
T69	IOCHRDY hold from SYSCLK rise	0		ns	
T70	SYSCLK rise to $\overline{IOR}$ fall		28	ns	
T71	SYSCLK rise to $\overline{IOR}$ rise		35	ns	
T72	SYSCLK rise to $\overline{MEMW}$ fall		47	ns	
T73	SYSCLK rise to $\overline{MEMW}$ rise		35	ns	
T82	SYSCLK rise to $\overline{IOW}$ fall		53	ns	
T83	SYSCLK rise to $\overline{IOW}$ rise		37	ns	
T84	SYSCLK rise to $\overline{MEMR}$ fall		17	ns	
T85	SYSCLK rise to $\overline{MEMR}$ rise		38	ns	
T100	$\overline{MEMW}$ fall to $\overline{RAS}$n fall		27	ns	
T101	$\overline{MEMW}$ rise to $\overline{RAS}$n rise		29	ns	
T102	$\overline{MEMW}$ fall to $\overline{CAS}$n fall		108	ns	
T103	$\overline{MEMW}$ rise to $\overline{CAS}$n rise		30	ns	
T105	$\overline{MEMW}$ fall to RA(11:00) valid		100	ns	
T107	$\overline{MEMW}$ fall to $\overline{DRMWR}$ low		29	ns	
T108	$\overline{MEMW}$ rise to $\overline{DRMWR}$ high	10		ns	

TABLE 14-5. DMA CYCLES

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T120	$\overline{MEMR}$ fall to $\overline{RAS}$n fall		28	ns	
T121	$\overline{MEMR}$ rise to $\overline{RAS}$ rise		29	ns	
T122	$\overline{MEMR}$ fall to $\overline{CAS}$n fall		110	ns	
T123	$\overline{MEMR}$ rise to $\overline{CAS}$ rise		31	ns	
T125	$\overline{MEMR}$ fall to RA(10:00) valid		100	ns	
T305	D(15:00) setup to $\overline{MEMR}$ rise	18		ns	

TABLE 14-5. DMA CYCLES (Continued)



NOTE 1: BALE and AEN may be asynchronous. Minimum valid time is shown. DMA Channels 0, 1, 2 and 3 will have two additional SYSCLK periods of valid time as shown by the alternate shaded region.

NOTE 2: $\overline{\text{CSEN}}$ is used to generate the terminal count signal and pulses low only during the last transfer in a block.

FIGURE 14-27. BASIC DMA CYCLE, DEFAULT TIMING

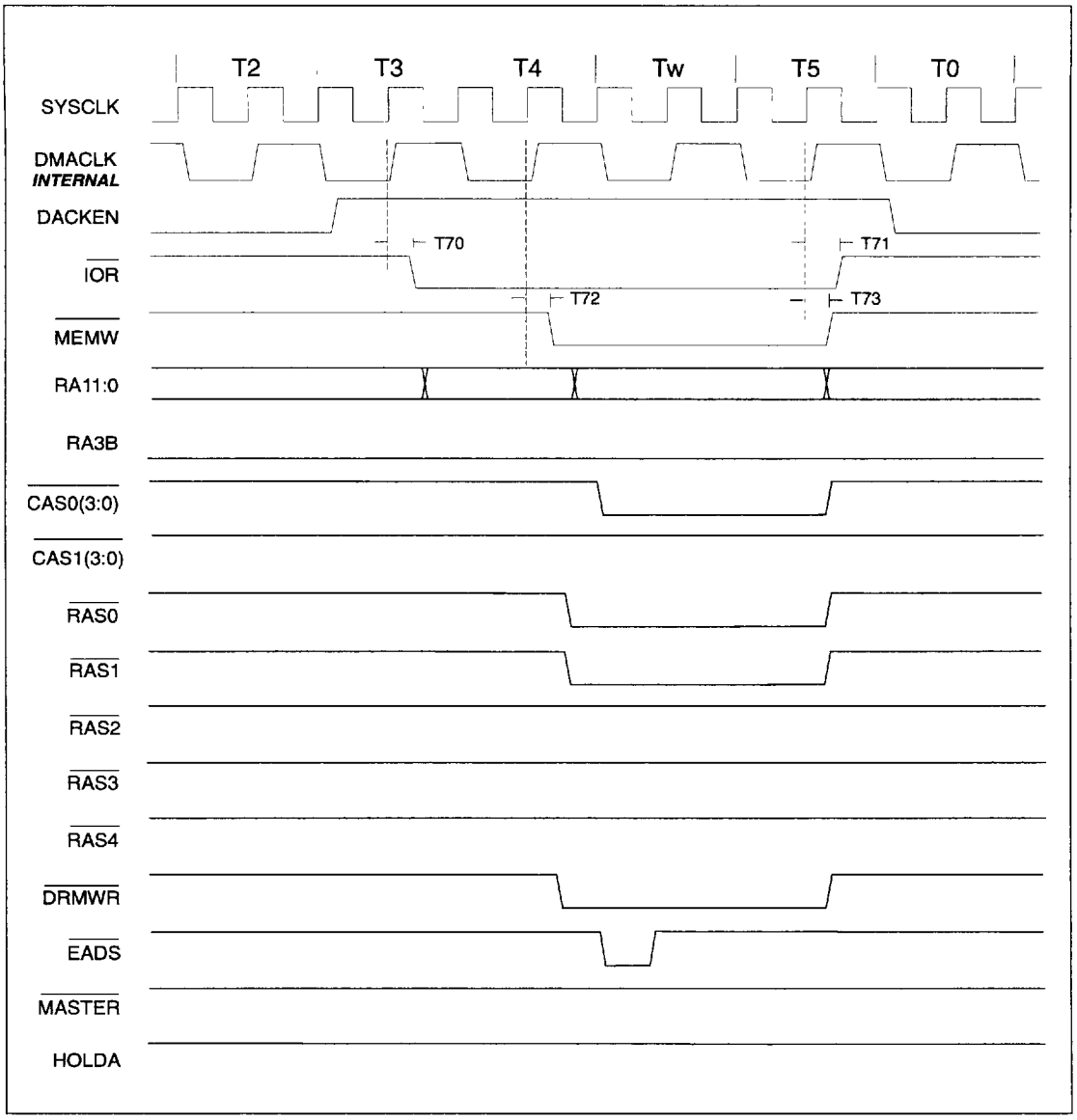


FIGURE 14-28. DMA CYCLE, 8-BIT I/O TO ON-BOARD MEMORY

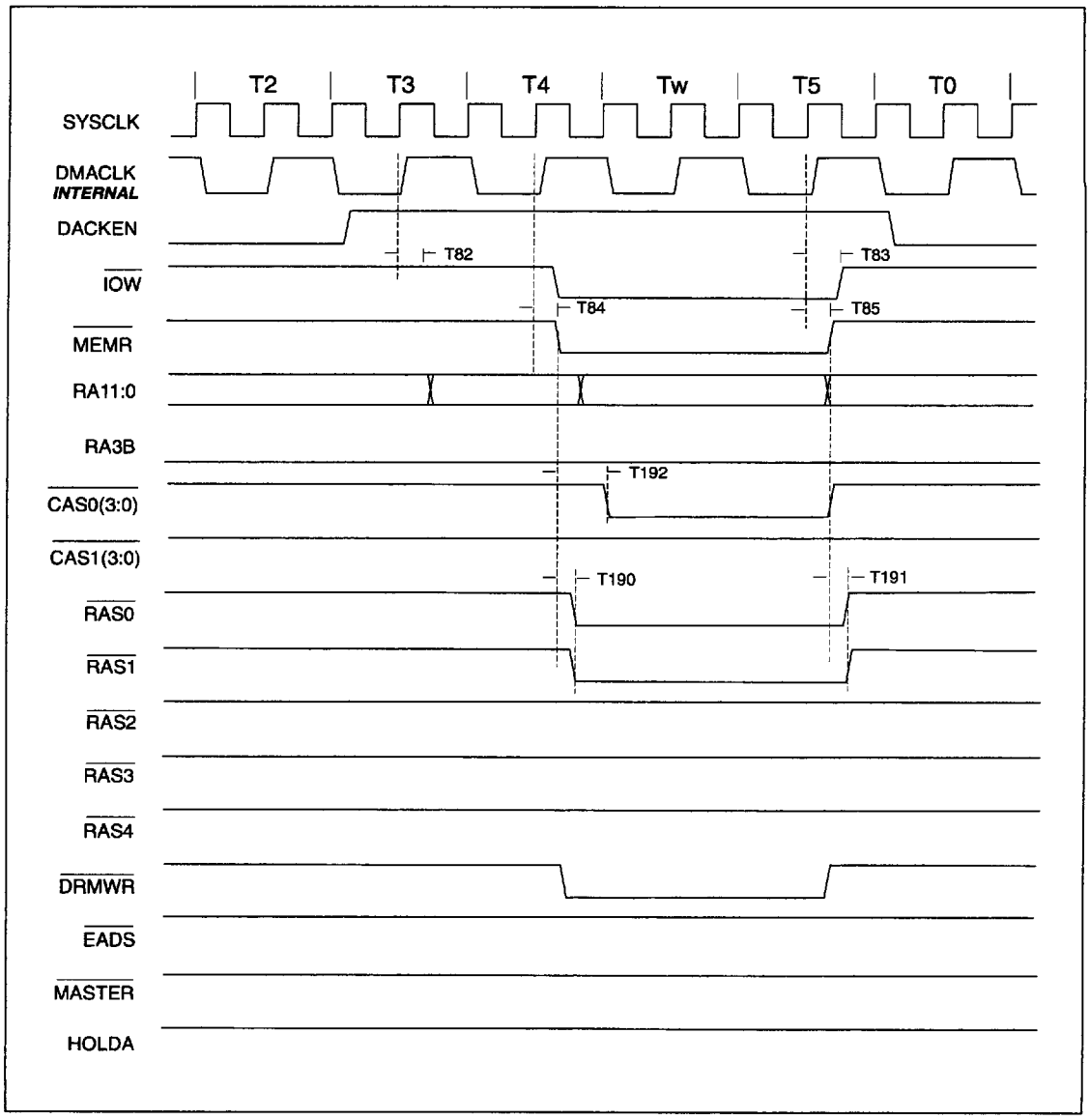


FIGURE 14-29. DMA CYCLE, ON-BOARD MEMORY TO 8-BIT I/O

14.2.3 AT Bus Master

The AT Bus master timing is covered in the following sequence:

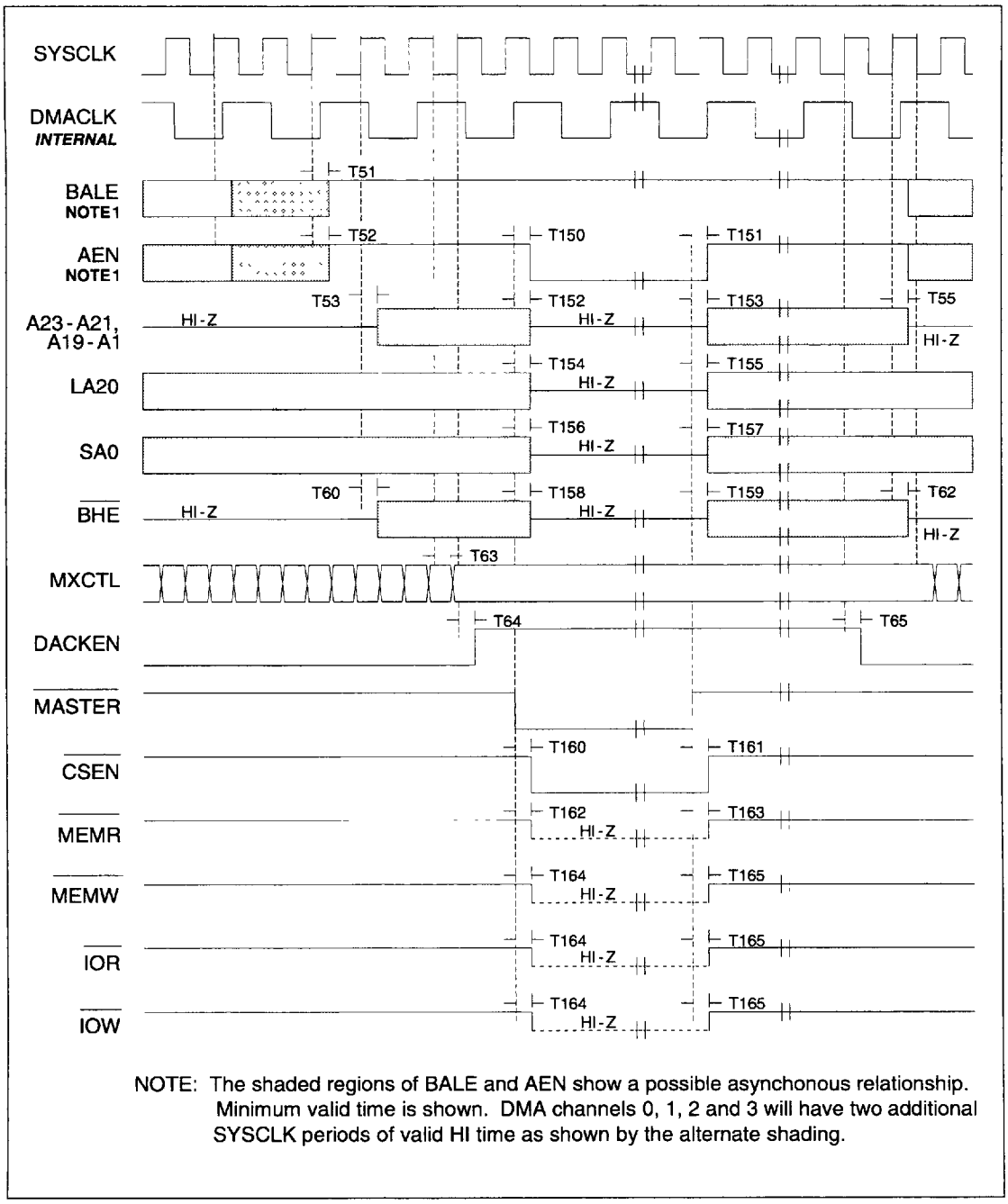
- Bus acquisition and release
- Writing to the onboard memory
- Reading from the onboard memory

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T55	Address hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T150	$\overline{\text{MASTER}}$ fall to AEN fall		30	ns	
T151	$\overline{\text{MASTER}}$ rise to AEN rise		30	ns	
T152	$\overline{\text{MASTER}}$ fall to A(23:21), A(19:01) float		30	ns	
T153	$\overline{\text{MASTER}}$ rise to A(23:21), A(19:01) driven	15		ns	
T154	$\overline{\text{MASTER}}$ fall to LA20 float		23	ns	
T155	$\overline{\text{MASTER}}$ rise to LA20 driven	10		ns	
T156	$\overline{\text{MASTER}}$ fall to SA0 float		24	ns	
T157	$\overline{\text{MASTER}}$ rise to SA0 driven	10		ns	
T159	$\overline{\text{MASTER}}$ rise to $\overline{\text{BHE}}$ driven	10		ns	
T160	$\overline{\text{MASTER}}$ fall to $\overline{\text{CSEN}}$ fall		32	ns	
T161	$\overline{\text{MASTER}}$ rise to $\overline{\text{CSEN}}$ rise		35	ns	
T162	$\overline{\text{MASTER}}$ fall to $\overline{\text{MEMR}}$ float		24	ns	
T163	$\overline{\text{MASTER}}$ rise to $\overline{\text{MEMR}}$ driven	10		ns	
T164	$\overline{\text{MASTER}}$ fall to $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, float		23	ns	
T165	$\overline{\text{MASTER}}$ rise to $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$ driven	10		ns	
T166	A(23:21), A(19:01) setup to $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$	45		ns	
T167	LA20 setup to $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$	50		ns	
T168	$\overline{\text{BHE}}$ setup to $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$	0		ns	
T169	SA0 setup to $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$	0		ns	
T170	A(23:21), A(19:01) hold from $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$	15		ns	
T171	LA20 hold from $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$	15		ns	
T172	$\overline{\text{BHE}}$ hold from $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$	15		ns	
T173	SA0 hold from $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$	15		ns	
T174	SA0 in to A0 out delay		45	ns	

TABLE 14-6. AT BUS MASTER CYCLE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T190	$\overline{MEMR}$, $\overline{MEMW}$ fall to $\overline{RASn}$ fall		83	ns	
T191	$\overline{MEMR}$, $\overline{MEMW}$ rise to $\overline{RASn}$ rise		33	ns	
T192	$\overline{MEMR}$, $\overline{MEMW}$ fall to $\overline{CASn}$ fall		126	ns	
T193	$\overline{MEMR}$, $\overline{MEMW}$ rise to $\overline{CASn}$ rise		33	ns	
T194	$\overline{MEMR}$, $\overline{MEMW}$ fall to RA(10:00) column address valid		120	ns	
T196	$\overline{MEMR}$, $\overline{MEMW}$ fall to RA(10:00) row address valid		42	ns	
T197	RA(10:00) column address hold from $\overline{MEMR}$, $\overline{MEMW}$ rise	5		ns	
T300	$\overline{MEMW}$ fall to $\overline{DRMWR}$ fall		33	ns	
T301	$\overline{MEMW}$ rise to $\overline{DRMWR}$ rise	10		ns	
T305	D(31:00) setup to $\overline{MEMR}$ rise	18		ns	

TABLE 14-6. AT BUS MASTER CYCLE (Continued)



NOTE: The shaded regions of BALE and AEN show a possible asynchonous relationship. Minimum valid time is shown. DMA channels 0, 1, 2 and 3 will have two additional SYSCLK periods of valid HI time as shown by the alternate shading.

FIGURE 14-30. AT BUS MASTER, BUS ACQUISITION/RELEASE

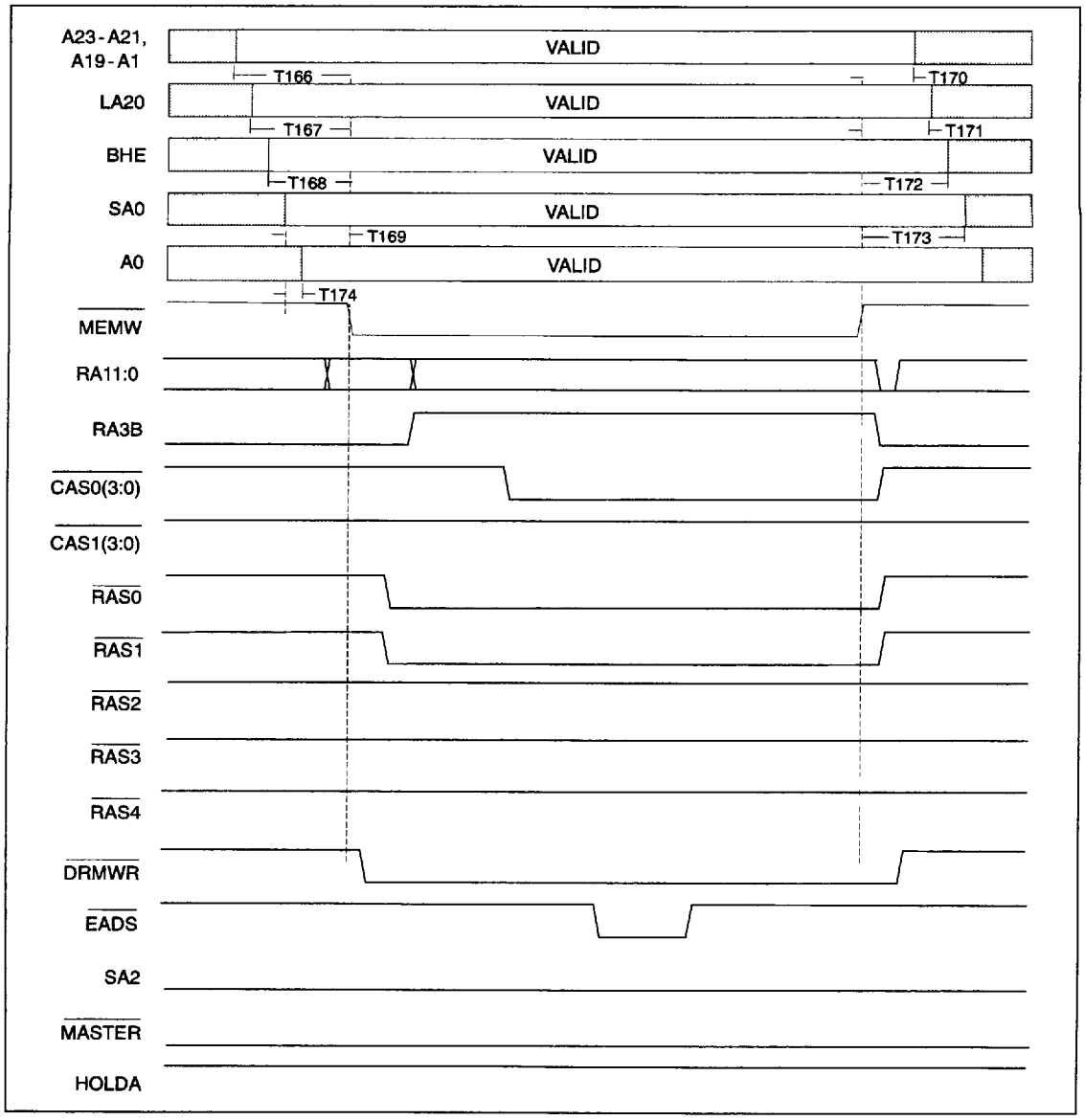


FIGURE 14-31. AT BUS MASTER, WRITE TO ON-BOARD MEMORY

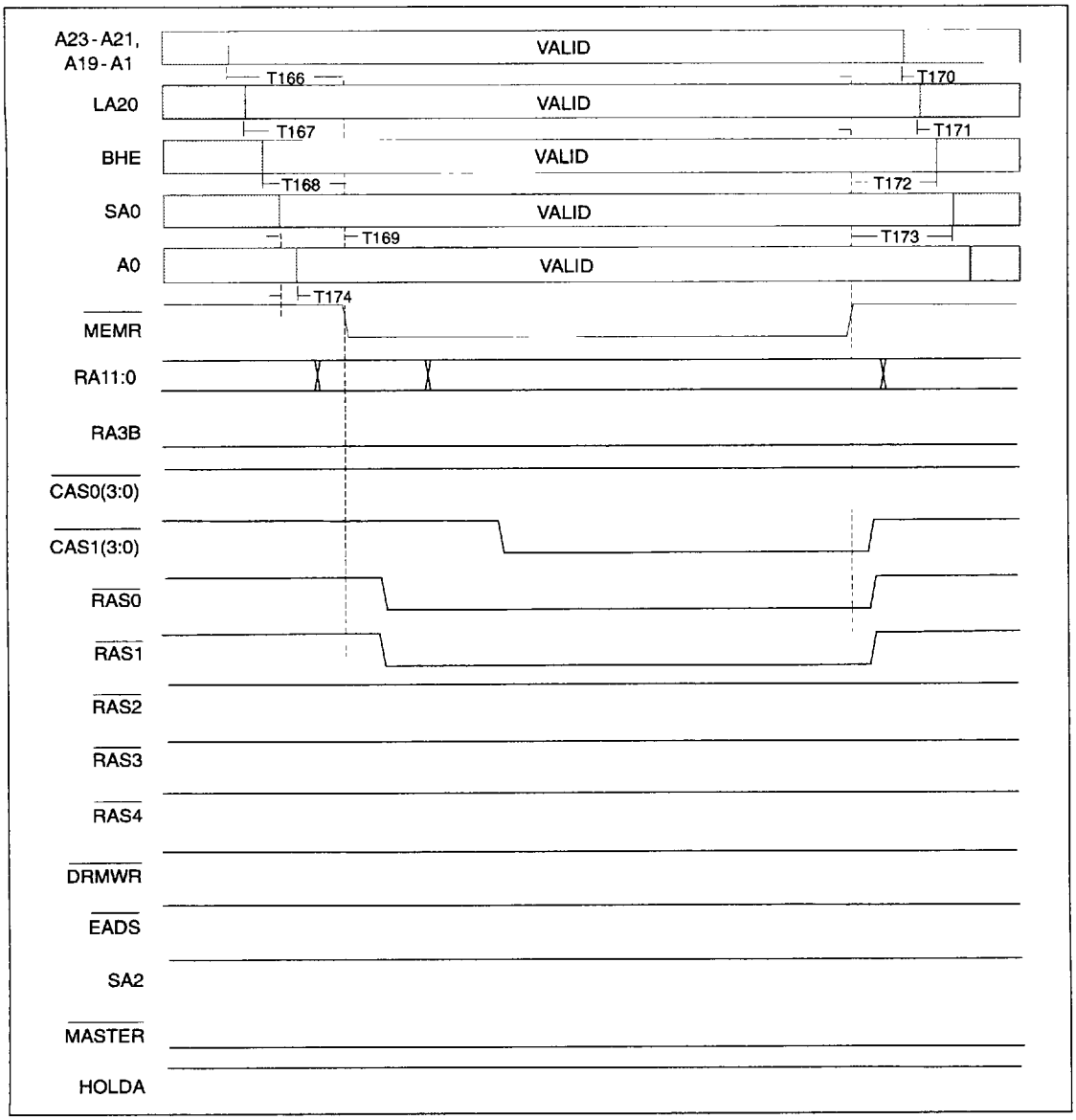
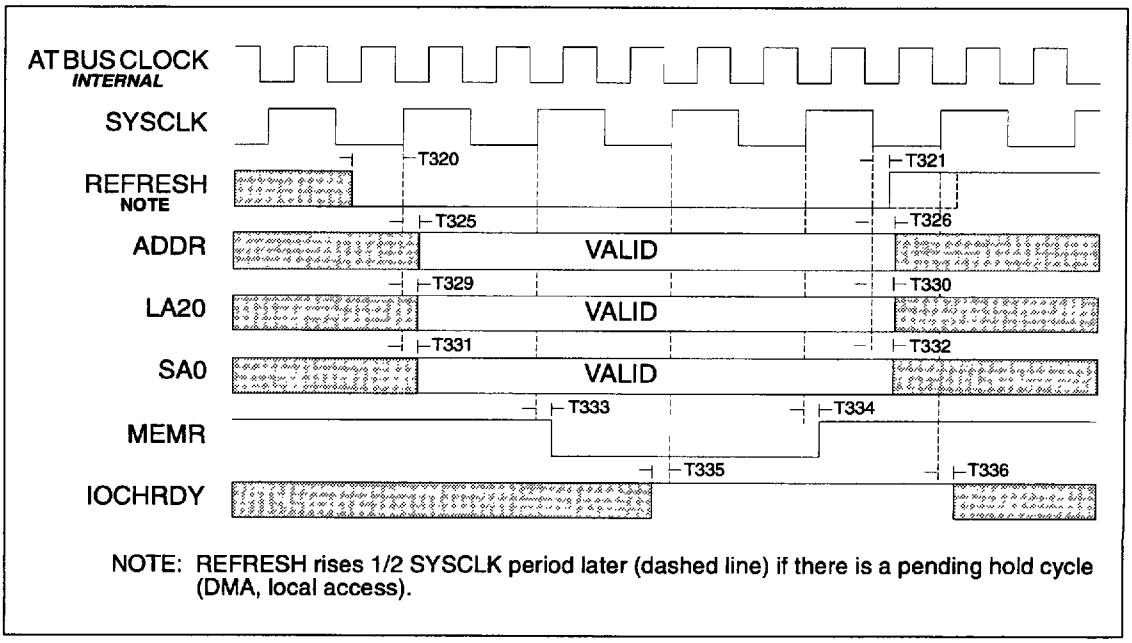


FIGURE 14-32. AT BUS MASTER, READ FROM ON-BOARD MEMORY

14.2.4 AT Bus Refresh

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T320	$\overline{\text{REFRESH}}$ low before SYSCLK rise	4		ns	$\overline{\text{REFRESH}}$ setup is number given plus (T00 × 0.25)
T321	SYSCLK fall to $\overline{\text{REFRESH}}$ rise		16	ns	
T325	SYSCLK rise to A(31:2) valid		35	ns	
T326	SYSCLK fall to A(31:2) invalid	2			
T329	SYSCLK rise to LA20 valid		30	ns	
T330	SYSCLK fall to LA20 invalid	2		ns	
T331	SYSCLK rise to SA0 valid		30	ns	
T332	SYSCLK fall to SA0 invalid	2		ns	
T333	SYSCLK rise to $\overline{\text{MEMR}}$ low		8	ns	
T334	SYSCLK rise to $\overline{\text{MEMR}}$ high		7	ns	
T335	IOCHRDY setup to SYSCLK rise	23		ns	
T336	IOCHRDY hold time from SYSCLK rise	0		ns	

TABLE 14-7. AT BUS REFRESH CYCLE, DEFAULT TIMING



NOTE: REFRESH rises 1/2 SYSCLK period later (dashed line) if there is a pending hold cycle (DMA, local access).

FIGURE 14-33. AT BUS REFRESH CYCLE, DEFAULT TIMING

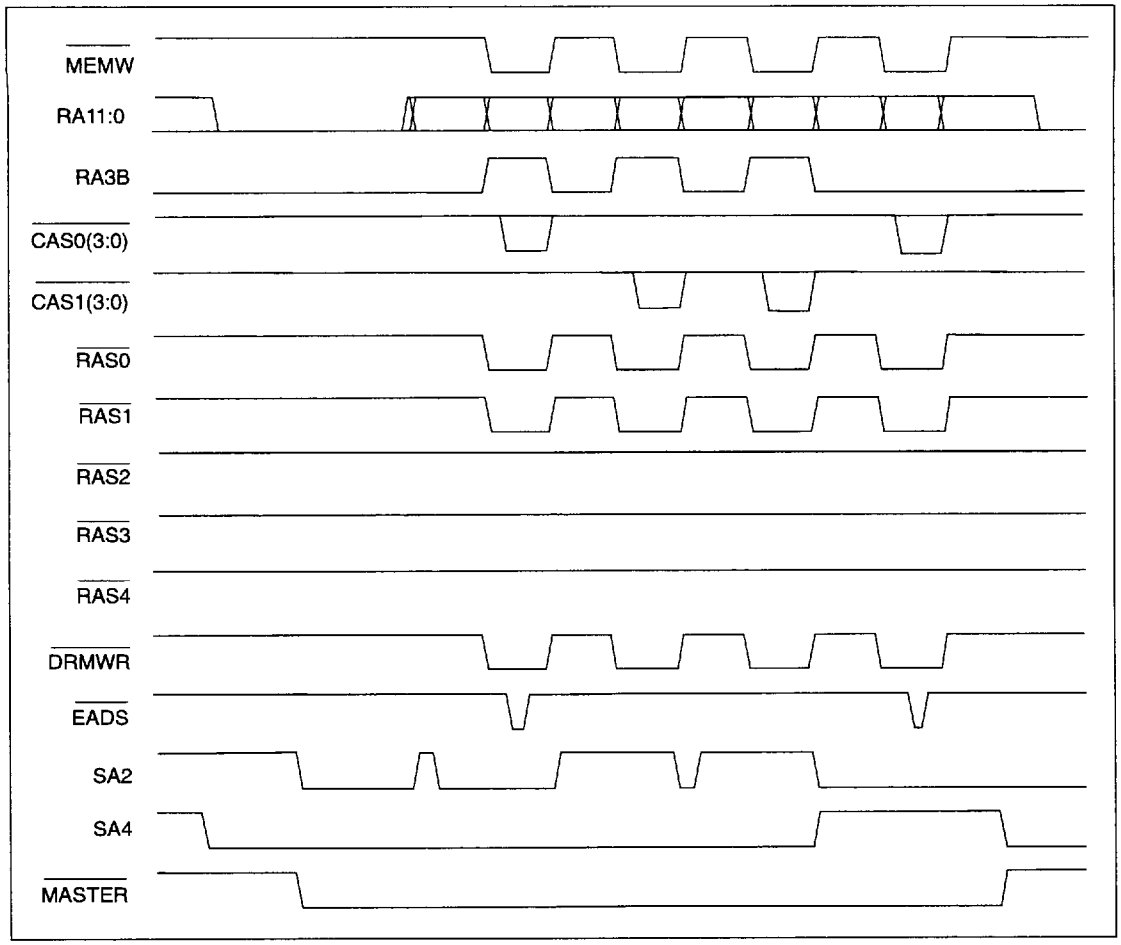


FIGURE 14-34. MULTIPLE BUS MASTER WRITE CYCLE, CACHE INVALIDATION

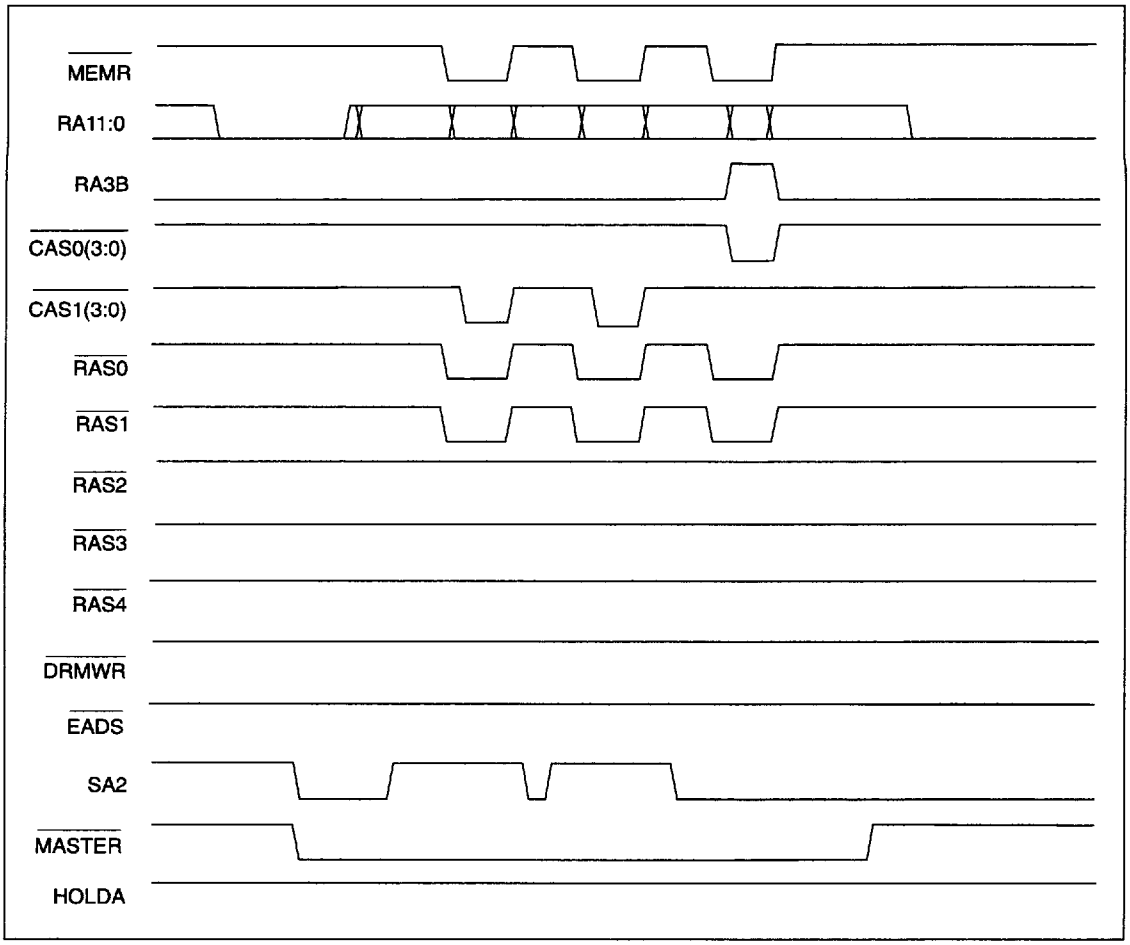


FIGURE 14-35. MULTIPLE BUS MASTER READ CYCLES, INTERLEAVE ON

14.3 PROCESSOR TIMING

This section covers the 5 volt and 3.3 volt WD8110/LV timing parameters for the 80486 CPU.

SYMBOL	CHARACTERISTICS	25 MHz		33 MHz		
		MIN	MAX	MIN	MAX	UNITS
T451	CPUCLK rise to CPURES rise delay		17		15	ns
T452	CPUCLK rise to CPURES fall delay		11		9	ns
T453	CPUCLK rise to NPRST rise delay		17		15	ns
T454	CPUCLK rise to NPRST fall delay		11		9	ns
T455	$\overline{\text{RDYIN}}$ setup time to CPUCLK rise	12		9		ns
T456	$\overline{\text{PCHK486}}$ setup time to CPUCLK rise	12		8		ns
T457	$\overline{\text{BLAST}}$ setup time to CPUCLK rise	12		9		ns
T462	$\overline{\text{ADS}}$ setup time to CPUCLK rise	21		14		ns
T463	$\overline{\text{ADS}}$ hold time from CPUCLK rise	3		3		ns
T464	W/$\overline{\text{R}}$ setup time to CPUCLK rise	21		14		ns
T465	W/$\overline{\text{R}}$ hold time from CPUCLK rise	3		3		ns
T466	D/$\overline{\text{C}}$ setup time to CPUCLK rise	21		14		ns
T467	D/$\overline{\text{C}}$ hold time from CPUCLK rise	3		3		ns
T468	M/$\overline{\text{IO}}$ setup time to CPUCLK rise	21		14		ns
T469	M/$\overline{\text{IO}}$ hold time from CPUCLK rise	3		3		ns
T472	HOLDA setup time to CPUCLK rise	21				
T473	HOLDA hold time from CPUCLK rise	3				
T474	HOLDR valid delay from CPUCLK rise		25		20	
T477	D(31:00) setup time to CPUCLK rise					
T478	D(31:00) hold time from CPUCLK rise					
T479	A(31:2), BE(3:0) setup time to CPUCLK fall in T2 state	15		10		ns
T480	LDS32 setup time with CPUCLK rise in T2 state	15		10		ns

TABLE 14-8. CPU TIMING

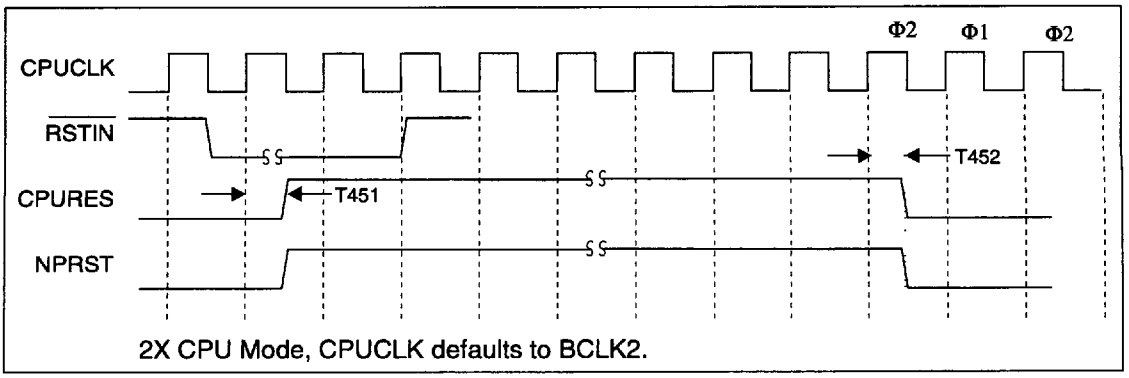


FIGURE 14-36. CPURES AND NPRST DURING POWER UP - 2X CPU MODE

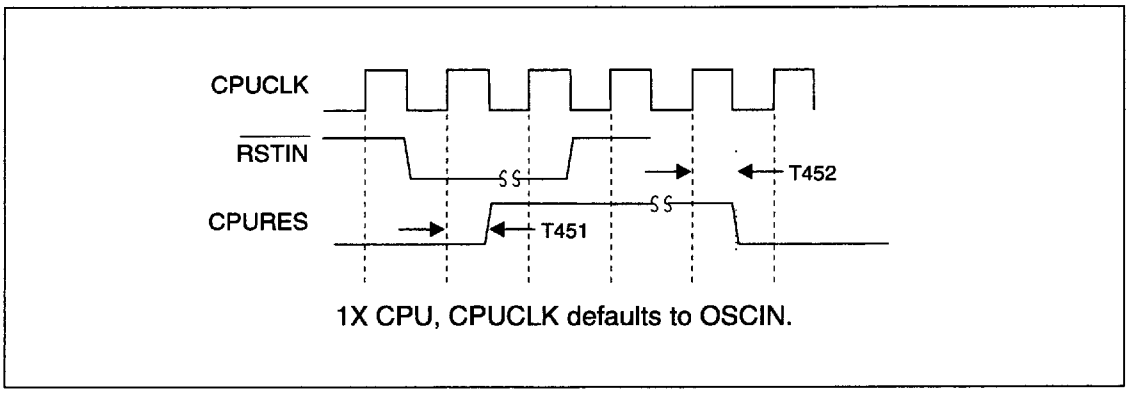
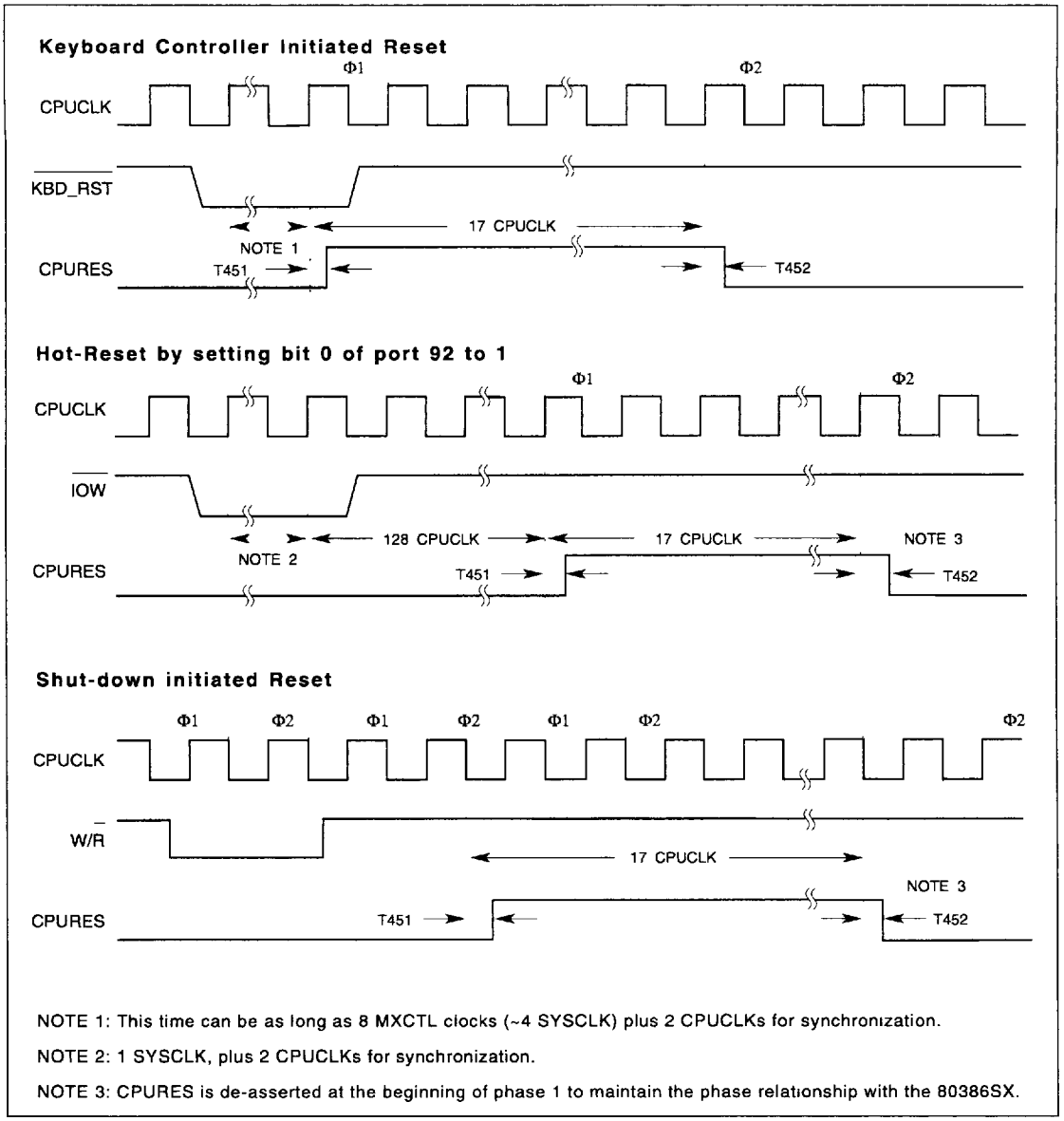


FIGURE 14-37. CPURES AND NPRST DURING POWER UP - 1X CPU MODE



NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is de-asserted at the beginning of phase 1 to maintain the phase relationship with the 80386SX.

FIGURE 14-38. PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET

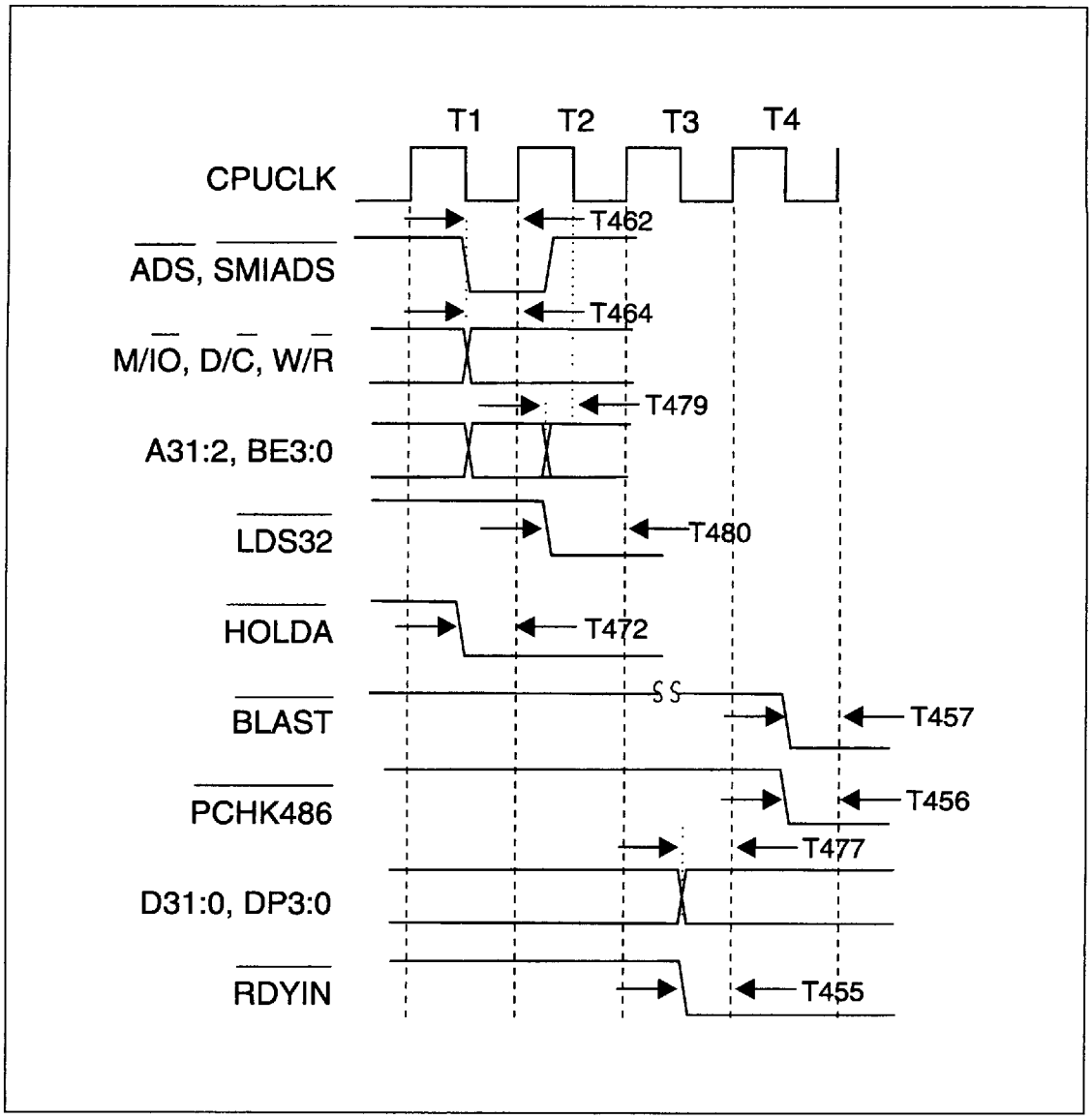
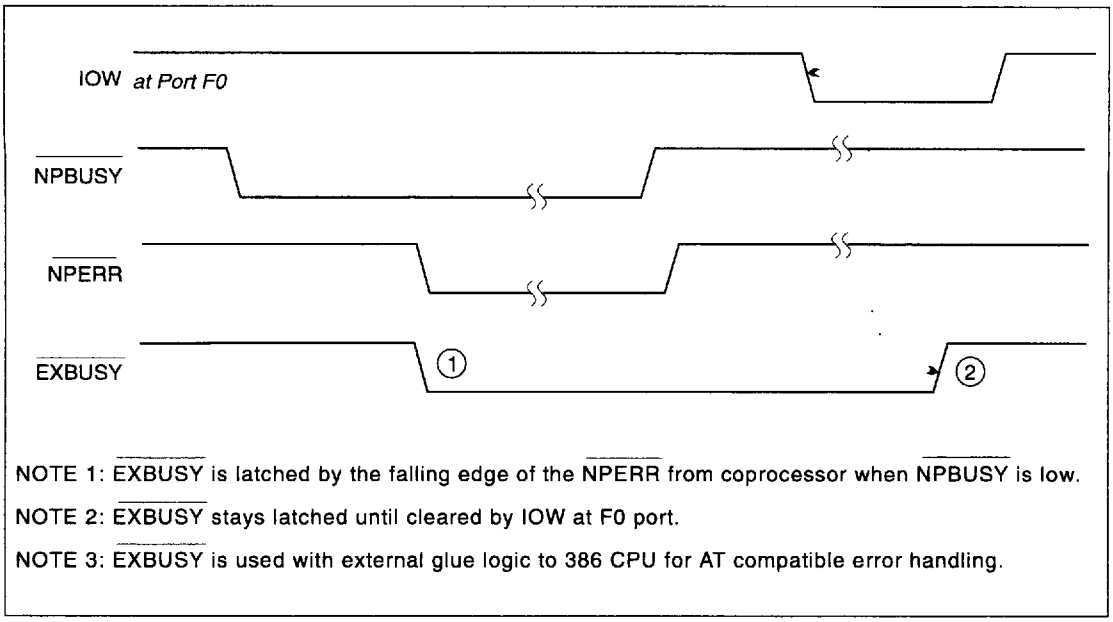


FIGURE 14-39. BUSYCPU ASSERTION DURING COPROCESSOR ACCESS



NOTE 1: $\overline{\text{EXBUSY}}$ is latched by the falling edge of the $\overline{\text{NPERR}}$ from coprocessor when $\overline{\text{NPBUSY}}$ is low.

NOTE 2: $\overline{\text{EXBUSY}}$ stays latched until cleared by IOW at F0 port.

NOTE 3: $\overline{\text{EXBUSY}}$ is used with external glue logic to 386 CPU for AT compatible error handling.

FIGURE 14-40. LATCHING $\overline{\text{BUSYCPU}}$ WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
T350	$\overline{SMIADS}$ setup time to CPUCLK rise	10		ns
T351	CPUCLK rise to $\overline{SMI}$ low output delay		25	ns
T352	CPUCLK rise to $\overline{NA}$ output delay		15	ns
T353	CPUCLK rise to $\overline{SMIRDY}$ output delay		18	ns

TABLE 14-9. WD8110/LV SMI TIMING

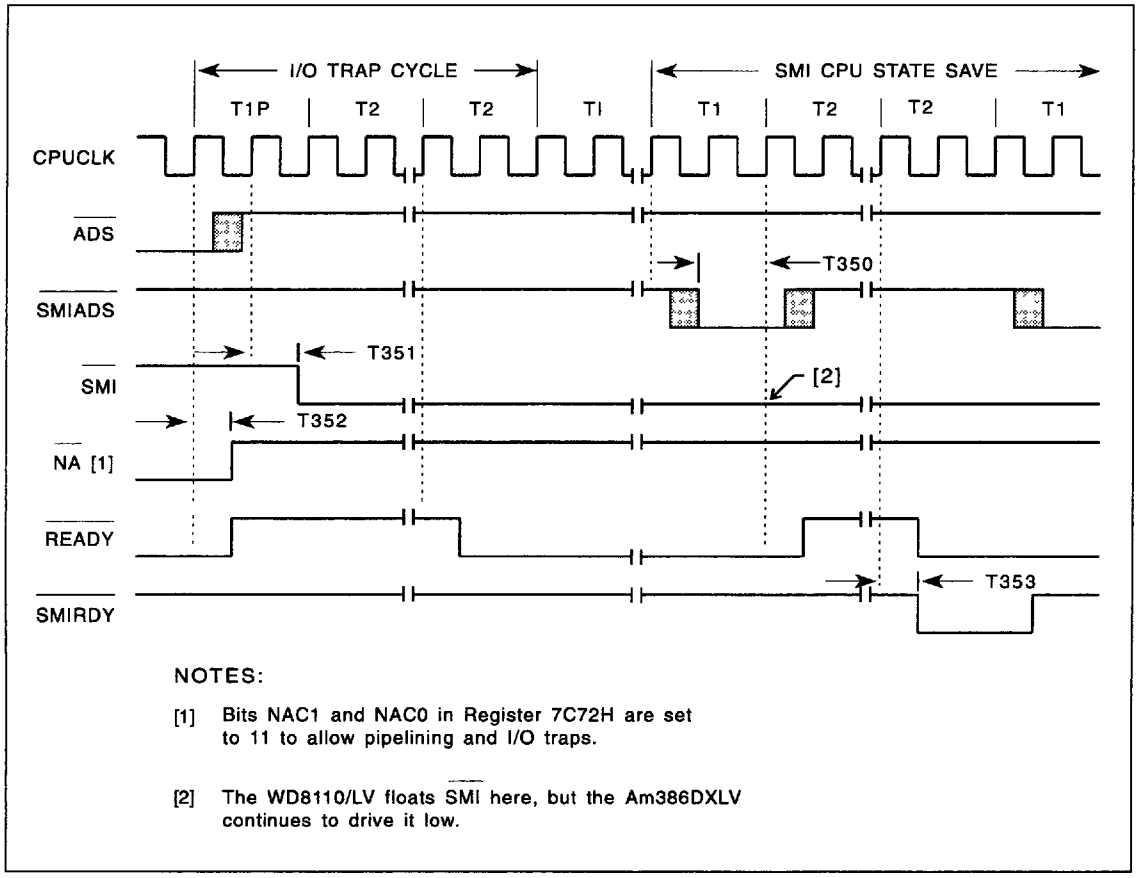


FIGURE 14-41. I/O TRAP CYCLE WITH AM386DXLV

14.4 CLOCK TIMING

CLOCK	VOL	VOH	TH	TL	T	TF	TR
CPUCLK, LBCLK	0.5	V_{DD} - .5	11 ns. min.	11 ns. min.		3 ns. max.	3 ns. max.
SYSCLK			T÷2-4 ns. min.		100 ns. min.		

TABLE 14-10. OUTPUT CLOCK TIMING FOR 1X33 MHz

CLOCK	VOL	VOH	TH	TL	T	TF	TR
CPUCLK, LBCLK	0.5	V_{DD} - .5	6 ns. min.	6 ns. min.		3 ns. max.	3 ns. max.
SYSCLK			T÷2-4 ns. min.		100 ns. min.		

TABLE 14-11. OUTPUT CLOCK TIMING FOR 2X66 MHz

CLOCK	VOL	VOH	SYMMETRY	TF	TR
BCLK2, OSCIN	0.4	2.4	40/60% measured at 1.4V	5 ns. max.	5 ns. max.

TABLE 14-12. INPUT CLOCK TIMING

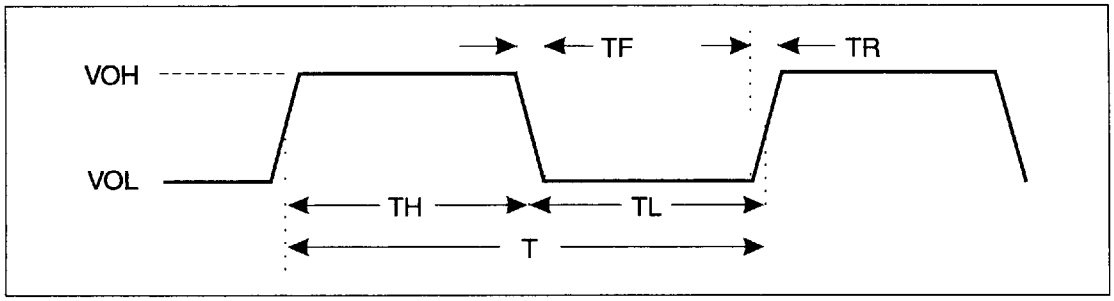


FIGURE 14-42. CLOCK TIMING

15.0 PIN STATES DURING CHIP RESET, SUSPEND AND CPU POWER DOWN

PIN NUMBER	SIGNAL NAME	RESET STATE	PROCESSOR POWER DOWN Input	PROCESSOR POWER DOWN Output	FULL POWER DOWN Input	FULL POWER DOWN Output
		INITIALIZATION AND CLOCKING				
23	CLK14	Input	I		I	
104	BCLK2	Input	I		IH	
105	OSCIN	Input	I		IH	
107	LBCLK	Output		Z		Z
198	$\overline{\text{RSTIN}}$	Input	I		I	
		AT BUS				
1	AEN	Low		O		Z
2	BALE	Low		O		Z
3	SYSCLK	Low		O		Z
4	$\overline{\text{LOWMEG}}$	Output		O		Z
5	SD15	Input	I	O	IL	Z
6	SD14	Input	I	O	IL	Z
7	SD13	Input	I	O	IL	Z
8	SD12	Input	I	O	IL	Z
9	SD11	Input	I	O	IL	Z
10	SD10	Input	I	O	IL	Z
11	SD9	Input	I	O	IL	Z
12	SD8	Input	I	O	IL	Z
13	SD7	Input	I	O	IL	Z
15	SD6	Input	I	O	IL	Z
16	SD5	Input	I	O	IL	Z
18	SD4	Input	I	O	IL	Z
19	SD3	Input	I	O	IL	Z
20	SD2	Input	I	O	IL	Z
21	SD1	Input	I	O	IL	Z
22	SD0	Input	I	O	IL	Z

IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

TABLE 15-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD.

PIN NUMBER	SIGNAL NAME	RESET STATE	PROCESSOR POWER DOWN Input	PROCESSOR POWER DOWN Output	FULL POWER DOWN Input	FULL POWER DOWN Output
		AT BUS Continued				
31	DRQ7	Input	I		IL	
32	DRQ6	Input	I		IL	
33	DRQ5	Input	I		IL	
34	DRQ3	Input	I		IL	
35	DRQ2	Input	I		IL	
36	DRQ1	Input	I		IL	
38	DRQ0	Input	I		IL	
39	$\overline{\text{SMEMW}}$	②	I	O	IH	Z
24	$\overline{\text{MASTER}}$ ③	Input	I		IH	
25	$\overline{\text{IOCK}}$ ③	Input	I		IH	
26	IOCHRDY ③	Input	I		IH	
27	$\overline{\text{ZEROWS}}$ ③	Input	I		IH	
29	$\overline{\text{MEMCS16}}$ ③	Input	I		IH	
30	$\overline{\text{IOCS16}}$ ③	Input	I		IH	
40	$\overline{\text{REFRESH}}$ ③	High	I	O	IH	O
42	$\overline{\text{SBHE}}$ ③	High	I	O	IH	Z
43	LA20	Output ①	I	O	IH	Z
44	$\overline{\text{IOW}}$ ③	High ①	I	O	IH	Z
45	$\overline{\text{IOR}}$ ③	High ①	I	O	IH	Z
46	$\overline{\text{MEMW}}$ ③	High ①	I	O	IH	Z
47	$\overline{\text{MEMR}}$ ③	High ①	I	O	IH	Z
48	SA1	Output ①	I	O	IH	Z
49	SA0	Output ①	I	O	IH	Z
153	$\overline{\text{CSEN}}$	④ Low		O		O
154	MXCTL0	Low		O		O
155	MXCTL1	Low		O		O
156	MXCTL2	High		O		O

① This pin is tristated if master = 0. For test purposes, if MASTER is asserted, outputs are tristated and the pins become inputs.
② High if Weitek Mode is not selected. Input if Weitek Mode is selected.
③ Internal 50 Kohm pullup, disabled in power-down mode.
④ Strap option input sensed while $\overline{\text{RSTIN}}$ active, then becomes an output.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

TABLE 15-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)

PIN NUMBER	SIGNAL NAME	RESET STATE	PROCESSOR POWER DOWN Input	PROCESSOR POWER DOWN Output	FULL POWER DOWN Input	FULL POWER DOWN Output
		AT BUS Continued				
193	IRQSET0	Input	I		IH	
195	IRQSET1	Input	I		IH	
200	SPKR	Low		O		O
208	DACKEN	High		O		O
		MAIN PROCESSOR CONTROL				
101	$\overline{\text{SMIRDY}}$	④ High	IH	Z	IH	Z
102	$\overline{\text{SMI}}$ ③	Input	IH	Z	IH	Z
125	$\overline{\text{ADS}}$ ③	Input	IH		IH	
196	$\overline{\text{SMIADS}}$ ③	Input	IH		IH	
52	NMI	Low		Z		Z
54	INTRQ	Output		Z		Z
55	A31 ⑦	⑤	IL	Z	IL	Z
56	A29 ⑦	⑥	IL	Z	IL	Z
57	A27 ⑦	⑤	IL	Z	IL	Z
58	A26 ⑦	Input	IL	Z	IL	Z
59	A25 ⑦	Input	IL	Z	IL	Z
60	A24 ⑦	Input	IL	Z	IL	Z
61	A23 ⑦	Input	IL	Z	IL	Z
62	A22 ⑦	Input	IL	Z	IL	Z
63	A21 ⑦	Input	IL	Z	IL	Z
64	A20 ⑦	Input	IL	Z	IL	Z
65	A19 ⑦	Input	IL	Z	IL	Z
67	A18 ⑦	Input	IL	Z	IL	Z
68	A17 ⑦	Input	IL	Z	IL	Z

③ Internal 50 kohm pullup, disabled in power-down mode.
④ Strap option input sensed while $\overline{\text{RSTIN}}$ active, then becomes an output.
⑤ Inputs when not in 80386SX mode (pin 55 = A31, pin 57 = A27). Outputs in 80386SX mode (pin 55 = $\overline{\text{SXLOWEN}}$, pin 57 = $\overline{\text{SXSWPEN}}$).
⑥ Input when in Weitek mode (A29). High output when not in Weitek mode ($\overline{\text{STP\_REQ}}$).
⑦ 100 Kohm pulldown resistors are turned on when the processor is in power-down or suspend mode to prevent the data bus or address bus from floating. In normal operation these pull down resistors are turned off.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

TABLE 15-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)

PIN NUMBER	SIGNAL NAME	RESET STATE	PROCESSOR POWER DOWN Input	PROCESSOR POWER DOWN Output	FULL POWER DOWN Input	FULL POWER DOWN Output
	MAIN PROCESSOR CONTROL Continued					
69	A16 ⑦	Input	IL	Z	IL	Z
70	A15 ⑦	Input	IL	Z	IL	Z
72	A14 ⑦	Input	IL	Z	IL	Z
73	A13 ⑦	Input	IL	Z	IL	Z
74	A12 ⑦	Input	IL	Z	IL	Z
75	A11 ⑦	Input	IL	Z	IL	Z
76	A10 ⑦	Input	IL	Z	IL	Z
77	A9 ⑦	Input	IL	Z	IL	Z
78	A8 ⑦	Input	IL	Z	IL	Z
79	A7 ⑦	Input	IL	Z	IL	Z
81	A6 ⑦	Input	IL	Z	IL	Z
82	A5 ⑦	Input	IL	Z	IL	Z
83	A4 ⑦	Input	IL	Z	IL	Z
84	A3 ⑦	Input	IL	Z	IL	Z
85	A2 ⑦	Input	IL	Z	IL	Z
87	$\overline{BE3}$	Input	IH		IH	
89	$\overline{BE2}$	Input	IH		IH	
90	$\overline{BE1}$	Input	IH		IH	
91	$\overline{BE0}$	Input	IH		IH	
93	$\overline{BRDY486}$	High		Z		Z
99	CPURES ③	High		Z		Z
106	CPUCLK	Output	IL	Z	IL	Z
108	$\overline{EADS}$	④ Output		Z		Z
126	W/$\overline{R}$ ③	Input	IH		IH	
127	D/$\overline{C}$ ③	Input	IH		IH	
128	M/$\overline{IO}$ ③	Input	IL		IL	

③ Internal 50 kohm pullup, disabled in power-down mode.
④ Strap option input sensed while $\overline{RSTIN}$ active, then becomes an output.
⑦ 100 Kohm pulldown resistors are turned on when the processor is in power-down or suspend mode to prevent the data bus or address bus from floating. In normal operation these pull down resistors are turned off.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

TABLE 15-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)

PIN NUMBER	SIGNAL NAME	RESET STATE	PROCESSOR POWER DOWN Input	PROCESSOR POWER DOWN Output	FULL POWER DOWN Input	FULL POWER DOWN Output
		MAIN PROCESSOR CONTROL Continued				
133	$\overline{\text{SUSPA}}$	Input	IH		IH	
134	PCHK486	Input	IL		IL	
135	$\overline{\text{BLAST}}$	Input	IL		IL	
152	$\overline{\text{RDY486}}$	High		Z		Z
197	HOLDA	Input	IL		IL	
199	HOLDR	Low		Z		Z
103	$\overline{\text{KEN}}$	④ Output		Z		Z
151	A20GT	④ High		Z		Z
207	$\overline{\text{BS16}}$	High		Z		Z
		NUMERIC PROCESSOR CONTROL				
92	$\overline{\text{NPERR}}$ ③	Input	IH		IH	
94	$\overline{\text{NPBUSY}}$	⑧	IH	⑨	IH	Z
100	NPRST ③	High		Z		Z
		DRAM MEMORY				
50	$\overline{\text{MDEN}}$	High		O		Z
51	MDIR	Low		O		Z
53	$\overline{\text{DRMWR}}$	High		O		O
110	$\overline{\text{RAS0}}$	High		O		O
111	$\overline{\text{RAS1}}$	High		O		O
112	$\overline{\text{RAS2}}$	High		O		O
113	$\overline{\text{RAS3}}$	High		O		O
114	$\overline{\text{RAS4}}$	High		O		O
115	$\overline{\text{CAS03}}$	High		O		O
116	$\overline{\text{CAS02}}$	High		O		O
118	$\overline{\text{CAS01}}$	High		O		O
119	$\overline{\text{CAS00}}$	High		O		O

③ Internal 50 kohm pullup, disabled in power-down mode.
④ Strap option input sensed while $\overline{\text{RSTIN}}$ active, then becomes an output.
⑧ Input if external coprocessor mode is selected by pin 108 strap option. High if external coprocessor mode is not selected.
⑨ Z if external coprocessor mode is selected by pin 108 strap option. O if external coprocessor mode is not selected.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

TABLE 15-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)

PIN NUMBER	SIGNAL NAME	RESET STATE	PROCESSOR POWER DOWN Input	PROCESSOR POWER DOWN Output	FULL POWER DOWN Input	FULL POWER DOWN Output
		DRAM MEMORY Continued				
121	$\overline{CAS13}$	High		O		O
122	$\overline{CAS12}$	High		O		O
123	$\overline{CAS11}$	High		O		O
124	$\overline{CAS10}$	High		O		O
136	RA0/ED0	Output	I	O	I	O
137	RA1/ED1	Output	I	O	I	O
138	RA2/ED2	Output	I	O	I	O
140	RA3A/CS3	Output		O		O
141	RA3B/CS4	Output		O		O
142	RA4/ED3	Output	I	O	I	O
143	RA5/ED4	Output	I	O	I	O
144	RA6/ED5	Output	I	O	I	O
145	RA7/ED6	Output	I	O	I	O
147	RA8/ED7	Output	I	O	I	O
148	RA9/CS0	Output		O		O
149	RA10/CS1	Output		O		O
150	RA11/CS2	Output		O		O
		DATA BUS				
86	$\overline{RDYIN}$	Input	IL		IL	
130	$\overline{LDS32}$ ③	Input	I		IH	
157	D0 ⑦	Input	IL	Z	IL	Z
158	D1 ⑦	Input	IL	Z	IL	Z
159	D2 ⑦	Input	IL	Z	IL	Z
160	D3 ⑦	Input	IL	Z	IL	Z
161	D4 ⑦	Input	IL	Z	IL	Z
162	D5 ⑦	Input	IL	Z	IL	Z
163	D6 ⑦	Input	IL	Z	IL	Z

③ Internal 50 kohm pullup, disabled in power-down mode.
⑦ 100 Kohm pulldown resistors are turned on when the processor is in power-down or suspend mode to prevent the data bus or address bus from floating. In normal operation these pull down resistors are turned off.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

TABLE 15-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)

PIN NUMBER	SIGNAL NAME	RESET STATE	PROCESSOR POWER DOWN		FULL POWER DOWN	
			Input	Output	Input	Output
		DATA BUS Continued				
164	D7 ⑦	Input	IL	Z	IL	Z
165	D8 ⑦	Input	IL	Z	IL	Z
167	D9 ⑦	Input	IL	Z	IL	Z
168	D10 ⑦	Input	IL	Z	IL	Z
169	D11 ⑦	Input	IL	Z	IL	Z
170	D12 ⑦	Input	IL	Z	IL	Z
171	D13 ⑦	Input	IL	Z	IL	Z
172	D14 ⑦	Input	IL	Z	IL	Z
174	D15 ⑦	Input	IL	Z	IL	Z
175	D16 ⑦	Input	IL	Z	IL	Z
176	D17 ⑦	Input	IL	Z	IL	Z
177	D18 ⑦	Input	IL	Z	IL	Z
178	D19 ⑦	Input	IL	Z	IL	Z
179	D20 ⑦	Input	IL	Z	IL	Z
180	D21 ⑦	Input	IL	Z	IL	Z
181	D22 ⑦	Input	IL	Z	IL	Z
182	D23 ⑦	Input	IL	Z	IL	Z
183	D24 ⑦	Input	IL	Z	IL	Z
185	D25 ⑦	Input	IL	Z	IL	Z
186	D26 ⑦	Input	IL	Z	IL	Z
187	D27 ⑦	Input	IL	Z	IL	Z
188	D28 ⑦	Input	IL	Z	IL	Z
189	D29 ⑦	Input	IL	Z	IL	Z
191	D30 ⑦	Input	IL	Z	IL	Z
192	D31 ⑦	Input	IL	Z	IL	Z

⑦ 100 Kohm pulldown resistors are turned on when the processor is in power-down or suspend mode to prevent the data bus or address bus from floating. In normal operation these pull down resistors are turned off.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

TABLE 15-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)

PIN NUMBER	SIGNAL NAME	RESET STATE	PROCESSOR POWER DOWN Input	PROCESSOR POWER DOWN Output	FULL POWER DOWN Input	FULL POWER DOWN Output
		DATA BUS Continued				
201	DP0	Input	IH	Z	IH	Z
203	DP1	Input	IH	Z	IH	Z
204	DP2	Input	IH	Z	IH	Z
205	DP3	Input	IH	Z	IH	Z
		POWER MANAGEMENT CONTROL				
129	PDREF ③	Input	I		I	
132	PMCIN	Input	I		I	
		MISCELLANEOUS				
96	ROMBA16 ④	Output		O		Z
97	ROMBA17 ④	Output		O		Z
98	ROMBA18 ④	Output		O		Z
206	$\overline{\text{EXBUSY}}$	High		⑩		Z

③ Internal 50 kohm pullup, disabled in power-down mode.
④ Strap option input sesned while $\overline{\text{RSTIN}}$ active, then becomes an output.
⑩ Z if pin 206 is selected as $\overline{\text{EXBUSY}}$.
O if pin 206 is selected as $\overline{\text{GPREGRD}}$.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

TABLE 15-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)

Pin Number	Signal Name
14	VSS
28	VSS
41	VSS
66	VSS
80	VSS
95	VSS
109	VSS
117	VSS
131	VSS
146	VSS
166	VSS
181	VSS
194	VSS
202	VSS
17	VDD5
37	VDD5
71	VDD3
88	VDD3
120	VDD3
139	VDD3
173	VDD3
190	VDD3

TABLE 15-2. POWER AND GROUND

16.0 I/O PIN MAPPING AND ASSIGNMENT

WD8110/LV provides in-circuit testability. During testing, all pins will follow the mapped connection shown in Table 16-1 and Figure 16-1 when I/O Pin Mapping Mode is activated. By providing the input levels, it is possible to check in-circuit shorts and opens at chip or board level.

To activate the I/O Pin Mapping Mode:

While MASTER, MEMR, MEMW and A2 are asserted and A3 de-asserted, assert RSTIN. The WD8110/LV remains latched in this mode if RSTIN is de-asserted while the above conditions are maintained. MASTER, MEMR, MEMW, A2 and A3 may change state while the WD8110/LV is latched in this mode.

To de-activate the I/O Pin Mapping Mode:

Assert RSTIN while either MEMR, MEMW, MASTER or A2 are de-asserted or A3 is asserted.

All grouped input pins are ORed together.

See Section 10 for more information regarding other diagnostic modes.

INPUT PINS		OUTPUT PINS	
PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
5, 7, 9, 11	SD15, SD13, SD11, SD9	1	AEN
12, 15, 18, 20	SD8, SD6, SD4, SD2	2	BALE
13, 16, 19, 21, 40	SD7, SD5, SD3, SD1, REFRESH	3	SYSCLK
23, 25, 39, 42	CLK14, IOCHK, SMEMW, SBHE	4	LOWMEG
22, 24, 26, 29, 49, 47, 56, 58	SD0, MASTER, IOCHRDY, MEMCS16, SA0, MEMR, A29, A26	52	NMI
27, 30, 32, 34, 36, 46, 44, 51	ZEROWS, IOCS16, DRQ6, DRQ1, MEMW, IOW, MDIR	53	DRMWR
31, 33, 35, 38, 48, 45, 43, 50	DRQ7, DRQ5, DRQ2, DRQ0, SA1, IOR, LA20, MDEN	54	INTRQ
60, 62, 64, 67	A24, A22, A20, A18	93	BRDY486
55, 57, 59, 61, 63, 65, 68, 92	A31, A27, A25, A23, A21, A19, A17, NPERR	99	CPURES
69, 72, 74, 94	A16, A14, A12, GPREGWR	100	NPRST
70, 73, 75, 77	A15, A13, A11, A9	110	RAS0
76, 78, 81, 83	A10, A8, A6, A4	111	RAS1
79, 82, 84, 86	A7, A5, A3, RDYIN	112	RAS2
85, 87, 90, 97	A2, BE3, BE1, ROMBA17	113	RAS3
89, 91, 96, 98	BE2, BE0, ROMBA16, ROMBA18	114	RAS4
101, 103	SMIRDY, KEN	115	CAS03
105	OSCIN	107	LBCLK
102, 104, 106, 108	SMI, BCLK2, CLK486, EADS	116	CAS02
132, 129, 127, 125	PMCIN, PDREF, D/C, ADS	118	CAS01*
133, 130, 128, 126	SUSPA, LDS32, M/IO, W/R	119	CAS00

TABLE 16-1. WD8110/LV PIN SCAN MAP

INPUT PINS		OUTPUT PINS	
PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
142, 137, 135	RA4, RA1, $\overline{\text{BLAST}}$	121	$\overline{\text{CAS13}}$
143, 138, 136, 134	RA5, RA2, RA0, PCHK486	122	$\overline{\text{CAS12}}$
151, 147, 144	A20GT, RA8, RA6	123	$\overline{\text{CAS11}}$
153, 145	$\overline{\text{CSEN}}$, RA5	124	$\overline{\text{CAS10}}$
157, 159, 161, 163	D0, D2, D4, D6	140, 148	RA3A, RA9
158, 160, 162, 164	D1, D3, D5, D7	141, 149	RA3B, RA10
165, 167, 169, 171	D8, D9, D11, D13	152, 150	$\overline{\text{RDY486}}$, RA11
168, 170, 172, 174	D10, D12, D14, D15	154	MXCTL0
175, 177, 179, 182	D16, D18, D20, D22	155	MXCTL1
180, 183, 185, 187	D21, D23, D25, D27	156	MXCTL2
189, 191, 193, 196	D29, D30, IRQSET0, $\overline{\text{SMIADS}}$	199	HOLDR
176, 178, 184, 186	D17, D19, D24, D26	200	SPKR
188, 192, 195, 197	D28, D31, IRQSET1, HOLDA	206	$\overline{\text{EXBUSY}}$
198, 201, 203, 205	$\overline{\text{RSTIN}}$, DP0, DP1, DP3	207	BS16
204, 6, 8, 10	DP2, SD14, SD12, SD10	208	DACKEN

* It is necessary to wait for 100 PDREF (pin 129) clock pulses after latching in IOMAP logic to test pin 118 ($\overline{\text{CAS01}}$).

TABLE 16-1. PIN SCAN MAP (Continued)

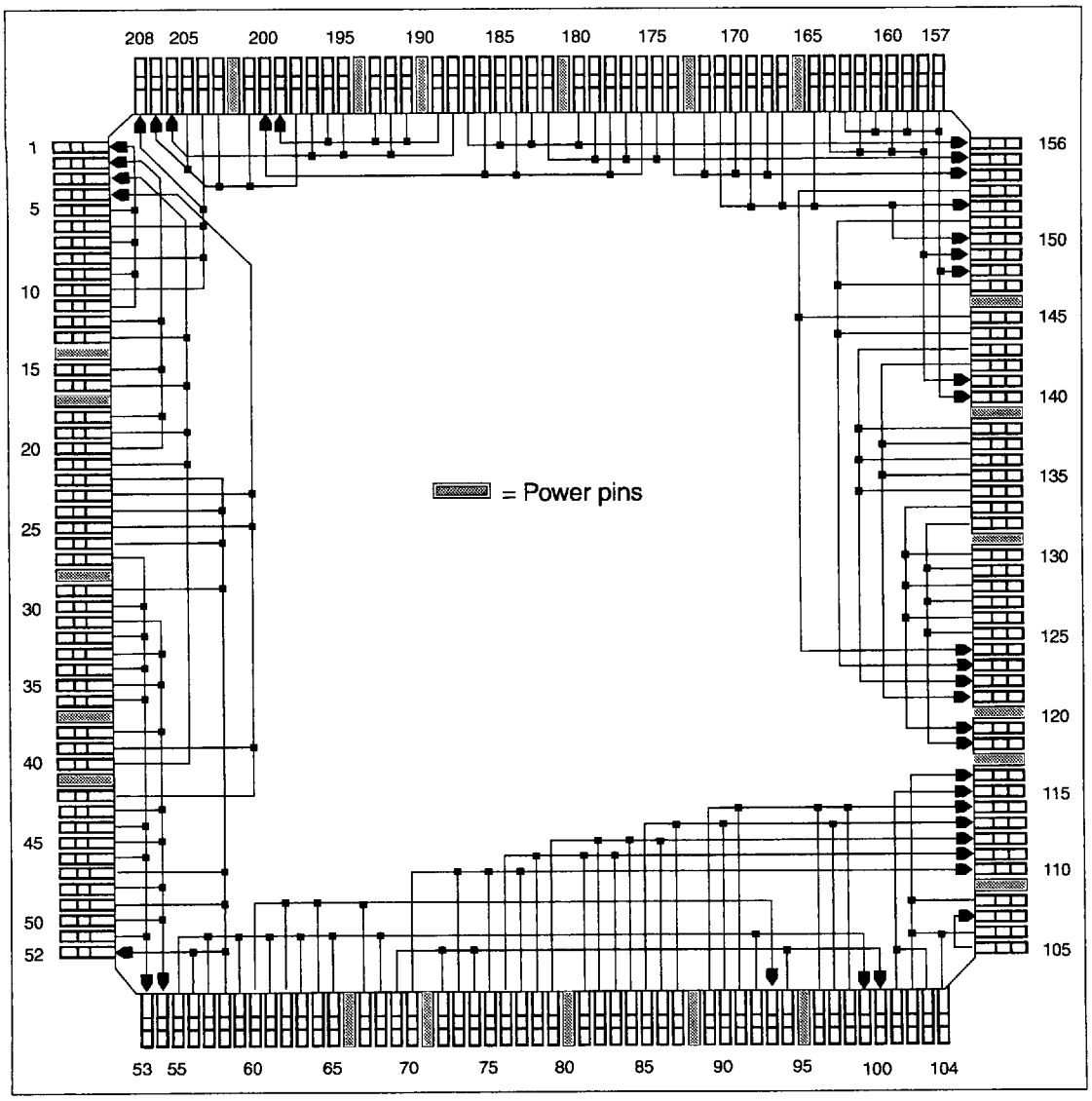


FIGURE 16-1. WD8110/LV PIN SCAN MAP

17.0 PACKAGE DIMENSIONS

Figure 17-1 Illustrates the 208-Pin MQFP package showing the dimensions in inches.

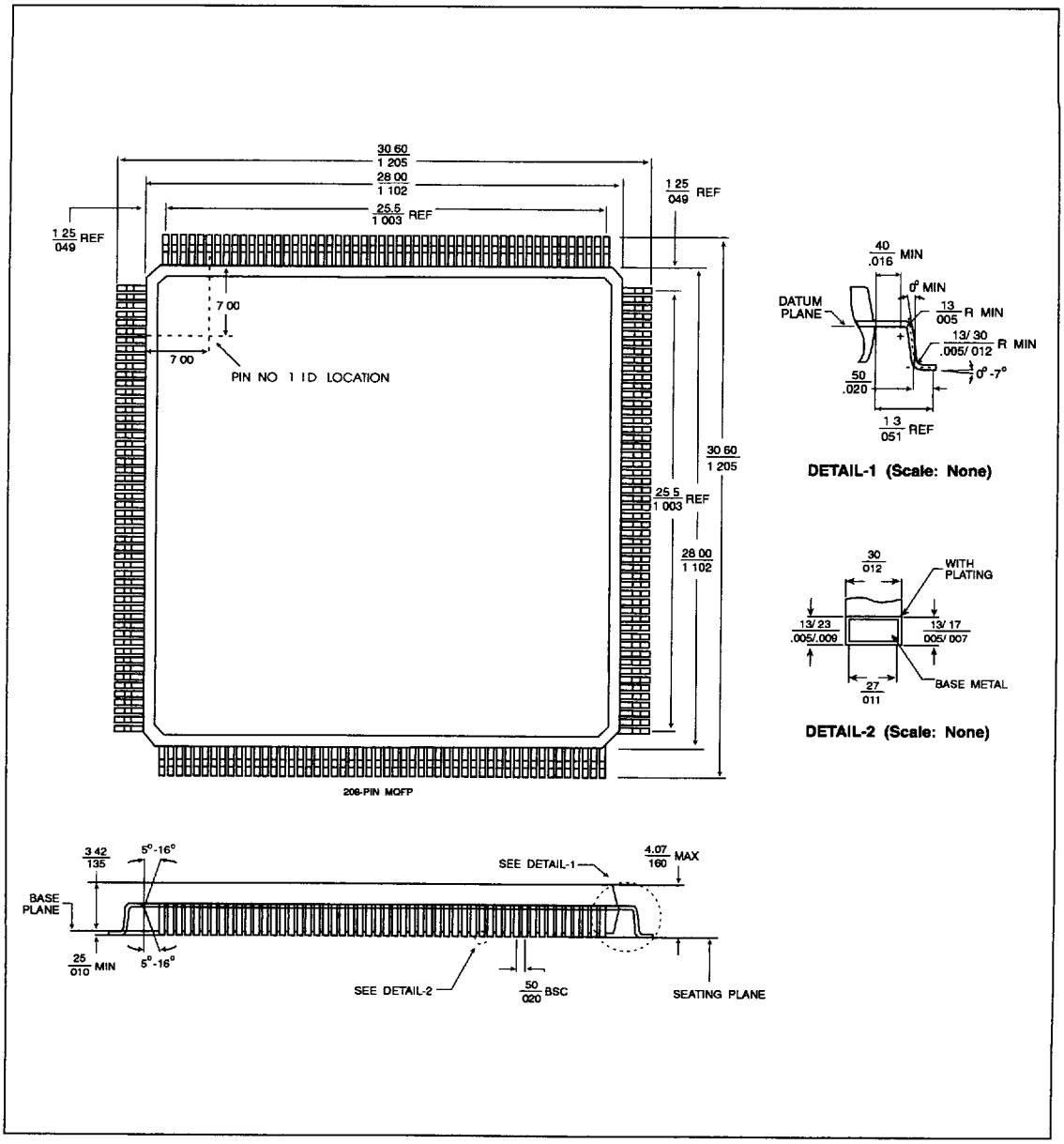


FIGURE 17-1. 208-PIN MQFP PACKAGE DIMENSIONS

APPENDICES

A.0 SPECIAL FEATURE REGISTERS

This section describes the registers peculiar to the special features. Except for Port Addresses F073H and FC72H all Port Addresses described in this section are peculiar to these special features.

A.1 ENABLING THE SPECIAL FEATURES

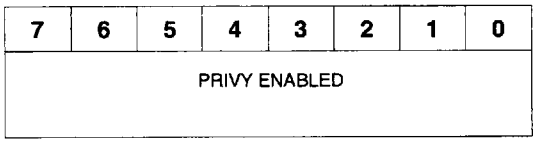
To enable the special features, the WD8110/LV must first be unlocked by writing DAH to the Lock/Unlock Register at Port Address F073H and then writing DA00H to the Lock Status Register at Port Address FC72H. As stated in Section 2.7.1, Port Address FC72H is normally a read only register, but will respond to a write value of DA00H.

These registers are described in detail in Sections 2.7, 2.7.1 and 2.7.2.

A.2 ENABLE PRIVY REGISTER

Port Address 0FBH - Write only

The special features must first be enabled, as described in Section A.1, and then writing any data to this register enables PRIVY.

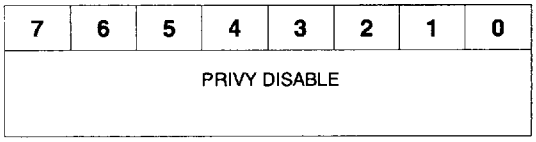


Signal Name	Default At RSTIN
All signals	None

A.3 DISABLE PRIVY REGISTER

Port Address 0F9H - Write only

Writing any data to this register disables PRIVY. When PRIVY is disabled, the 4 KB RAM is treated as the rest of memory in the F000H segment.



Signal Name	Default At RSTIN
All signals	None

A.4 BUSY BYPASS CONTROL REGISTER

Port Address 0ECH - Read and Write

NOTE

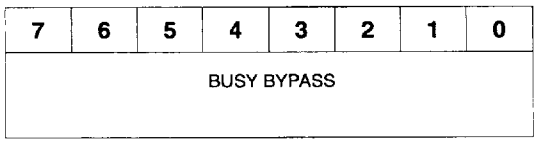
This feature only functions when the WD8110/LV is strapped for 386 mode and does not function when the WD8110/LV is strapped for 486 mode.

Before the Bypass Mode can be enabled or disabled, PRIVY must first be set by writing any data to Port Address 0FBH.

Bypass Mode is enabled by writing any data to Port Address 0ECH.

When the Bypass Mode is enabled, ERROR from the Numeric Processing Unit (NPU) does not cause an IRQ13 and the BUSY signal is not sent to the CPUBUSY output without modification.

Bypass Mode is disabled by reading Port Address 0ECH.



Signal Name	Default At RSTIN
All signals	None

A.5 FAST A20 GATE CONTROL REGISTER

Port Address 0EEH - Read and Write

Before the special feature FAST A20 GATE can be enabled or disabled, PRIVY must first be set by writing any data to Port Address 0FBH.

FAST A20 GATE is enabled by writing any data to Port Address 0EEH.

The special feature FAST A20 GATE is ORed with the A20GT signal from the Keyboard Controller and with Port 92H A20 gate signal.

FAST A20 GATE is disabled by reading Port Address 0EEH.

7	6	5	4	3	2	1	0
Special Feature FAST A20 GATE							

Signal Name	Default At RSTIN
All signals	None

A.6 FAST CPU RESET CONTROL REGISTER

Port Address 0EFH - Read only

Before the FAST CPU RESET can be initiated, PRIVY must be set by writing any data to Port Address 0FBH.

A processor reset is initiated by reading Port Address 0EFH. The processor reset pulse is 16 CPUCLKs. This processor reset signal is ORed with the Hot Reset at Port 092H and with the Keyboard Controller processor reset.

7	6	5	4	3	2	1	0
FAST CPU RESET CONTROL							

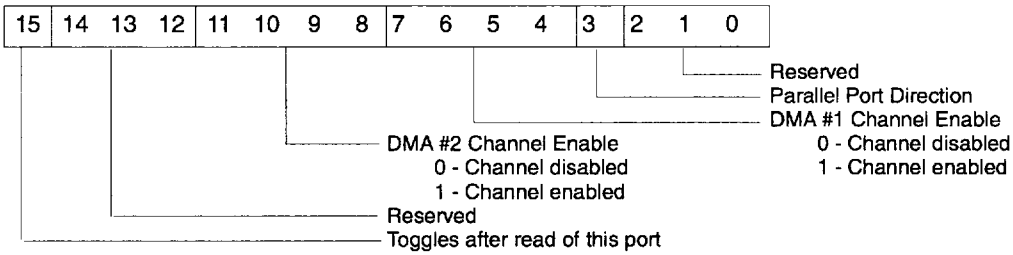
Signal Name	Default At RSTIN
All signals	None

B.0 REGISTER DESCRIPTION QUICK REFERENCE

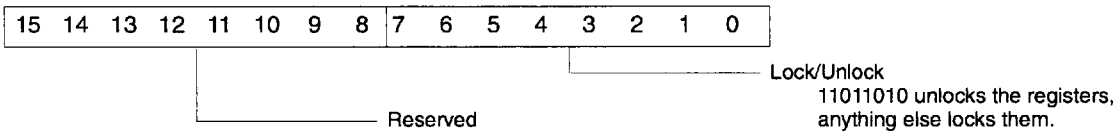
This section provides a brief description of the format and content of the registers within the WD8110/LV. It is assumed that the user is knowledgeable about the register functions and how to apply them. Table B-1 on page 228 lists the registers default setting at reset. An index to the registers in this section is provided on page 231.

B.1 LOCK/UNLOCK

Port Address FC72H - Lock Status Register - Read Only

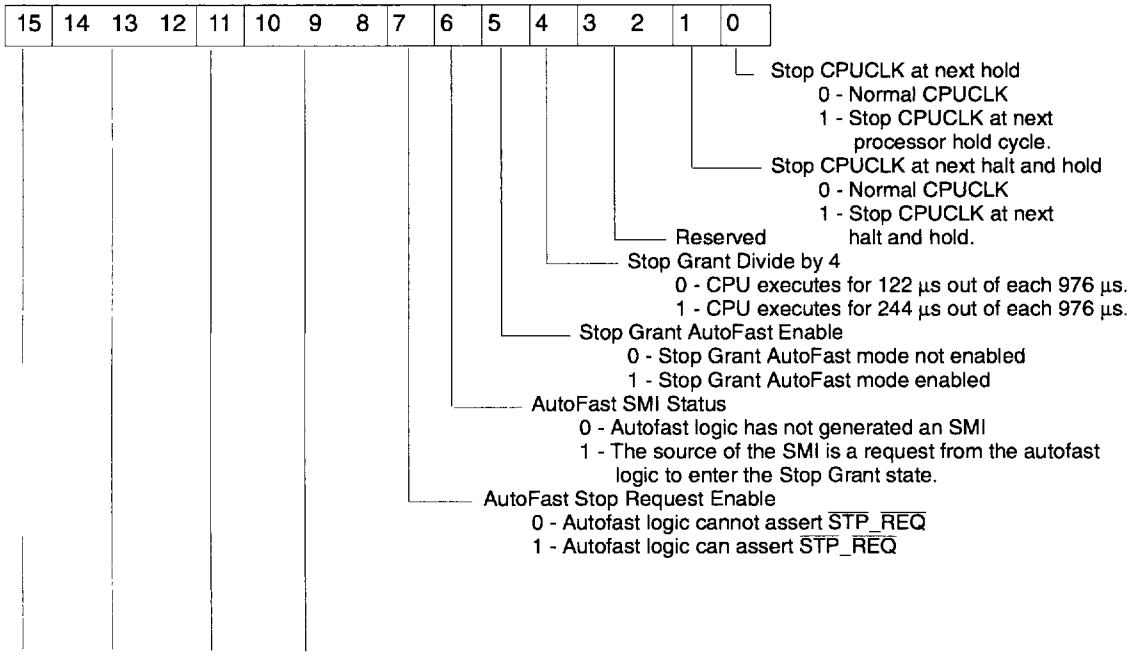


Port Address F073H - Lock/Unlock Register - Write Only



B.2 CLOCK CONTROL

Port Address 1072H - CPU Clock Control Register - Bits 15:8, 6:0 Read and Write, Bit 6 R/W/C



Alternate Clock Speed
- 000 - CPUCLK unchanged
- 001 - Equals source
- 010 - Source ÷ 2
- 011 - Source ÷ 4, 25% duty cycle
- 100 - Source ÷ 4, 75% duty cycle
- 101 - Source ÷ 8, 12% duty cycle
- 110 - Source ÷ 8, 88% duty cycle
- 111 - Source ÷ 64, 98% duty cycle

Auto CPUCLK Speed Switching
- 0 - Auto clock switching disabled
- 1 - Auto clock speed enabled

CPUCLK clock speed
- 000 - Reserved
- 001 - Source ÷ 1
- 010 - Source ÷ 2
- 011 - Source ÷ 4, 25% duty cycle
- 100 - Source ÷ 4, 75% duty cycle
- 101 - Source ÷ 8, 12% duty cycle
- 110 - Source ÷ 8, 88% duty cycle
- 111 - Reserved

CPUCLK clock source
- 0 - BCLK2
- 1 - OSCIN

Port Address 8C72H - Clock Stop/Speed Control Register - Bits 15:10 Read Only, Bits 9:0 Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Alternate IRQ1 source

Alternate IRQ12 source

IRQ1 select
- 0 - Int. sampled by IRQSET1
- 1 - Bit 0 selects source

IRQ12 select
- 0 - Int, sampled by IRQSET1
- 1 - Bit 1 selects source

AT Bus pullup enable
- 0 - Pullup resistors not enabled
- 1 - Pullup resistors enabled

SMI Fast handler execution
- 0 - AUT_FST not affected
- 1 - AUT_FST switches CPUCLK

Enable stop clock handshake
- 0 - Intel, Cyrix mode stop clock control functions disabled
- 1 - Intel, Cyrix mode stop clock control functions enabled

Stop clock control function
- 00 - Intel mode
- 01 - Cyrix mode
- 10 - IBM mode
- 11 - Reserved

Clock Speed Change Delay Enable
- 0 - Clock Speed Change Delay disabled
- 1 - 1 to 2 ms delay is enforced between a speed change in the CPU clock and the deassertion of STP_REQ

3 volt core
- 0 - WD8110 core logic is powered by 5 volts
- 1 - WD8110 core logic is powered by 3.3 volts

3 volt AT buffer
- 0 - AT buffer operates at 5 volts
- 1 - AT buffer operates at 3.3 volts

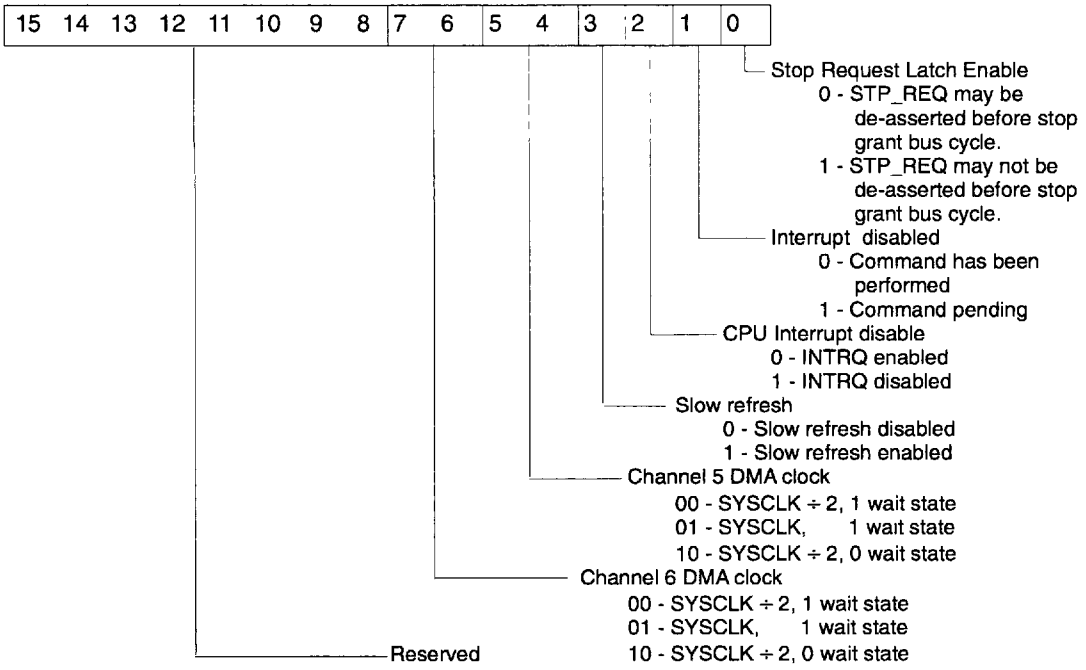
External coprocessor
- 0 - External 80387 is not supported
- 1 - External 80387 is supported

80486SX/DX mode
- 0 - SXM selects between SX and DX
- 1 - $\overline{\text{SXM}}$ is ignored

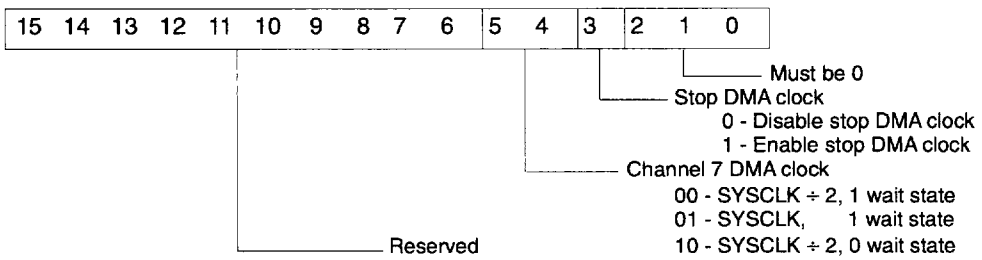
SX Mode
- 0 - 80386DX mode is selected
- 1 - 80386SX mode is selected

Stop clock request polarity
- 0 - STP_REQ is active high
- 1 - STP_REQ is active low

Port Address BC72H - Enhanced DMA Clock Register - Read and Write

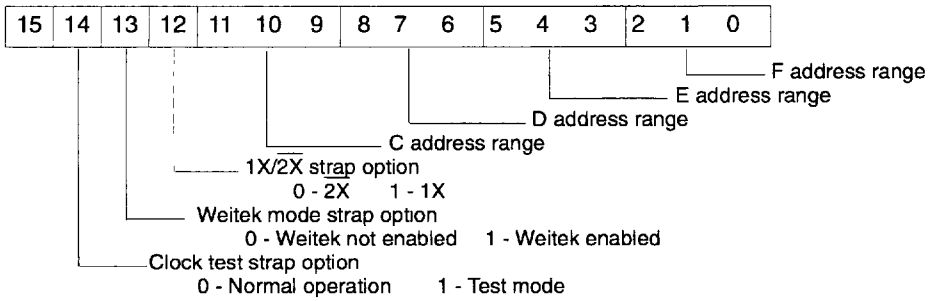


Port Address B472H - Enhanced DMA Clock Register - Read and Write



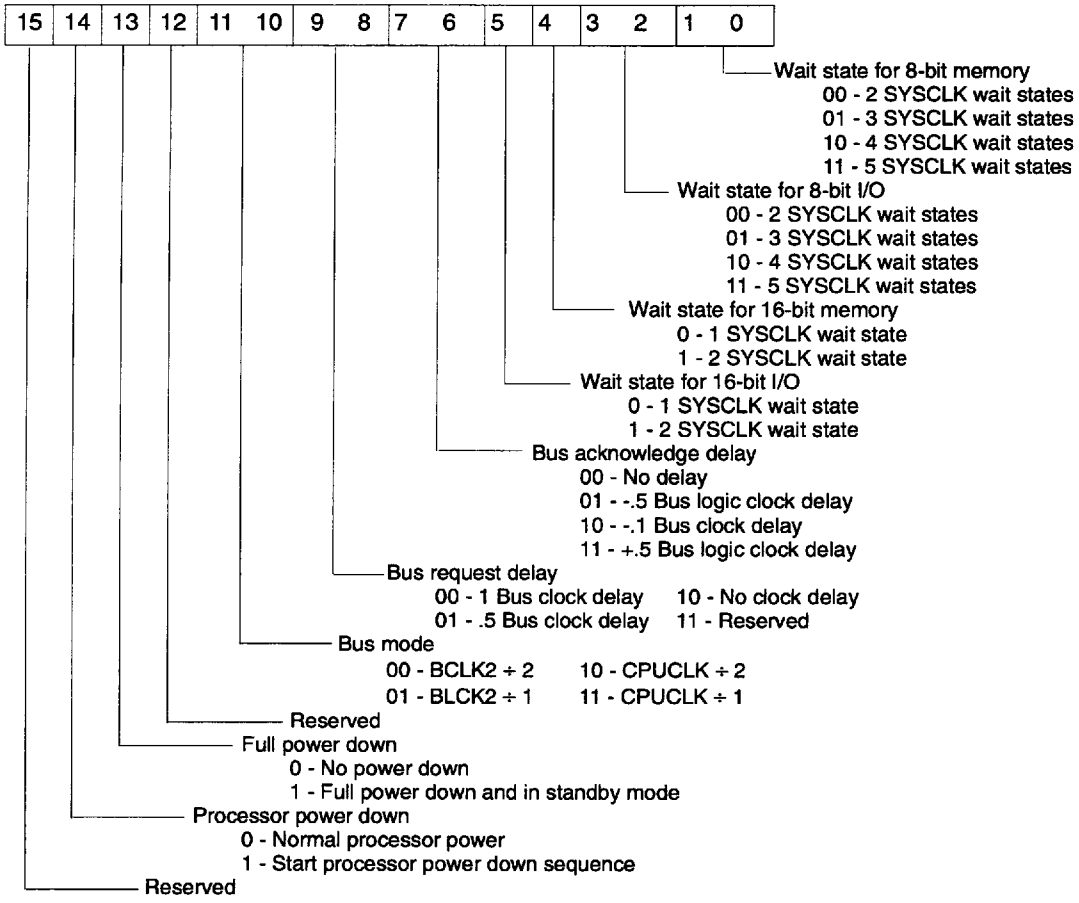
B.3 ROM BANK SELECTION

Port Address C072H - ROM Bank Selection Register - Bits 15:12 Read Only, 11:0 Read and Write



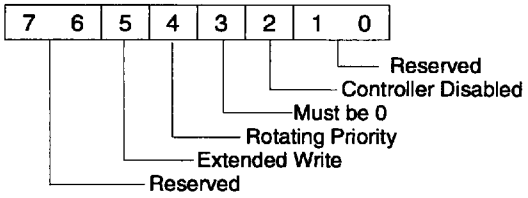
B.4 NUMERIC PROCESSOR

Port Address 1872H - Numeric Processor Busy, Bus Timing, Power Down Register - Read and Write

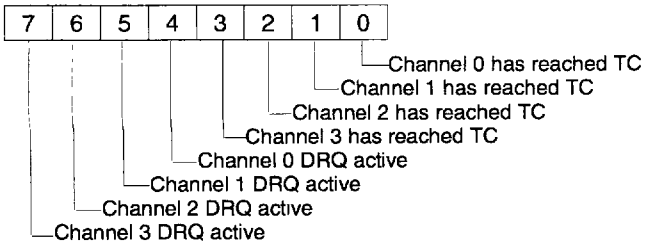


B.5 DMA CONTROL

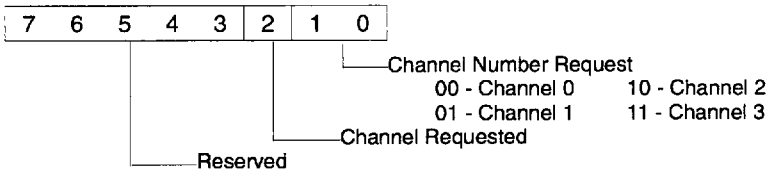
Port Address 008H, 0D0H - Command Register - Write Only



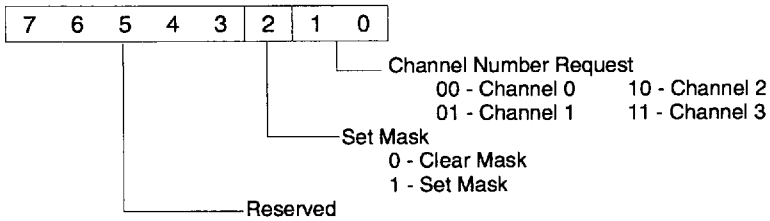
Port Address 008H, 0D0H - Status Register - Read Only



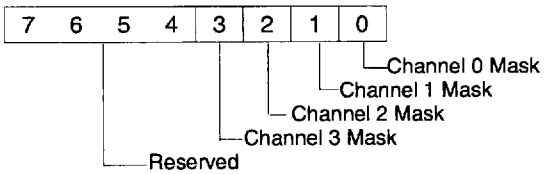
Port Address 009H, 0D2H - Request Register - Write Only



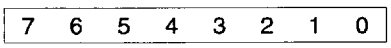
Port Address 00AH, 0D4H - Single Mask Register - Write Only



Port Address 00FH, 0DEH - Mask Multiple Register - Write Only

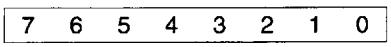


Port Address 00EH, 0DCH - Clear Mask Register - Write Only



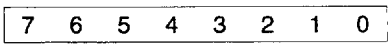
Any data clears all Masks. Data is ignored.

Port Address 00CH, 0D8H - Clear Pointer Register - Write Only



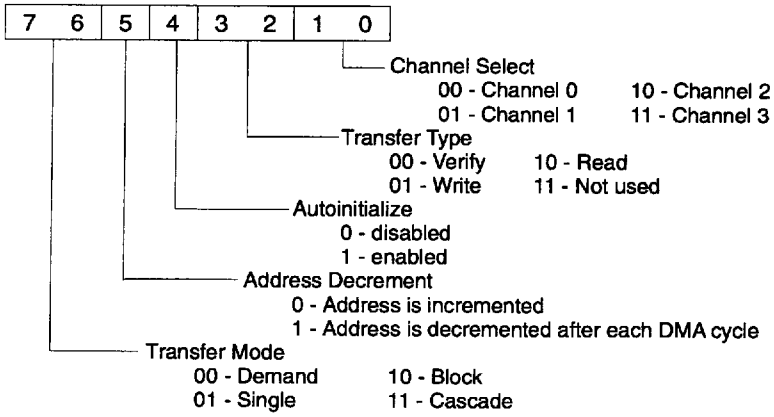
Any data clears the pointer. Data is ignored.

Port Address 00DH, 0DAH - Master Clear Register - Write Only

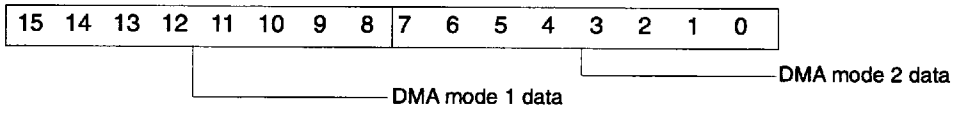


Any data performs a master clear. Data is ignored.

Port Address 00BH, 0D6H - Mode Register - Write Only

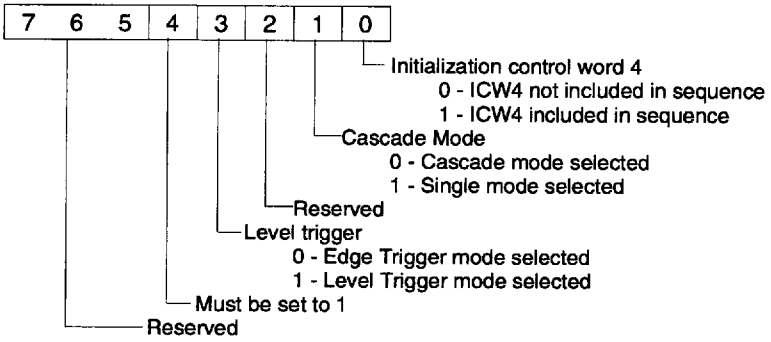


Port Address B872H - DMA Shadow Register - Read Only

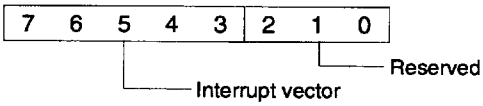


B.6 INTERRUPT CONTROLLERS

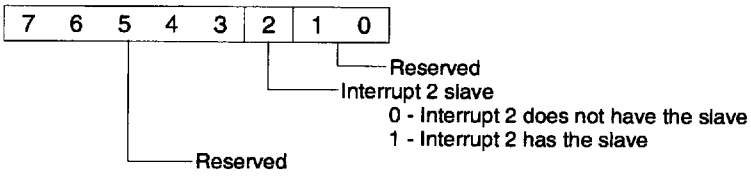
Port Address 020H, 0A0H - ICW1 - Initialization Command Word 1Register - Write only



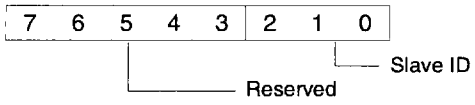
Port Address 021H, 0A1H - ICW2 - Initialization Command Word 2 Register - Write Only



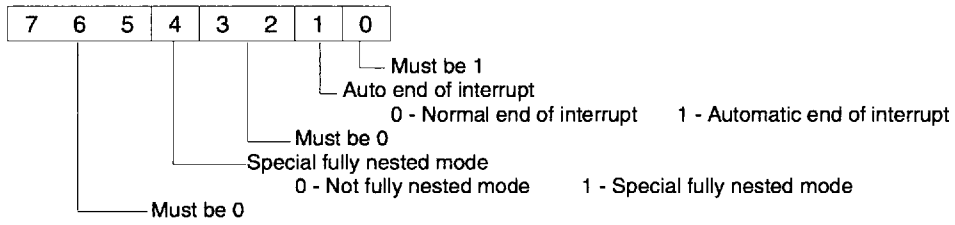
Port Address 021H - ICW3 - Initialization Command Word 3 Register - Write Only
Interrupt controller 1



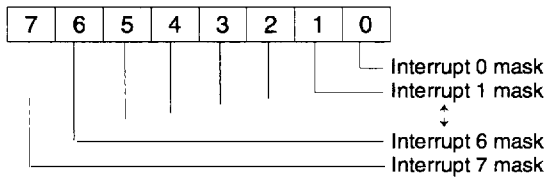
Port Address 0A1H - ICW3 - Initialization Command Word 3 Register - Write Only
Interrupt controller 2



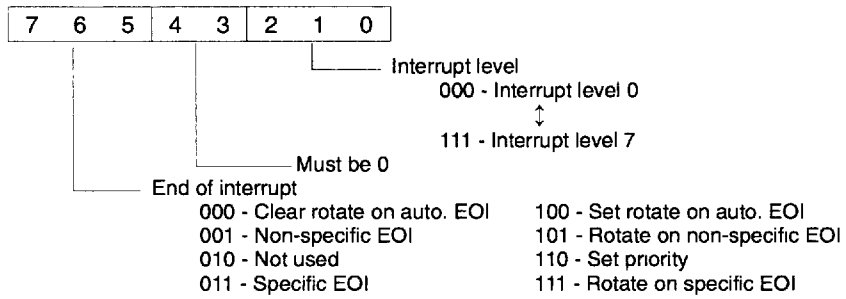
Port Address 021H, 0A1H - ICW4 - Initialization Command Word 4 Register - Write Only



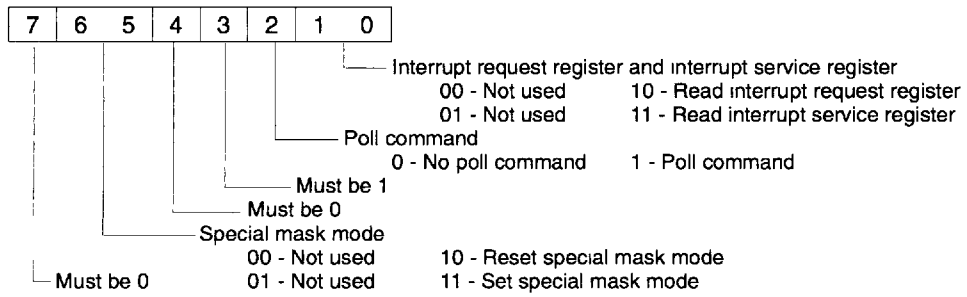
Port Address 021H, 0A1H - OCW1 - Operation Control Word 1 Register - Write Only



Port Address 020H, 0A0H - OCW2 - Operation Control Word 2 Register - Write Only

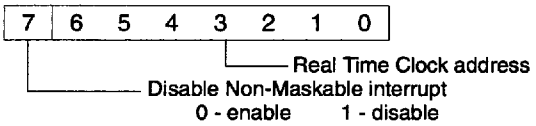


Port Address 020H, 0A0H - OCW3 - Operation Control Word 3 Register - Write Only

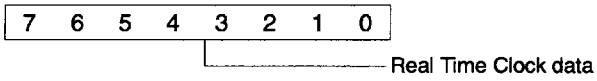


B.7 NMI AND REAL TIME CLOCK

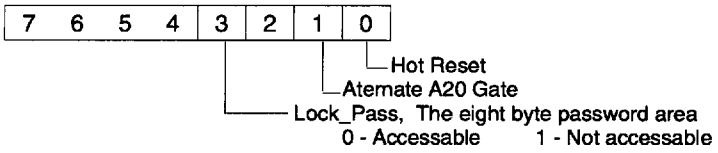
Port Address 070H in 10-bit mode, 0070H in 16-bit mode - Address Register - Write Only



Port Address 071H in 10-bit mode, 0071H in 16-bit mode - Data Register - Read and Write

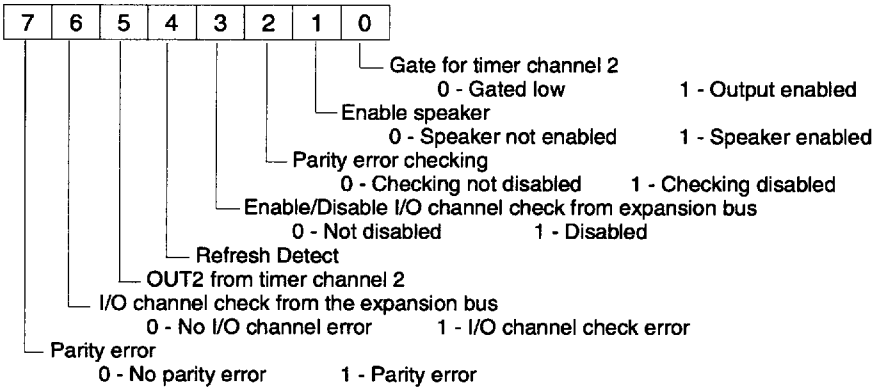


Port Address 092H in 10-bit mode, 0092H in 16-bit mode - Lock Pass, Alt. A20G, Hot Reset - Read/Write



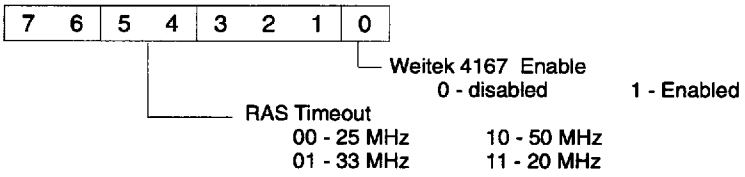
B.8 PORT B - PARITY ERROR AND I/O CHANNEL CHECK

Any odd numbered Port Address 061:06FH in 10-bit mode, 0061H in 16-bit mode - Bits 7:4 Read Only, Bits 3:0 Read and Write

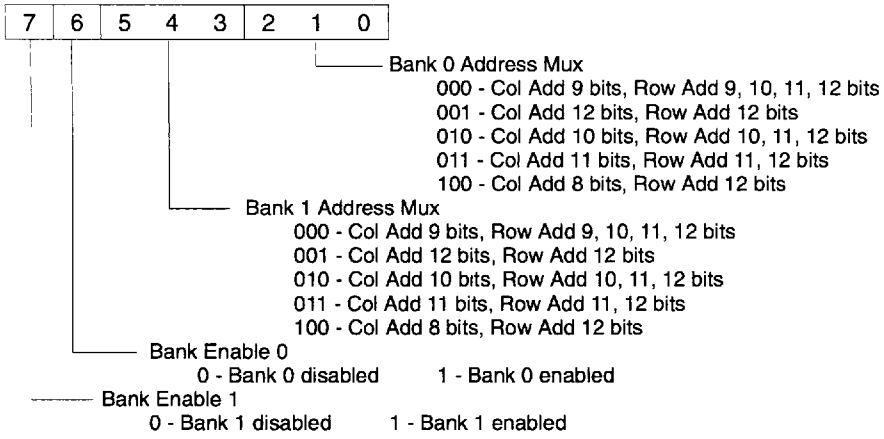


B.9 ESF REGISTERS

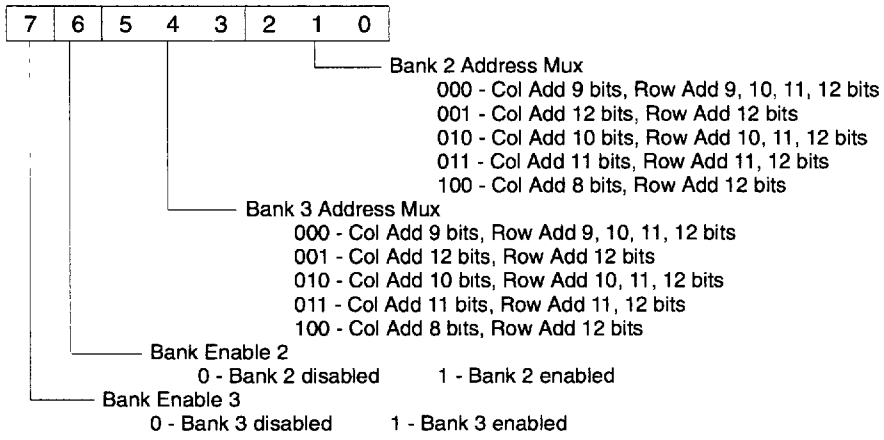
ESF Port Address 19FH - System Configuration Register - Bits 7:4, 0 Read and Write - Bits 3:1 Read Only



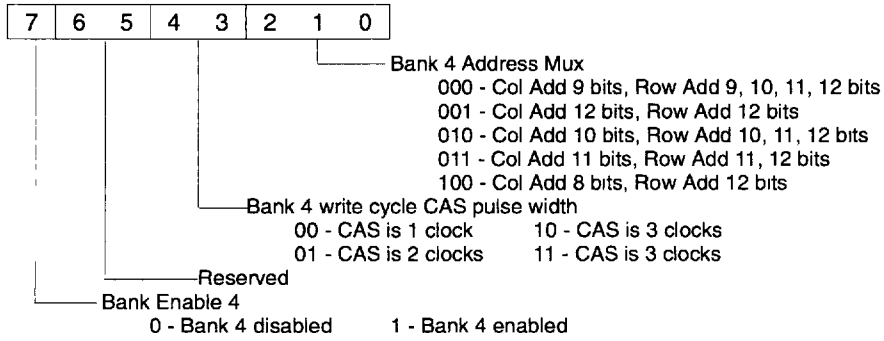
ESF Port Address 190H - Banks 0:1 Enabling and Address Multiplexing - Read and Write



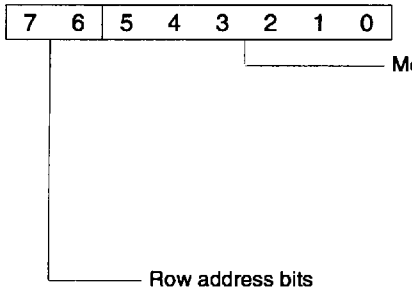
ESF Port Address 191H - Banks 2:3 Enabling and Address Multiplexing - Read and Write



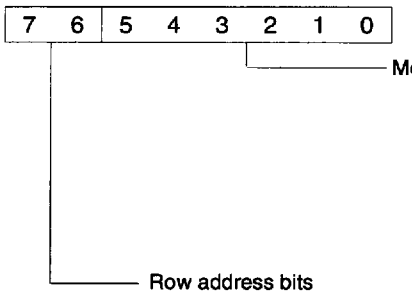
ESF Port Address 1A0H - Bank 4 Enabling and Address Multiplexing Register - Read and Write



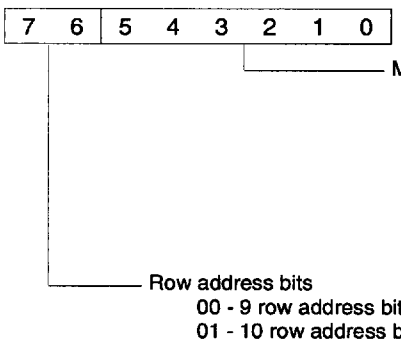
ESF Port Address 192H - Bank 0 Size Control Register - Read and Write



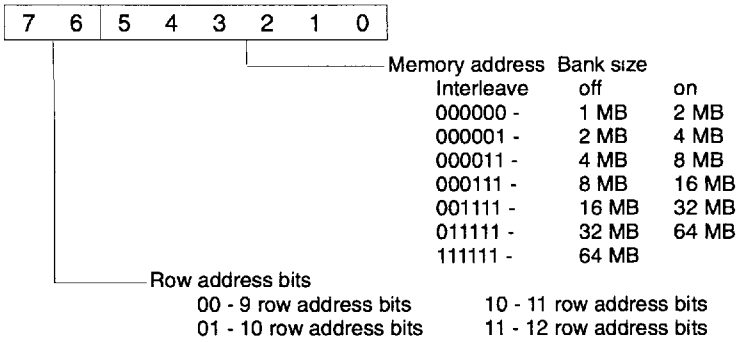
ESF Port Address 19AH - Bank 1 Size Control Register - Read and Write



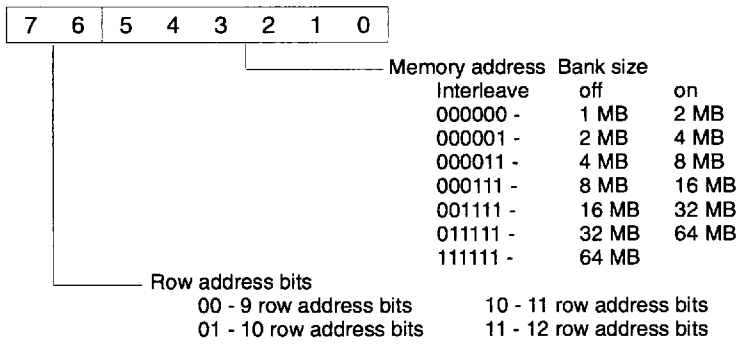
ESF Port Address 19BH - Bank 2 Size Control Register - Read and Write



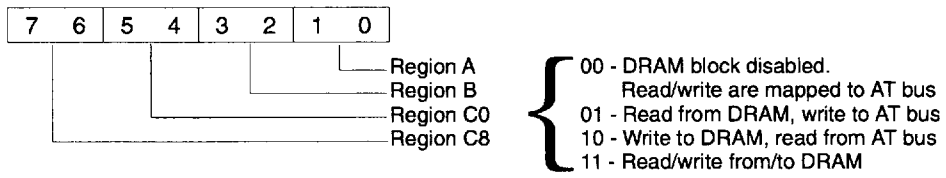
ESF Port Address 19CH - Bank 3 Size Control Register - Read and Write



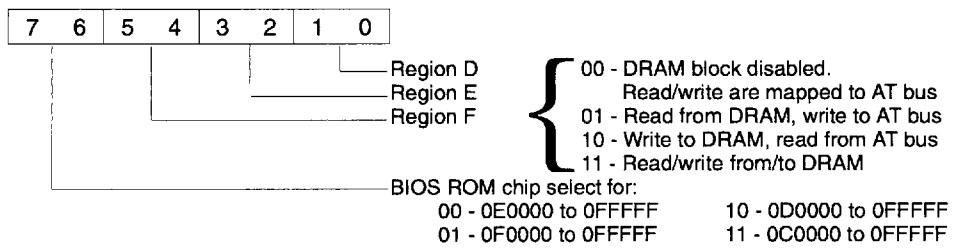
ESF Port Address 19DH - Bank 4 Size Control Register - Read and Write



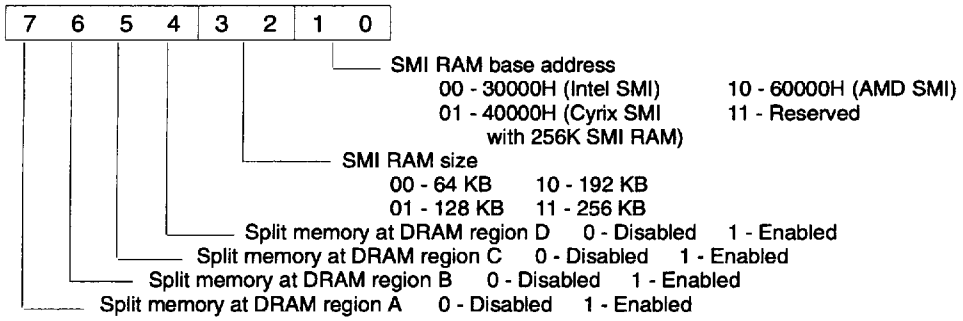
ESF Port Address 1AAH - Memory Shadow Control Register 1 - Read and Write



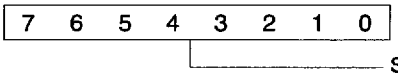
ESF Port Address 1A9H - Memory Shadow Control Register 2 - Read and Write



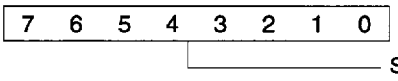
ESF Port Address 1ABH - Split Memory Control And SMI RAM Start Address Register - Read and Write



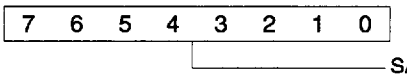
ESF Port Address 193H - Split Start Address Register - Read and Write



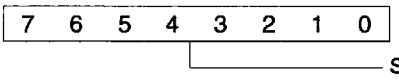
ESF Port Address 194H - Bank 0 Start Address Register - Read and Write



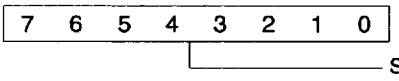
ESF Port Address 195H - Bank 1 Start Address Register - Read and Write



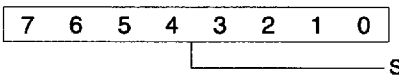
ESF Port Address 196H - Bank 2 Start Address Register - Read and Write



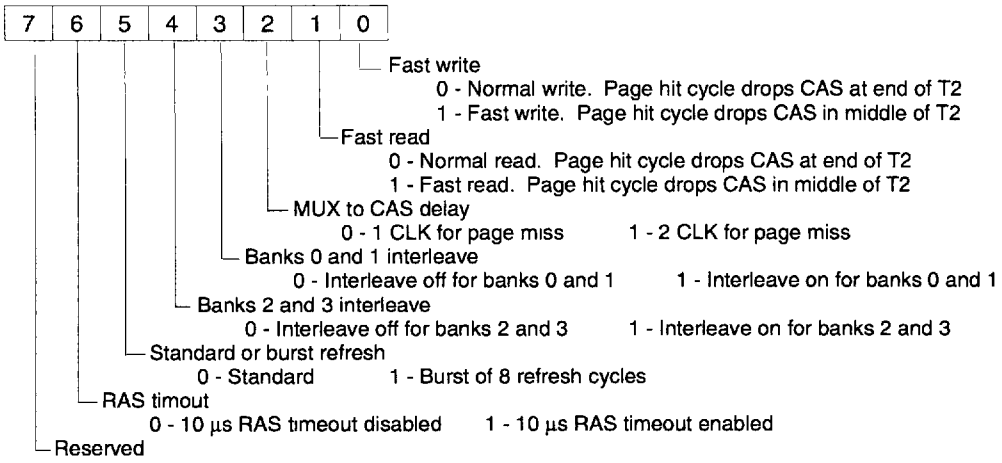
ESF Port Address 197H - Bank 3 Start Address Register - Read and Write



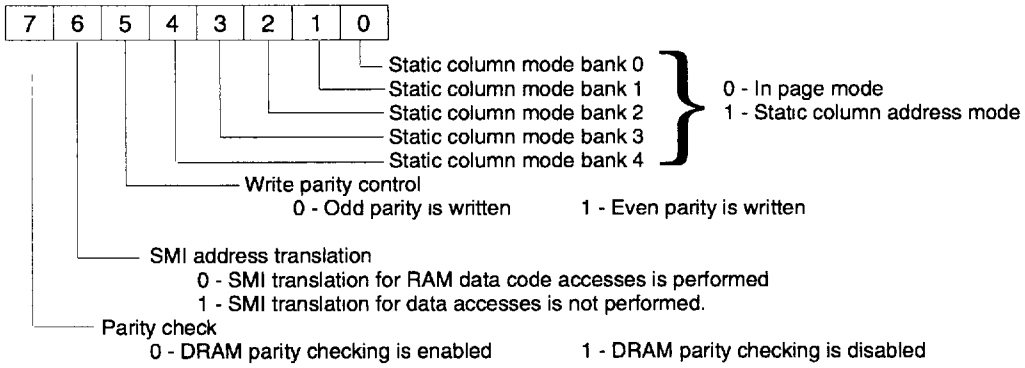
ESF Port Address 19EH - Bank 4 Start Address Register - Read and Write



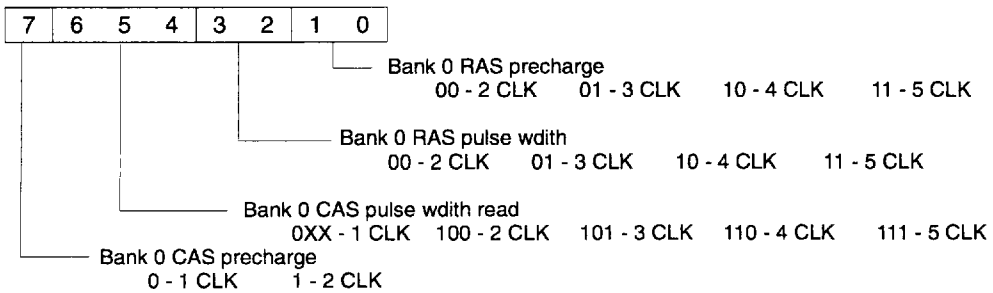
ESF Port Address 198H - DRAM Mode Register - Read and Write



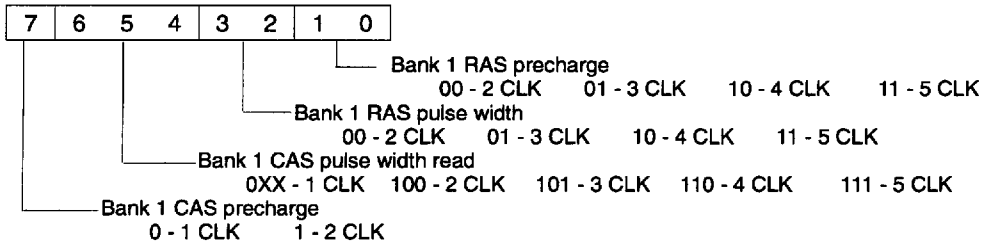
ESF Port Address 1A8H - Static Column Or Page Mode Register - Read and Write



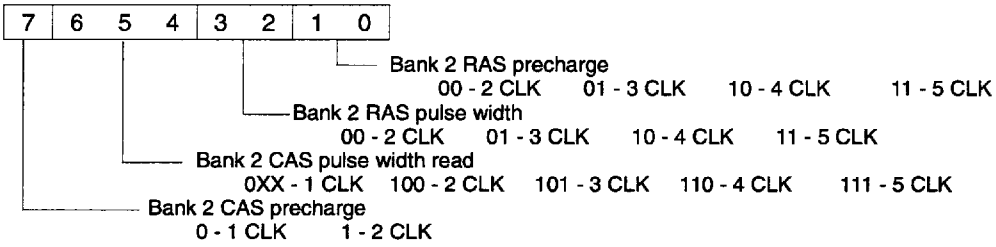
ESF Port Address 199H - Bank 0 RAS/CAS Pulse Width and Precharge Register - Read and Write



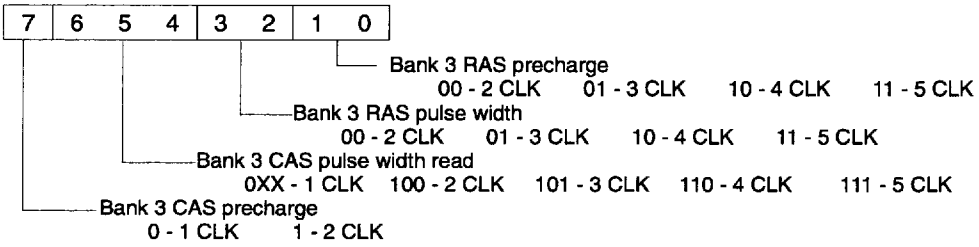
ESF Port Address 1A1H - Bank 1 RAS/CAS Pulse Width and Precharge Register - Read and Write



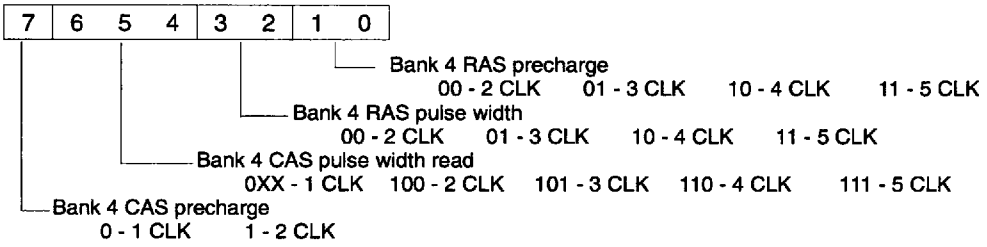
ESF Port Address 1A2H - Bank 2 RAS/CAS Pulse Width and Precharge Register - Read and Write



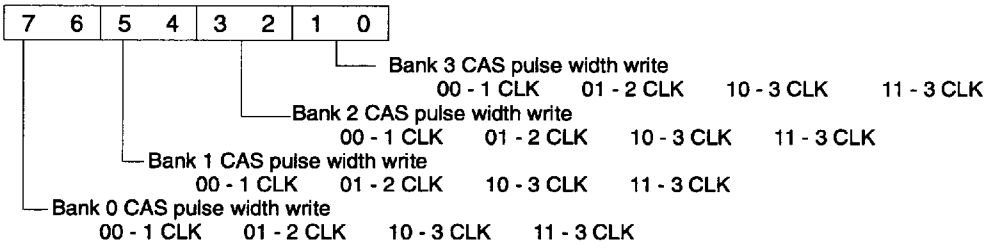
ESF Port Address 1A3H - Bank 3 RAS/CAS Pulse Width and Precharge Register - Read and Write



ESF Port Address 1A5H - Bank 4 RAS/CAS Pulse Width and Precharge Register - Read and Write

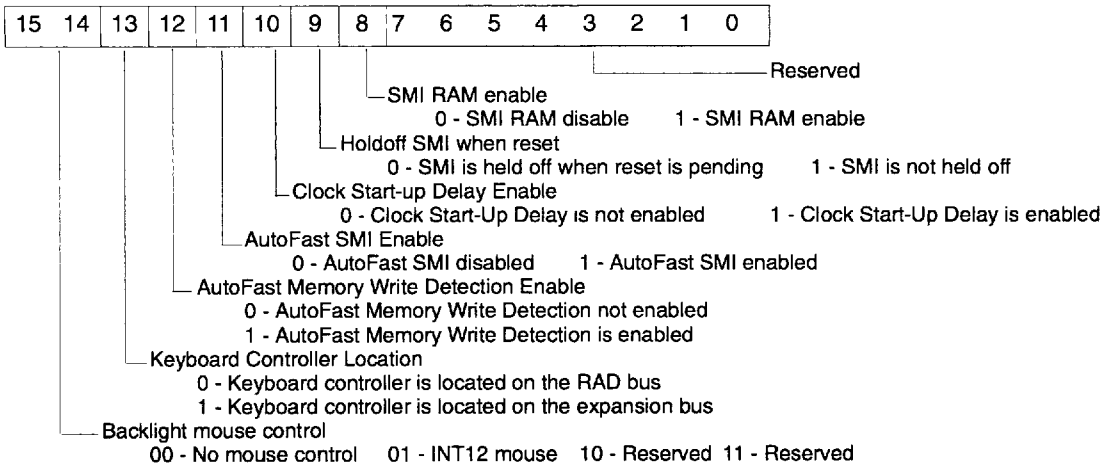


ESF Port Address 1A4H - Banks 3:0 CAS Pulse Width For Write Cycle Register - Read and Write



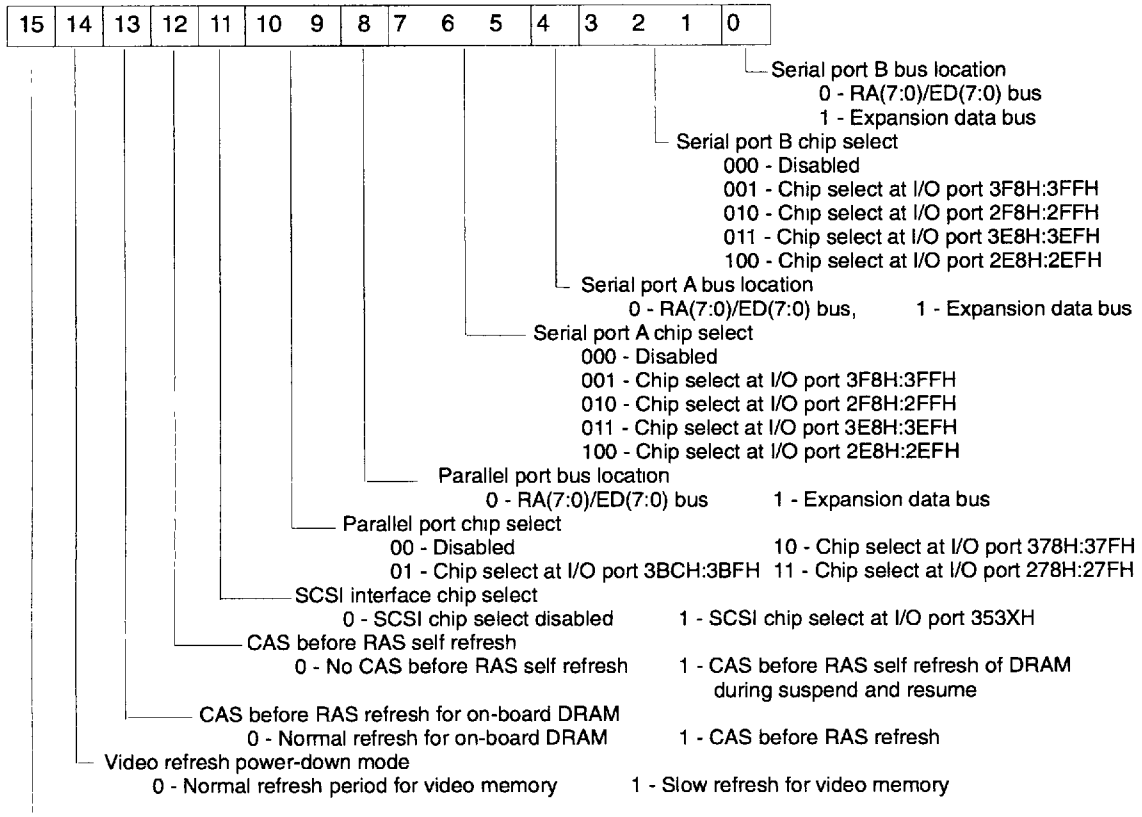
B.10 BACKLIGHT MOUSE AND SMI CONTROL

Port Address 7472H - Backlight Mouse and SMI Control Register - Read and Write



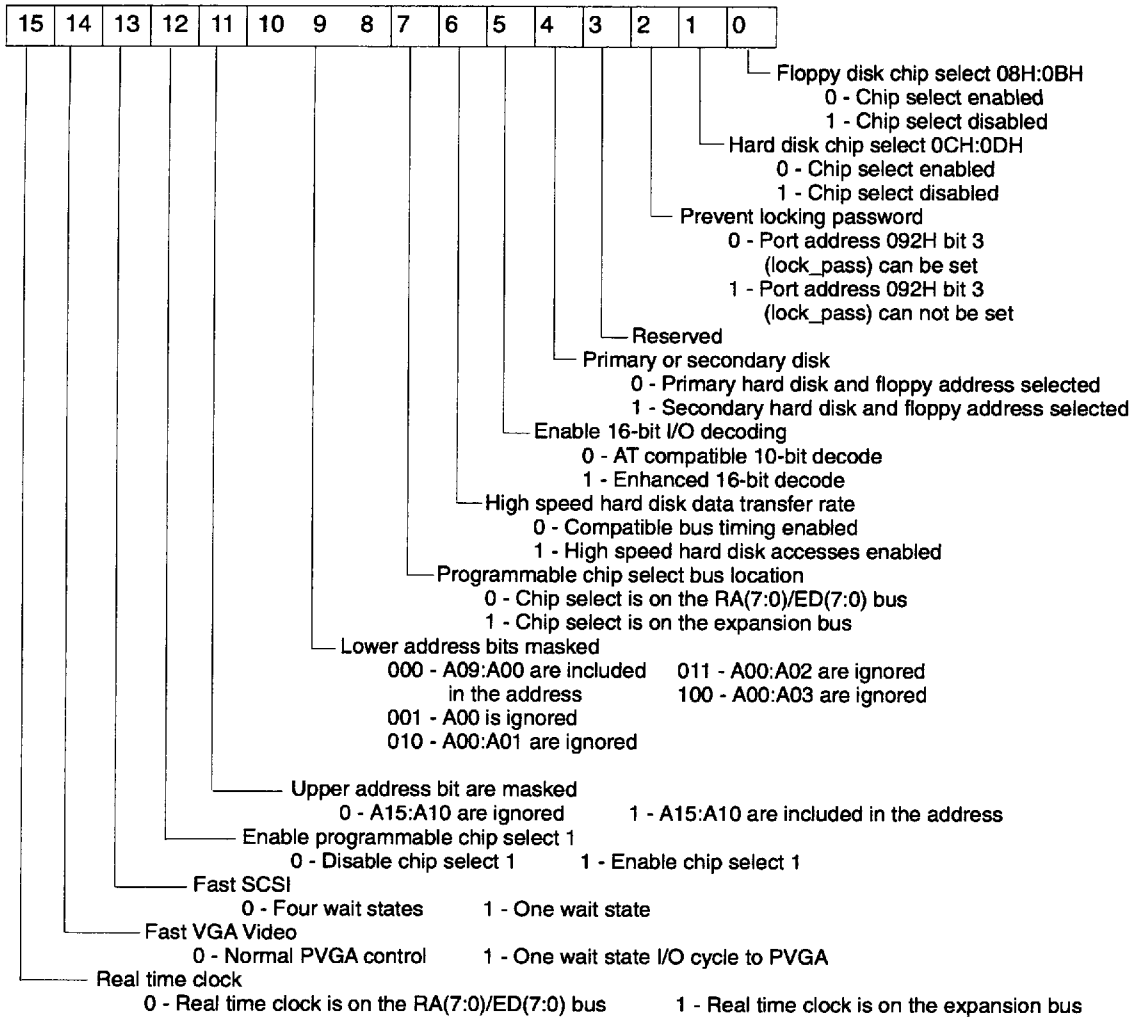
B.11 PORT CHIP SELECT AND REFRESH

Port Address 2072H - Serial and Parallel Chip Selects, Refresh Control - Read and Write

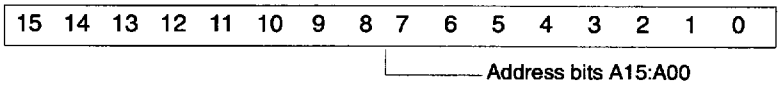


└ Memory refresh power-down mode
0 - Normal refresh for main on-board memory 1 - Slow refresh main on-board memory

Port Address 2872H - RTC, PVGA and Disk Chip Selects - Read and Write

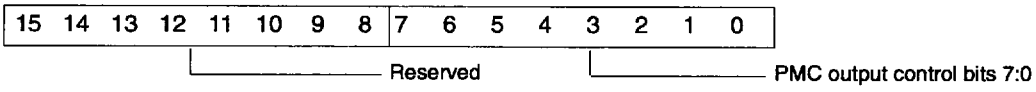


Port Address 3072H - Programmable Chip Select 1 Address - Read and Write

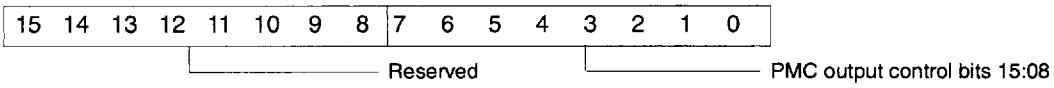


B.12 POWER MANAGEMENT CONTROL (PMC)

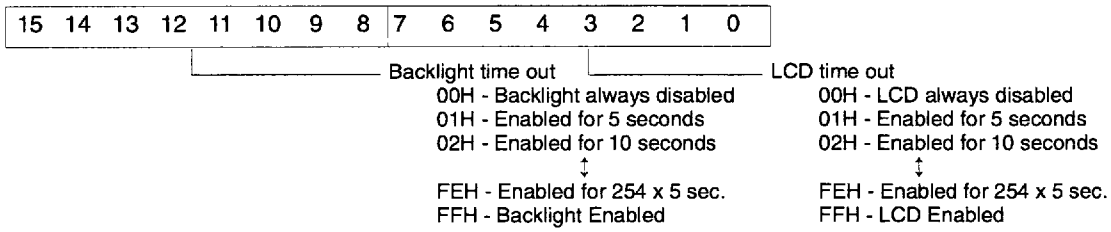
Port Address 7072H - PMC Output Control Register - Bits 7:0 Read Only



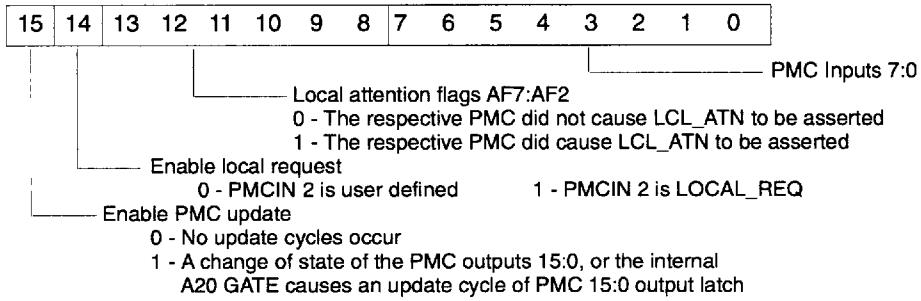
Port Address 7872H - PMC Output Control Register - Bits 7:0 Read and Write



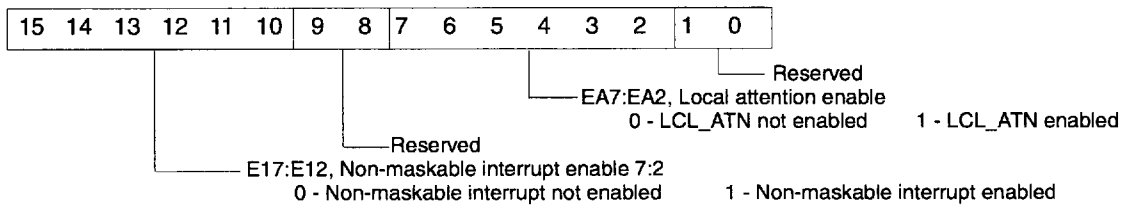
Port Address 8072H - PMC Timers - Read and Write



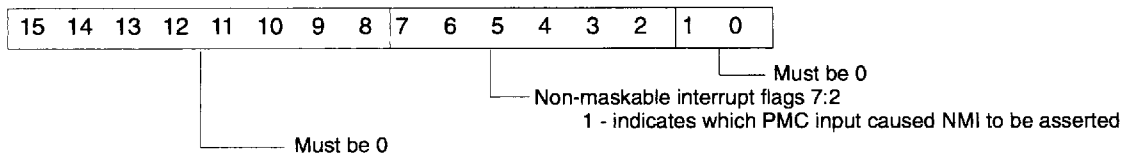
Port Address 8872H - PMC Inputs - Bits 15:8 Read and Write, Bits 7:0 Read Only



Port Address C872H - PMC Interrupt Enable - Read and Write

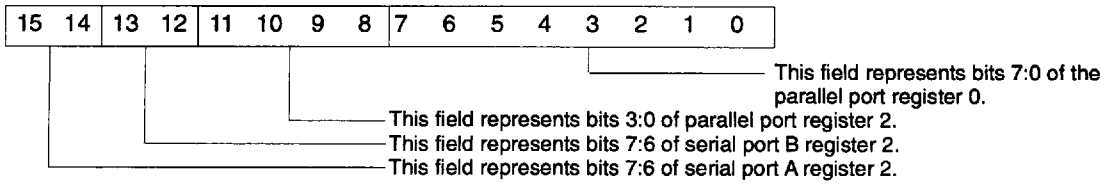


Port Address 9072H - NMI Status Register - Read and Write

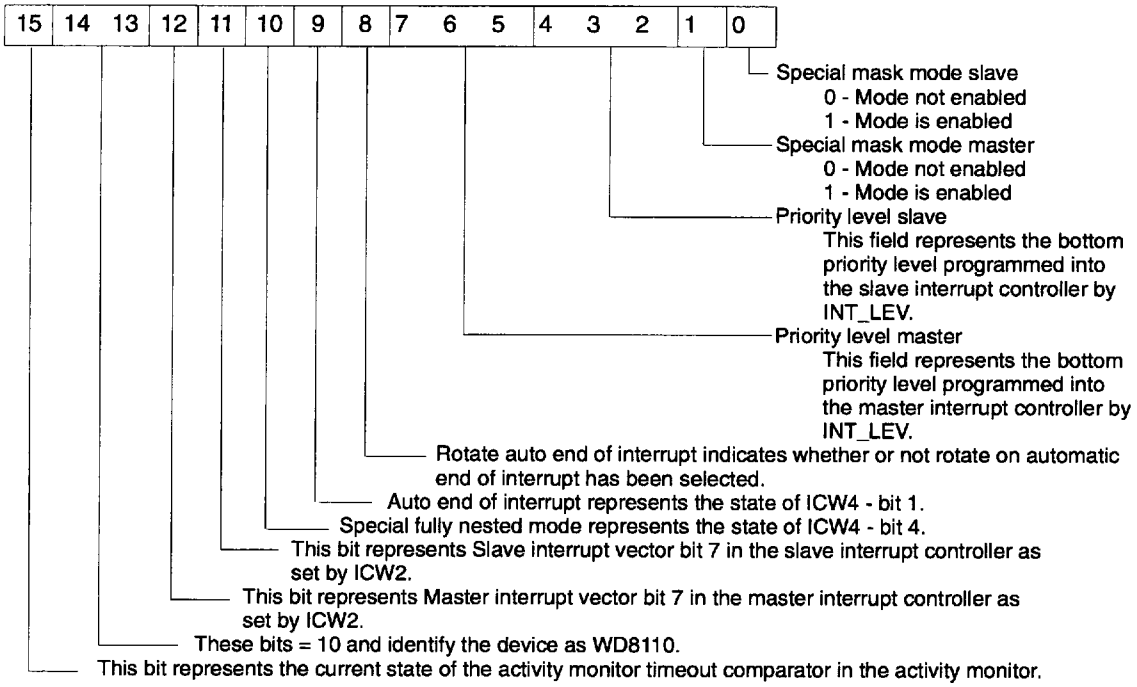


B.13 SHADOW REGISTERS

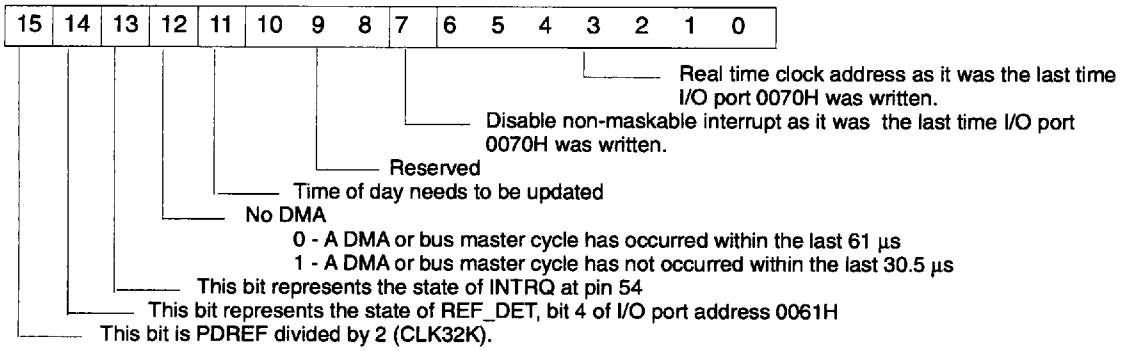
Port Address D072H - Serial/Parallel Shadow Register - Read Only



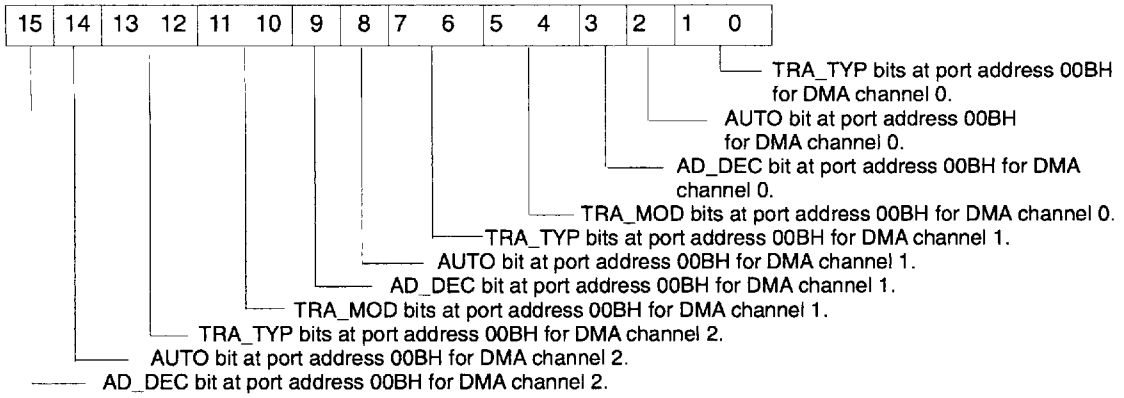
Port Address D472H - Interrupt Controller Shadow Register - Read Only



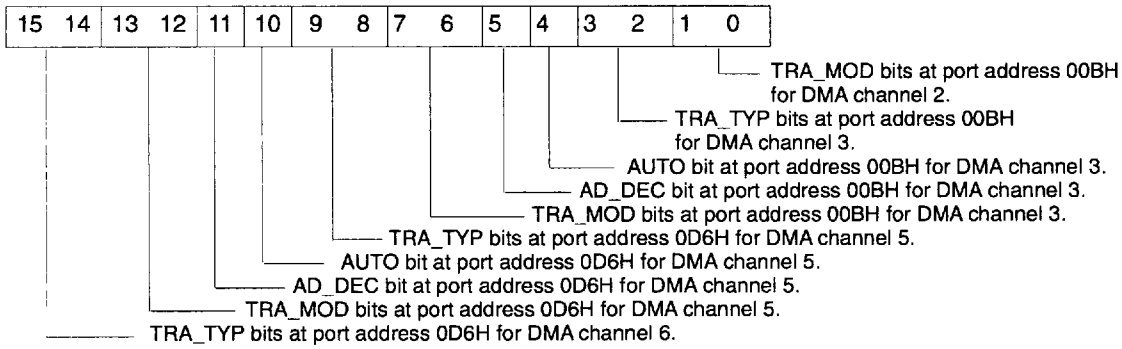
Port Address E472H - Port 70H Shadow Register - Bits 15:12, 10:00 Read Only, Bit 11 Read and Write



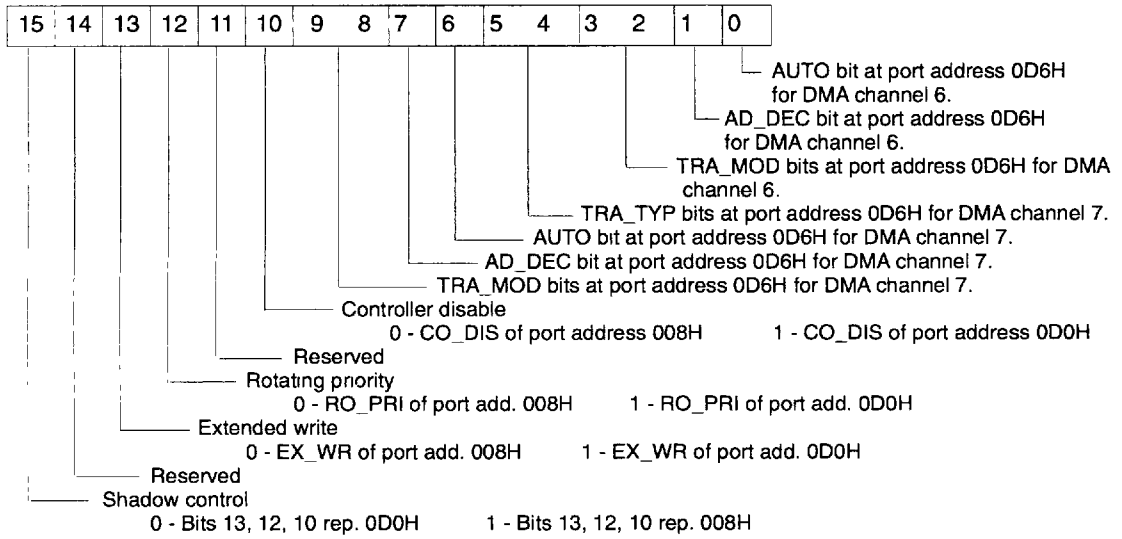
Port Address 3C72H - DMA Shadow Register 1 - Read Only



Port Address 4472H - DMA Shadow Register 2 - Read Only

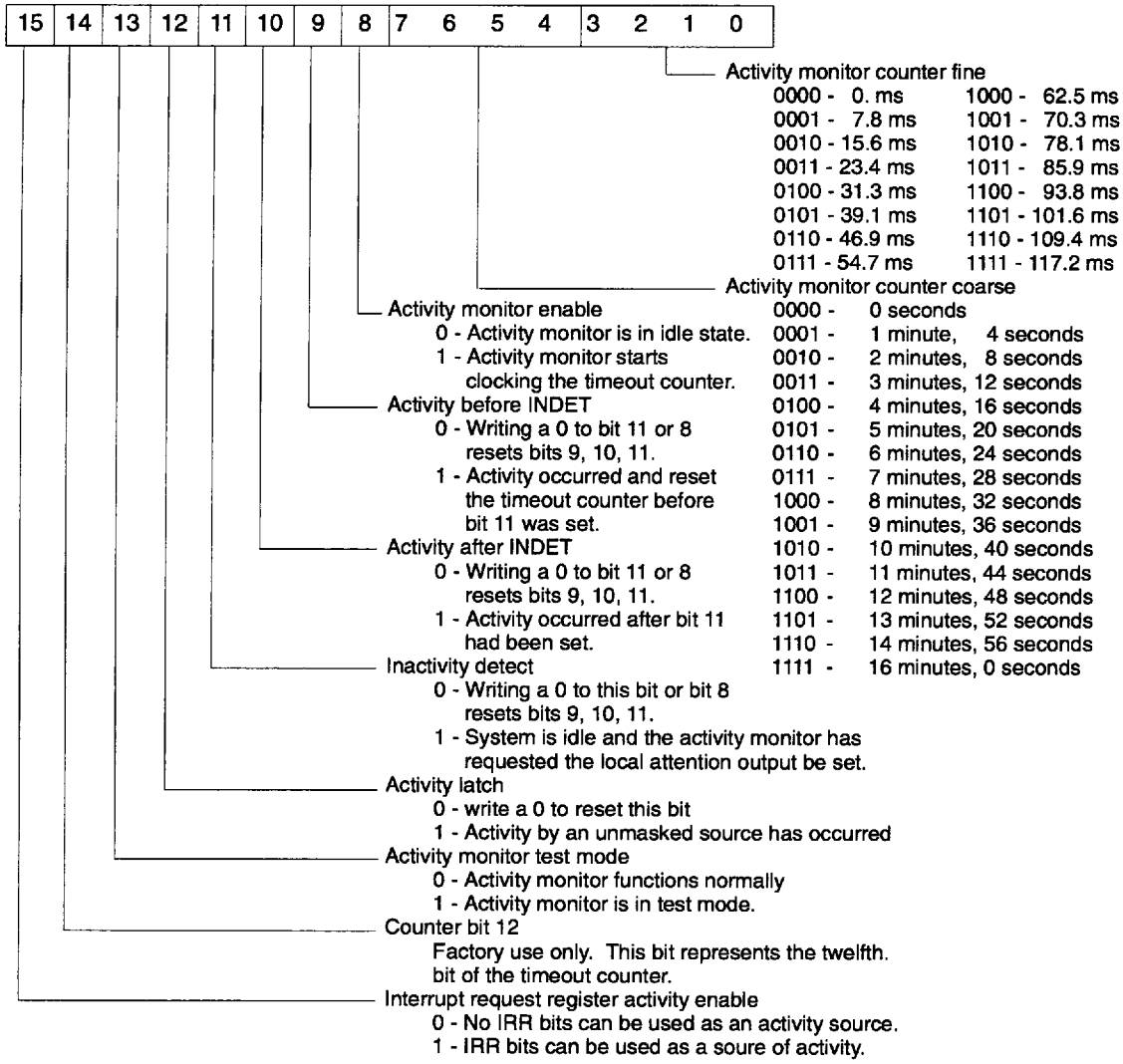


Port Address 4C72H - DMA Shadow Register 3 - Bit 15 Read and Write, Bits 14:00 Read Only

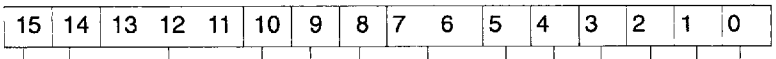


B.14 ACTIVITY MONITOR

Port Address B072H - Activity Monitor Control Register
- Bits 15, 13:11, 08:00 Read and Write, Bits 14, 10, 09 Read Only



Port Address D872H - Activity Monitor Mask Register - Read and Write



Interrupt service register 0 mask
0 - Time of day interrupt may be detected as a source of activity.
1 - Time of day interrupt is ignored

Interrupt service register 7 mask
0 - Parallel port or spurious interrupt may be detected as a source of activity.
1 - Parallel port or spurious interrupt is ignored.

Interrupt service register 8 mask
0 - Real-time clock interrupt may be detected as a source of activity.
1 - Real-time clock interrupt is ignored.

Interrupt request register 0 mask
0 - Time of day interrupt may be a source of activity. Bit 15 at port address B072H must also be set.
1 - Time of day interrupt is ignored.

Interrupt request register 7 mask
0 - Parallel port or spurious interrupt may be detected as a source of activity. Bit 15 at port address B072H must also be set.
1 - Parallel port or spurious interrupt is ignored.

Interrupt request register 8 mask
0 - Real time clock interrupt may be detected as a source of activity. Bit 15 at port address B072H must also be set.
1 - Real time clock interrupt is ignored.

Interrupt mask select
00 - IRQ5 10 - IRQ11
01 - IRQ10 11 - IRQ15

Coprocessor mask
0 - I/O cycles to the coprocessor are treated as a source of activity.
1 - I/O to the coprocessor is ignored.

Hard disk data port mask
0 - If the hard disk chip select has been enabled by bit 1 at port address 2872H, I/O read and write operations to the 16-bit hard disk dataport are allowed as a source of activity.
1 - The hard disk data port I/O is ignored.

Non-maskable interrupt mask
0 - The NMI output is used as a source of activity.
1 - The NMI output is ignored.

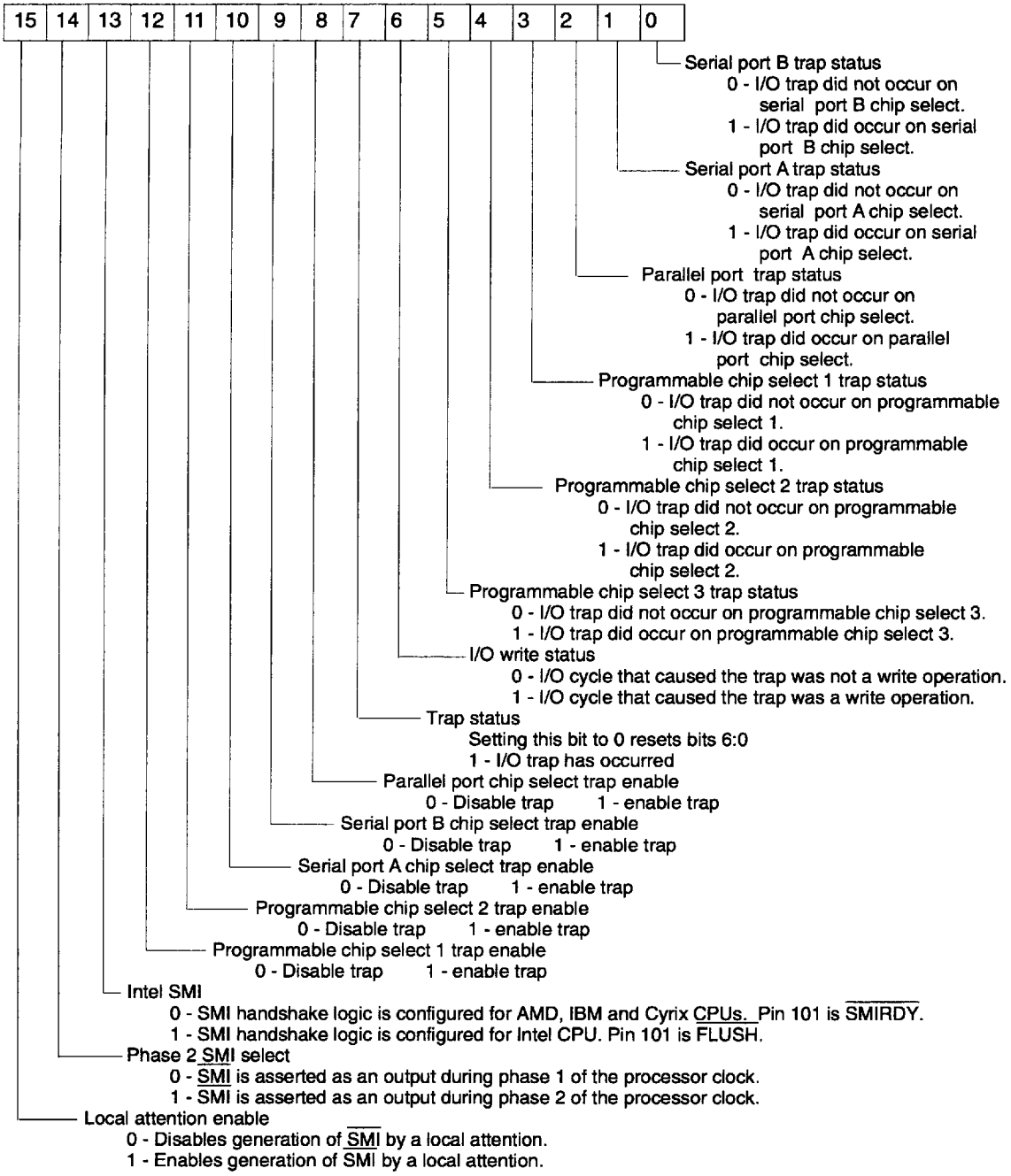
Power management control input select
000 - PMC input 2 seleted 100 - PMC input 6 seleted
001 - PMC input 3 seleted 101 - PMC input 7 seleted
010 - PMC input 4 seleted 110 - Reserved
011 - PMC input 5 seleted 111 - Disabled, no PMC inputs checked

Power management control input level select
0 - PMCIN is active low
1 - PMCIN is active high

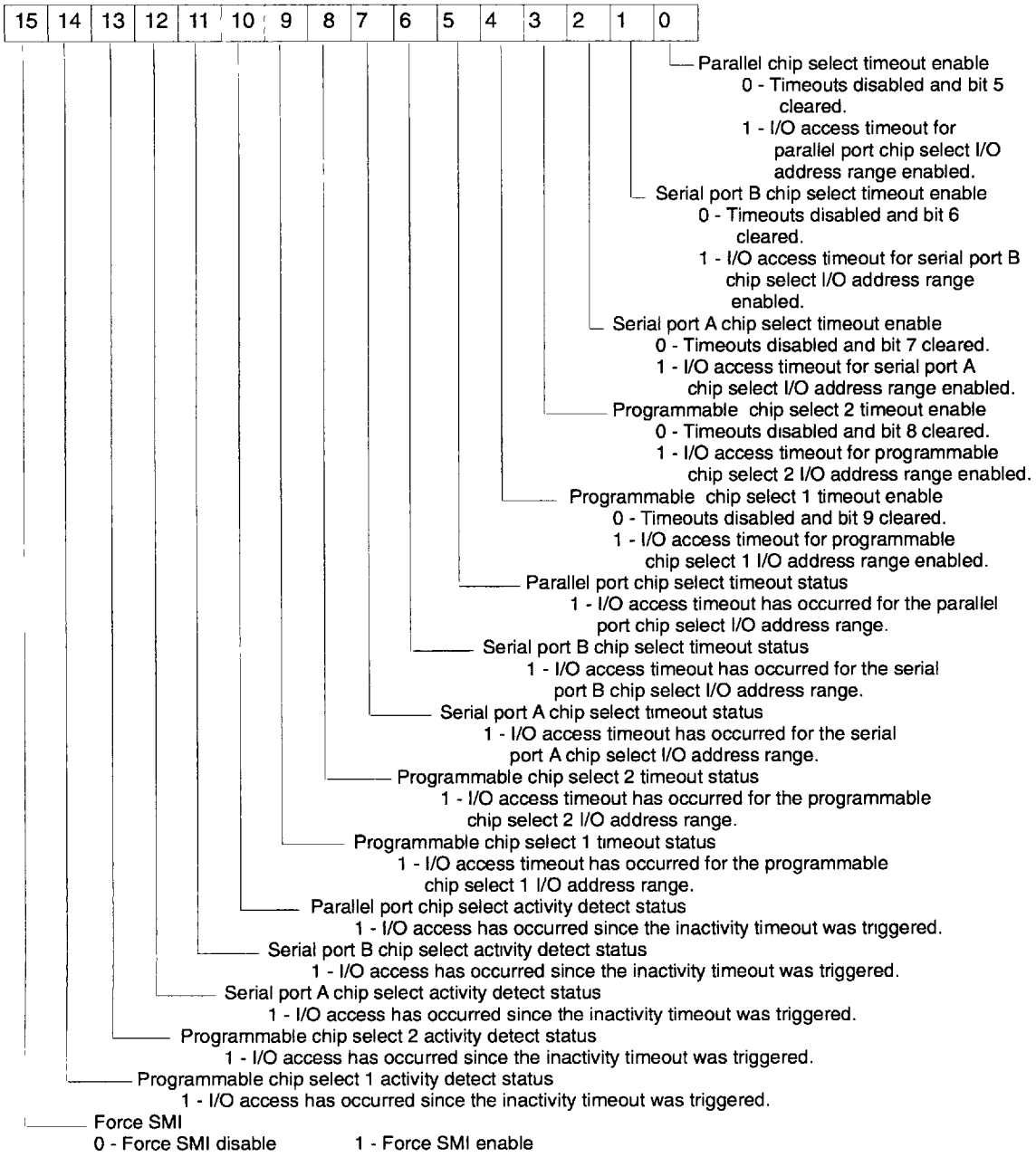
Programmable chip select 1 mask
0 - Read or write I/O accesses to the ports defined by the programmable chip select 1 in the WD8110/LV are considered activity.
1 - Read or write I/O accesses to the ports defined by the programmable chip select 1 in the WD8110/LV are ignored.

B.15 SYSTEM MANAGEMENT INTERRUPT (SMI)

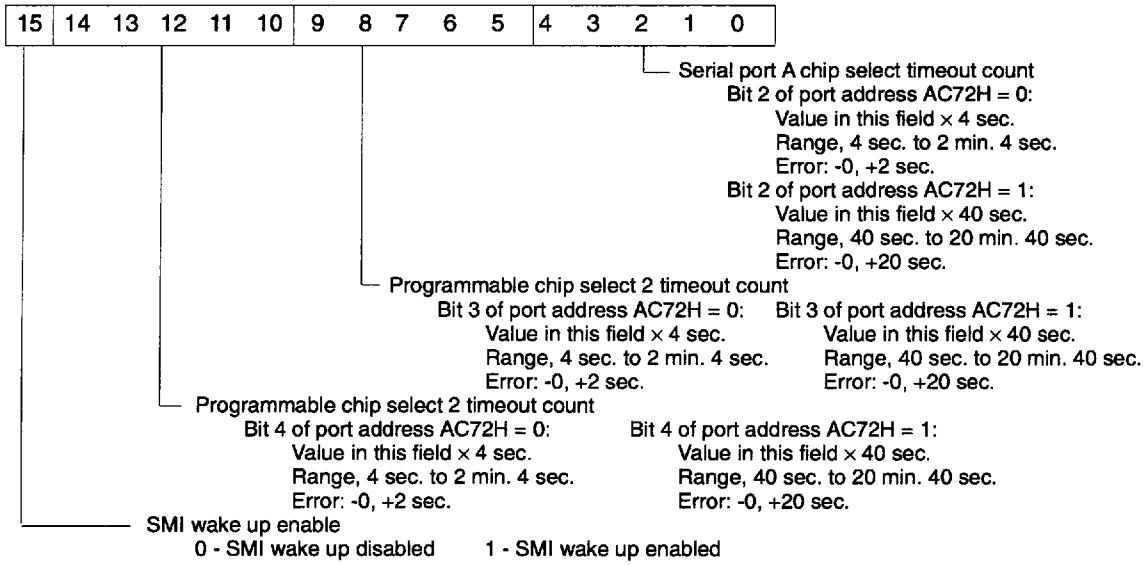
Port Address 7C72H - SMI I/O Trap Control Register
- Bits 15:8 Read and Write, Bit 7 Read and Clear, Bits 6:0 Read Only



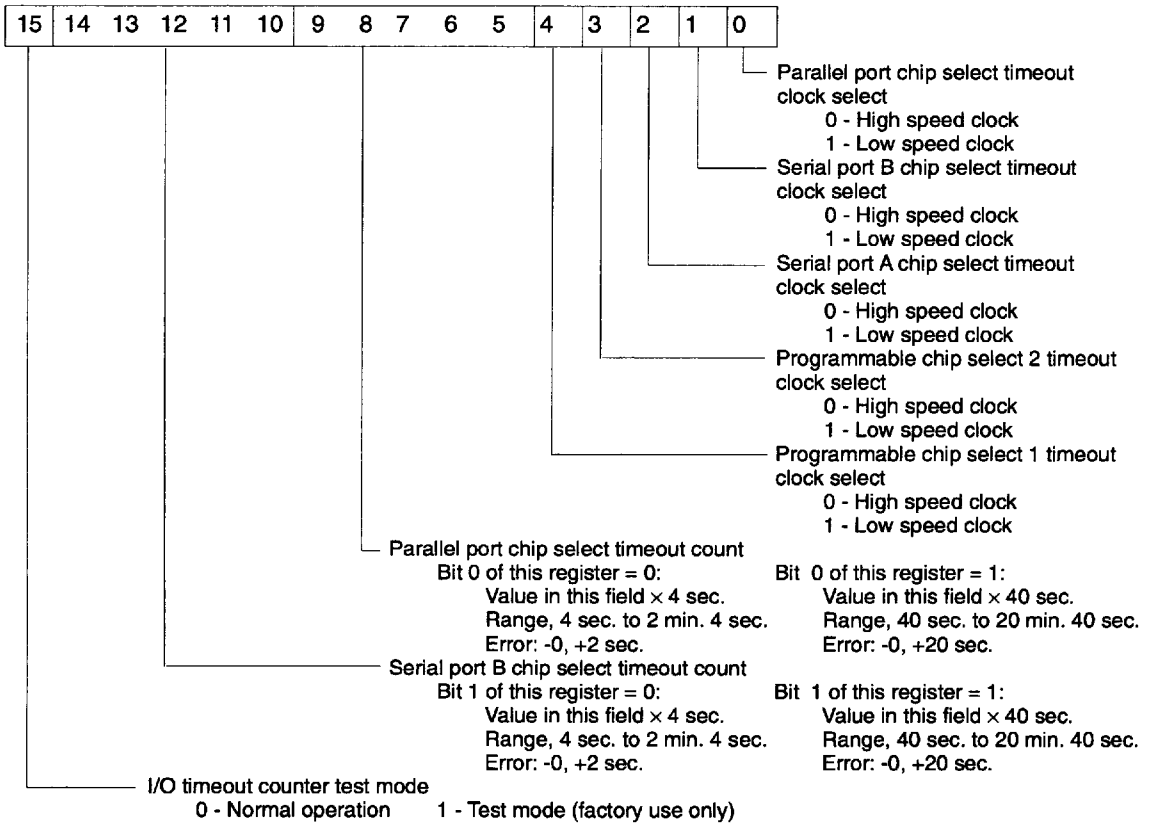
Port Address 9C72H - SMI I/O Timeout Control Register
- Bits 15, 4:0 Read and Write, Bits 14:0 Read Only



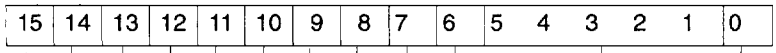
Port Address A472H - SMI Timeout Count Register 1 - Read and Write



Port Address AC72H - SMI Timeout Count Register 2 - Read and Write

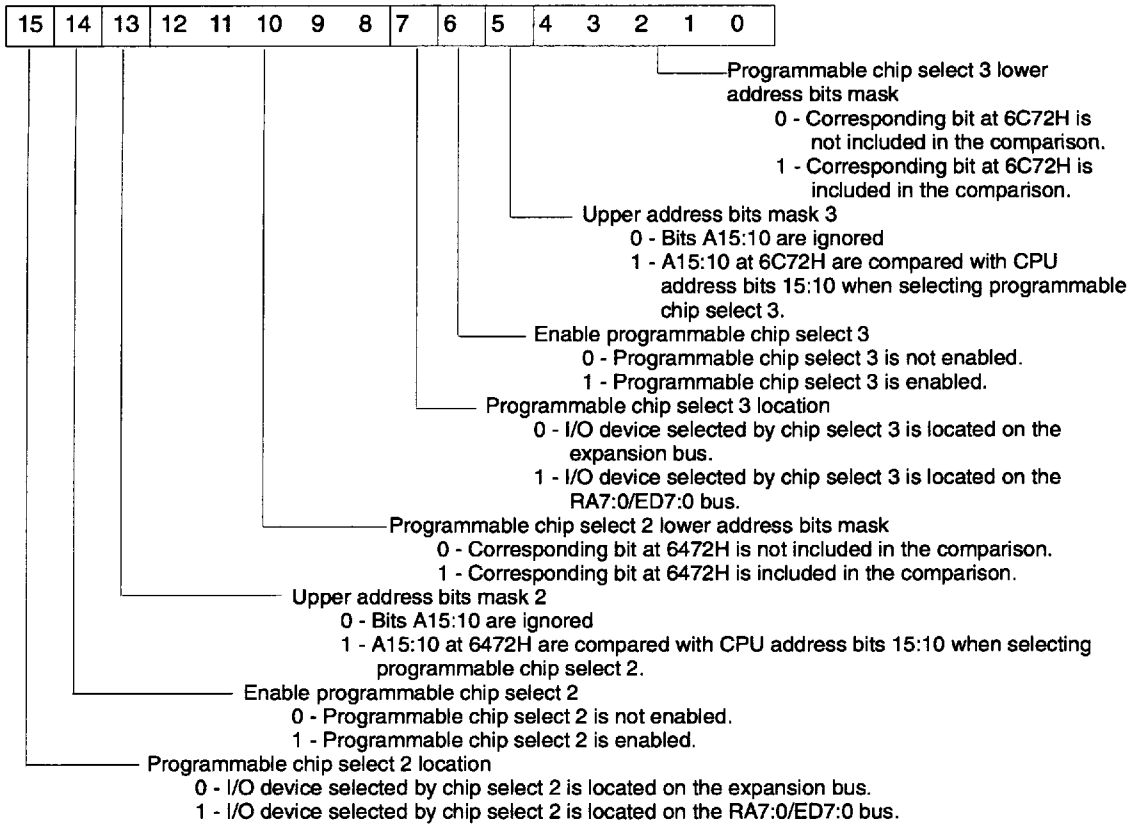


Port Address 5472H - SMI Auxiliary Control Register
- Bits 15, 13, 11:8, 5:0 Read and Write, Bit 12 Read and Clear, Bits 7:6 Read Only

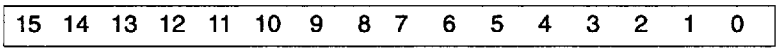


- Bit 0: Programmable chip select 3 timeout clock select
  - 0 - High sped clock
  - 1 - Slow speed clock
- Bits 1:5: Programmable chip 3 select timeout count
  - Bit 0 of this register = 0:
    Value in this field x 4 sec.
    Range, 4 sec. to 2 min. 4 sec.
    Error: -0, +2 sec.
  - Bit 0 of this register = 1:
    Value in this field x 40 sec.
    Range, 40 sec. to 20 min. 40 sec.
    Error: -0, +20 sec.
- Bit 6: Programmable chip select 3 activity detect status
  - 0 - Reset occrred or bit 8 cleared.
  - 1 - An I/O access has occurred since the inactivity timeout was triggerd.
- Bit 7: Programmable chip select 3 timeout status
  - 0 - Reset occrred or bit 8 is cleared.
  - 1 - An I/O access timeout has occerred for programmable chip select 3 I/O address range.
- Bit 8: Programmable chip select 3 timeout enable
  - 0 - Programmable chip select 3 timeouts are disabled. Bits 7 and 6 are cleared.
  - 1 - I/O access timeout for programmable chip select 3 I/O address range is enabled.
- Bit 9: Programmable chip select 3 trap enable
  - 0 - Trap not enabled
  - 1 - I/O trap occurs when an I/O read or write occurs within the address range covered by programmable chip select 3.
- Bit 10: Programmable chip select 2 mask
  - 0 - I/O access to programmable chip select 2 address range is observed as activity by SAM.
  - 1 - I/O access to programmable chip select 2 address range is masked from SAM.
- Bit 11: Programmable chip select 3 mask
  - 0 - I/O access to programmable chip select 3 address range is observed as activity by SAM.
  - 1 - I/O access to programmable chip select 3 address range is masked from SAM.
- Bit 12: Watch dog interrupt status
  - 0 - Bit 13 set to 0 or a 0 written to this bit.
  - 1 - LCL_ATN has been set due to watchdog timer interrupt request.
- Bit 13: Watchdog timer interrupt enable
  - 0 - Disable periodic interrupt
  - 1 - Periodic interrupt generated every 125 ms.
- Bit 14: Reserved
- Bit 15: Timeout mask
  - 0 -
  - 1 - I/O device timeouts are prevented from asserting SMI outputs. I/O device timers continue to count down.

Port Address 5C72H - Programmable CS2 and CS3 Control Register - Read and Write

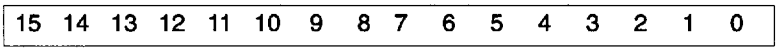


Port Address 6472H - Programmable CS2 Address Register - Read and Write



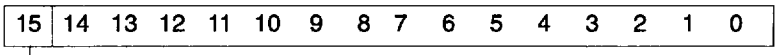
Bits 15:0 provide the base address of the I/O device corresponding to programmable chip select 2.

Port Address 6C72H - Programmable CS3 Address Register - Read and Write



Bits 15:0 provide the base address of the I/O device corresponding to programmable chip select 3.

Port Address 8472H - IBM I/O Trap Register - Read only when in Virus Protection mode.

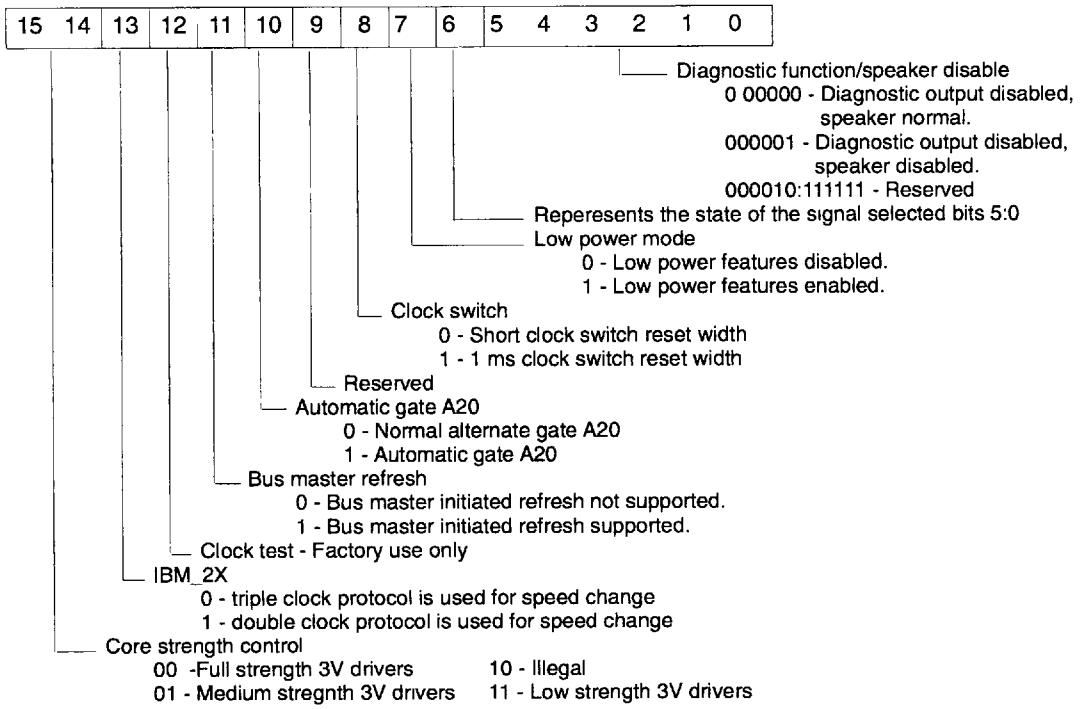


Bits 14:0 are reserved.

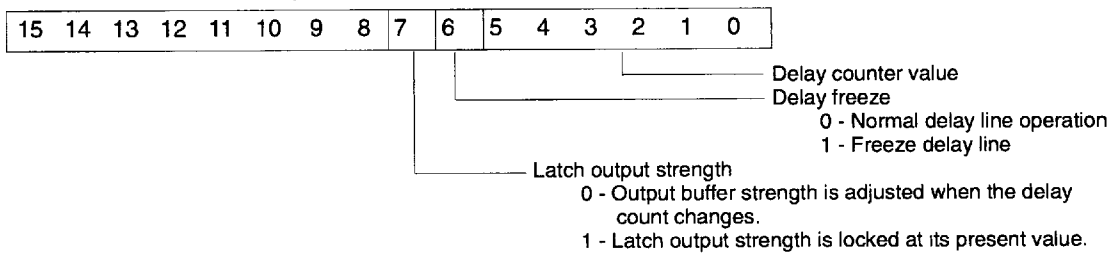
IBM Trap Mode
When set, a minimum of 12 CLKs between the assertion of SMI for an I/O trap and the end of the I/O instruction is ensured.

B.16 DIAGNOSTICS

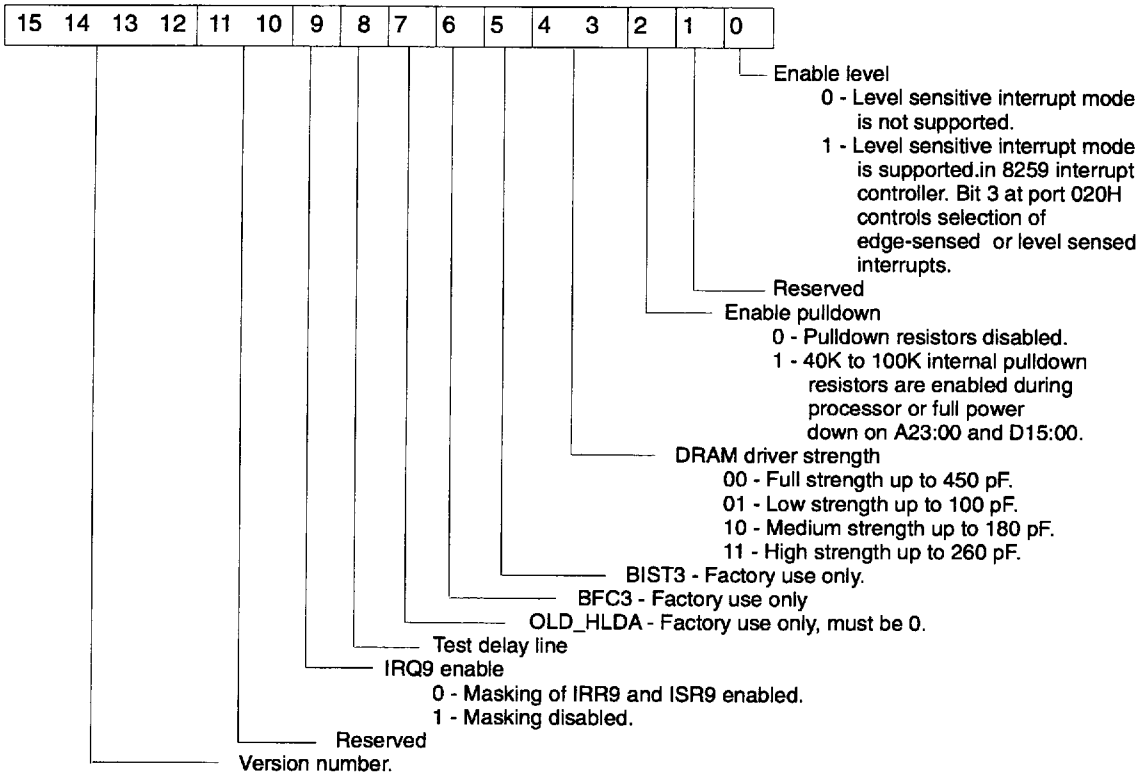
Port Address 9872H - Diagnostic Register - Read and Write



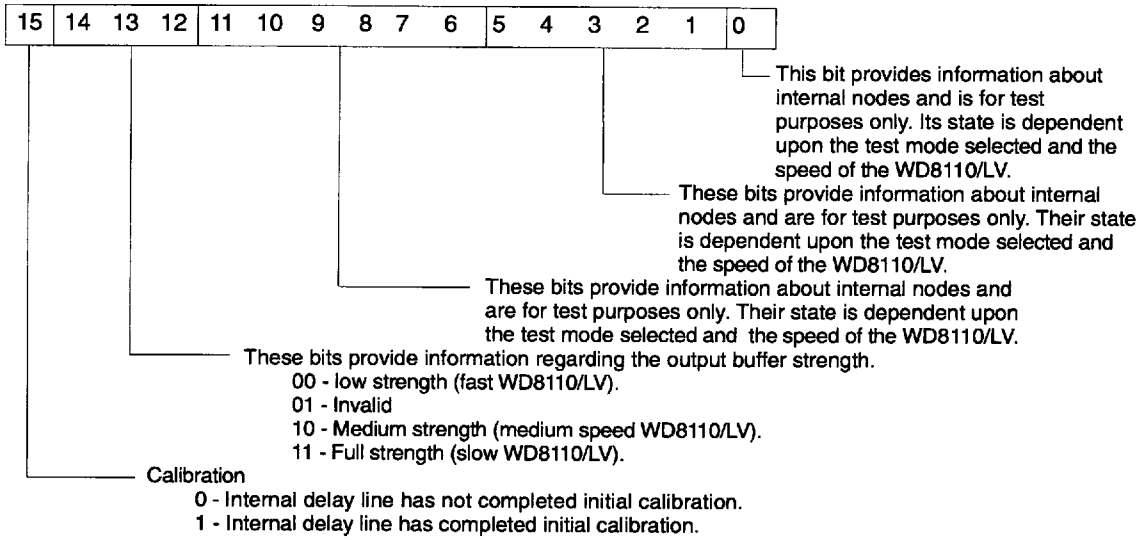
Port Address A072H - Delay Line Diagnostic Register - Read and Write



Port Address A872H - Test Enable Register - Bits 15:10 Read Only, Bits 9:0 Read and Write

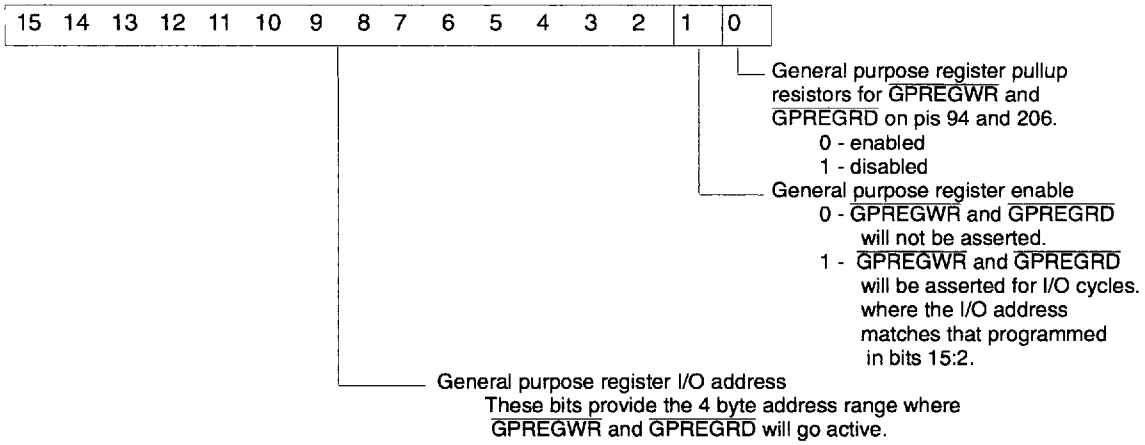


Port Address DC72H - Test Status Register - Read Only

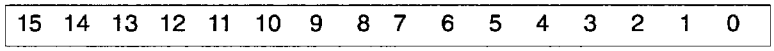


B.17 MISCELLANEOUS REGISTERS

Port Address 9472H - General Purpose I/O Control Register - Read and Write

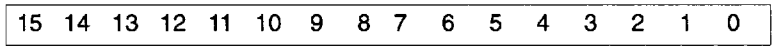


Port Address 3872H - General Purpose I/O Write Shadow Register - Read Only



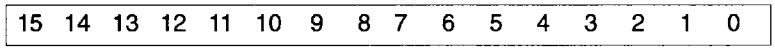
The last data written to external latches by GPREGWR.

Port Address C472H - Scratch Pad A Register - Read and Write



The last data written to this register. It performs no other function.

Port Address CC72H - Scratch Pad B Register - Read and Write



The last data written to this register. It performs no other function.

PORT ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
008, 0D0									Depends on application. See sections 5.4.8, 5.4.9							
009, 0D2									0	0	0	0	0	0	0	0
00A, 0D4									1	1	1	1	1	1	1	1
00B, 0D6									No default							
00C, 0D8									No default							
00D, 0DA									No default							
00E, 0DC									No default							
00F, 0DE									1	1	1	1	1	1	1	1
020, 0A0									No default							
021, 0A1									No default							
061:06F									0	0	X	1	0	0	0	0
070, 0070									1	X	X	X	X	X	X	X
071, 0071									No default							
092, 0092									X	X	X	X	0	X	0	0
ESF190									0	0	0	0	0	0	0	0
ESF191									0	0	0	0	0	0	0	0
ESF192									0	0	0	0	0	0	0	0
ESF193									0	0	0	0	0	0	0	0
ESF194									0	0	0	0	0	0	0	0
ESF195									0	0	0	0	0	0	0	1
ESF196									0	0	0	0	0	0	1	0
ESF197									0	0	0	0	0	0	1	1
ESF198									0	0	0	0	0	0	0	0
ESF199									1	1	1	1	1	1	1	1
ESF19A									0	0	0	0	0	0	0	0
ESF19B									0	0	0	0	0	0	0	0
ESF19C									0	0	0	0	0	0	0	0
ESF19D									0	0	0	0	0	0	0	0
ESF19E									0	0	0	0	0	1	0	0
ESF19F									0	0	0	0	0	0	0	0
ESF1A0									1	1	0	0	0	0	0	0
ESF1A1									1	1	1	1	1	1	1	1
ESF1A2									1	1	1	1	1	1	1	1

TABLE B-1. REGISTER DEFAULT STATES AT RESET

PORT ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ESF1A3									1	1	1	1	1	1	1	1
ESF1A4									1	1	1	1	1	1	1	1
ESF1A5									1	1	1	1	1	1	1	1
ESF1A8									1	0	0	0	0	0	0	0
ESF1A9									0	0	0	0	0	0	0	0
ESF1AA									0	0	0	0	0	0	0	0
ESF1AB									1	1	0	0	0	1	1	1
1072	0/1	0	0	1	0	0	0	0	X	0	0	0	X	X	0	0
1872	0	0	0	X	0	0	0	0	1	1	0	0	1	0	1	0
2072	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2872	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3072	No default															
3872	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3C72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4472	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4C72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5472	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5C72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6472	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6C72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7072	No default															
7472	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7872	No default															
7C72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8072	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8472	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8872	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
8C72	X	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0
9072	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9472	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9872	0	0	0	0	0	0	X	0	X	0	0	0	0	0	0	0
9C72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A072	X	X	X	X	X	X	X	X	0	0	X	X	X	X	X	X
A472	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TABLE B-1. REGISTER DEFAULT STATES AT RESET (Continued)

PORT ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A872	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
AC72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B072	0	X	0	X	X	X	X	0	0	0	0	0	0	0	0	0
B472	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B872	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BC72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C072	0	X	X	X	1	0	0	1	0	1	1	1	0	1	1	1
C472	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C872	0	0	0	0	0	0	X	X	0	0	0	0	0	0	X	X
CC72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D072	No default															
D472	X	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X
D872	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DC72	No default															
E472	X	X	X	X	X	0	0	0	1	X	X	X	X	X	X	X
F073	No default															
FC72	No default															

1. Shaded area indicates that no bits are present.
2. X indicates that there is no default setting.

TABLE B-1. REGISTER DEFAULT STATES AT RESET (Continued)

B.18 REGISTER DESCRIPTION QUICK REFERENCE INDEX

PORT ADDRESS (HEX)	REGISTER NAME	PAGE
008, 0D0	Command Register	202, 203
009, 0D2	Request Register	203
00A, 0D4	Single Mask Register	203
00B, 0D6	Mode Register	204
00C, 0D8	Clear Point Register	203
00D, 0DA	Master Clear Register	203
00E, 0DC	Clear Mask Register	203
00F, 0DE	Mask Multiple Register	203
020, 0A0	ICW1 - Initilization Command Word 1	204
020, 0A0	OCW2 - Operation Control Word 2	205
020, 0A0	OCW3 - Operation Control Word 3	205
021, 0A1	ICW2 - Initilization Command Word 2	204
021	ICW3 - Initilization Command Word 3, Interrupt Controller 1	204
0A1	ICW3 - Initilization Command Word 3, Interrupt Controller 1	205
021, 0A1	ICW4 - Initilization Command Word 4	205
021, 0A1	OCW1 - Operation Control Word 1	205
061 - 06F odd	Port B Parity Error and I/O Channel Check	206
070, 0070	NMI and Real-Time Clock Address Register	206
071, 0071	NMI and Real-Time Clock Data Register	206
080, 0D0	Command Register	199
092, 0092	Lock Pass, ALT A20 Gate and Hot Reset	206
0EC	Busy Bypass Control	197
0EE	Fast A20 Gate Control	198
0EF	Fast CPU Reset Control	198
0F9	Disable Privy	197
0FB	Enable Privy	197
ESF190	Bank 0:1 Address Mux Control	207
ESF191	Bank 2:3 Address Mux Control	207
ESF192	Bank 0 Size Control	208
ESF193	Split Address Start	210
ESF194	Bank 0 Start Address	210
ESF195	Bank 1 Start Address	210
ESF196	Bank 2 Start Address	210
ESF197	Bank 3 Start Address	210
ESF198	DRAM Mode	211
ESF199	DRAM Parameters Bank 0	211
ESF19A	Bank 1 Size Control	208
ESF19B	Bank 2 Size Control	208
ESF19C	Bank 3 Size Control	209
ESF19D	Bank 4 Size Control	209
ESF19E	Bank 4 Start Address	210
ESF19F	System Configuration	206
ESF1A0	Bank 4 Address Mux Control	207
ESF1A1	DRAM Parameters Bank 1	212
ESF1A2	DRAM Parameters Bank 2	212
ESF1A3	DRAM Parameters Bank 3	212
ESF1A4	DRAM Write Cycle Parameters Banks (3:0)	212
ESF1A5	DRAM Parameters Bank 4	212
ESF1A8	Static Column Or Page Mode	211

PORT ADDRESS (HEX)	REGISTER NAME	PAGE
ESF1A9	Memory Shadow Control 2	209
ESF1AA	Memory Shadow Control	209
ESF1AB	Split Memory Control and SMI RAM Start Address	210
1072	CPU Clock Control	199
1872	Bus Timing And Power Down Control	202
2072	Refresh Control, Serial And Parallel Chip Selects	213
2872	RTC, PVGA, Chip Selects	214
3072	Programmable Chip Select Address	214
3872	General Purpose I/O Write	227
3C72	DMA Shadow 1	217
4472	DMA Shadow 2	217
4C72	DMA Shadow 3	217
5472	SMI Auxiliary Control	223
5C72	Programmable CS2 and CS3 Control	224
6472	Programmable CS2 Address	224
6C72	Programmable CS3 Address	224
7072	PMC Output Control 7:0	214
7472	Backlight Mouse And SMI Control	213
7872	PMC Output Control 15:8	215
7C72	SMI I/O Trap Control	220
8072	PMC Timers	215
8472	IBM I/O Trap	224
8872	PMC Inputs 7:0	215
8C72	Stop Clock Control	200
9072	NMI Status	215
9472	General Purpose I/O Control	227
9872	Diagnostic	225
9C72	SMI I/O Timeout Control 1	221
A072	Delay Line Diagnostic	225
A472	SMI I/O Timeout Count 2	222
A872	Test Enable	226
AC72	SMI I/O Timeout Count 3	222
B072	Activity Monitor Control	218
B472	Enhanced DMA Clock	201
B872	DMA Mode Shadow	204
BC72	Enhanced DMA Clock	201
C072	ROM Bank Select Control	201
C472	Scratchpad A	227
C872	PMC Interrupt Enables	215
CC72	Scratchpad B	227
D072	Serial/Parallel Shadow	216
D472	Interrupt Controller Shadow	216
D872	Activity Monitor Mask	219
DC72	Test Status	226
E472	Port 70H Shadow	216
F073	Lock/Unlock	199
FC72	Lock Status	199

C.0 REVISION HISTORY

C.1 REVISION HISTORY 1

Revision History 1 identifies the changes made from the document dated 3/25/93 to the document dated 6/9/93.

The changes incorporated in the document dated 6/9/93 consist of:

1. Section 1.2 - Second feature modified
2. Section 1.3.1 - Last paragraph added.
3. Section 1.3.2 - Third paragraph - WD8120LV Super I/O added.
4. Section 1.3.3.3 - Modified
5. Section 1.3.3.4 - Modified
6. Section 1.4 - New
7. Table 3-2 - Pin 107, LBCLK description modified. Pin 102 corrected. $\overline{STP}$_$\overline{REQ}$ description modified. $\overline{FERR}$ description modified. MDIR description modified. $\overline{MDEN}$ description modified.
8. Section 4.2 - Expanded.
9. Section 4.2.3 - Expanded.
10. Figure 4-1 - Modified
11. Section 4.2.6 - Bits 07:04 added. 98% duty cycle added.
12. Section 4.2.7 - Bit 09 added. SCK(1:0) = 00 modified.
13. Section 5.4.8 - Section reference corrected.
14. Section 5.9 - D_PE = 0 -, description modified.
15. Section 6.4.1 - Bits 5:4 - CPU Speed, description added
16. Table 6-1 - ON column modified
17. Section 6.4.9 - Bit 7 - PAR_CHE, Description added.
18. Section 6.5 - Bits 13:10 added
19. Table 7-3. - EMS replaced with reserved.
20. Section 10.3 - Version A and B added.
21. Table 13-1 - SD(15:0) given its own table.
22. Table 14-1 - Modified.
23. Table 14-3 - New.
24. Figure14-1 - Modified.
25 Figure 14-2 - Modified.
26. Figure 14-29 - Modified.
27. Table 14-7 - T60:T62, T158 deleted, T305 modified.
28. Section 14.3 - Paragraph modified.
29. Table 14-9 - Modified.
30. Figure 14-36 - New.
31. Figure 14-37 - New.
32. Figure 14-38 - Modified.
33. Figure 14-39 - New.
34. Figure 14-40 - New.
35. Figure 14-41 - Modified caption.
36. Table 15-1 - Modified.
37. Appendix A - Space assigned. Data to be provided in future document.
38. Appendix B - New.
39. Appendix C - New.

C.2 REVISION HISTORY 2

Revision History 2 identifies the changes made from the document dated 6/9/93 to the document dated 8/12/93.

The changes incorporated in the document dated 8/12/93 consist of:

1. Section 1.2 - Seventh feature modified.
2. Section 1.4 - Corrected.
3. Figures 1-1, 1-2 - 74ACT45S changed to (Optional)
4. Table 2-1 - References to table updated, F073 relocated.
5. Section 4.2.5 - Second paragraph deleted.
6. Section 4.2.7 - Bits 08:07 modified.
7. Section 4.2.8 - Bit 02, active changed to inactive. Bit 00, new description.
8. Section 6.4.1 - Default list corrected.
9. Section 6.4.8 - Bit 1 and Bit 2 signal description, polarity reversed.
10. Section 6.4.10 - Default value added to the six registers.
11. Section 6.5 - Bits 10:08, missing A01 added.
12. Section 8.15.1.1 - Paragraph 4 modified.
13. Section 10.1 - Default list update.
14. Section 10.3 - Default list updated. Bits 15:12, Version C added.
15. Section 12.1 - Second paragraph, two changed to three.
16. All of sections 13 and 14 - Changed to provide WD8110LV secifications. WD8110LV deleted from appendix A.
17. Table 14-1 - 14-4 TBD deleted and table numbers update.
18. Table 14-3 - T203 spec. added.
19. Table 14-4 - Deleted. Following table numbers updated and pagination updated.
20. Table 14-8 - T451:T454 sepcification added.
21. Figures 14-1:10 - T numbers added.
22. Figure 14-41 - WD7855 changed to WD8110/LV
23. Section B.0 - Modified.
24. Section B.4 - Port Address BC72H modified to reflect change made to section 4.2.8.
25. Section B.9 - Port Address 198H modified to reflect change made to section 6.4.8.
26. Table B-1 - Added.
27. Quick Reference Index - Redone.

C.3 REVISION HISTORY 3

Revision History 3 identifies the changes made from the document dated 8/12/93 to the document dated 9/15/93.

The changes incorporated in the document dated 9/15/93 consist of:

1. Section 1.0 - "all" added to 80486SX
2. Section 1.2 - Features 1, 2, 3, 6, 12, 18, 24, 26, 27, modified.
3. Section 1.3 - First paragraph last sentence modified.
4. Section 1.3.1 - Two way interleave deleted.
5. Section 1.3.3.1 - Title modified.
6. Section 1.3.3.2 - Modified.
7. Section 1.3.3.5 - Modified.
8. Section 1.3.3.6 - Modified
9. Section 1.3.3.8 - Modified.
10. Figure 1-1 - Modified.
11. Figure 1-2 - Modified.
12. Section 2.1.2 - First paragraph modified.

13. Section2.3 - First paragraph modified.
14. Section 2.6 - Modified.
15. Section 2.8 - Modified.
16. Table 2-1 - Modified.
17. Table 3-1 - Pin 120 corrected.
18. Table 3-2 - Data Bits 31 through 00 description modified. VDD description modified and pin 120 added.
19. Section 4-1 - Main Processor changed to CPU.
20. Section 4.2.5 - Last two paragraphs modified.
21. Section 4.2.6 - AUT_FST = 1, reference to EXT_HOLD deleted. ATPUEN = 1, modified.
22. Section 5.1 - (ROM AT BUS) deleted.
23. Table 5-1 - Last line added.
24. Figure 5-1 - Modified.
25. Section 5.5.2.4 - Spaces removed from SFNM.
26. Section 6.0 - Static Column Mode added.
27. Section 6.1 - First two paragraphs modified.
28. Section 6.3 - "or system BIOS" added to item 3. All items marked with an * deleted.
29. Section 6.4 - (VPMODE) deleted from last paragraph.
30. Section 6.4.1 - CPU Speed changed to RAS Timeout.
31. Section 6.4.5.1 - Opening statement deleted.
32. Section 6.4.8 - Bits 1 and 0 switched.
33. Section 6.4.9 - Cross reference added to bits 6:4
34. Section 6.5 - Bits 15:14 = 10 and 11 reserved.
35. Section 7.1 - Video replaced on-board memory.
36. Section 7.2 - NOTE modified.
37. Section 8.1 - a) Last paragraph modified. 6. Last line modified.
38. Figure 8-1 - 8042 changed to Keyboard Controller.
39. Table 8-1 - Source column added.
40. Section 9.1 - Last paragraph modified.
41. Section 9.1.1 - New.
42. Section 9.1.2 - Was section 9.2. Bit 13 description modified.
43. Sections 9.2 - Renumbered from 9.3 through 9.10 through 9.6
44. Section 9.3 - Was section 9.7. Bits 05:01 modified.
45. Section12.1 - IO Trapping paragraph modified. ATA/IDE Hard Disk Interface paragraph, 5CH changed to C5H.
46. Section 12.3 - Items 1-3 deleted.
47. Table 14-3 - T201 modified.
48. Figure 14-1 - Caption modified.
49. Figure 14-3 - Caption modified.
50. Figure 14-4 - Caption modified.
51. Figure 14-10 - Caption modified.
52. Table 14-8 - Caption modified.
53. Figure 14-41 - Note 2 and caption modified.
54. Table 14-10 - New.
55. Table 14-11 - New.
56. Table 14-12 - New.
56. Figure 14-42 - New.
57. Table 15-2 - Pin 120 added.
58. Section 16 - New, previous section 16 renumbered to section 17.
59. Section B.9 - ESF Port Address 19FH bits 5:4 name changed. ESF Port Address 198H bits 1 and 0 switched.
60. Section B.10 - Bits 15:14, 10 and 11 reserved.
61. Index - New.

C.4 REVISION HISTORY 4

Revision History 4 identifies the changes made from the document dated 9/15/93 to the document dated 11/30/93.

The changes incorporated in the document dated 11/30/93 consist of:

1. Table 13-1 - Modified MIN, MAX for VIH, VIL and IIL. Deleted $\overline{\text{RDYIN}}$, PMCIN and DP(3:0).

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