NEC

MOS INTEGRATED CIRCUIT

μPD444012A-X

4M-BIT CMOS STATIC RAM
256K-WORD BY 16-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD444012A-X is a high speed, low power, 4,194,304 bits (262,144 words by 16 bits) CMOS static RAM.

The μPD444012A-X has two chip enable pins (/CE1, CE2) to extend the capacity.

The μPD444012A-X is packed in 48-pin plastic TSOP (I).

Features

- 262,144 words by 16 bits organization
- Fast access time: 55, 70, 85, 100, 120, 150 ns (MAX.)
- Byte data control: /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Low voltage operation
  (B version: V_{CC} = 2.7 to 3.6 V, C version: V_{CC} = 2.2 to 3.6 V, D version: V_{CC} = 1.8 to 3.6 V)
- Operating ambient temperature: T_A = –25 to +85 °C
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply Voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.)
μPD444012A-BxxX	55, 70, 85, 100	2.7 to 3.6	–25 to +85	40 Note	7	TBD
μPD444012A-CxxX	70, 85, 100, 120	2.2 to 3.6		40		
μPD444012A-DxxX	100, 120, 150	1.8 to 3.6				

Note Cycle time ≥ 70 ns. μPD444012A-B55X : TBD

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Document No. M14464EJ1V0DS00 (1st edition)
Date Published September 1999 NS CP (K)
Printed in Japan

© NEC Corporation 1999

Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
μPD444012AGY-B55X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	55	2.7 to 3.6	−25 to +85	B version
μPD444012AGY-B55X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-B70X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	70			
μPD444012AGY-B70X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-B85X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	85			
μPD444012AGY-B85X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-B10X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	100			
μPD444012AGY-B10X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-C70X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	70	2.2 to 3.6		C version
μPD444012AGY-C70X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-C85X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	85			
μPD444012AGY-C85X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-C10X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	100			
μPD444012AGY-C10X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-C12X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	120			
μPD444012AGY-C12X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-D10X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	100	1.8 to 3.6		D version
μPD444012AGY-D10X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-D12X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	120			
μPD444012AGY-D12X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012AGY-D15X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	150			
μPD444012AGY-D15X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				

Pin Configurations (Marking Side)

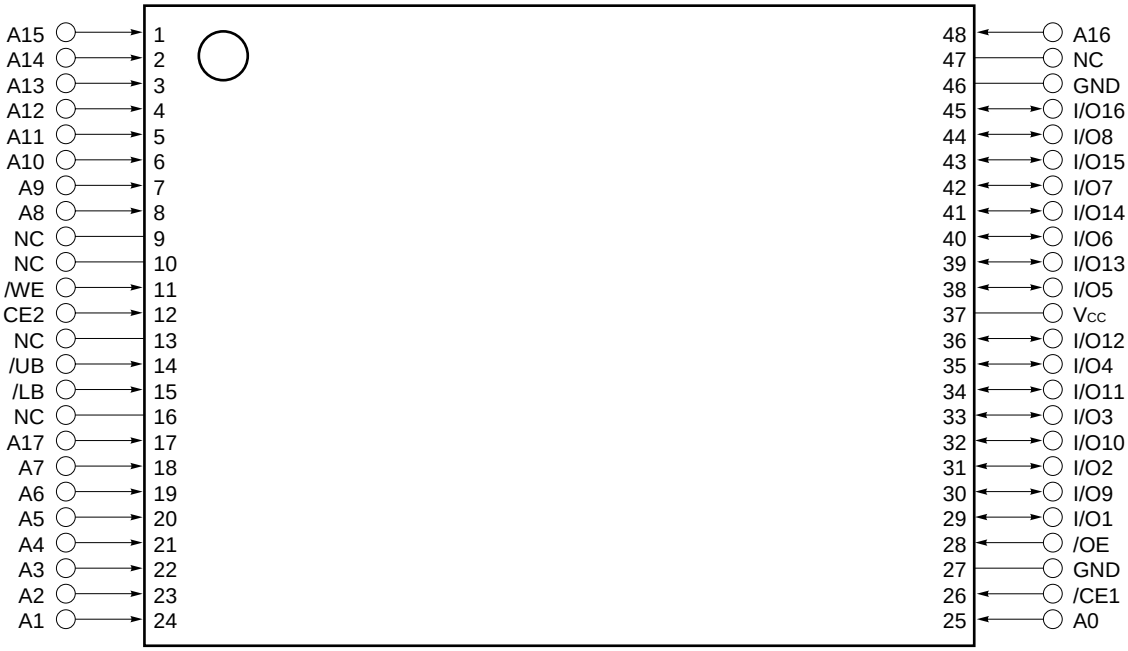
/xxx indicates active low signal.

48-pin Plastic TSOP (I) (12×18 mm) (Normal Bent)

[μPD444012AGY-BxxX-MJH]

[μPD444012AGY-CxxX-MJH]

[μPD444012AGY-DxxX-MJH]



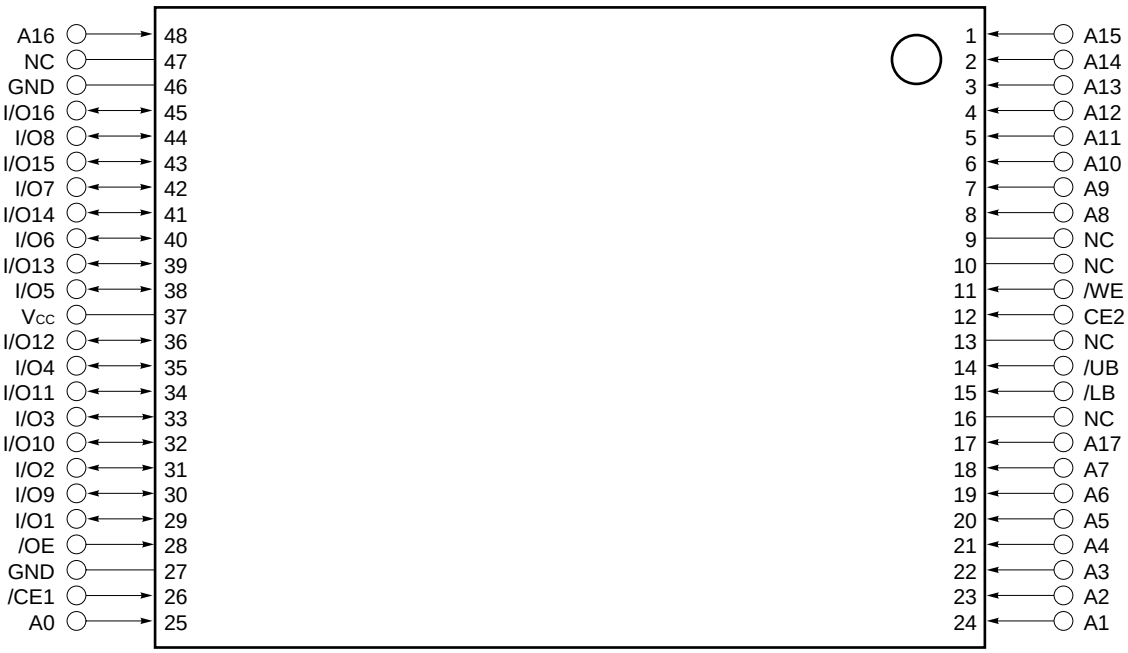
A0 - A17	:	Address inputs
I/O1 - I/O16	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
/LB, /UB	:	Byte data select
V_{CC}	:	Power supply
GND	:	Ground
NC	:	No Connection

48-pin Plastic TSOP (I) (12×18 mm) (Reverse Bent)

[μPD444012AGY-BxxX-MKH]

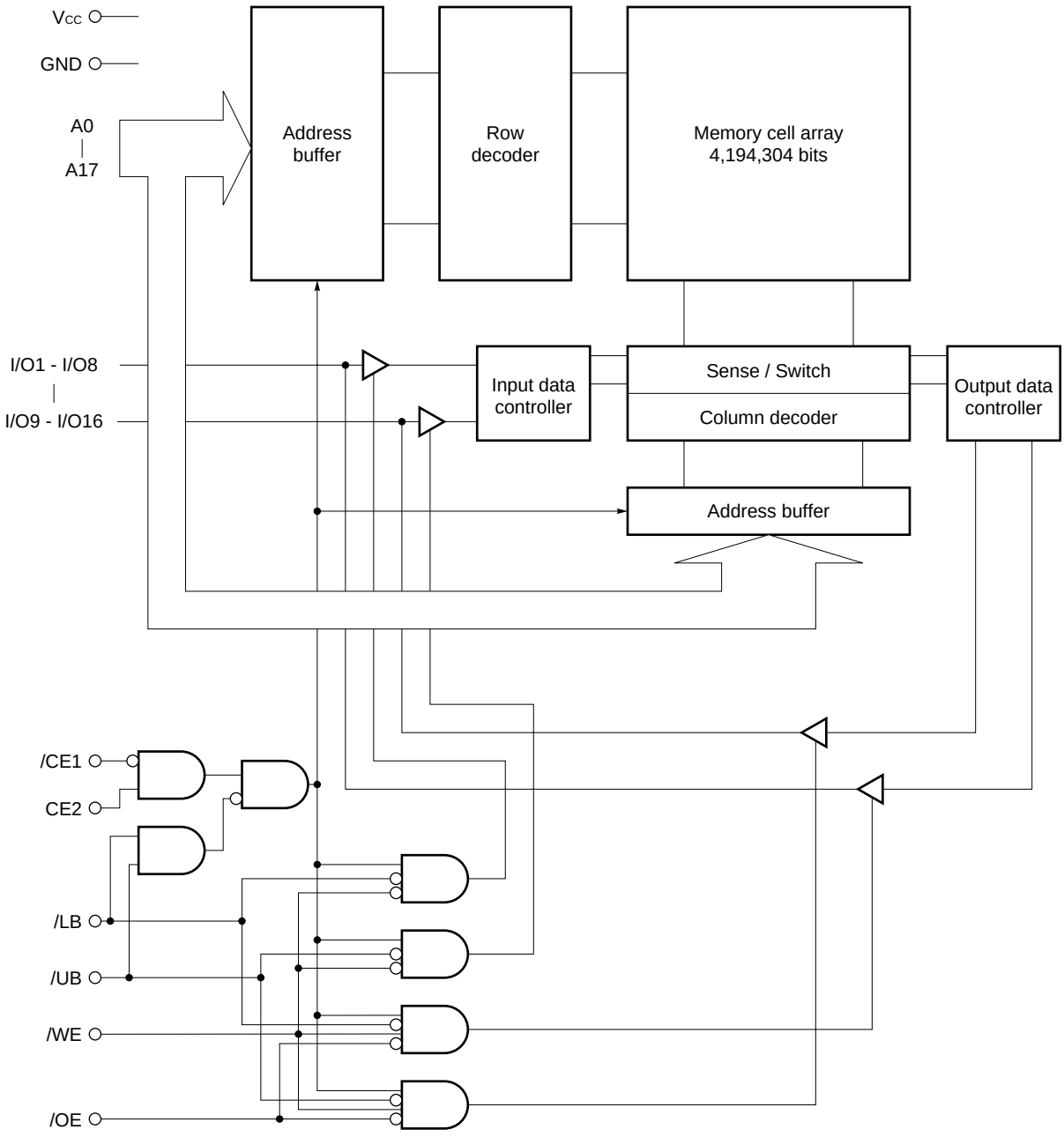
[μPD444012AGY-CxxX-MKH]

[μPD444012AGY-DxxX-MKH]



A0 - A17	:	Address inputs
I/O1 - I/O16	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
/LB, /UB	:	Byte data select
VCC	:	Power supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
							I/O1 - I/O8	I/O9 - I/O16	
H	×	×	×	×	×	Not selected	High impedance	High impedance	I_{SB}
×	L	×	×	×	×				
L	H	H	H	×	×	Output disable	High impedance	High impedance	I_{CCA}
		L	H	L	L	Word read	D_{OUT}	D_{OUT}	
				L	H	Lower byte read	D_{OUT}	High impedance	
				H	L	Upper byte read	High impedance	D_{OUT}	
		×	L	L	L	Word write	D_{IN}	D_{IN}	
				L	H	Lower byte write	D_{IN}	High impedance	
				H	L	Upper byte write	High impedance	D_{IN}	
×	×	×	×	H	H	Not selected	High impedance	High impedance	I_{SB}[Note]

Note /CE1, CE2 = V_{IH} or V_{IL}

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 [Note] to +4.0	V
Input / Output voltage	V_T		–0.5 [Note] to V_{CC} + 0.4 (4.0 V MAX.)	V
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD444012A-BxxX		μPD444012A-CxxX		μPD444012A-DxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	3.6	V
High level input voltage	V_{IH}	2.7 V ≤ V_{CC} ≤ 3.6 V	2.4	V_{CC}+0.4	2.4	V_{CC}+0.4	2.4	V_{CC}+0.4	V
		2.2 V ≤ V_{CC} < 2.7 V	–	–	2.0	V_{CC}+0.3	2.0	V_{CC}+0.3	
		1.8 V ≤ V_{CC} < 2.2 V	–	–	–	–	1.6	V_{CC}+0.2	
Low level input voltage	V_{IL}		–0.3 [Note]	+0.5	–0.3 [Note]	+0.3	–0.3 [Note]	+0.2	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	°C

Note –1.5 V (MIN.) (Pulse width: 30 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN} : Input voltage

2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		$V_{CC} \geq 2.7$ V			$V_{CC} \geq 2.2$ V			$V_{CC} \geq 1.8$ V			Unit
				μPD444012A-BxxX			μPD444012A-CxxX			μPD444012A-DxxX			
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH},			–	40[Note]		–	40		–	40	mA
		Minimum cycle time, $I_{I/O}$ = 0 mA	$V_{CC} \leq 2.7$ V		–	–		–	38		–	38	
			$V_{CC} \leq 2.2$ V		–	–		–	–		–	35	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH},			–	10		–	10		–	10	
		$I_{I/O}$ = 0 mA	$V_{CC} \leq 2.7$ V		–	–		–	8		–	8	
			$V_{CC} \leq 2.2$ V		–	–		–	–		–	6	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA,			–	8		–	8		–	8	
		$V_{IL} \leq 0.2$ V,	$V_{CC} \leq 2.7$ V		–	–		–	6		–	6	
		$V_{IH} \geq V_{CC}$ – 0.2 V	$V_{CC} \leq 2.2$ V		–	–		–	–		–	6	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL} or			–	1.2		–	1.2		–	1.2	mA
		/LB = /UB = V_{IH},	$V_{CC} \leq 2.7$ V		–	–		–	1.2		–	1.2	
		/CE1, CE2 = V_{IH} or V_{IL}	$V_{CC} \leq 2.2$ V		–	–		–	–		–	1.2	
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V,			0.5	7		0.5	7		0.5	7	μA
		CE2 ≥ V_{CC} – 0.2 V	$V_{CC} \leq 2.7$ V		–	–		0.4	6		0.4	6	
			$V_{CC} \leq 2.2$ V		–	–		–	–		0.3	5	
	I_{SB2}	CE2 ≤ 0.2 V			0.5	7		0.5	7		0.5	7	
			$V_{CC} \leq 2.7$ V		–	–		0.4	6		0.4	6	
			$V_{CC} \leq 2.2$ V		–	–		–	–		0.3	5	
	I_{SB3}	/LB = /UB ≥ V_{CC} – 0.2 V,			0.5	7		0.5	7		0.5	7	
		/CE1 ≤ 0.2 V,	$V_{CC} \leq 2.7$ V		–	–		0.4	6		0.4	6	
		CE2 ≥ V_{CC} – 0.2 V	$V_{CC} \leq 2.2$ V		–	–		–	–		0.3	5	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			2.4			2.4			V
			$V_{CC} \leq 2.7$ V	–			1.8			1.8			
			$V_{CC} \leq 2.2$ V	–			–			1.5			
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4			0.4			0.4	V

Note Cycle time ≥ 70 ns. μPD444012A-B55X : TBD

Remarks 1. V_{IN} : Input voltage

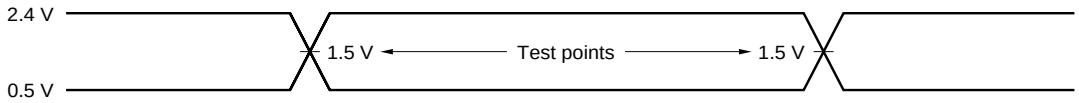
2. These DC characteristics are in common regardless of package types and access time.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

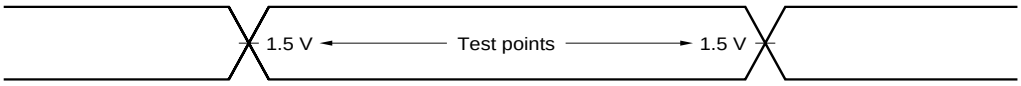
AC Test Conditions

[μPD444012A-B55X, μPD444012A-B70X, μPD444012A-B85X, μPD444012A-B10X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

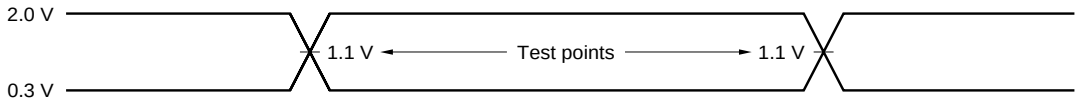


Output Load

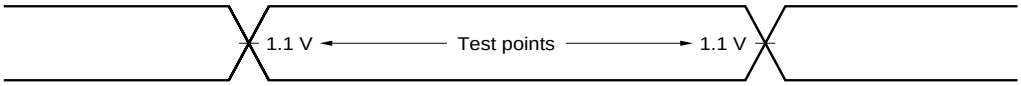
1TTL + 50 pF

[μPD444012A-C70X, μPD444012A-C85X, μPD444012A-C10X, μPD444012A-C12X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

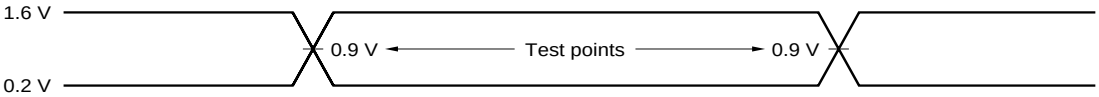


Output Load

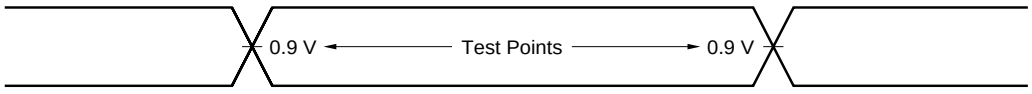
1TTL + 30 pF

[μPD444012A-D10X, μPD444012A-D12X, μPD444012A-D15X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 30 pF

Read Cycle (1/3) (B version)

Parameter	Symbol	$V_{CC} \geq 2.7$ V								Unit	Condition
		μPD444012A -B55X		μPD444012A -B70X		μPD444012A -B85X		μPD444012A -B10X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	55		70		85		100		ns	
Address access time	t_{AA}		55		70		85		100	ns	**Note 1**
/CE1 access time	t_{CO1}		55		70		85		100	ns	
CE2 access time	t_{CO2}		55		70		85		100	ns	
/OE to output valid	t_{OE}		30		35		40		50	ns	
/LB, /UB to output valid	t_{BA}		55		70		85		100	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		10		ns	
/CE1 to output in high impedance	t_{HZ1}		20		25		30		35	ns	
CE2 to output in high impedance	t_{HZ2}		20		25		30		35	ns	
/OE to output in high impedance	t_{OHZ}		20		25		30		35	ns	
/LB, /UB to output in high impedance	t_{BHZ}		20		25		30		35	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (2/3) (C version)

Parameter	Symbol	$V_{CC} \geq 2.2$ V								Unit	Condition
		μPD444012A -C70X		μPD444012A -C85X		μPD444012A -C10X		μPD444012A -C12X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		120		ns	
Address access time	t_{AA}		70		85		100		120	ns	**Note 1**
/CE1 access time	t_{CO1}		70		85		100		120	ns	
CE2 access time	t_{CO2}		70		85		100		120	ns	
/OE to output valid	t_{OE}		35		40		50		60	ns	
/LB, /UB to output valid	t_{BA}		70		85		100		120	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		10		ns	
/CE1 to output in high impedance	t_{HZ1}		25		30		35		40	ns	
CE2 to output in high impedance	t_{HZ2}		25		30		35		40	ns	
/OE to output in high impedance	t_{OHZ}		25		30		35		40	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25		30		35		40	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (3/3) (D version)

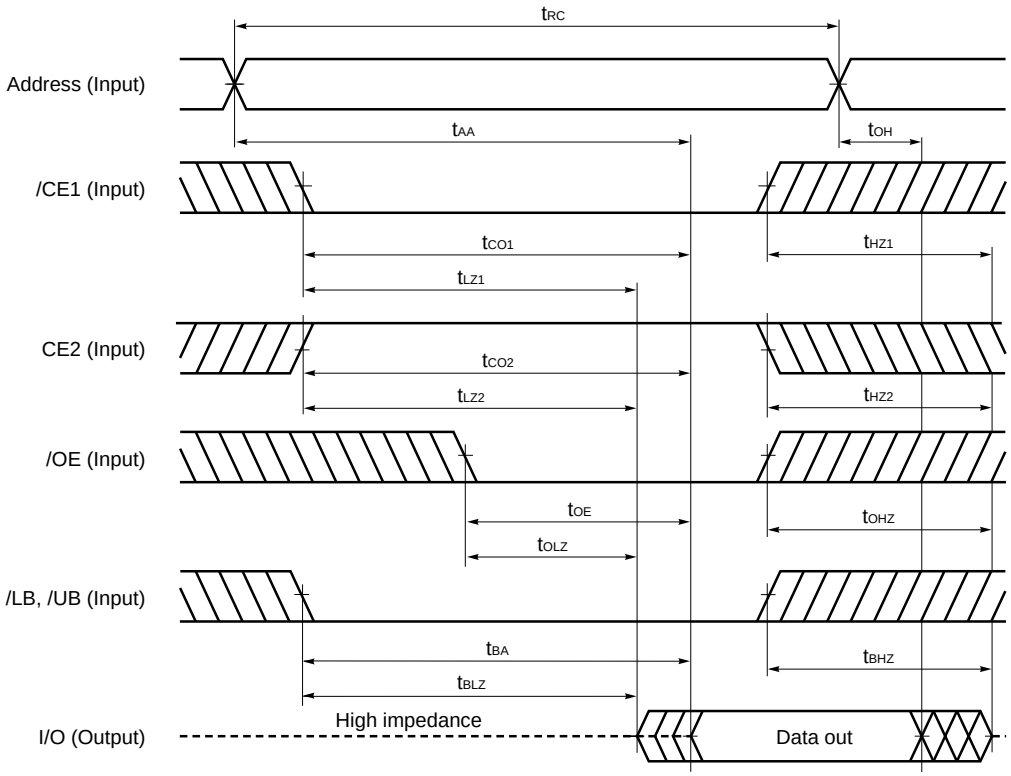
Parameter	Symbol	$V_{CC} \geq 1.8$ V						Unit	Condition
		μPD444012A -D10X		μPD444012A -D12X		μPD444012A -D15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		150		ns	
Address access time	t_{AA}		100		120		150	ns	**Note 1**
/CE1 access time	t_{CO1}		100		120		150	ns	
CE2 access time	t_{CO2}		100		120		150	ns	
/OE to output valid	t_{OE}		50		60		70	ns	
/LB, /UB to output valid	t_{BA}		100		120		150	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		ns	
/CE1 to output in high impedance	t_{HZ1}		35		40		50	ns	
CE2 to output in high impedance	t_{HZ2}		35		40		50	ns	
/OE to output in high impedance	t_{OHZ}		35		40		50	ns	
/LB, /UB to output in high impedance	t_{BHZ}		35		40		50	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/3) (B version)

Parameter	Symbol	$V_{CC} \geq 2.7$ V								Unit	Condition
		μPD444012A-B55X		μPD444012A-B70X		μPD444012A-B85X		μPD444012A-B10X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	55		70		85		100		ns	
/CE1 to end of write	t_{CW1}	50		55		70		80		ns	
CE2 to end of write	t_{CW2}	50		55		70		80		ns	
/LB, /UB to end of write	t_{BW}	50		55		70		80		ns	
Address valid to end of write	t_{AW}	50		55		70		80		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	45		50		55		60		ns	
Write recovery time	t_{WR}	0		0		0		0		ns	
Data valid to end of write	t_{DW}	25		30		35		40		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		20		25		30		35	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle (2/3) (C version)

Parameter	Symbol	$V_{CC} \geq 2.2$ V								Unit	Condition
		μPD444012A-C70X		μPD444012A-C85X		μPD444012A-C10X		μPD444012A-C12X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		120		ns	
/CE1 to end of write	t_{CW1}	55		70		80		100		ns	
CE2 to end of write	t_{CW2}	55		70		80		100		ns	
/LB, /UB to end of write	t_{BW}	55		70		80		100		ns	
Address valid to end of write	t_{AW}	55		70		80		100		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	50		55		60		85		ns	
Write recovery time	t_{WR}	0		0		0		0		ns	
Data valid to end of write	t_{DW}	30		35		40		60		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		25		30		35		40	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

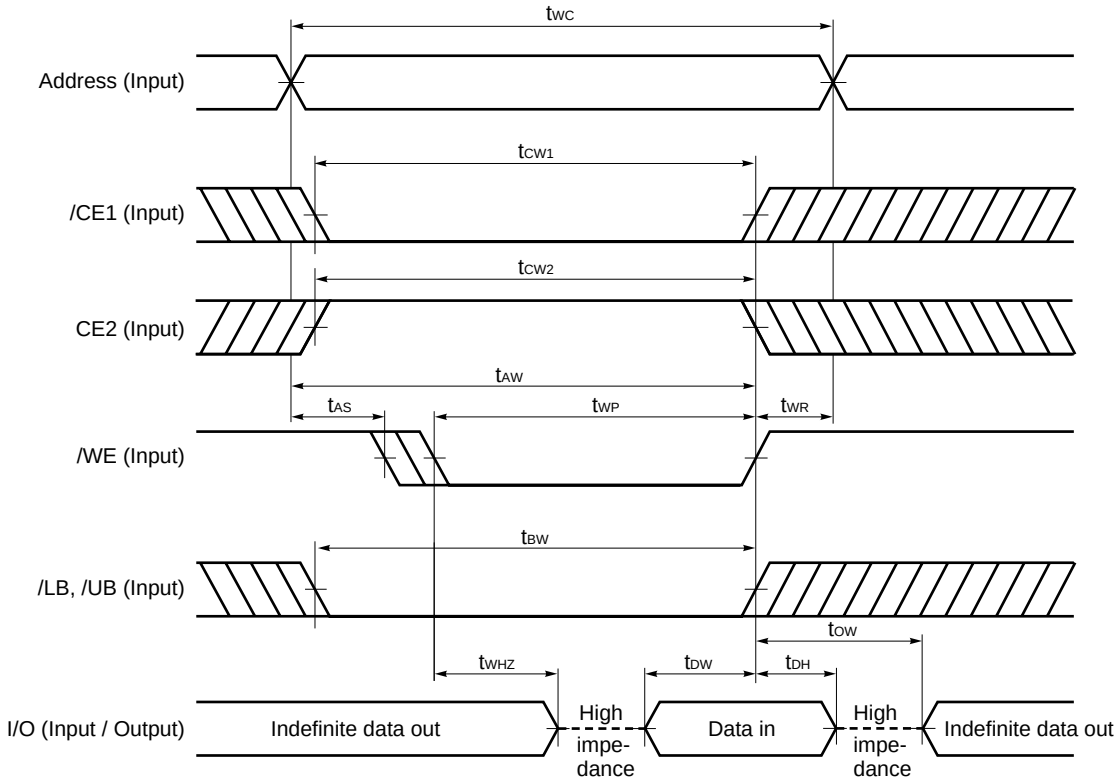
Write Cycle (3/3) (D version)

Parameter	Symbol	$V_{CC} \geq 1.8$ V						Unit	Condition
		μPD444012A -D10X		μPD444012A -D12X		μPD444012A -D15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		150		ns	
/CE1 to end of write	t_{CW1}	80		100		120		ns	
CE2 to end of write	t_{CW2}	80		100		120		ns	
/LB, /UB to end of write	t_{BW}	80		100		120		ns	
Address valid to end of write	t_{AW}	80		100		120		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	60		85		100		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	40		60		80		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		35		40		50	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

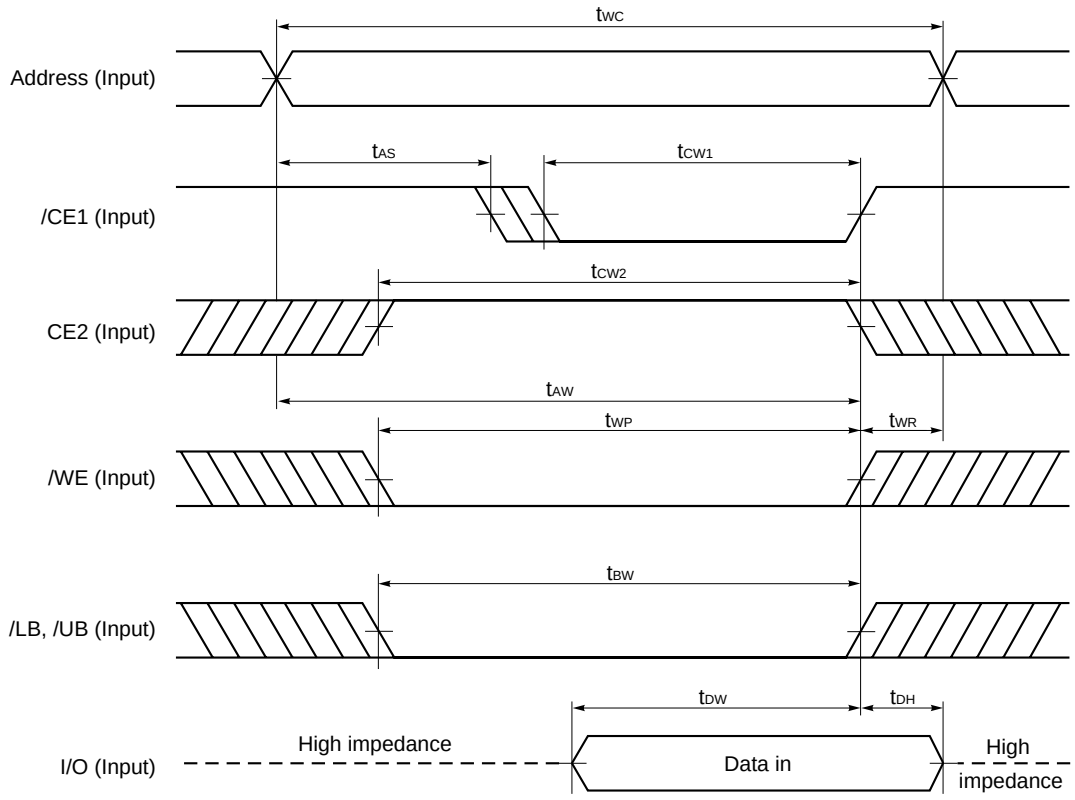
2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

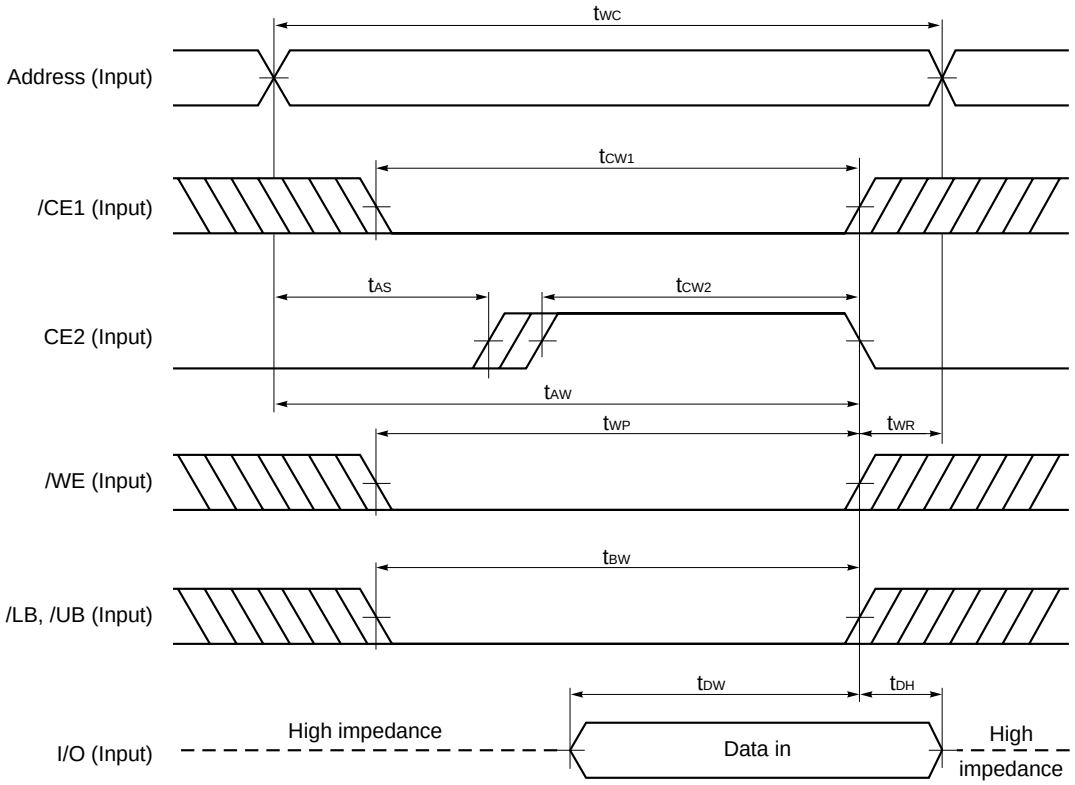


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)

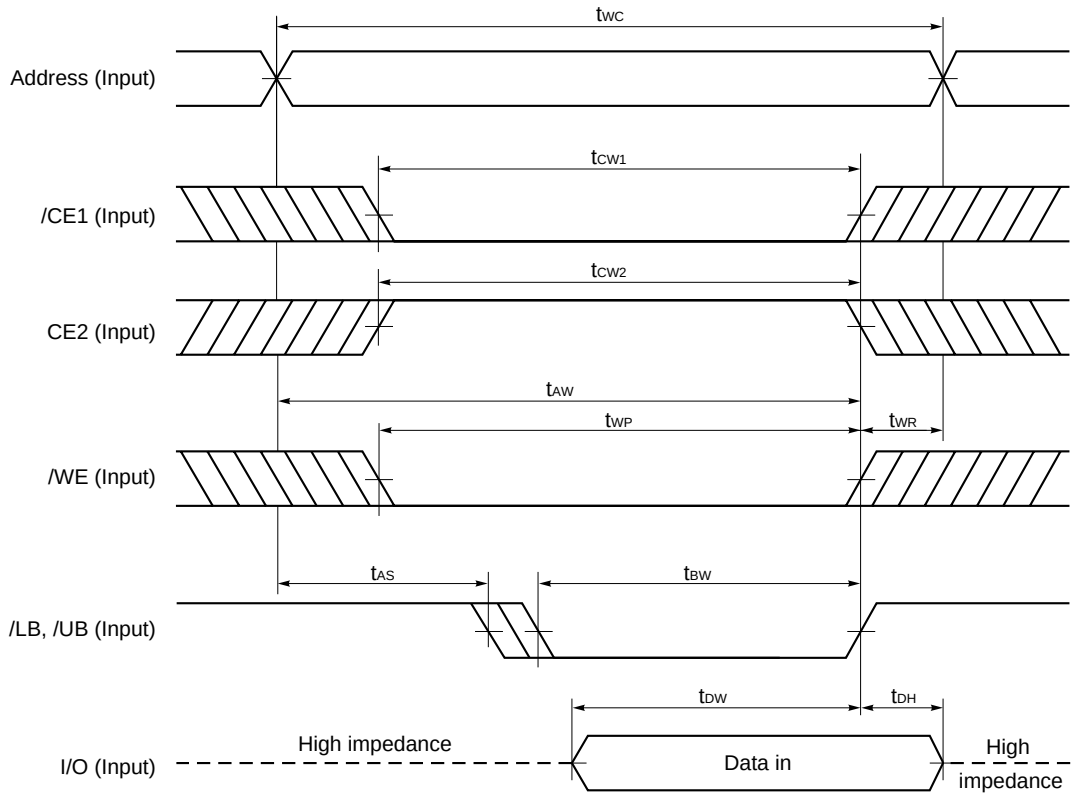


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

Write Cycle Timing Chart 4 (/LB, /UB Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

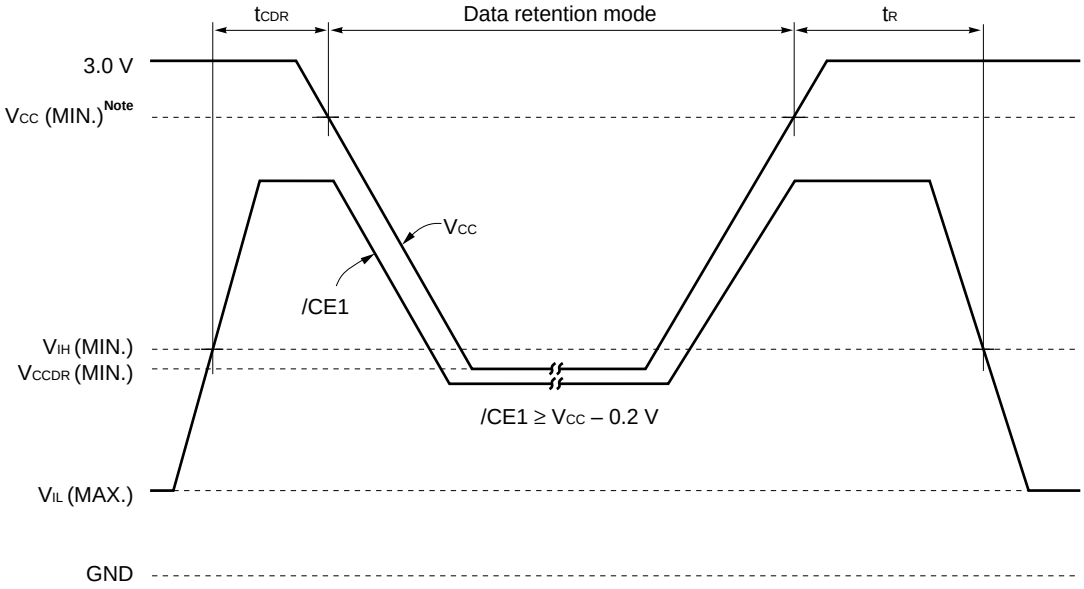
Low V_{CC} Data Retention Characteristics (T_A = –25 to +85 °C)

Parameter	Symbol	Test Condition	V_{CC} ≥ 2.7 V			V_{CC} ≥ 2.2 V			V_{CC} ≥ 1.8 V			Unit
			μPD444012A -B××X			μPD444012A -C××X			μPD444012A -D××X			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V	1.0		3.6	1.0		3.6	1.0		3.6	V
	V_{CCDR2}	CE2 ≤ 0.2 V	1.0		3.6	1.0		3.6	1.0		3.6	
	V_{CCDR3}	/LB = /UB ≥ V_{CC} – 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V	1.0		3.6	1.0		3.6	1.0		3.6	
Data retention supply current	I_{CCDR1}	V_{CC} = 1.0 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V		TBD	TBD		TBD	TBD		TBD	TBD	μA
	I_{CCDR2}	V_{CC} = 1.0 V, CE2 ≤ 0.2 V		TBD	TBD		TBD	TBD		TBD	TBD	
	I_{CCDR3}	V_{CC} = 1.0 V, /LB = /UB ≥ V_{CC} – 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V		TBD	TBD		TBD	TBD		TBD	TBD	
Chip deselection to data retention mode	t_{CDR}		0			0			0			ns
Operation recovery time	t_R		t_{RC} Note			t_{RC} Note			t_{RC} Note			ns

Note t_{RC} : Read cycle time

Data Retention Timing Chart

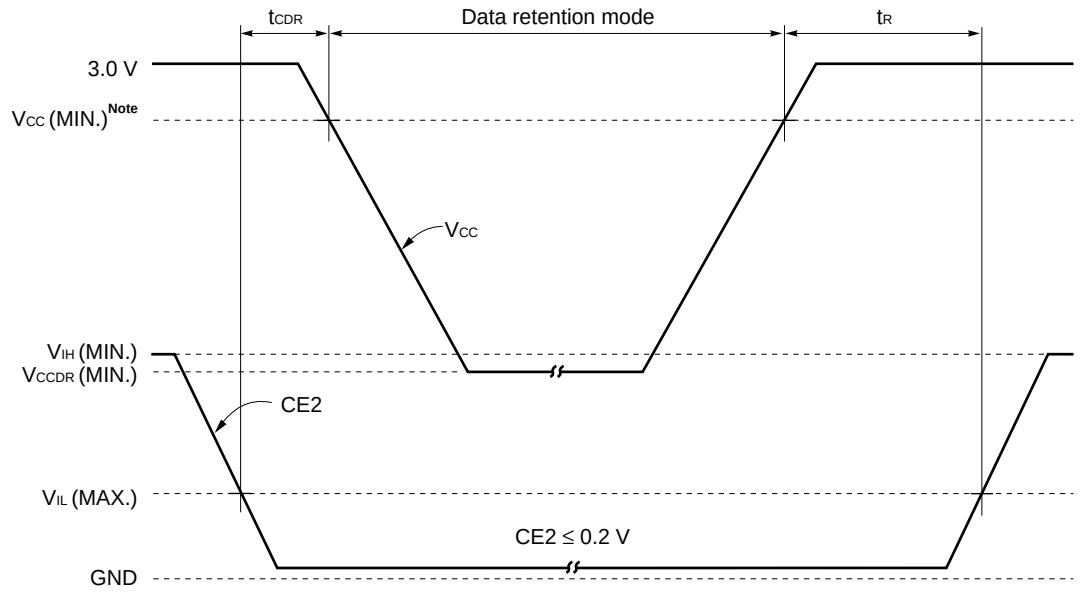
(1) /CE1 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling /CE1, the input level of CE2 must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

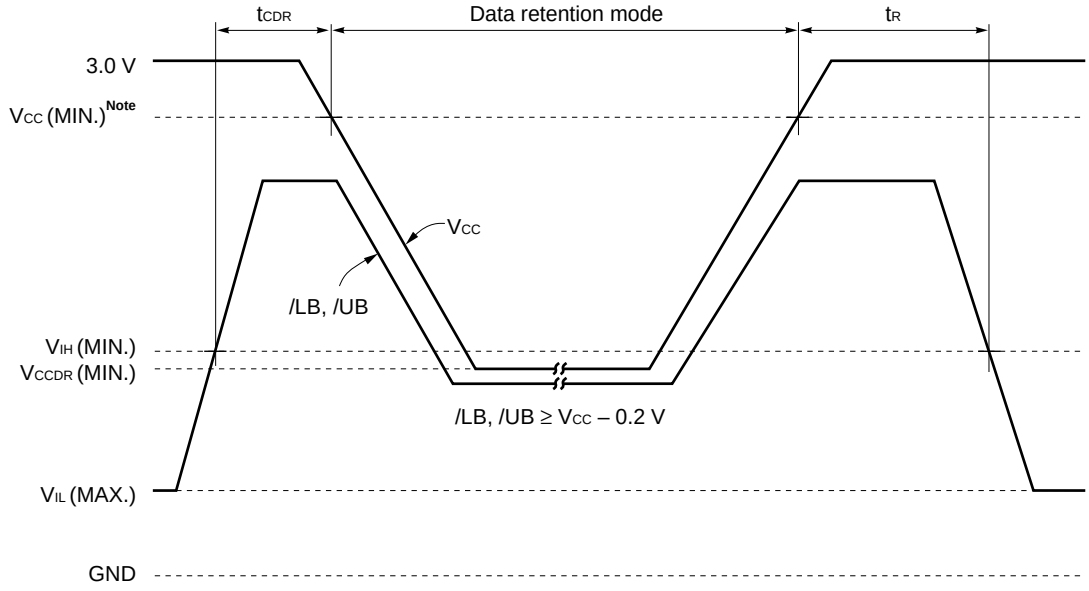
(2) CE2 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark The other pins (/CE1, Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

(3) /LB, /UB Controlled

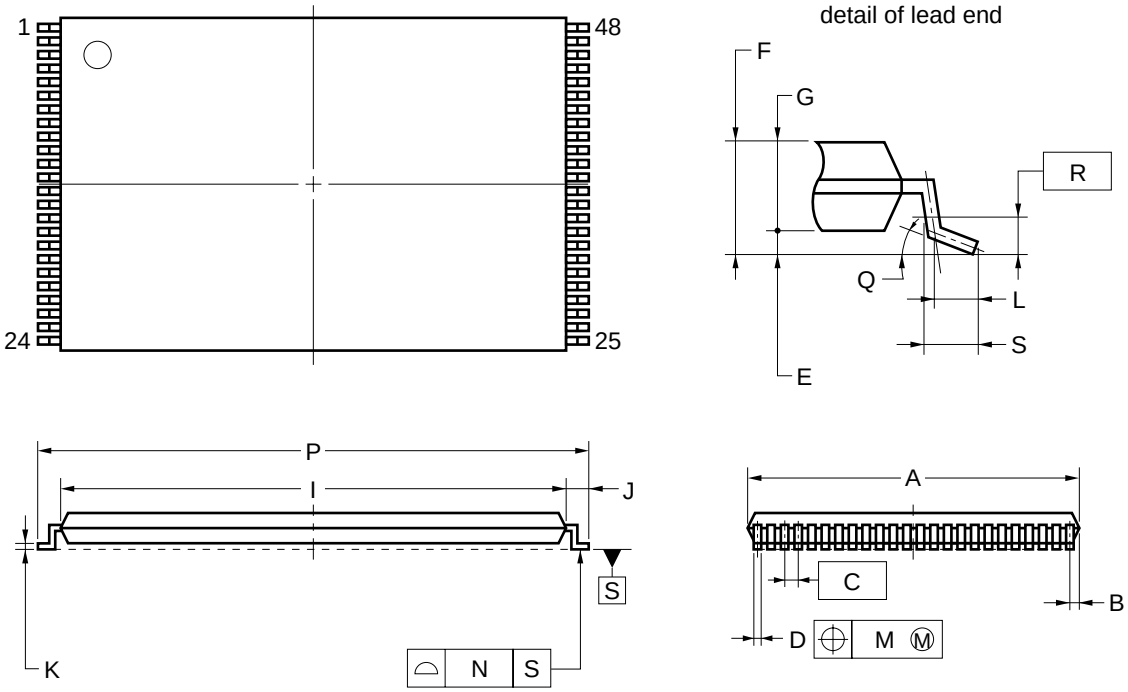


Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling /LB and /UB, the input level of /CE1 and CE2 must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

48-PIN PLASTIC TSOP(I) (12x18)



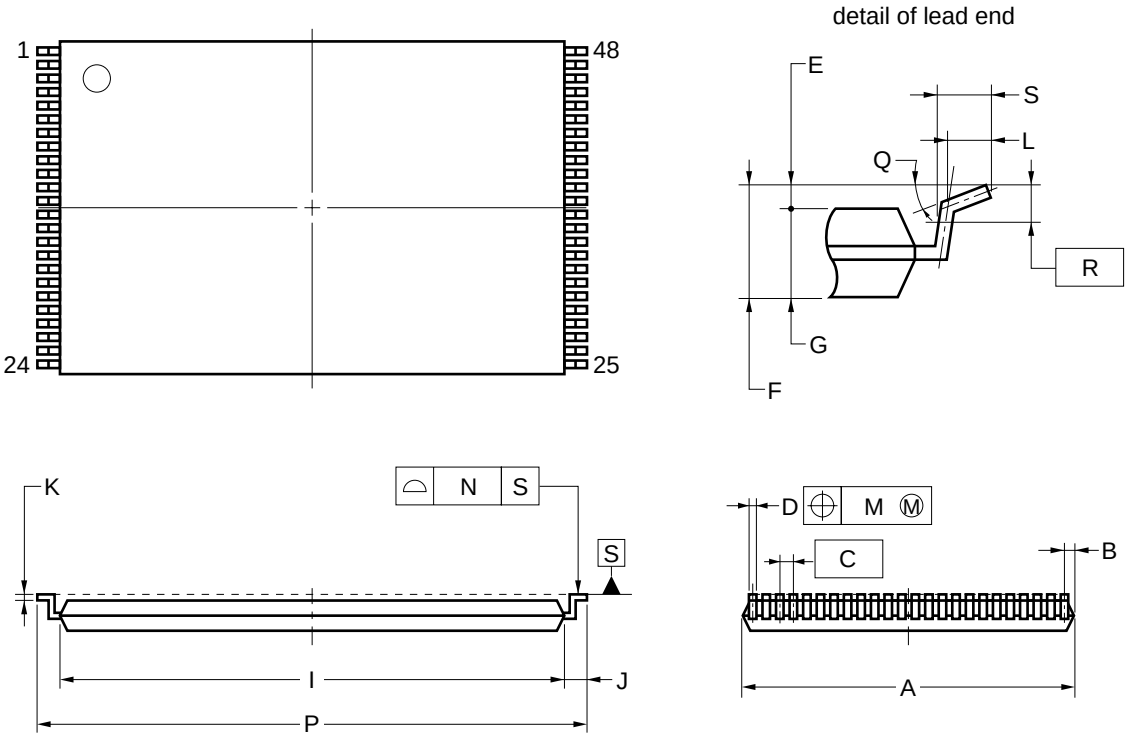
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GY-50-MJH1-1

48-PIN PLASTIC TSOP(I) (12x18)



NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GY-50-MKH1-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD444012A-X.

Types of Surface Mount Device

μPD444012AGY-BxxX-MJH: 48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)
μPD444012AGY-BxxX-MKH: 48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)
μPD444012AGY-CxxX-MJH: 48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)
μPD444012AGY-CxxX-MKH: 48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)
μPD444012AGY-DxxX-MJH: 48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)
μPD444012AGY-DxxX-MKH: 48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
- NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
- Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
- While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
- NEC devices are classified into the following three quality grades:
  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

  The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

M7 98.8