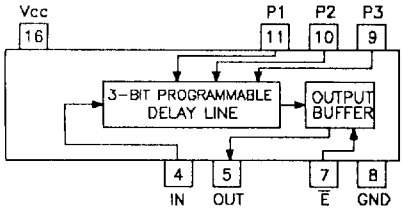
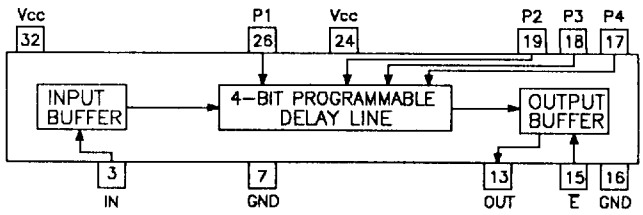
PLDM Series 3 & 4Bit Programmable TTL Delay Modules





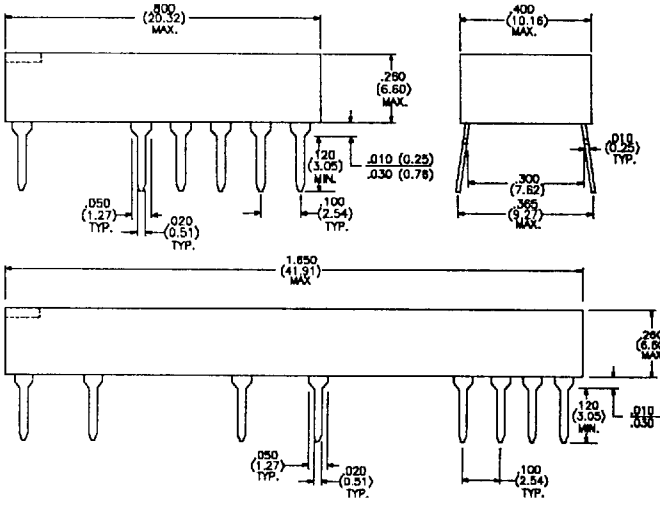
Electrical Specifications at 25°C

Part Number	Delay per Step (ns)	Output Delay (ns) per Program Setting (P3*P2*P1)								Max. Deviation ref. to 000 (ns)
		000	001	010	011	100	101	110	111	
PLDM7-0.5	0.5 ± .25	7 ± 1.0	7.5	8	8.5	9	9.5	10	10.5	± .30
PLDM7-1	1.0 ± .40	7 ± 1.0	8	9	10	11	12	13	14	± .50
PLDM7-1.5	1.5 ± .50	7 ± 1.0	8.5	10	11.5	13	14.5	16	17.5	± .70
PLDM7-2	2.0 ± .70	7 ± 1.0	9	11	13	15	17	19	21	± .80
PLDM7-2.5	2.5 ± .70	7 ± 1.0	9.5	12	14.5	17	19.5	22	24.5	± .90
PLDM7-3	3.0 ± .70	7 ± 1.0	10	13	16	19	22	25	28	± 1.0
PLDM7-3.5	3.5 ± .80	7 ± 1.0	10.5	14	17.5	21	24.5	28	31.5	± 1.0
PLDM7-4	4.0 ± .80	7 ± 1.0	11	15	19	23	27	31	35	± 1.0
PLDM7-4.5	4.5 ± 1.0	7 ± 1.0	11.5	16	20.5	25	29.5	34	38.5	± 1.5
PLDM7-5	5.0 ± 1.0	7 ± 1.0	12	17	22	27	32	37	42	± 1.5
PLDM7-8	8.0 ± 1.0	7 ± 1.0	15	23	31	39	47	55	63	± 2.5
PLDM7-10	10.0 ± 1.5	7 ± 1.0	17	27	37	47	57	67	77	± 3.0

4 Bit TTL Part Number	Delay per Step (ns)	Output Delay (ns) per Program Setting (P4*P3*P2*P1)																Max. Deviation ref. to 0000 (ns)
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
PLDM15-0.5	0.5 ± .25	15 ± 1	15.5	16.0	16.5	17.0	17.5	18.0	18.5	19.0	19.5	20.0	20.5	16.0	16.5	17.0	17.5	± 0.8
PLDM15-1	1.0 ± 0.5	15 ± 1	16.0	17.0	18.0	19.0	20.0	21.0	22.0	23.0	24.0	25.0	26.0	27.0	28.0	29.0	30.0	± 1.0
PLDM15-1.5	1.5 ± 0.6	15 ± 1	16.5	18.0	19.5	21.0	22.5	24.0	25.5	27.0	28.5	30.0	31.5	33.0	34.5	36.0	37.5	± 1.0
PLDM15-2	2.0 ± 0.7	15 ± 1	17.0	19.0	21.0	23.0	25.0	27.0	29.0	31.0	33.0	35.0	37.0	39.0	41.0	43.0	45.0	± 1.5
PLDM15-2.5	2.5 ± 0.7	15 ± 1	17.5	20.0	22.5	25.0	27.5	30.0	32.5	35.0	37.5	40.0	42.5	45.0	47.5	50.0	52.5	± 1.5
PLDM15-3	3.0 ± 0.7	15 ± 1	18.0	21.0	24.0	27.0	30.0	33.0	36.0	39.0	42.0	45.0	48.0	51.0	54.0	57.0	60.0	± 1.5
PLDM15-4	4.0 ± 0.8	15 ±1	19.0	23.0	27.0	31.0	35.0	39.0	43.0	47.0	51.0	55.0	59.0	63.0	67.0	71.0	75.0	± 3.0
PLDM15-5	5.0 ± 1.0	15 ±1	20.0	25.0	30.0	35.0	40.0	45.0	50.0	55.0	60.0	65.0	70.0	75.0	80.0	85.0	90.0	± 3.0

CUMULATIVE TOLERANCES: Maximum Deviation Tolerances for Programmed Delays Referenced to Initial Delay, Setting "0000." Tables display values of delay with respect to input, whose tolerance is the cumulative error of the initial delay (± 1.0) and the Maximum Deviation. For example, the setting "1111" delay of PLDM15-1 is 15.0 ± 1.0 ref. to "0000," and 30.0 ± 2.0 ref. to the input.

ENABLE: Enable input (Pin 7 for PLDM7, Pin 15 for PLDM15) is active low. Output will be disabled (remain low) when the Enable is high.



PHYSICAL DIMENSIONS
inches (mm)

GENERAL: For Operating Specifications and Test Conditions, see Tables I and VII on page 7 of this catalog. Delays specified for the Leading Edge. Buffered input and output.

INPUT FAN-IN: For 3 Bit PLDM7 type, input, pin 4, is loaded by the internal passive network and 8 gate inputs (74S type). Therefore, these modules are designed for pin 4 to be driven by a source that is 74S/74F type or equivalent; this output should not be used to drive any load in addition to the delay line input.

Minimum Input Pulse Width .....40% max. Delay
Temperature Coefficient..... ≤ 500 ppm/°C typical
Supply Current, I_{CC} :
PLDM7..... 60 mA typ., 80 mA max
PLDM15..... 90 mA typ., 105 mA max

VARIATIONS AVAILABLE. FOR INTERMEDIATE VALUES AND/OR CUSTOM DESIGNS PLEASE CONSULT THE FACTORY.

Specifications subject to change without notice.

PLDMX-7/93

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