1/4-Inch SOC VGA CMOS Active-Pixel Digital Image Sensor

MT9V111I29STC

Features

- Aptina® DigitalClarity® CMOS imaging technology
- System-On-a-Chip (SOC)—Completely integrated camera system
- Ultra low-power, low cost CMOS image sensor
- Superior low-light performance
- Up to 30 fps progressive scan at 27 MHz for high-quality video at VGA resolution
- On-chip Image Flow Processor (IFP) performs sophisticated processing: color recovery and correction, sharpening, gamma, lens shading correction, on-the-fly defect correction, 2X fixed zoom
- Image decimation to arbitrary size with smooth, continuous zoom and pan
- Automatic exposure, white balance and black compensation, flicker avoidance, color saturation, and defect identification and correction, auto frame rate, back light compensation
- Xenon and LED-type flash support
- Two-wire serial programming interface
- ITU_R BT.656 (YCbCr), YUV, 565RGB, 555RGB, and 444RGB output data formats

Applications

- Cellular phones
- PDAs
- PC Camera
- Toys and other battery-powered products

Table 1: Key Performance Parameters

Parameter		Value
Optical Format		1/4-inch (4:3)
Active Imager Size		3.58mm(H) x 2.69mm(V) 4.48mm (Diagonal)
Active Pixels		640H x 480V (VGA)
Pixel Size		5.6um x 5.6um
Color Filter Array		RGB Bayer Pattern
Shutter Type		Electronic Rolling Shutter (ERS)
Maximum Data Rate/ Master Clock		12—13.5 MPS/24—27 MHz
Frame Rate	VGA (640 x 480)	15 fps at 12 MHz (default), programmable up to 30 fps at 27 MHz
	CIF (352 x 288)	Programmable up to 60 fps
	QVGA (320 x 240)	Programmable up to 90 fps
ADC Resolution		10-bit, on-chip
Responsivity		1.9 V/lux-sec (550nm)
Dynamic Range		60dB
SNR_{MAX}		45dB
Supply Voltage		2.8V ±0.25V
Power Consumption		<80mW at 2.8V, 15 fps at 12MHz
Operating Temperature		-20°C to +60°C
Packaging		44-Ball ICSP, wafer or die

General Description

The Aptina® MT9V111 is a 1/4-inch VGA-format CMOS active-pixel digital image sensor, the result of combining the MT9V011 image sensor core with Aptina Imaging's third-generation digital image flow processor technology. The MT9V111 has an active imaging pixel array of 649 x 489, capturing high-quality color images at VGA resolution. The sensor is a complete camera-on-a-chip solution and is designed specifically to meet the demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

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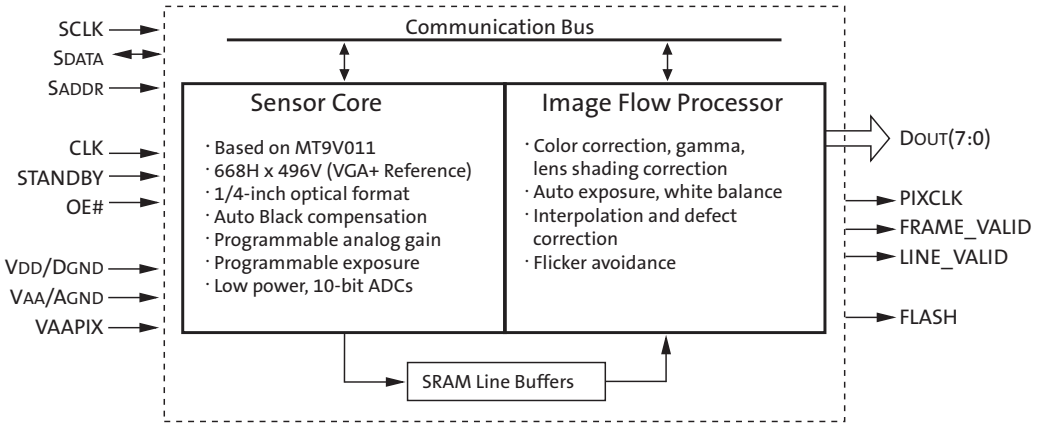
General Description

This SOC VGA CMOS image sensor features DigitalClarity—Aptina's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost and integration advantages of CMOS.

The MT9V111 is a fully-automatic, single-chip camera, requiring only a power supply, lens and clock source for basic operation. Output video is streamed via a parallel eight-bit DOUT port as shown in Figure 1. Output pixel clock is used to latch the data, while FRAME_VALID and LINE_VALID signals indicate the active video. The sensor can be put in an ultra-low power sleep mode by asserting the STANDBY pin. Output pads can also be tri-stated by de-asserting the OE# pin. The MT9V111 internal registers can be configured using a two-wire serial interface.

The MT9V111 can be programmed to output progressive scan images up to 30 fps in an 8-bit ITU_R BT.656 (YCbCr) formerly CCIR656, YUV, 565RGB, 555RGB, or 444RGB formats. The FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Figure 1: Chip Block Diagram

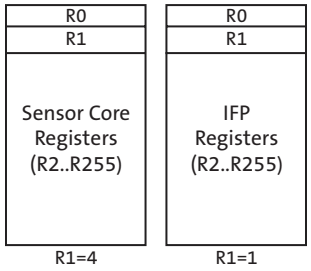


The MT9V111 can accept the input clock of up to 27 MHz, delivering 30 fps. With power-on defaults (see Appendix B for recommended defaults), the camera is configured to deliver 15 fps at 12 MHz and automatically slows down the frame rate in low-light conditions to achieve longer exposures and better image quality.

Internally, the MT9V111 consists of a sensor core and an image flow processor. The sensor core functions to capture raw Bayer-encoded images that are input into the IFP as shown in Figure 1. The IFP processes the incoming stream to create interpolated, color-corrected output and controls the sensor core to maintain the desirable exposure and color balance.

Sensor core and IFP registers are grouped into two separate address spaces, as shown in Figure 2. The internal registers can be accessed via the two-wire serial interface. Selecting the desired address space can be accomplished by programming register R1 which remains present in both register sets.

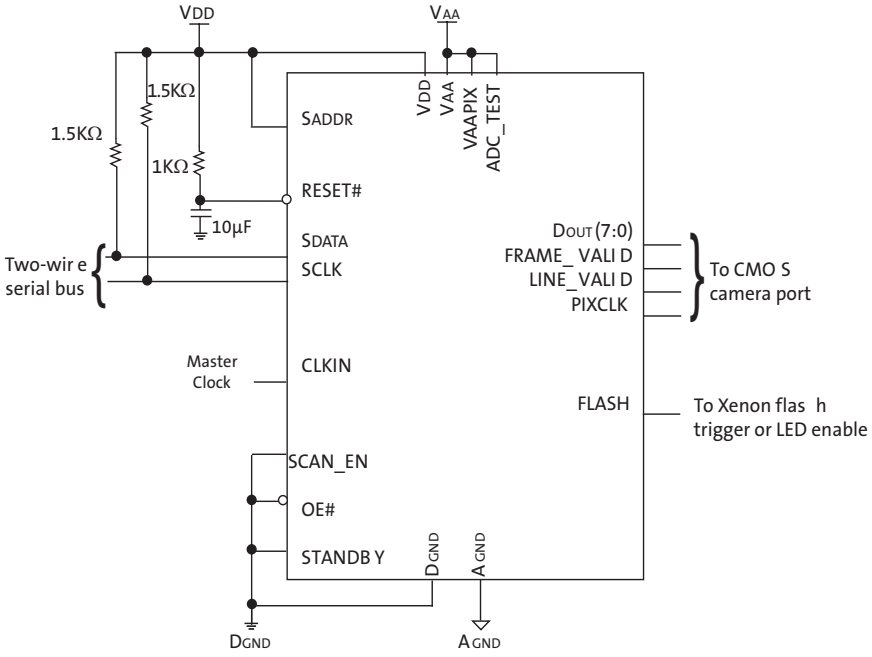
Figure 2: Internal Register Grouping



Note: Program R1 to select the desired space (4 = sensor core registes, 1 = IFP/SOC registers).

Figure 3 shows MT9V111 typical connections. For low-noise operation, the MT9V111 requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together right next to the die. Both power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

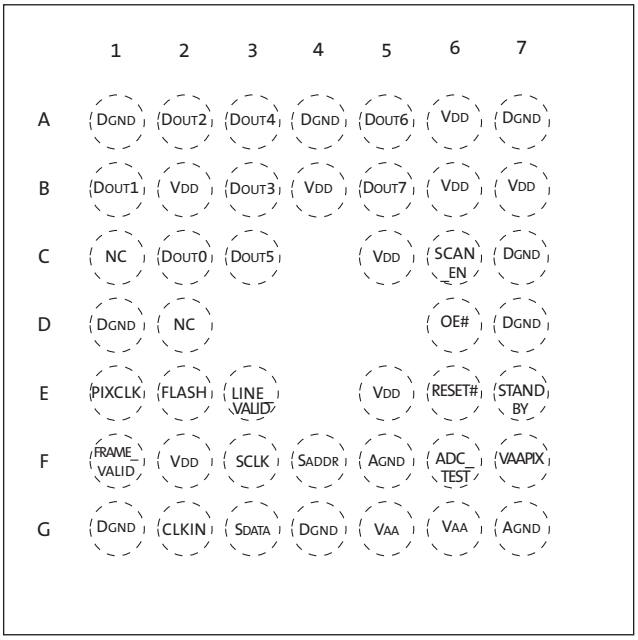
Figure 3: Typical Configuration (Connection)



Note: 1.5KΩ resistor value is recommended, but may be greater for slower two-wire speed.

Ball Assignment

Figure 4: 44-Ball ICSP Package



Top View
(Ball Down)

Table 2: Ball Description

Ball Numbers	Name	Type	Description
G2	CLKIN	Input	Master Clock into sensor. Default is 12 MHz (27 MHz maximum).
F3	SCLK	Input	Serial Clock.
F4	SADDR	Input	Serial Interface address select: Reg0xB8 when HIGH (default). Reg0x90 when LOW.
F6	ADC_TEST	Input	Tie to VAAPIX (factory use only).
E6	RESET#	Input	Asynchronous reset of sensor when LOW. All registers assume factory defaults.
E7	STANDBY	Input	When HIGH puts the imager in ultra-low power standby mode.
D6	OE#	Input	Output_Enable_Bar pin. When HIGH tri-state all outputs except SDATA (tie LOW for normal operation).
C6	SCAN_EN	Input	Tie to Digital ground.
G3	SDATA	I/O	Serial data I/O.
E2	FLASH	Output	Flash Strobe.
E1	PIXCLK	Output	Pixel Clock Out. Pixel data output are valid during rising edge of this clock. IFP Reg0x08 [9] inverts polarity. Frequency = Master Clock.
E3	LINE_VALID	Output	Active HIGH during line of selectable valid pixel data.
F1	FRAME_VALID	Output	Active HIGH during frame of valid pixel data.
B5	DOUT7	Output	ITU_R BT.656/RGB data bit 7 (MSB).
A5	DOUT6	Output	ITU_R BT.656/RGB data bit 6.

Table 2: Ball Description (continued)

Ball Numbers	Name	Type	Description
C3	DOUT5	Output	ITU_R BT.656/RGB data bit 5.
A3	DOUT4	Output	ITU_R BT.656/RGB data bit 4.
B3	DOUT3	Output	ITU_R BT.656/RGB data bit 3.
A2	DOUT2	Output	ITU_R BT.656/RGB data bit 2.
B1	DOUT1	Output	ITU_R BT.656/RGB data bit 1.
C2	DOUT0	Output	ITU_R BT.656/RGB data bit 0 (LSB).
A6,B2,B4,B6, B7,C5,E5,F2	VDD	Supply	Digital Power (2.8V).
G5,G6	VAA	Supply	Analog Power (2.8V).
F7	VAAPIX	Supply	Pixel Array Power (2.8V).
F5,G7	AGND	Supply	Analog Ground.
A1,D1,A4,A7 ,C7,D7,G1,G 4	DGND	Supply	Digital Ground.
C1,D2	NC	—	No connect.

Image Flow Processor

Overview of Architecture

The image flow processor consists of a color processing pipeline and a measurement and control logic block as shown in Figure 5. The stream of raw data from the sensor enters the pipeline and undergoes a number of transformations. Image stream processing starts from conditioning the black level and applying a digital gain. The lens shading block compensates for signal loss caused by the lens. Next, the data is interpolated to recover missing color components for each pixel and defective pixels are corrected. The resulting interpolated RGB data passes through the current color correction matrix (CCM), gamma, and saturation corrections and is formatted for final output.

The measurement and control logic continuously accumulates statistics about image brightness and color. Indoor 50/60 Hz flicker is detected and automatically updated when possible. Based on these measurements the IFP calculates updated values for exposure time and sensor analog gains, which are sent to the sensor core via the communication bus.

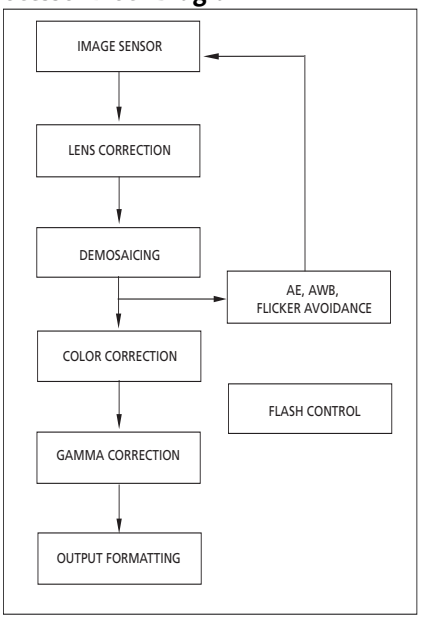
Color correction is achieved through linear transformation of the image with a 3 x 3 color correction matrix. Color saturation can be adjusted in the range from zero (black and white) to 1.25 (125% of full color saturation).

Gamma correction compensates for non-linear dependence of the display device output vs. driving signal (e.g. monitor brightness vs. CRT voltage).

Output and Formatting

Processed video can be output in the form of a standard ITU_R BT.656 or RGB stream. ITU_R BT.656 (default) stream contains 4:2:2 data with optional embedded synchronization codes. This kind of output is typically suitable for subsequent display by standard video equipment. For JPEG/MPEG compression, YUV/ encoding is suitable. RGB functionality is provided to support LCD devices. The MT9V111 can be configured to output 16-bit RGB (RGB565), 15-bit RGB (RGB555) as well as two types of 12-bit RGB (RGB444). The user can configure internal registers to swap odd and even bytes, chrominance channels and luminance and chrominance components to facilitate interface to application processors.

Figure 5: Image Flow Processor Block Diagram



The MT9V111 features smooth, continuous zoom and pan. This functionality is available when the IFP output is downsized in the decimation block. The decimation block can downsize the original VGA image to any integer size, including QVGA, QQVGA, CIF and QCIF with no loss to the field of view. The user can program the desired size of the output image in terms of horizontal and vertical pixel count. In addition the user can program the size of a region for downsizing. Continuous zoom is achieved every time the region of interest is less than the entire VGA image. The maximum zoom factor is equal to the ratio of VGA to the size of the region of interest. For example, an image rendered on a 160x120 display can be zoomed by 640/160=480/120=4 times. Continuous pan is achieved by adjusting the starting coordinates of the region of interest.

Also a fixed 2X up-zoom is implemented by means of windowing down the sensor core. In this mode the IFP receives a QVGA-sized input data and outputs a VGA-size image. The sub-window can be panned both vertically and horizontally by programming sensor core registers.

The MT9V111 supports both LED and Xenon-type flash light sources using a dedicated output pad. For Xenon devices the pad generates a strobe to fire when the imager's shutter is fully open. For LED the pad can be asserted or de-asserted asynchronously. Flash modes are configured and engaged over the two-wire serial interface using IFP Reg0x98.

Output Data Ordering

In YCbCr the first and second bytes can be swapped. Luma/chroma bytes can be swapped as well. R and B channels are bit-wise swapped when chroma swap is enabled. See IFP Reg0x3A for channel swapping configuration.

Table 3: YUV/YCbCr Output Data Ordering

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte
Default (no swap)	Cb_i	Y_i	Cr_i	Y_{i+1}
Swapped CrCb	Cr_i	Y_i	Cb_i	Y_{i+1}
Swapped YC	Y_i	Cb_i	Y_{i+1}	Cr_i
Swapped CrCb, YC	Y_i	Cr_i	Y_{i+1}	Cb_i

Table 4: RGB Output Data Ordering in Default Mode

Mode (Swap Disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
RGB 565	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
RGB 555	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G4	G3	G2	B7	B6	B5	B4	B3
RGB 444x	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
RGB x444	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

A bypass mode is available whereby raw Bayer 10-bits data is output as two bytes. See IFP Reg8[7].

Table 5: Byte Ordering in 8 + 2 Bypass Mode

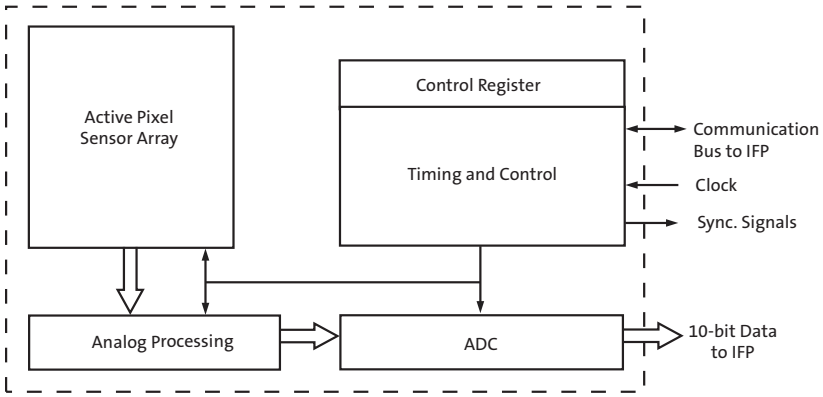
Byte Ordering									
8+2 Bypass	First	D9	D8	D7	D6	D5	D4	D3	D2
	Second	0	0	0	0	0	0	D1	D0

Sensor Core Overview

The sensor consists of a pixel array of 668 x 496 total, analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control.

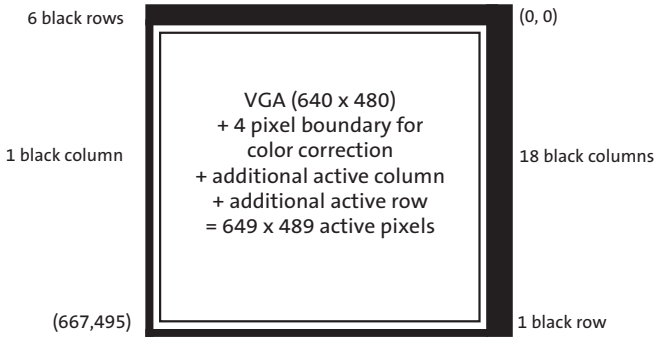
Note: See Sensor Core (MT9V011) data sheet for more details.

Figure 6: Sensor Core Block Diagram



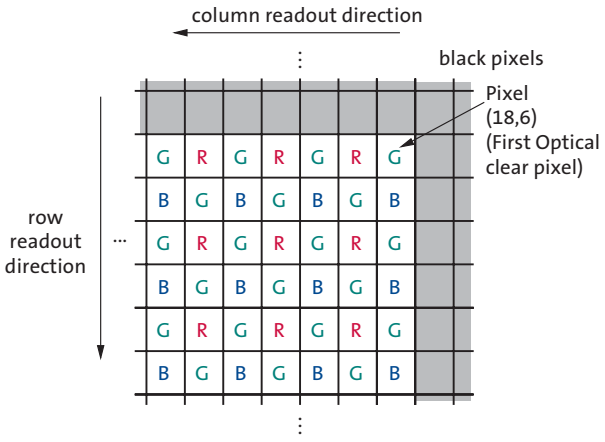
The sensor core's pixel array is configured as 668 columns by 496 rows (shown in Figure 7). The first 18 columns and the first 6 rows of pixels are optically black and can be used to monitor the black level. The last column and the last row of pixels are also optically black. The black row data is used internally for the automatic black level adjustment. There are 649 columns by 489 rows of optically active pixels, which provides a four-pixel boundary around the VGA (640 x 480) image to avoid boundary affects during color interpolation and correction. The additional active column and additional active row are used to allow horizontally and vertically mirrored readout to also start on the same color pixel, as shown in Figure 7.

Figure 7: Pixel Array Description



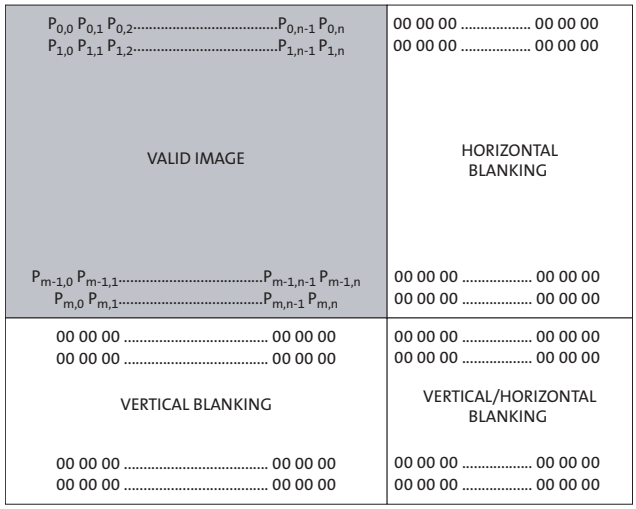
The sensor core uses the RGB Bayer color pattern (shown in Figure 8). Even-numbered rows contain green and red color pixels, and odd-numbered rows contain blue and green color pixels. Even-numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels.

Figure 8: Pixel Color Pattern Detail (Top Right Corner)



The sensor core image data is read-out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 9. The amount of horizontal and vertical blanking is programmable through the sensor core registers Reg0x05 and Reg0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. See "Appendix A – Sensor Timing" on page 19 for the description of FRAME_VALID timing.

Figure 9: Spatial Illustration of Image Readout



Notes:
1. Do not change these registers. Contact Aptina support for settings different from defaults.
2. IFP controls these registers when AE, AWE, or flicker avoidance are enabled.

Electrical Specifications

The recommended die operating temperature ranges from -20°C to +40°C. The sensor image quality may degrade above +40°C.

Table 6: DC Electrical Characteristics
$V_{DD} = V_{AA} = 2.8 \pm 0.25V$; $T_A = 25°C$

Symbol	Definition	Condition	MIN	TYP	MAX	Unit
V_{IH}	Input High Voltage		V_{DD} - 0.25		V_{DD} + 0.25	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IN}	Input Leakage Current	No Pull-up Resistor; $V_{IN} = V_{DD}$ or DGND	-5		5.0	µA
V_{OH}	Output High Voltage		V_{DD} - 0.2			V
V_{OL}	Output Low Voltage				0.2	V
I_{OH}	Output High Current				15.0	mA
I_{OL}	Output Low Current				20.0	mA
I_{OZ}	Tri-state Output Leakage Current				5.0	µA
I_{AA}	Analog Operating Supply Current	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz CLKIN = 27 MHz	 10.0 10.0	 20.0 20.0	 25.0 25.0	mA
I_{DD}	Digital Operating Supply Current	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz CLKIN = 27 MHz	 5.0 10.0	 8.0 15.0	 20.0 20.0	mA
I_{AA} Standby	Analog Standby Supply Current	STDBY = V_{DD}	0.0	2.5	5.0	µA
I_{DD} Standby	Digital Standby Supply Current	STDBY = V_{DD}	0.0	2.5	5.0	µA

Notes:
1. To place the chip in standby mode, first raise STANDBY to V_{DD}, then wait two master clock cycles before turning off the master clock. Two master clock cycles are required to place the analog circuitry into standby, low-power mode.
2. When STANDBY is de-asserted, standby mode is exited immediately (within several master clocks), but the current frame and the next two frames will be invalid. The fourth frame will contain a valid image.

Table 7: AC Electrical Characteristics

$V_{DD} = V_{AA} = 2.8 \pm 0.25V$; $T_A = 25°C$

Symbol	Definition	Condition	MIN	TYP	MAX	Unit
f_{CLKIN}	Input Clock Frequency			12	27	MHz
	Clock Duty Cycle		45	50	55	%
t_R	Input Clock Rise Time			2.0		ns
t_F	Input Clock Fall Time			2.0		ns
t_{PLHP} t_{PHLP}	CLKIN to PIXCLK propagation delay: LOW-to-HIGH HIGH-to-LOW	C_{LOAD} = 10pF		 12 10		ns
t_{DSETUP} t_{DHOLD}	PIXCLK to DOUT(7:0) at 27 MHz Setup Time Hold Time	C_{LOAD} = 10pF		 13.0 13.0		ns
t_{DSETUP} t_{DHOLD}	PIXCLK to DOUT(7:0) at 12 MHz Setup Time Hold Time	C_{LOAD} = 10pF		 25.0 25.0		ns
t_{OH}	Data Hold Time from PIXCLK falling edge			9.0		ns
$t_{PLHF,L}$ $t_{PHLF,L}$	CLKIN to FRAME_VALID and LINE_VALID propagation delay: LOW-to-HIGH HIGH-to-LOW	C_{LOAD} = 10pF		 9.0 7.5		ns
t_{OUTR}	Output Rise Time	C_{LOAD} = 10pF		7.0		ns
t_{OUTF}	Output Fall Time	C_{LOAD} = 10pF		9.0		ns

Notes: 1. For 30 fps operation with a 27 MHz clock, it is very important to have a precise duty cycle equal to 50%. With a slower frame rate and a slower clock the clock duty cycle can be relaxed.

Propagation Delays

Propagation Delays for PIXCLK and Data Out Signals

The typical output delay, relative to the master clock edge, is 7.5 ns. Note that the data outputs change on the falling edge of the master clock, with the pixel clock rising on the subsequent rising edge of the master clock.

Propagation Delays for FRAME_VALID and LINE_VALID Signals

The LINE_VALID and FRAME_VALID signals change on the same falling master clock edge as the data output. The LINE_VALID goes HIGH on the same falling master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock falling edge as the end of the output of the last valid pixel's data.

As shown in Figure 12, Data Output Timing Diagram, on page 17, FRAME_VALID goes HIGH 6 pixel clocks prior to the time that the first LINE_VALID goes HIGH. It returns LOW at a time corresponding to 6 pixel clocks after the last LINE_VALID goes LOW.

Figure 10: Propagation Delays for PIXCLK and Data Out Signals

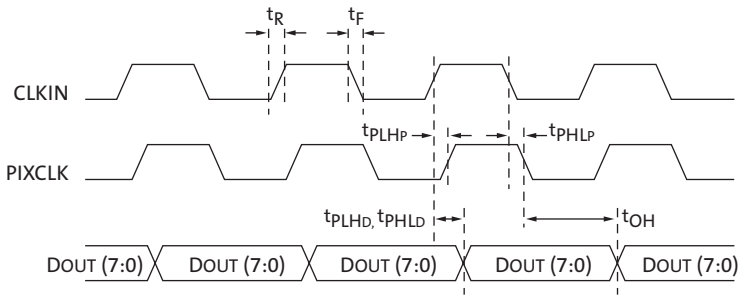


Figure 11: Propagation Delays for FRAME_VALID and LINE_VALID Signals

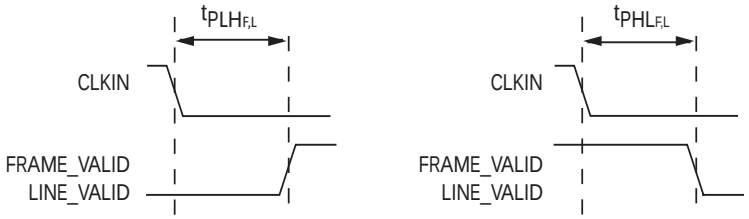
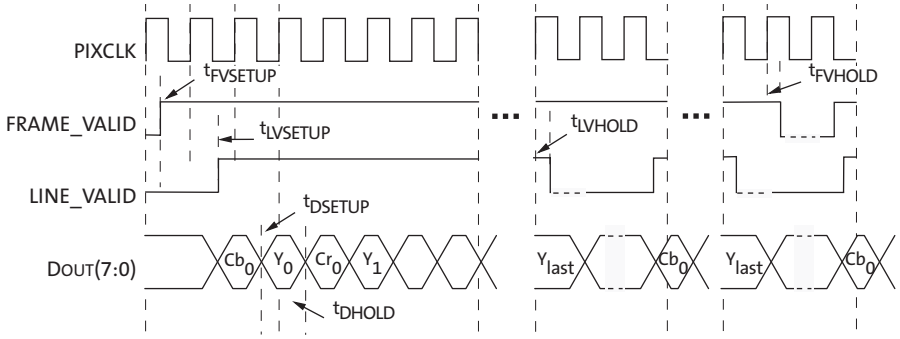


Figure 12: Data Output Timing Diagram



Note: PIXCLK = MAX 27 MHz
^{t}FVSETUP = / setup time for FRAME_VALID before rising edge of PIXCLK / = 18ns
^{t}FVHOLD = / hold time for FRAME_VALID after rising edge of PIXCLK / = 18ns
^{t}LVSETUP = / setup time for LINE_VALID before rising edge of PIXCLK / = 18ns
^{t}LVHOLD = / hold time for LINE_VALID after rising edge of PIXCLK / = 18ns
^{t}DSETUP = / setup time for DOUT before rising edge of PIXCLK / = 13ns
^{t}DHOLD = / hold time for DOUT after rising edge of PIXCLK / = 13ns
Frame start: FF00 00A0
Line start: FF00 0080
Line end: FF00 0090
Frame end: FF00 00B0

Figure 13: Spectral Response

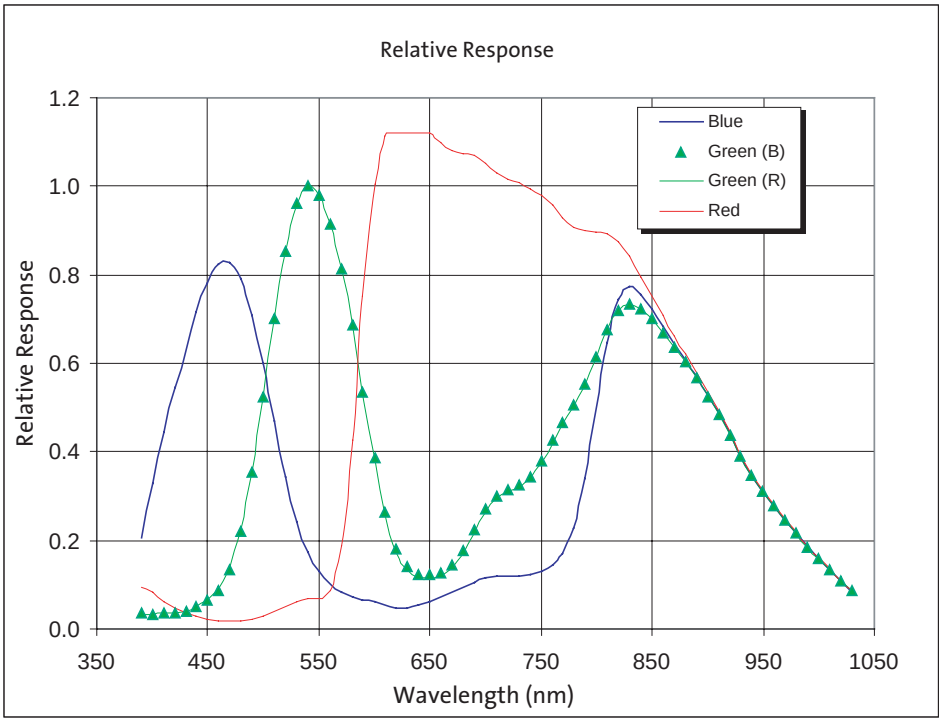
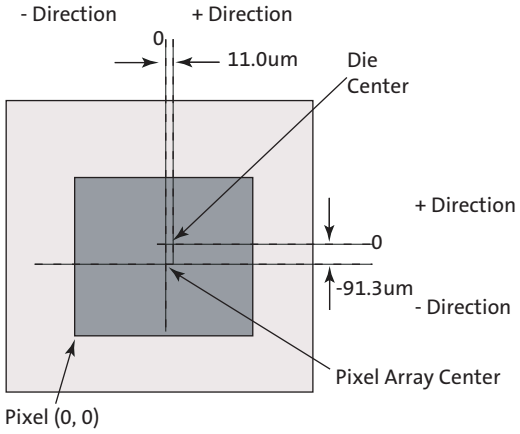


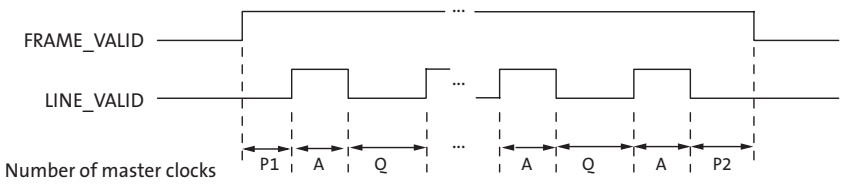
Figure 14: Die Center - Image CenterOffset



Note: Not to scale.

Appendix A – Sensor Timing

Figure 15: Row Timing and FRAME_VALID/LINE_VALID Signals



Note: The signals in Figure 15 are defined in Table 8.

Table 8: Frame Time

Parameter	Name	Equation (Master Clocks)	Default Timing At 12 MHz
A	Active Data Time	(Reg0x04 - 7) x 2	= 1,280 pixel clocks = 1,280 master clocks = 106.7us
P1	Frame Start Blanking	(Reg0x05 + 112) x 2	= 300 pixel clocks = 300 master clocks = 25.0us
P2	Frame End Blanking	14 CLKS	= 14 pixel clocks = 14 master clocks = 1.17us
Q	Horizontal Blanking	(Reg0x05 + 121) x 2 (MIN Reg0x05 value = 9)	= 318 pixel clocks = 318 master clocks = 26.5us
A + Q	Row Time	(Reg0x04 + Reg0x05 +114) x 2	= 1,598 pixel clocks = 1,598 master clocks = 133.2us
V	Vertical Blanking	(Reg0x06 + 9) x (A + Q) + (Q - P1 - P2)	= 20, 778 pixel clocks = 20,778 master clocks = 1.73ms
Nrows x (A + Q)	Frame Valid Time	(Reg0x03 - 7) x (A + Q) - (Q - P1 - P2)	= 767,036 pixel clocks = 767,036 master clocks = 63.92ms
F	Total Frame Time	(Reg0x03 + Reg0x06 + 2) x (A + Q)	= 787,814 pixel clocks = 787,814 master clocks = 65.65ms

Note: In order to avoid flicker, frame time is 65.65ms.

Sensor timing is shown above in terms of master clock cycle. The vertical blanking and total frame time equations assume that the number of integration rows (bits 11 through 0 of Reg0x09) is less than the number of active row plus blanking rows (Reg0x03 + 1 + Reg0x06 + 1). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 9.

Table 9: Frame Time—Larger than One Frame

Parameter	Name	Equation (Master Clocks)	Default Timing
V'	Vertical Blanking (long integration time)	(Reg0x09 - Reg0x03) x (A + Q)	–
F'	Total Frame Time (long integration time)	(Reg0x09 + 1) x (A + Q)	–

Serial Bus Description

Registers are written to and read from the MT9V111 through the two-wire serial interface bus. The sensor is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9V111 through the serial data (SDATA) line. The SDATA line is pulled up to 2.8V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time. The registers are 16 bits wide and can be accessed through 16-bit or eight-bit two-wire serial bus sequences.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device eight-bit address. SADDR is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xB8.
- a(n) (no) acknowledge bit
- an eight-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's eight-bit address. The last bit of the address determines if the request will be a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9V111 uses 16-bit data for its internal registers, thus requiring two eight-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and eight-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

The MT9V111 allows for eight-bit data transfers through the two-wire serial interface by writing (or reading) the most significant eight bits to the register and then writing (or reading) the least significant eight bits to Reg0x7F (127).

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A "0" in the least significant bit (LSB) of the address indicates write mode, and a "1" indicates read mode. The write address of the sensor is 0xB8, while the read address is 0xB9; this only applies when SADDR is set HIGH.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock—it can only change when the two-wire serial interface clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

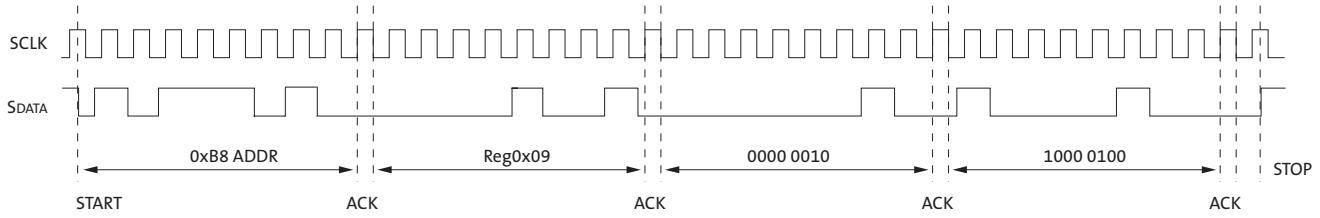
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-wire Serial Interface Sample Write and Read Sequences (with SADDR = 1)

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 16. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight-bit the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

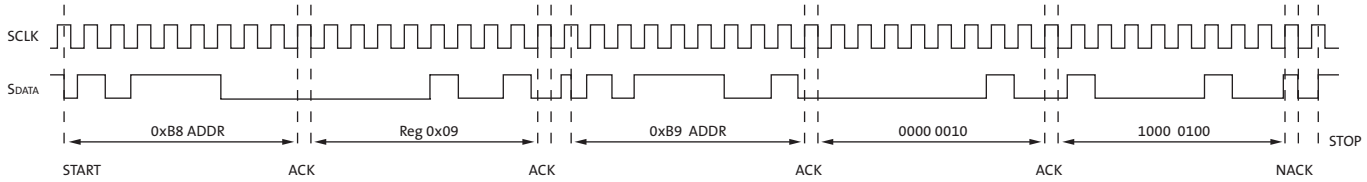
Figure 16: Timing Diagram Showing a Write to Reg0x09 with Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure . First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 17: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284

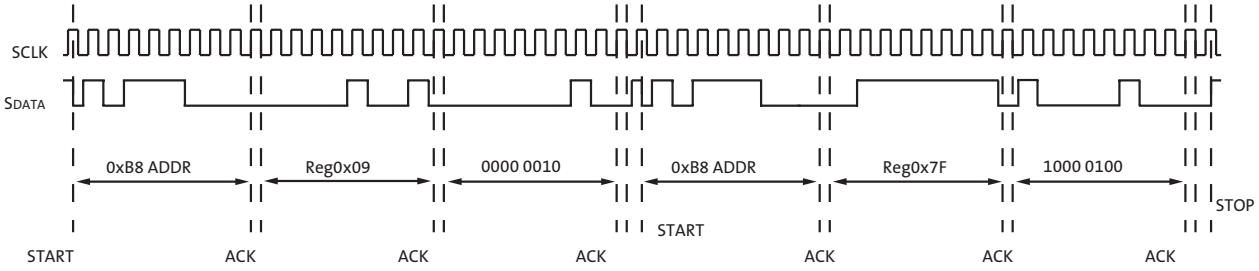


Eight-Bit Write Sequence

All registers in the camera are treated and accessed as 16-bit, even when some registers do not have all 16-bits used. However, certain hosts only support 8-bit serial communication access. The camera provides a special accommodation for these hosts.

To be able to write one byte at a time to the register a special register address is added. The 8-bit write is done by first writing the upper 8 bits to the desired register and then writing the lower 8 bits to the special register address (Reg0x7F). The register is not updated until all 16 bits have been written. It is not possible to just update half of a register. In Figure 18, a typical sequence for 8-bit writing is shown. The second byte is written to the special register (Reg0x7F).

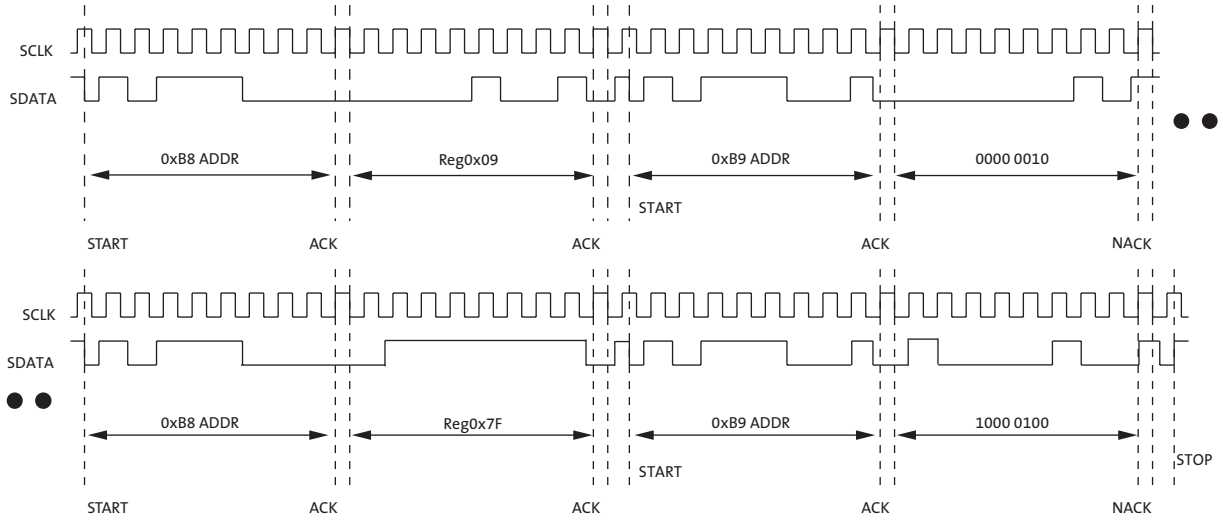
Figure 18: Timing Diagram Showing a Bytewise Write to Reg0x09 with Value 0x0284



Eight-Bit Read Sequence

To read one byte at a time the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (Reg0x7F) the lower 8 bits are accessed, as shown in Figure 19 The master sets the no-acknowledge bits.

Figure 19: Timing Diagram Showing a Bytewise Read from Reg0x09; Returned Value 0x0284



Two-wire Serial Bus Timing

The two-wire serial interface operation requires a certain minimum of master clock cycles between transitions. These are specified below in master clock cycles.

Figure 20: Serial Host Interface Start Condition Timing

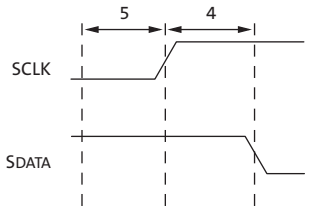
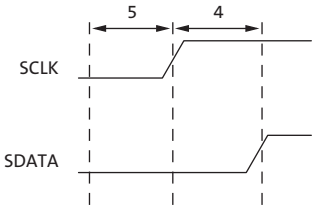
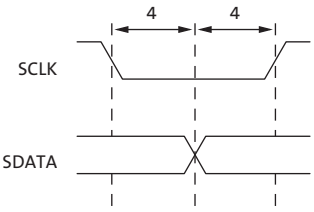


Figure 21: Serial Host Interface Stop Condition Timing



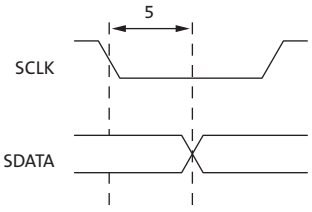
Note: All timing are in units of master clock cycle.

Figure 22: Serial Host Interface Data Timing for Write



Note: SDATA is driven by an off-chip transmitter.

Figure 23: Serial Host Interface Data Timing for Read



Note: SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 24: Acknowledge Signal Timing After an 8-bit Write to the Sensor

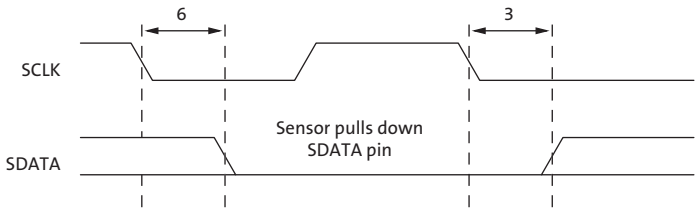
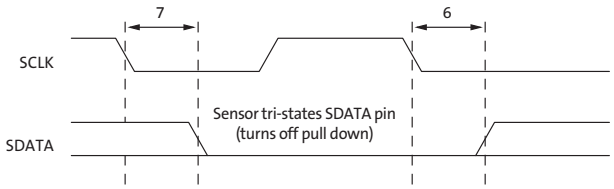


Figure 25: Acknowledge Signal Timing After an 8-bit Read from the Sensor



Note: After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Appendix B – Overview of Programming

Default Sensor Configuration

In its default configuration, the sensor outputs up to 15 fps at 12 MHz master clock frequency. Auto exposure, automatic white balance, 60Hz flicker avoidance, defect correction, and automatic noise suppression in low light conditions are enabled. The frame rate is controlled by AE and can be slowed down to 5 fps in low light. Lens shading correction is disabled. Gamma correction uses gamma = 0.6. Image data are output in YCbCr ITU_R.BT.656 VGA format, with Y, Cb, and Cr values ranging from 16 to 240.

The use of the non-default register settings shown in Table 10 are recommended to optimize sensor performance in the above configuration.

Table 10: Non-Default Register Settings Optimizing 15 fps at 12 MHz Operation

Core:	R5 = 46, R7[4] = 0, R33 = 58369, R47 = 63414
IFP:	R51= 5137, R56 = 2168, R57= 290, R59 = 1068, R62 = 4095, R64 = 7696, R65 = 5143, R66 = 4627, R67 = 4370, R68 = 28944, R69 = 29811

Note: Non-default register settings required for an optimal 30 fps, 27 MHz operation are shown in Table 11

Table 11: Non-Default Register Settings Optimizing 30 fps at 27 MHz Operation

Core:	R5 = 132, R6 = 10, R7[4] = 0, R33 = 58369
IFP:	R51 = 5137, R57 = 290, R59 = 1068, R62 = 4095, R89 = 504, R90 = 605, R92 = 8222, R93 = 10021, R100 = 4477

Note: To obtain register settings for other frame rates and clock speeds, please contact a Aptina FAE.

Auto Exposure

Target image brightness and accuracy of AE are set by IFP R46[7:0] and R46[15:8], respectively. For example, to overexpose images, set IFP R46[7:0] = 120. To change image brightness on LCD in RGB preview mode, use IFP R52[15:8]. AE logic can be programmed to keep the frame rate constant or vary it within certain range, by writing to IFP R55[9:5] one of the values tabulated in Table 12.

Table 12: Relation Between IFP R55[9:5] Setting and Frame Rate Range

Minimum Frame Rate	Maximum Frame Rate = 15 fps	Maximum Frame Rate = 30 fps
30 fps	N/A	4
15 fps	8	8
7.5 fps	16	16
5 fps	24	24

The speed of AE is set using IFP R47. The speed should be high in preview modes and lower for video output to avoid sudden changes in brightness between frames.

Auto exposure is disabled by setting IFP R6[14] = 0. When AE, AWB, and flicker avoidance are all disabled (IFP R6[14] = 0, IFP R6[1] = 0, and IFP R8[11] = 0), exposure and analog gains can be adjusted manually (see core registers R9, R12, and R43 through R46).

Automatic White Balance

AWB can be disabled by setting IFP R6[1]=0. Use IFP R37[2:0] and R37[6:3] to speed up AWB response. Please note that speeding AWB up may result in color oscillation. If necessary, AWB range can be restricted by changing the upper limit in IFP R36[14:8] and lower limit in IFP R36[6:0].

Flicker Avoidance

Use IFP R91 to choose automatic/manual, 50Hz/60Hz flicker avoidance and IFP R8[11] = 0 to disable this feature.

Flash

For flash programming, see IFP R152 description.

Decimation, Zoom, and Pan

For output decimation programming, see IFP R165 description. Table 13 provides a few examples.

Table 13: Decimation, Zoom, and Pan

Ifp Registers	CIF Output (Correct Aspect Ratio)	QVGA Output 2:1 Zoom	QVGA Output 1:1 Zoom
R165	26	160	0
R166	586	320	640
R167	352	320	320
R168	0	120	0
R169	480	240	480
R170	288	240	240

Note: For fixed 2x upsize zoom, set core R30[0] = 1.

Interpolation

Use IFP R5[2:0] to adjust image sharpness. By default, sharpness is automatically reduced in low-light conditions (see IFP R5[3]). For RGB565 16-bit capture, set IFP R6[12] = 0 and IFP R5[3] = 0 to avoid contouring.

Special Effects

To switch from color to gray scale output, set IFP R8[5] = 1. Contact a Aptina FAE for register settings producing other special effects (e.g. sepia output).

Image Mirroring

To mirror images horizontally, set core R32[14] = 1 and IFP R8[0] = 1. To flip images vertically, set core R32[15] = 1 and IFP R8[1] = 1.

Test Pattern

See IFP R72 and IFP Reg58[5:3] description.

Gamma Correction

See Table 14 and Table for register settings required to setup non-default gamma correction. Please note that these settings determine output signal range. Use YCbCr settings with ITU_R BTU-compatible devices. Use YUV settings for JPEG capture and RGB preview; switching to YUV mode requires setting IFP R52 = 0 and IFP R53 = 65281.

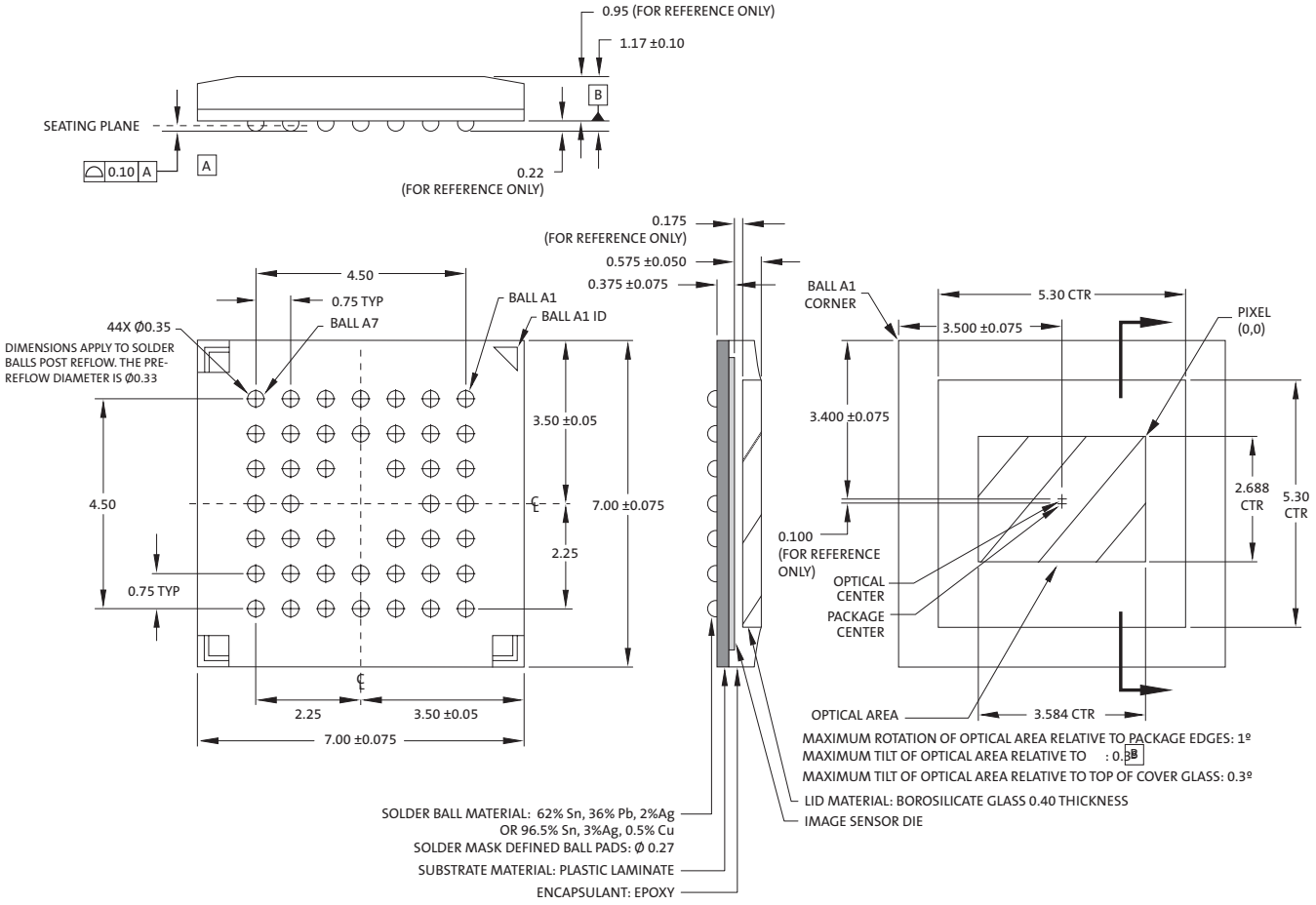
Table 14: YCbCr Settings

Gamma	0.45	0.5	0.55	0.6 (Default)	0.7	1.0
IFP R83	12836	10781	8984	7700	5389	2052
IFP R84	23876	21563	19508	17709	14627	8208
IFP R85	39039	37495	35952	34409	31581	24640
IFP R86	49326	48553	47780	47008	45207	41088
IFP R87	57552	57551	57549	57548	57545	57536

Table 15: YUV Settings

Gamma	0.45	0.5	0.55	0.6	0.7	1.0
IFP R83	14377	12321	10267	8726	6159	2308
IFP R84	26957	24643	22331	20276	16680	9234
IFP R85	44432	42631	40831	39031	35945	27720
IFP R86	56005	54976	54202	53173	51371	46481
IFP R87	65260	65259	65257	65255	65252	65241

Figure 26: 44-Ball ICSP Package Outline Drawing



Notes:
1. All dimensions in millimeters.
2. ICSP package information is preliminary.

Revision History

Rev. K 6/10

- Updated to non-confidential

Rev. J 5/10

- Updated to Aptina template
- Transfered registers to a seperate document

Rev. H, Production 6/06

- Updated Table 6, “IFP Register List,” on page 12

Rev. G, Production 1/05

- Modified ^{t}OH definition in Table 7, “AC Electrical Characteristics,” on page 15
- Updated Figure 10, Propagation Delays for PIXCLK and Data Out Signals, on page 16

Rev. F, Production 8/04

- Updated 44-Ball ICSP Package Outline Drawing

Rev. E 7/04

- Replaced 28-Pin PLCC package information with the 44-Ball ICSP
- Updated Table 12 (Frame Time)
- Updated Electrical Specifications

Rev. D, Preliminary 3/04

- Modify for external web posting - streamlined register descriptions
- Add Appendix B

Rev. C, Preliminary 2/04

- Added Key Performance Parameter Table, Update Register Tables, Update Electrical Specification Table, Added Figures (Image Center Offset, Die Placement, 28-Pin PLCC Package Outline Drawing and Spectral Response)

Rev. B, Preliminary, Draft 1/04

- Format edits on 1/15/04

Rev. A, Preliminary, Draft 12/03

- Initial Release of document

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