LH1548

240-output LCD Segment Driver IC

DESCRIPTION

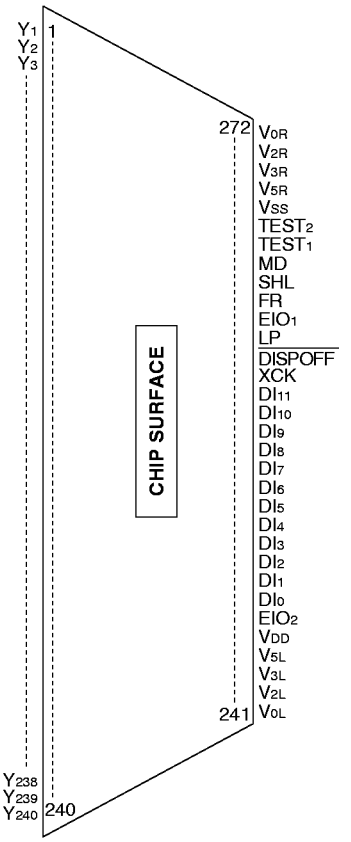
The LH1548 is a 240-output segment driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/ work stations. Through the use of UST (Ultra Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. When combined with the LH1530 common driver, it can create a low power consuming, high-resolution LCD.

FEATURES

- Number of LCD drive outputs : 240
- Supply voltage for LCD drive : +10.0 to +42.0 V
- Supply voltage for the logic system : +2.5 to +5.5 V
- Shift clock frequency
  - 25 MHz (Max.) : V_{DD} = +5.0±0.5 V
  - 15 MHz (Max.) : V_{DD} = +3.0 to +4.5 V
  - 12 MHz (Max.) : V_{DD} = +2.5 to +3.0 V
- Low power consumption
- Low output impedance
- Adopts a data bus system
- 8-bit/12-bit parallel input modes are selectable with a mode (MD) pin.
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input data
- Package : 272-pin TCP (Tape Carrier Package)

PIN CONNECTIONS

272-PIN TCP TOP VIEW

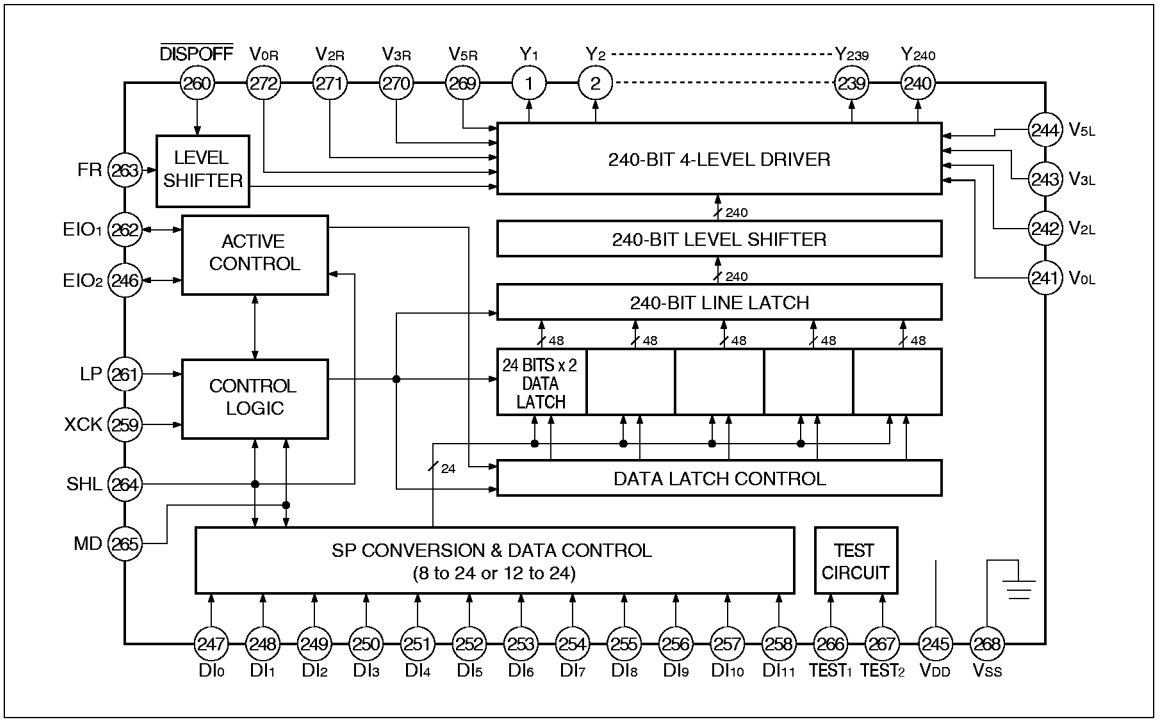


NOTE :
Doesn't prescribe TCP outline.

PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 240	Y_1-Y_{240}	O	LCD drive output
241, 272	V_{0L}, V_{0R}	–	Power supply for LCD drive
242, 271	V_{2L}, V_{2R}	–	Power supply for LCD drive
243, 270	V_{3L}, V_{3R}	–	Power supply for LCD drive
244, 269	V_{5L}, V_{5R}	–	Power supply for LCD drive
245	V_{DD}	–	Power supply for logic system (+2.5 to +5.5 V)
264	SHL	I	Input for selecting the reading direction of display data
265	MD	I	Mode selection input
246, 262	EIO_2, EIO_1	I/O	Input/output for chip selection
247 to 258	DI_0-DI_{11}	I	Display data input
259	XCK	I	Clock input for taking display data
260	$\overline{DISPOFF}$	I	Control input for output of non-select level
261	LP	I	Latch pulse input for display data
263	FR	I	AC-converting signal input for LCD drive waveform
266, 267	$TEST_1$, $TEST_2$	I	Test mode selection input
268	V_{SS}	–	Ground (0 V)

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	Controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected.
SP Conversion & Data Control	Data is retained until 24 bits have been completely input, after which they are put on the internal data bus 24 bits at a time.
Data Latch Control	Selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 48 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	Latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 240 bits of data are read in 10 sets of 24 bits.
Line Latch	All 240 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the latch data, and selects one of 4 levels (V_0, V_2, V_3 or V_5) based on the FR and $\overline{DISPOFF}$ signals.
Control Logic	Controls the operation of each block. When an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 240 bits of data are read in, and the chip is non-selected.
Test Circuit	The circuit for testing. During normal operation, it isn't activated.

INPUT/OUTPUT CIRCUITS

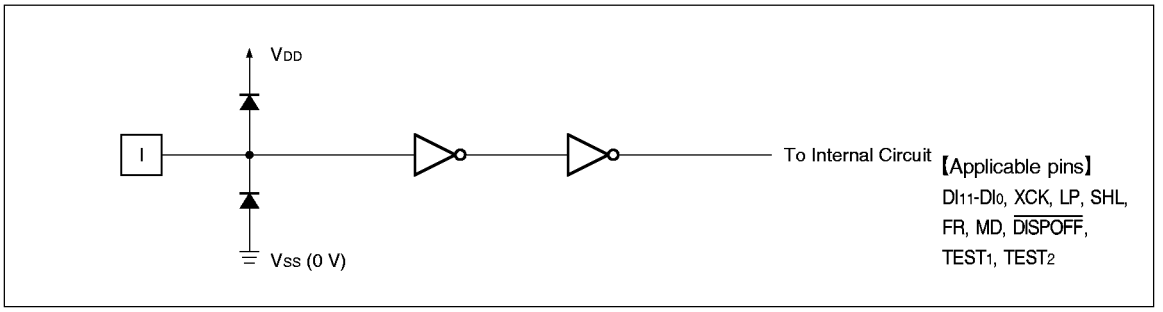


Fig. 1 Input Circuit

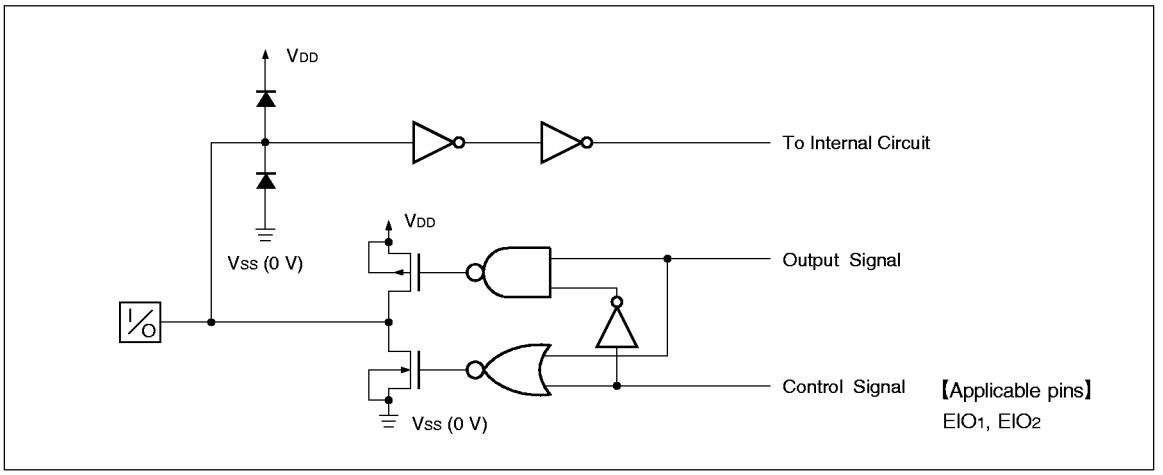


Fig. 2 Input/Output Circuit

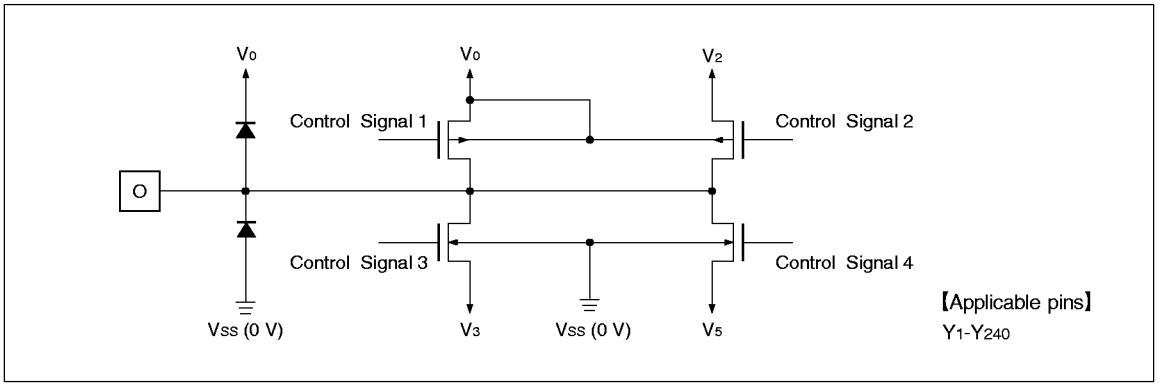


Fig. 3 LCD Drive Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{2L}, V_{2R} V_{3L}, V_{3R} V_{5L}, V_{5R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that $V_{SS} \leq V_5 < V_3 < V_2 < V_0$. • V_{iL} and V_{iR} (i = 0, 2, 3, 5) aren't connected with inside IC. Therefore, it is necessary that these pins connect with an external power supply.
DI_{11}-DI_0	Input pins for display data • In 8-bit parallel input mode, input data into the 8 pins, DI_7-DI_0. Connect DI_{11}-DI_8 to V_{SS} or V_{DD}. • In 12-bit parallel input mode, input data into the 12 pins, DI_{11}-DI_0. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
SHL	Input pin for selecting the reading direction of display data • When set to V_{SS} level "L", data is read sequentially from Y_{240} to Y_1. • When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{240}. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
$\overline{DISPOFF}$	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{240}) are set to level V_5. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD driving waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to V_{SS} level "L", 8-bit parallel input mode is set. • When set to V_{DD} level "H", 12-bit parallel input mode is set. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.

SYMBOL	FUNCTION
EIO_1 EIO_2	Input/output pins for chip selection • When SHL input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. • When SHL input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. • During output, set to "H" while LP · $\overline{XCK}$ is "H", and after 240 bits of data have been read, set to "L" for one cycle (from rising edge to rising edge of XCK), after which it returns to "H". • During input, the chip is selected while $\overline{EI}$ · $\overline{XCK}$ is "H" after the LP signal is input. The chip is non-selected after 240 bits of data have been read. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
$TEST_1$ $TEST_2$	Test mode selection pins • During normal operation, fix to V_{SS} level "L".
Y_1-Y_{240}	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_2, V_3, or V_5) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

Functional Operations

TRUTH TABLE

FR	LATCH DATA	$\overline{DISPOFF}$	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y_1-Y_{240})
L	L	H	V_3
L	H	H	V_5
H	L	H	V_2
H	H	H	V_0
X	X	L	V_5

NOTES :

- $V_{SS} \leq V_5 < V_3 < V_2 < V_0$, L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.
  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.
  Supply regular voltage which is assigned by specification for each power pin.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(a) 8-bit Parallel Input Mode

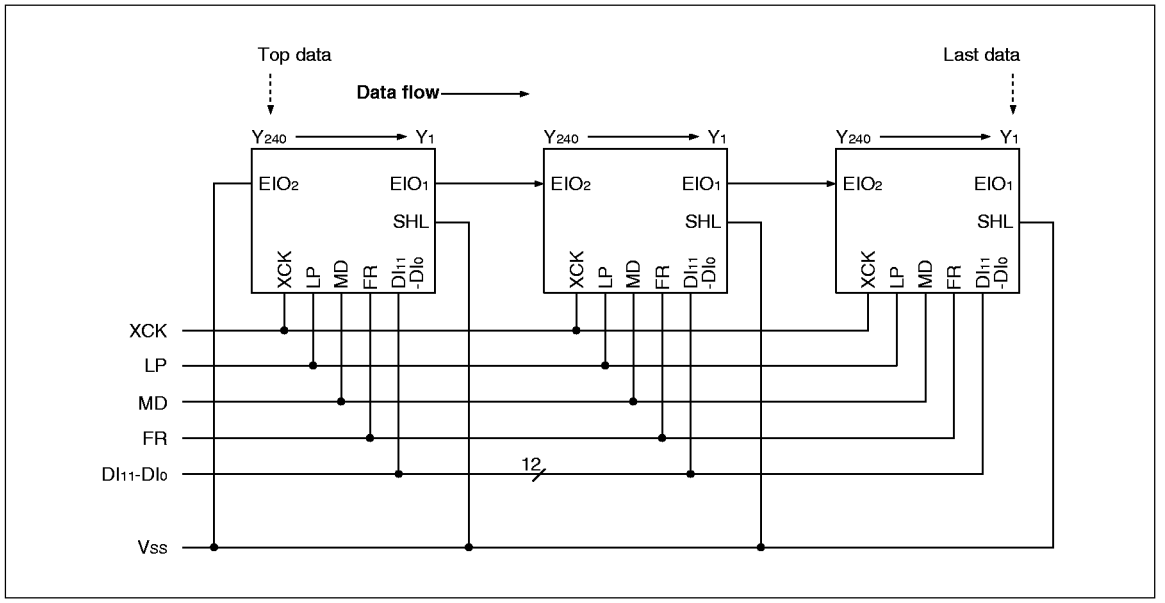
MD	SHL	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					30 CLOCK	29 CLOCK	28 CLOCK	···	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	···	Y_{217}	Y_{225}	Y_{233}
				DI_1	Y_2	Y_{10}	Y_{18}	···	Y_{218}	Y_{226}	Y_{234}
				DI_2	Y_3	Y_{11}	Y_{19}	···	Y_{219}	Y_{227}	Y_{235}
				DI_3	Y_4	Y_{12}	Y_{20}	···	Y_{220}	Y_{228}	Y_{236}
				DI_4	Y_5	Y_{13}	Y_{21}	···	Y_{221}	Y_{229}	Y_{237}
				DI_5	Y_6	Y_{14}	Y_{22}	···	Y_{222}	Y_{230}	Y_{238}
				DI_6	Y_7	Y_{15}	Y_{23}	···	Y_{223}	Y_{231}	Y_{239}
				DI_7	Y_8	Y_{16}	Y_{24}	···	Y_{224}	Y_{232}	Y_{240}
L	H	Input	Output	DI_0	Y_{240}	Y_{232}	Y_{224}	···	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{239}	Y_{231}	Y_{223}	···	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{238}	Y_{230}	Y_{222}	···	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{237}	Y_{229}	Y_{221}	···	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{236}	Y_{228}	Y_{220}	···	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{235}	Y_{227}	Y_{219}	···	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{234}	Y_{226}	Y_{218}	···	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{233}	Y_{225}	Y_{217}	···	Y_{17}	Y_9	Y_1

(b) 12-bit Parallel Input Mode

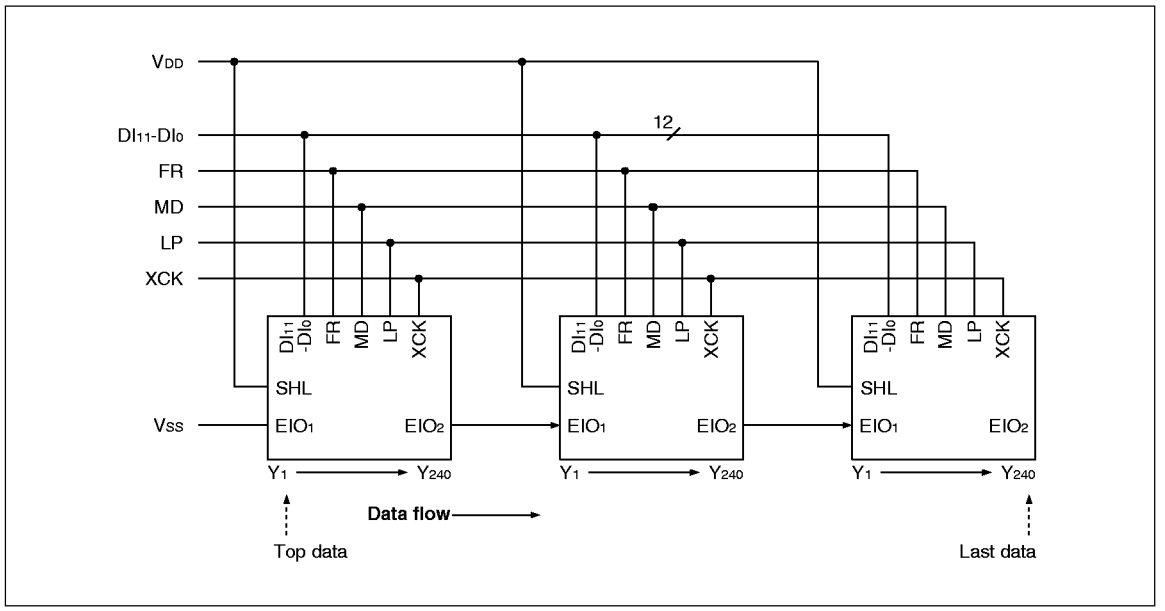
MD	SHL	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					20 CLOCK	19 CLOCK	18 CLOCK	···	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI_0	Y_1	Y_{13}	Y_{25}	···	Y_{205}	Y_{217}	Y_{229}
				DI_1	Y_2	Y_{14}	Y_{26}	···	Y_{206}	Y_{218}	Y_{230}
				DI_2	Y_3	Y_{15}	Y_{27}	···	Y_{207}	Y_{219}	Y_{231}
				DI_3	Y_4	Y_{16}	Y_{28}	···	Y_{208}	Y_{220}	Y_{232}
				DI_4	Y_5	Y_{17}	Y_{29}	···	Y_{209}	Y_{221}	Y_{233}
				DI_5	Y_6	Y_{18}	Y_{30}	···	Y_{210}	Y_{222}	Y_{234}
				DI_6	Y_7	Y_{19}	Y_{31}	···	Y_{211}	Y_{223}	Y_{235}
				DI_7	Y_8	Y_{20}	Y_{32}	···	Y_{212}	Y_{224}	Y_{236}
				DI_8	Y_9	Y_{21}	Y_{33}	···	Y_{213}	Y_{225}	Y_{237}
				DI_9	Y_{10}	Y_{22}	Y_{34}	···	Y_{214}	Y_{226}	Y_{238}
				DI_{10}	Y_{11}	Y_{23}	Y_{35}	···	Y_{215}	Y_{227}	Y_{239}
				DI_{11}	Y_{12}	Y_{24}	Y_{36}	···	Y_{216}	Y_{228}	Y_{240}
H	H	Input	Output	DI_0	Y_{240}	Y_{228}	Y_{216}	···	Y_{36}	Y_{24}	Y_{12}
				DI_1	Y_{239}	Y_{227}	Y_{215}	···	Y_{35}	Y_{23}	Y_{11}
				DI_2	Y_{238}	Y_{226}	Y_{214}	···	Y_{34}	Y_{22}	Y_{10}
				DI_3	Y_{237}	Y_{225}	Y_{213}	···	Y_{33}	Y_{21}	Y_9
				DI_4	Y_{236}	Y_{224}	Y_{212}	···	Y_{32}	Y_{20}	Y_8
				DI_5	Y_{235}	Y_{223}	Y_{211}	···	Y_{31}	Y_{19}	Y_7
				DI_6	Y_{234}	Y_{222}	Y_{210}	···	Y_{30}	Y_{18}	Y_6
				DI_7	Y_{233}	Y_{221}	Y_{209}	···	Y_{29}	Y_{17}	Y_5
				DI_8	Y_{232}	Y_{220}	Y_{208}	···	Y_{28}	Y_{16}	Y_4
				DI_9	Y_{231}	Y_{219}	Y_{207}	···	Y_{27}	Y_{15}	Y_3
				DI_{10}	Y_{230}	Y_{218}	Y_{206}	···	Y_{26}	Y_{14}	Y_2
				DI_{11}	Y_{229}	Y_{217}	Y_{205}	···	Y_{25}	Y_{13}	Y_1

CONNECTION EXAMPLES OF PLURAL SEGMENT DRIVERS

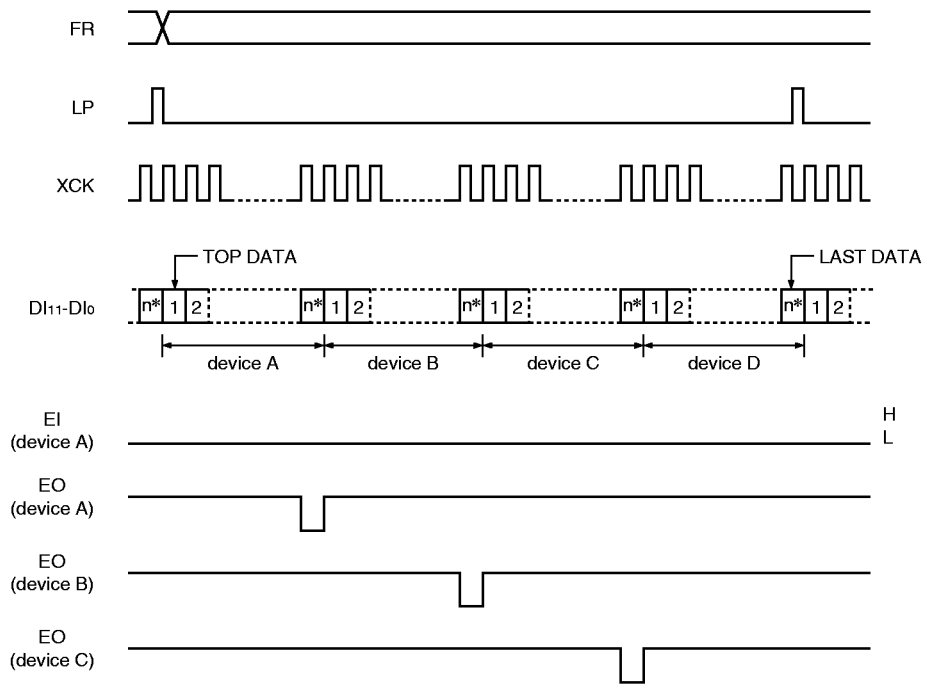
(a) When SHL = "L"



(b) When SHL = "H"



TIMING CHART OF 4-DEVICE CASCADE CONNECTION



* n = 30 in 8-bit parallel input mode.
n = 20 in 12-bit parallel input mode.

PRECAUTIONS

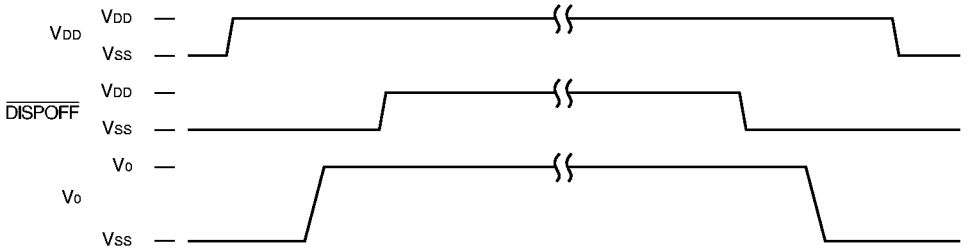
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on $\overline{\text{DISPOFF}}$ function. After that, cancel the $\overline{\text{DISPOFF}}$ function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_5 on $\overline{\text{DISPOFF}}$ function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	−0.3 to +7.0	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	−0.3 to +45.0	V	
	V_2	V_{2L}, V_{2R}	−0.3 to V_0 + 0.3	V	
	V_3	V_{3L}, V_{3R}	−0.3 to V_0 + 0.3	V	
	V_5	V_{5L}, V_{5R}	−0.3 to V_0 + 0.3	V	
Input voltage	V_I	DI_{11}-DI_0, XCK, LP, SHL, FR, MD, EIO_1, EIO_2, $\overline{DISPOFF}$, $TEST_1$, $TEST_2$	−0.3 to V_{DD} + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	°C	

NOTES :

1. T_A = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+10.0		+42.0	V	
Operating temperature	T_{OPR}		−20		+85	°C	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} \leq V_5 < V_3 < V_2 < V_0$.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +10.0 to +42.0 V, T_{OPR} = −20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_{11}-DI_0, XCK, LP, SHL, FR, MD, EIO_1, EIO_2, $\overline{DISPOFF}$			0.3V_{DD}	V	
Input "High" voltage	V_{IH}			0.7V_{DD}			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.4 mA		V_{DD} − 0.4			V	
Input leakage current	I_{LI}	$V_{SS} \le V_I \le V_{DD}$	All input pins			±10.0	µA	
I/O leakage current	$I_{LI/O}$	$V_{SS} \le V_I \le V_{DD}$	EIO_1, EIO_2			±10.0	µA	
Output resistance	R_{ON}	$\lvert \Delta V_{ON} \rvert$ = 0.5 V, V_0 = 40 V	Y_1-Y_{240}		1.0	1.5	kΩ	
		$\lvert \Delta V_{ON} \rvert$ = 0.5 V, V_0 = 30 V			1.5	2.0		
		$\lvert \Delta V_{ON} \rvert$ = 0.5 V, V_0 = 20 V			2.0	2.5		
Standby current	I_{STB}		V_{SS}			75.0	µA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.4	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			14.4	mA	3
Supply current (3)	I_0		V_{0L}, V_{0R}			2.0	mA	4

NOTES :

1. V_{DD} = +5.0 V, V_0 = +40.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}.
2. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{XCK} = 25 MHz, no-load, EI = V_{DD}.
   The input data is turned over by data taking clock (8-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{XCK} = 25 MHz, no-load, EI = V_{SS}.
   The input data is turned over by data taking clock (8-bit parallel input mode).
4. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{XCK} = 25 MHz, f_{LP} = 38.4 kHz, f_{FR} = 80 Hz, no-load.
   The input data is turned over by data taking clock (8-bit parallel input mode).

AC Characteristics

(Mode 1) (V_{SS} = V_5 = 0 V, V_{DD} = +5.0±0.5 V, V_0 = +10.0 to +42.0 V, T_{OPR} = −20 to +85 °C, the figure in parenthesis applies when T_{OPR1} = −20 to +60 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, t_F ≤ 7 (5) ns	40 (36)			ns	1
Shift clock "H" pulse width	t_{WCKH}		12			ns	
Shift clock "L" pulse width	t_{WCKL}		14			ns	
Data setup time	t_{DS}		5			ns	
Data hold time	t_{DH}		15			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		5			ns	
Shift clock fall to latch pulse fall time	t_{SL}		25			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		5 (4)			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
Output delay time (1)	t_D	C_L = 15 pF			28 (27)	ns	
Output delay time (2)	t_{PD1}	C_L = 15 pF			1.2	µs	
Output delay time (3)	t_{PD2}	C_L = 15 pF			1.2	µs	

NOTES :

1. Takes the cascade connection into consideration.
2. (t_{WCK} − t_{WCKH} − t_{WCKL})/2 is maximum in the case of high speed operation.

(Mode 2) (V_{SS} = V_5 = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = +10.0 to +42.0 V, T_{OPR} = −20 to +85 °C, the figure in parenthesis applies when T_{OPR1} = −20 to +60 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, t_F ≤ 10 ns	66 (60)			ns	1
Shift clock "H" pulse width	t_{WCKH}		23 (20)			ns	
Shift clock "L" pulse width	t_{WCKL}		23 (20)			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		25 (20)			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		10			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		12 (10)			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
Output delay time (1)	t_D	C_L = 15 pF			44 (40)	ns	
Output delay time (2)	t_{PD1}	C_L = 15 pF			1.2	µs	
Output delay time (3)	t_{PD2}	C_L = 15 pF			1.2	µs	

NOTES :

1. Takes the cascade connection into consideration.
2. (t_{WCK} − t_{WCKH} − t_{WCKL})/2 is maximum in the case of high speed operation.

(Mode 3) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = +10.0 to +42.0 V, T_{OPR} = –20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, $t_F \leq$ 10 ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		30			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		10			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
Output delay time (1)	t_D	C_L = 15 pF			57	ns	
Output delay time (2)	t_{PD1}	C_L = 15 pF			1.2	µs	
Output delay time (3)	t_{PD2}	C_L = 15 pF			1.2	µs	

NOTES :

1. Takes the cascade connection into consideration.
2. (t_{WCK} – t_{WCKH} – t_{WCKL})/2 is maximum in the case of high speed operation.

Timing Chart

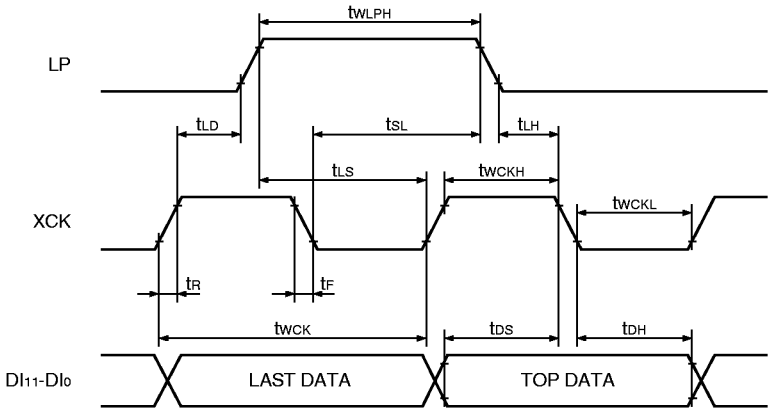
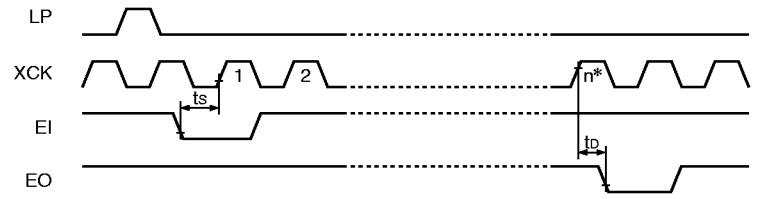


Fig. 4 Timing Characteristics (1)



* n = 30 in 8-bit parallel input mode.
n = 20 in 12-bit parallel input mode.

Fig. 5 Timing Characteristics (2)

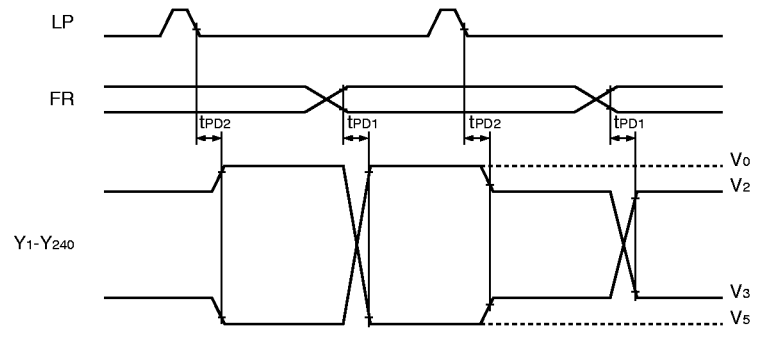
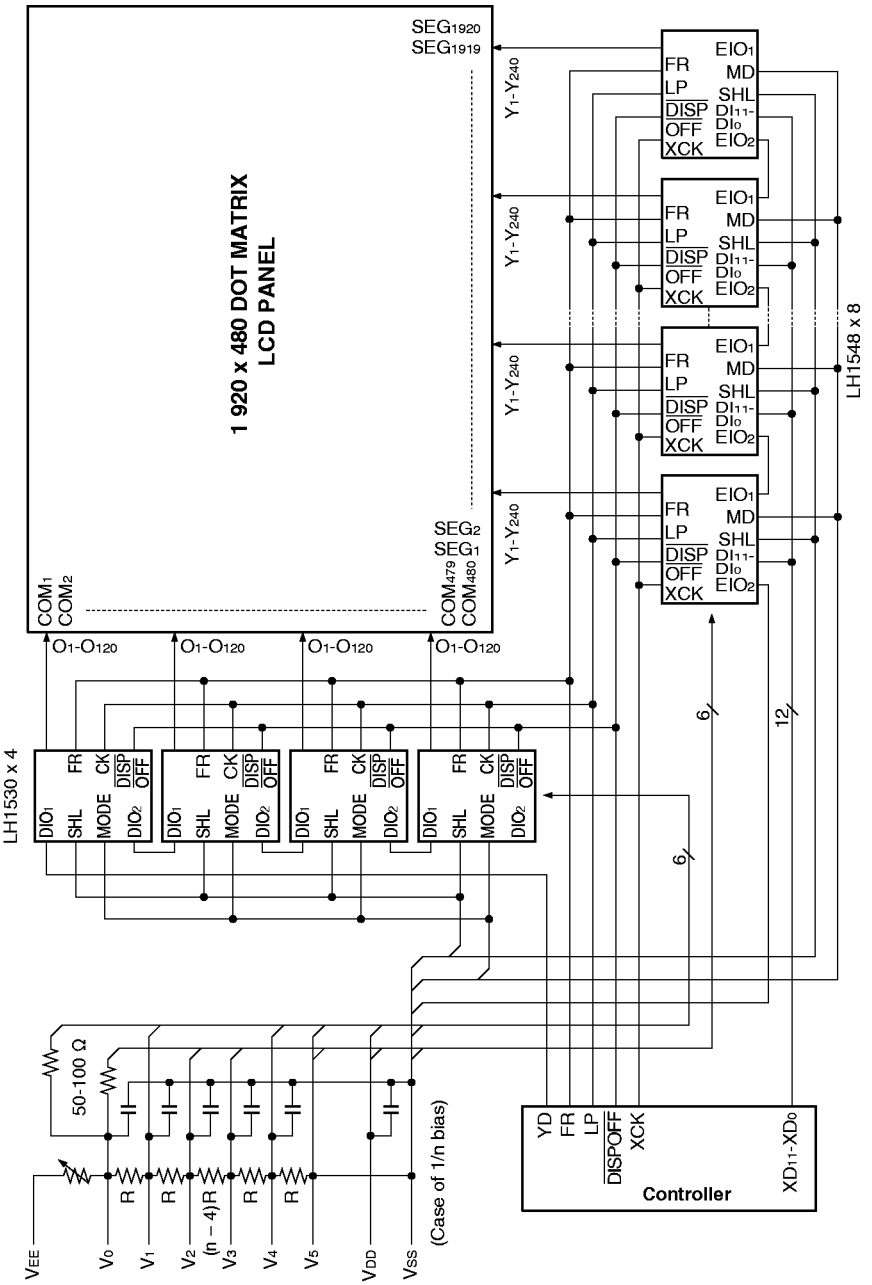


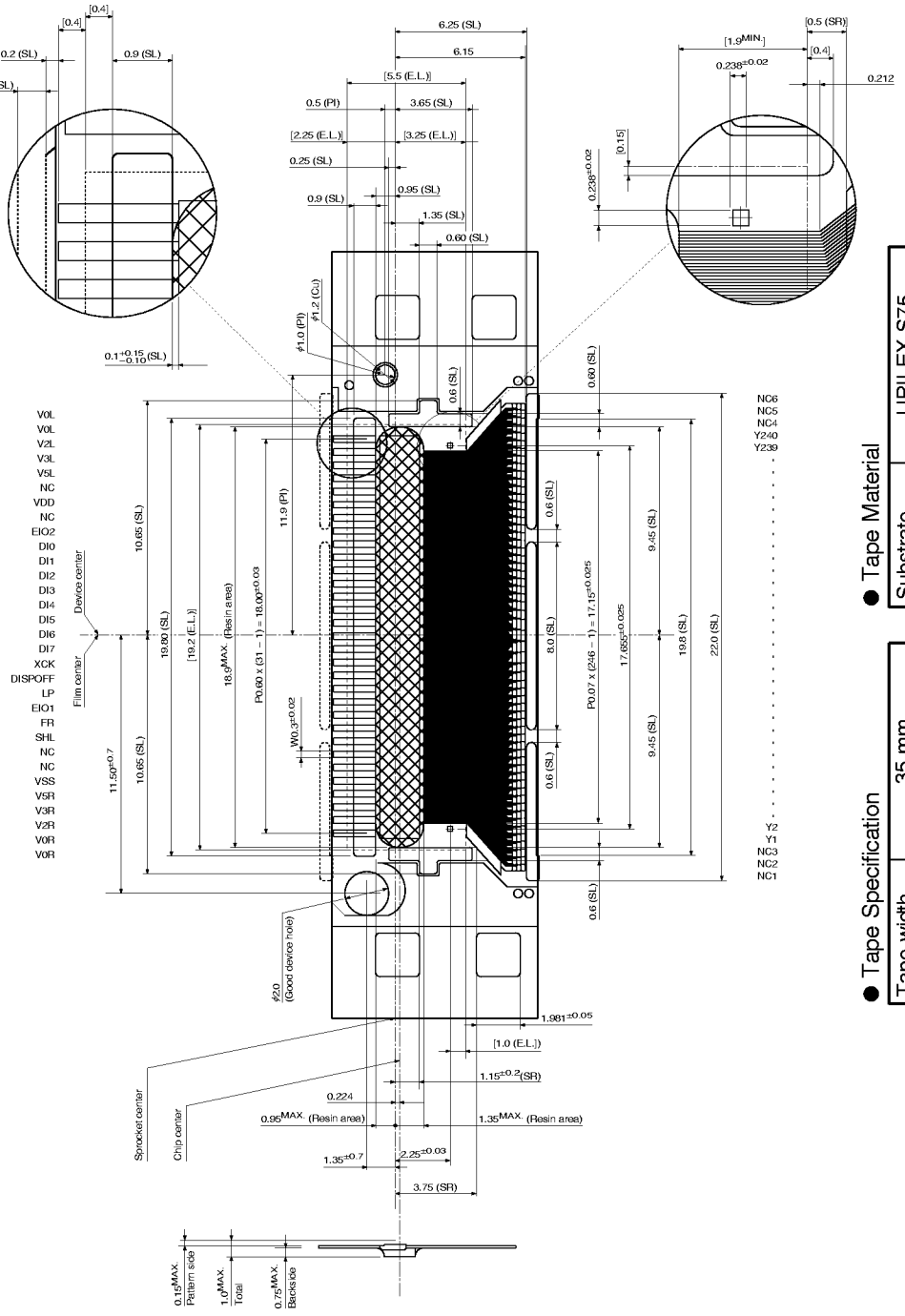
Fig. 6 Timing Characteristics (3)

SYSTEM CONFIGURATION EXAMPLE



PACKAGE

(Unit : mm)



● Tape Material

Substrate	UPILEX S75
Adhesive	#7100
Cu foil [thickness]	SLP 18 µm
Solder resist	Epoxy resin

● Tape Specification

Tape width	35 mm
Tape type	Wide
Perforation pitch	2 pitches

LH1548F

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