3.3V 16M x 64/72-Bit 1 BANK SDRAM Module HYS64/72V16300GU
3.3V 32M x 64/72-Bit 2 BANK SDRAM Module HYS64/72V32220GU

168 pin unbuffered DIMM Modules

- 168 Pin unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications
- PC100 & PC133 versions
- 1 bank 16M x 64, 16M x 72 and 2 bank 132M x 64, 32M x 72 organisation
- Optimized for byte-write non-parity (x64) or ECC (x72) applications
- JEDEC standard Synchronous DRAMs (SDRAM)
- Fully PC board layout compatible to INTEL's Rev. 1.0 module specification
- SDRAM Performance:

		-7.5	-8	Units
		PC133	PC100	
f_{CK}	Clock frequency (max.)	133	100	MHz
t_{AC}	Clock access time	5.4	6	ns

- Programmed Latencies :

Product Speed		CL	tRCD	tRP
-7.5	PC133	3	3	3
-8	PC100	2	2	2

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{CAS}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Utilizes 16M x 8 SDRAMs in TSOPII-54 packages with 4096 refresh cycles every 64 ms
- 133,35 mm x 31.75 mm x 4,00 mm card size with gold contact pads

The HYS64(72)16300GU and HYS64(72)32220 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 16M x 64, 16M x 72 in one bank and 32M x 64 and 32M x 72 in two banks high speed memory arrays designed with 128M Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use -7.5 speed sorted 16M x 8 SDRAM devices in TSOP54 packages to meet the PC133-333 requirements and -8 & -8A components for the standard PC100 applications. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL's PC SDRAM Rev. 1.0 module specification.The DIMMs have a serial presence detect, implemented with a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All INFINEON 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint, with 1,25" (31,75 mm) height.

Ordering Information

Type	Code	Package	Descriptions	Module Height
64MByte DIMMs:				
HYS 64V16300GU-7.5-...	PC133-333-520	L-DIM-168-33	133 Mhz 16M x 64 1 bank SDRAM module	1,25"
HYS 72V16300GU-7.5-...	PC133-333-520	L-DIM-168-33	133 Mhz 16M x 72 1 bank SDRAM module	1,25"
HYS 64V16300GU-8-...	PC100-222-620	L-DIM-168-33	100 MHz 16M x 64 1 bank SDRAM module	1,25"
HYS 72V16300GU-8-...	PC100-222-620	L-DIM-168-33	100 MHz 16M x 72 1 bank SDRAM module	1,25"
128 MByte DIMMs:				
HYS 64V32220GU-7.5-...	PC133-333-520	L-DIM-168-30	133 MHz 32M x 64 2 bank SDRAM module	1,25"
HYS 64V32220GU-7.5-...	PC133-333-520	L-DIM-168-30	133 Mhz 32M x 72 2 bank SDRAM module	1,25"
HYS 64V32220GU-8-...	PC100-222-620	L-DIM-168-30	100 MHz 32M x 64 2 bank SDRAM module	1,25"
HYS 72V32220GU-8-...	PC100-222-620	L-DIM-168-30	100 Mhz 32M x 72 2 bank SDRAM module	1,25"

Note: All partnumbers end with a place code (not shown), designating the die revision. Consult factory for current revision. Example: HYS64V16300GU-8-C, indicating Rev.C dies are used for SDRAM components.

Pin Names

A0-A11	Address Inputs	WE	Read / Write Input	Vss	Ground
BA0, BA1	Bank Selects	$\overline{CKE0}$, $\overline{CKE1}$	Clock Enable	SCL	Clock for SPD
DQ0 - DQ63	Data Input/Output	CLK0 - CLK3	Clock Input	SDA	Serial Data Out
CB0-CB7	Check Bits (x72 only)	DQMB0 - DQMB7	Data Mask	N.C.	No Connection
$\overline{RAS}$	Row Address Strobe	$\overline{CS0}$ - $\overline{CS3}$	Chip Select		
$\overline{CAS}$	Column Address Strobe	Vcc	Power (+3.3 Volt)		

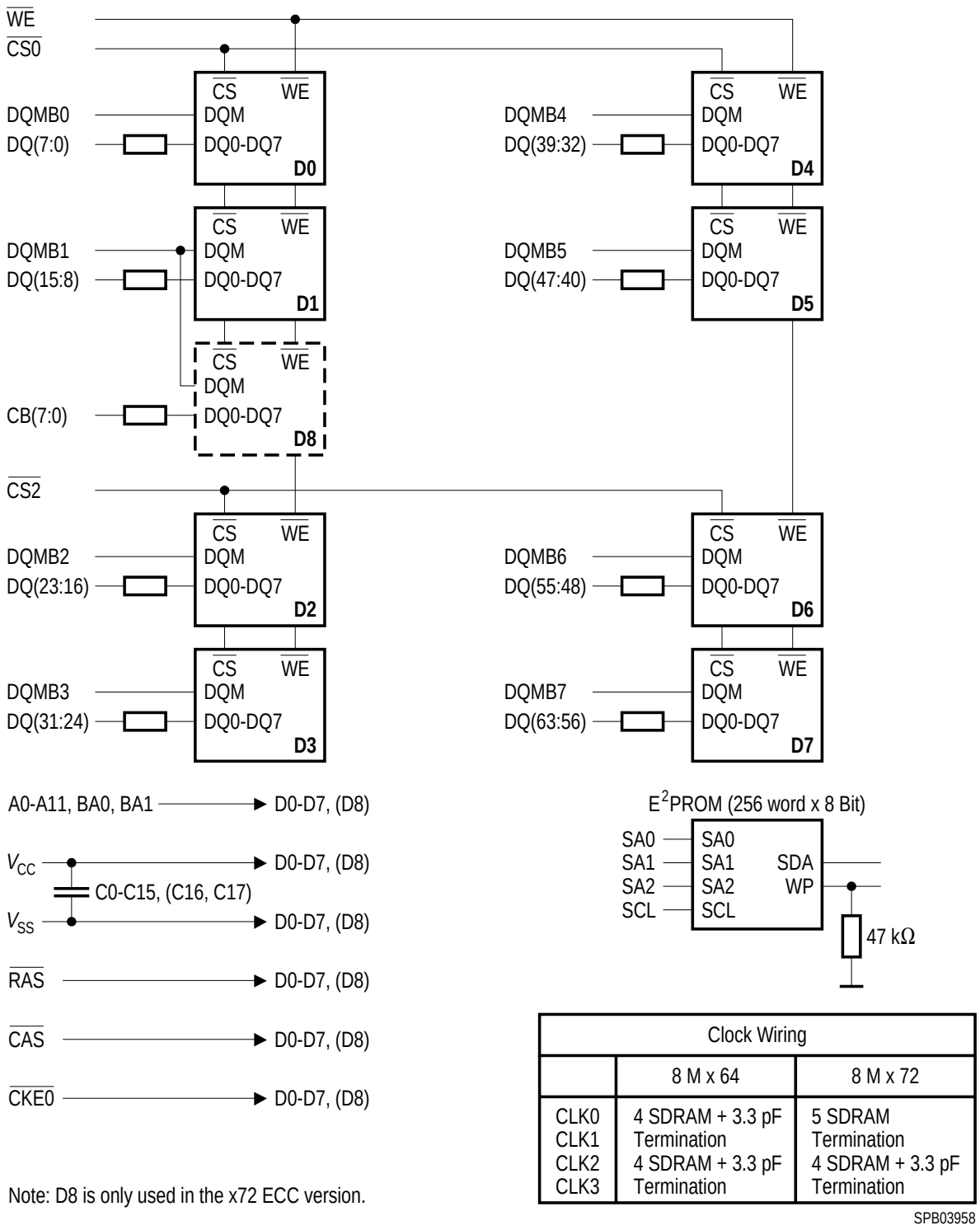
Address Format:

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
16M x 64	HYS 64V16300GU	12	10	2	4k	64 ms	15,6 µs
16M x 72	HYS 72V16300GU	12	10	2	4k	64 ms	15,6 µs
32M x 64	HYS 64V32220GU	12	10	2	4k	64 ms	15,6 µs
32M x 72	HYS 72V32220GU	12	10	2	4k	64 ms	15,6 µs

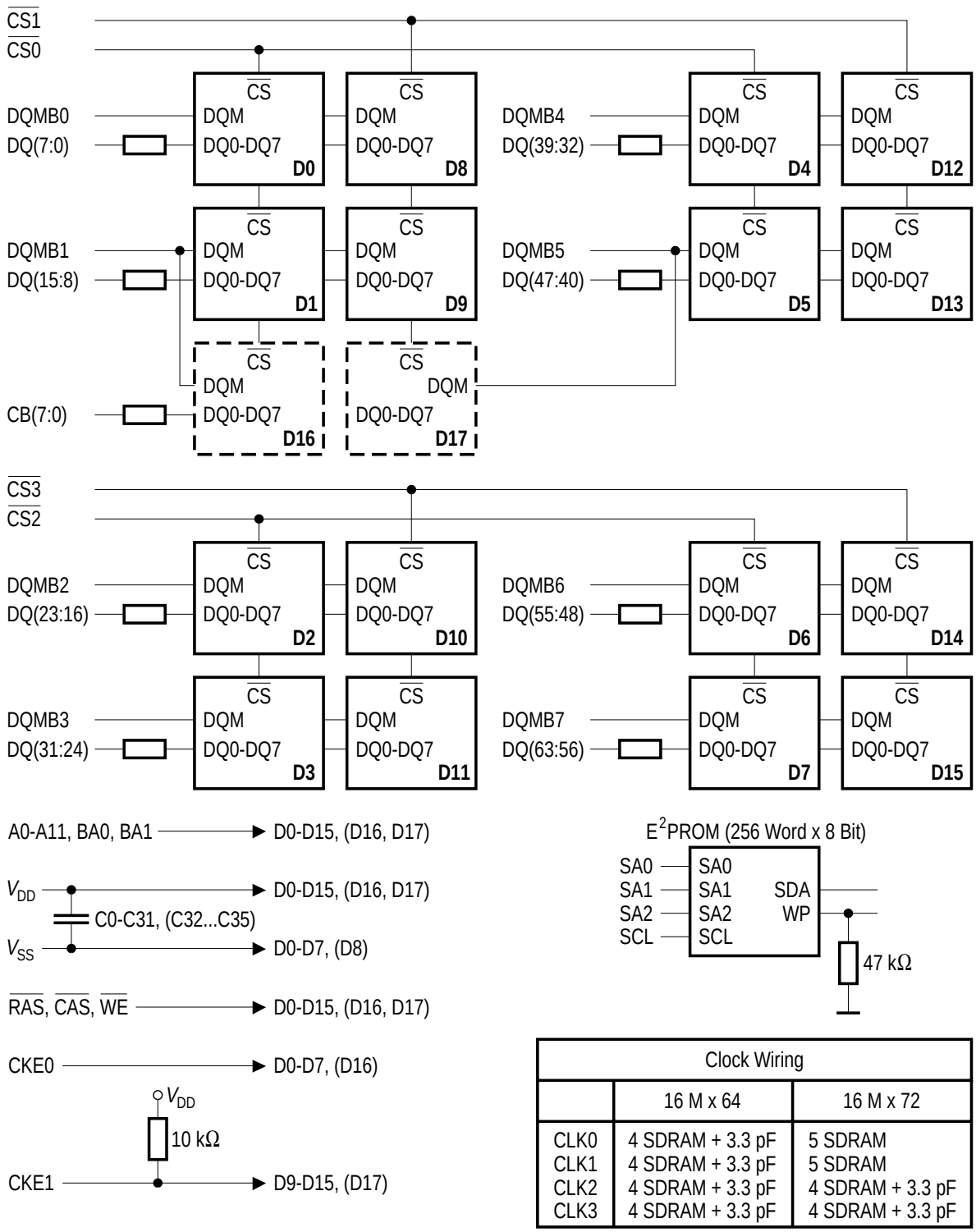
Pin Configuration

PIN #	Symbol	PIN #	Symbol		PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS		85	VSS	127	VSS
2	DQ0	44	DU		86	DQ32	128	CKE0
3	DQ1	45	CS2		87	DQ33	129	CS3
4	DQ2	46	DQMB2		88	DQ34	130	DQMB6
5	DQ3	47	DQMB3		89	DQ35	131	DQMB7
6	VCC	48	DU		90	VCC	132	NC
7	DQ4	49	VCC		91	DQ36	133	VCC
8	DQ5	50	NC		92	DQ37	134	NC
9	DQ6	51	NC		93	DQ38	135	NC
10	DQ7	52	NC (CB2)		94	DQ39	136	CB6
11	DQ8	53	NC (CB3)		95	DQ40	137	CB7
12	VSS	54	VSS		96	VSS	138	VSS
13	DQ9	55	DQ16		97	DQ41	139	DQ48
14	DQ10	56	DQ17		98	DQ42	140	DQ49
15	DQ11	57	DQ18		99	DQ43	141	DQ50
16	DQ12	58	DQ19		100	DQ44	142	DQ51
17	DQ13	59	VCC		101	DQ45	143	VCC
18	VCC	60	DQ20		102	VCC	144	DQ52
19	DQ14	61	NC		103	DQ46	145	NC
20	DQ15	62	DU		104	DQ47	146	DU
21	NC (CB0)	63	CKE1		105	NC (CB4)	147	NC
22	NC (CB1)	64	VSS		106	NC (CB5)	148	VSS
23	VSS	65	DQ21		107	VSS	149	DQ53
24	NC	66	DQ22		108	NC	150	DQ54
25	NC	67	DQ23		109	NC	151	DQ55
26	VCC	68	VSS		110	VCC	152	VSS
27	WE	69	DQ24		111	CAS	153	DQ56
28	DQMB0	70	DQ25		112	DQMB4	154	DQ57
29	DQMB1	71	DQ26		113	DQMB5	155	DQ58
30	CS0	72	DQ27		114	CS1	156	DQ59
31	DU	73	VCC		115	RAS	157	VCC
32	VSS	74	DQ28		116	VSS	158	DQ60
33	A0	75	DQ29		117	A1	159	DQ61
34	A2	76	DQ30		118	A3	160	DQ62
35	A4	77	DQ31		119	A5	161	DQ63
36	A6	78	VSS		120	A7	162	VSS
37	A8	79	CLK2		121	A9	163	CLK3
38	A10	80	NC		122	BA0	164	NC
39	BA1	81	WP		123	A11	165	SA0
40	VCC	82	SDA		124	VCC	166	SA1
41	VCC	83	SCL		125	CLK1	167	SA2
42	CLK0	84	VCC		126	NC	168	VCC

Note : Pinnames in brackets are for the x72 ECC versions



Block Diagram for 8M x 64/72 SDRAM DIMM modules (HYS64/72V82(3)00GU)



Clock Wiring		
	16 M x 64	16 M x 72
CLK0	4 SDRAM + 3.3 pF	5 SDRAM
CLK1	4 SDRAM + 3.3 pF	5 SDRAM
CLK2	4 SDRAM + 3.3 pF	4 SDRAM + 3.3 pF
CLK3	4 SDRAM + 3.3 pF	4 SDRAM + 3.3 pF

Note: D16 & D17 is only used in the x72 ECC version and all resistor values are 10 Ω except otherwise noted. SPB03769

Block Diagram for 16M x 64/72 SDRAM DIMM modules (HYS64/72V1620GU)

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD},V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	Vcc+0.3	V
Input low voltage	V_{IL}	– 0.5	0.8	V
Output high voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 40	40	µA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 40	40	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values				Unit
		max. 16Mx64	max. 16Mx72	max. 32Mx64	max. 32Mx72	
Input capacitance (A0 to A11, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I1}	65	72	105	144	pF
Input capacitance (CS0 -CS3,)	C_{I2}	32	40	32	40	pF
Input capacitance (CLK0 - CLK3)	C_{ICL}	35	38	35	38	pF
Input capacitance (CKE0, CKE1)	C_{I3}	65	72	65	72	pF
Input capacitance (DQMB0 - DQMB7)	C_{I4}	13	13	20	20	pF
Input / Output capacitance (DQ0-DQ63, CB0-CB7)	C_{IO}	10	10	15	15	pF
Input Capacitance (SCL,SA0-2)	C_{sc}	8	8	8	8	pF
Input/Output Capacitance	C_{sd}	10	10	10	10	pF

Operating Currents per SDRAM component (T_A = 0 to 70°C, Vdd = 3.3V ± 0.3V 1)

(Recommended Operating Conditions unless otherwise noted))

Parameter & Test Condition		Symb.	-7.5	-8		Note
			max.			
OPERATING CURRENT trc=trcmin., tck=tckmin. Ouputs open, Burst Length = 4, CL=3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access		ICC1	130	120	mA	1
PRECHARGE STANDBY CURRENT in Power Down Mode $\overline{CS}$ =VIH (min.), CKE<=Vil(max)	tck = min.	ICC2P	1.5		mA	1
PRECHARGE STANDBY CURRENT in Non-Power Down Mode $\overline{CS}$ = VIH (min.), CKE>=Vih(min)	tck = min.	ICC2N	40	35	mA	1
NO OPERATING CURRENT tck = min., $\overline{CS}$ = VIH(min), active state (max. 4 banks)	CKE>=VIH(min.)	ICC3N	50	45	mA	1
	CKE<=VIL(max.)	ICC3P	10		mA	1
BURST OPERATING CURRENT tck = min., Read command cycling		ICC4	130	120	mA	1,2
AUTO REFRESH CURRENT tck = min., Auto Refresh command cycling		ICC5	180	170	mA	1
SELF REFRESH CURRENT Self Refresh Mode, CKE=0.2V	standard version	ICC6	1.5		mA	1

AC Characteristics 3)4)

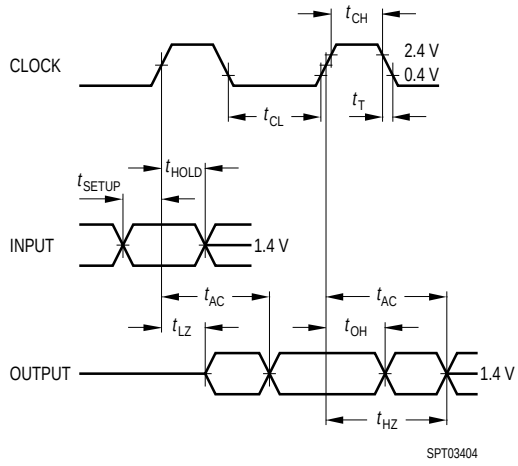
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

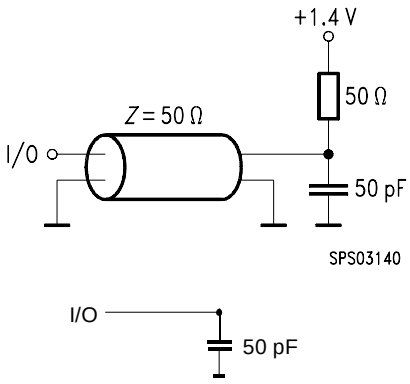
Parameter	Symbol	Limit Values				Unit	Note
		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.		
Clock and Access Time							
Clock Cycle Time	t_{CK}						
$\overline{CAS}$ Latency = 3		7.5	–	10	–	ns	
$\overline{CAS}$ Latency = 2		10	–	10	–	ns	
System Frequency	f_{CK}						
$\overline{CAS}$ Latency = 3		–	133	–	100	MHz	
$\overline{CAS}$ Latency = 2		–	100	–	100	MHz	
Clock Access Time	t_{AC}						
$\overline{CAS}$ Latency = 3		–	5.4	–	6	ns	4,5)
$\overline{CAS}$ Latency = 2		–	6	–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	3	–	ns	6)
Clock Low Pulse Width	t_{CL}	2.5	–	3	–	ns	6)
Set and Hold Parameters							
Input Setup time	t_{IS}	1.5	–	2	–	ns	7)
Input Hold Time	t_{IH}	0.8	–	1	–	ns	7)
Power Down Mode Entry Time	t_{SB}	–	1	–	1	CLK	8)
Power Down Mode Exit Setup Time	t_{PDE}	1	–	1	–	CLK	9)
Mode Register Setup Time	t_{RCS}	2	–	2	–	CLK	
Transition time (rise and fall)	t_T	1	–	1	–	ns	
Common Parameters							
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	20	–	20	–	ns	
Precharge Time	t_{RP}	20	–	20	–	ns	
Active Command Period	t_{RAS}	45	100k	50	100k	ns	
Cycle Time	t_{RC}	67.5	–	70	–	ns	
Bank to Bank Delay Time	t_{RRD}	15	–	16	–	ns	
$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	t_{CCD}	1	–	1	–	CLK	

Parameter	Symbol	Limit Values				Unit	Note
		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.		
Refresh Cycle							
Refresh Period (4096 cycles)	t_{REF}	–	64	–	64	ms	
Self Refresh Exit Time	t_{SREX}	1	–	1	–	CLK	10)
Read Cycle							
Data Out Hold Time	t_{OH}	3	–	3	–	ns	4)
Data Out to Low Impedance	t_{LZ}	0	–	0	–	ns	
Data Out to High Impedance	t_{HZ}	3	7	3	8	ns	11)
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	CLK	
Write Cycle							
Data input to Precharge (write recovery)	t_{WR}	2	–	2	–	CLK	
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	

Notes:

1. These parameters depend on the cycle rate. These values are measured at 133 MHz for -7.5 and at 100 Mhz for -8 modules. Input signals are changed once during tck, excepts for ICC6 and for standby currents when tck=infinity. All values are shown per memory component.
2. These parameters are measured with continous data stream during read access and all DQ toggling. CL=3 and BL=4 assumed and the VDDQ current is excluded.
3. All AC characteristics are shown on SDRAM component level.
   An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have V_{il} = 0.4 V and V_{ih} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il}. All AC measurements assume t_T=1ns with the AC output load circuit show. Specified tac and toh parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.





Measurement conditions for tac and toh

5. If clock rising time is longer than 1ns, a time (t_T/2 -0.5) ns has to be added to this parameter.
6. Rated at 1.5 V
7. If t_T is longen than 1 ns, a time (t_T -1) ns has to be added to this parameter.
8. Anytime the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake-up“ the device.
9. Timing is asynchronous. if setup time is not met by rising edge of the clock then the CKE signal is assumed latched on the next cycle.
10. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
11. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

SPD-Table for PC133 Modules:

Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -7.5	16Mx72 -7.5	32Mx64 -7.5	32Mx72 -7.5
0	Number of SPD bytes	128	80			
1	Total bytes in Serial PD	256	08			
2	Memory Type	SDRAM	04			
3	Number of Row Addresses (without BS bits)	12	0C			
4	Number of Column Addresses(for 8Mx8 SDRAMs)	10	0A			
5	Number of DIMM Banks	1 / 2	01		02	
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	LVTTL	01			
9	SDRAM Cycle Time at CL=3	7.5 ns	75			
10	SDRAM Access time from Clock at CL=3	5.4 ns	54			
11	Dimm Config	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80			
13	SDRAM width, Primary	x8	08			
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01			
16	Burst Length supported	1, 2, 4 & 8	0F			
17	Number of SDRAM banks	4	04			
18	Supported CAS Latencies	CAS latency = 2 & 3	06			
19	CS Latencies	CS latency = 0	01			
20	WE Latencies	Write latency = 0	01			
21	SDRAM DIMM module attributes	non buffered/non reg.	00			
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	0E			
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 ns	A0			
24	Max. data access time from Clock for CL=2	6.0 ns	60			
25	Minimum Clock Cycle Time at CL = 1	not supported	FF			
26	Maximum Data Access Time from Clock at CL=1	not supported	FF			
27	Minimum Row Precharge Time	20 ns	14			
28	Minimum Row Active to Row Active delay tRRD	15 ns	0F			

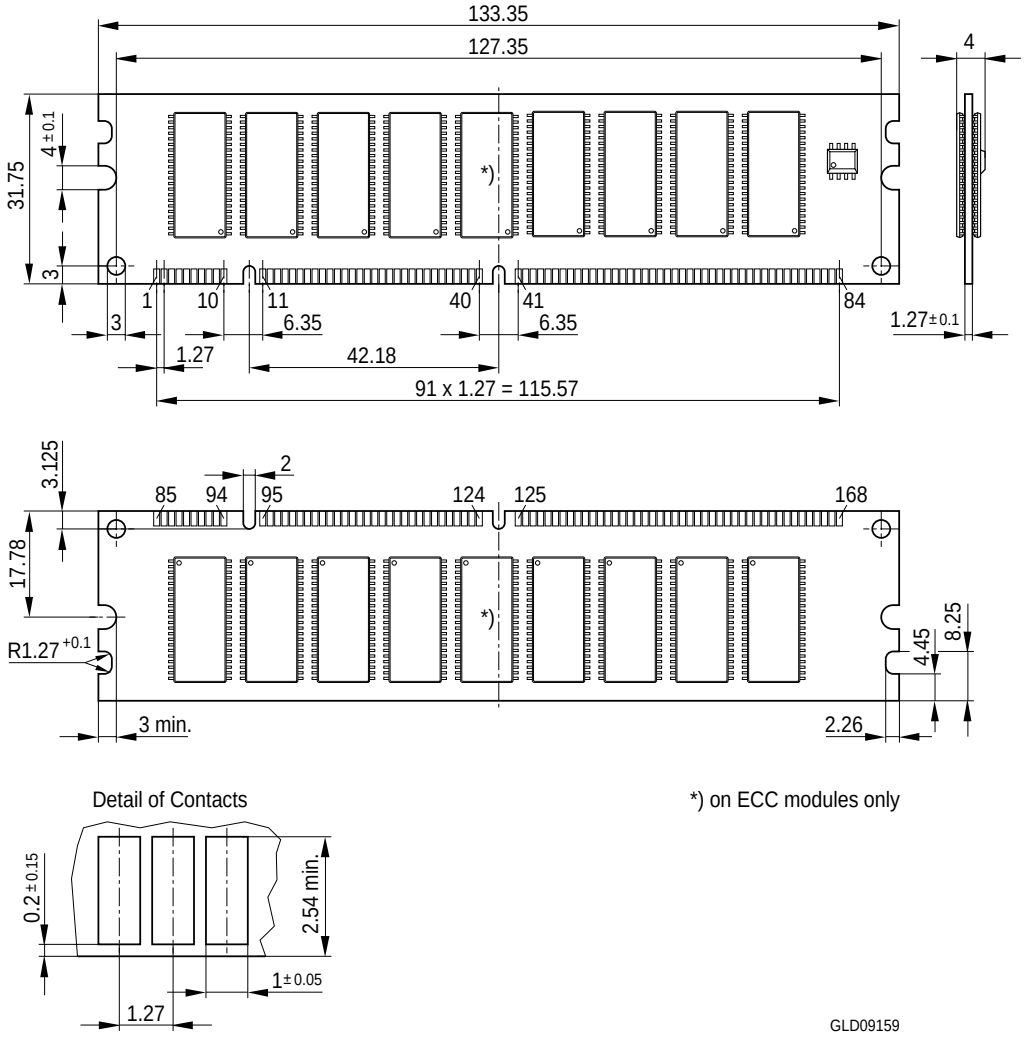
Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -7.5	16Mx72 -7.5	32Mx64 -7.5	32Mx72 -7.5
29	Minimum RAS to CAS delay tRCD	20 ns	14			
30	Minimum RAS pulse width tRAS	45 ns	2D			
31	Module Bank Density (per bank)	128 MByte	20			
32	SDRAM input setup time	1.5 ns	15			
33	SDRAM input hold time	0.8 ns	08			
34	SDRAM data input hold time	1.5 ns	15			
35	SDRAM data input setup time	0.8 ns	08			
62-61	Superset information (may be used in future)		FF			
62	SPD Revision	Revision 1.2	12			
63	Checksum for bytes 0 - 62		13	25	14	26
64-125	Manufacturers information (optional) (FFh if not used)		XX	XX	XX	XX
126	Frequency Specification		64			
127	133 MHz support details		AF		FF	
128+	Unused storage locations		FF			

SPD-Table for PC100 Modules:

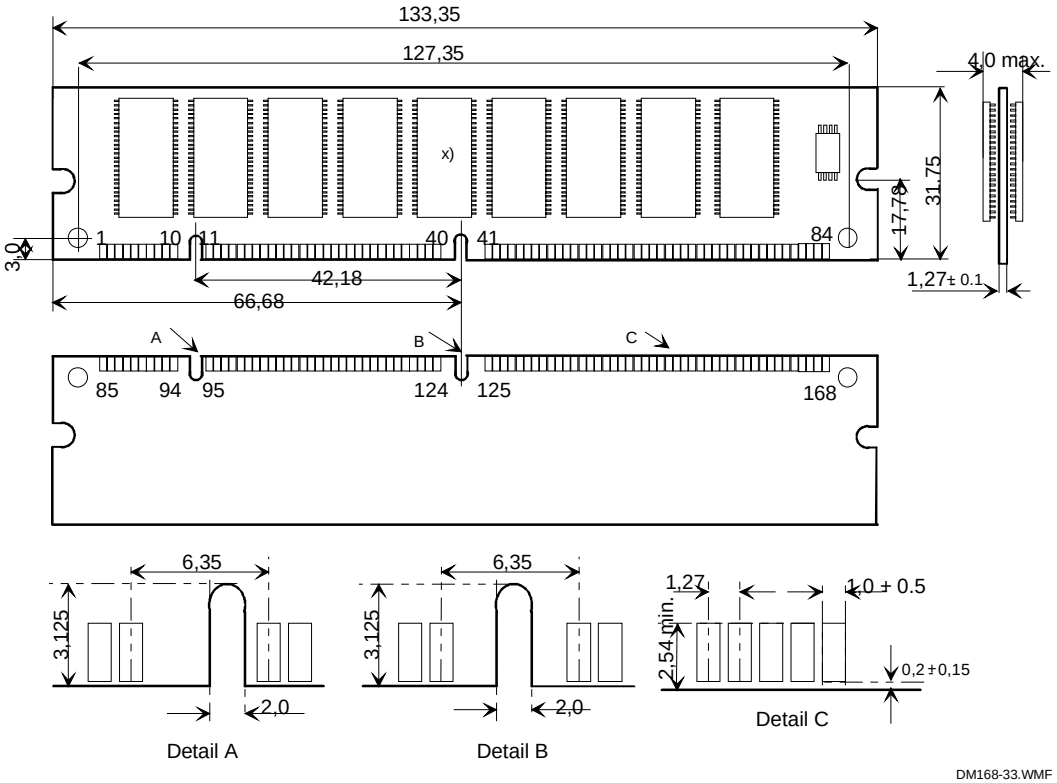
Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -8	16Mx72 -8	32Mx64 -8	32Mx72 -8
0	Number of SPD bytes	128	80			
1	Total bytes in Serial PD	256	08			
2	Memory Type	SDRAM	04			
3	Number of Row Addresses (without BS bits)	12	0C			
4	Number of Column Addresses(for 8Mx8 SDRAMs)	10	0A			
5	Number of DIMM Banks	1 / 2	01		02	
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	LVTTL	01			
9	SDRAM Cycle Time at CL=3	10.0 ns	A0			
10	SDRAM Access time from Clock at CL=3	6.0 ns	60			
11	Dimm Config	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80			
13	SDRAM width, Primary	x8	08			
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01			
16	Burst Length supported	1, 2, 4 & 8	0F			
17	Number of SDRAM banks	4	04			
18	Supported CAS Latencies	CAS latency = 2 & 3	06			
19	CS Latencies	CS latency = 0	01			
20	WE Latencies	Write latency = 0	01			
21	SDRAM DIMM module attributes	non buffered/non reg.	00			
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	0E			
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 ns	A0			
24	Max. data access time from Clock for CL=2	6.0 ns	60			
25	Minimum Clock Cycle Time at CL = 1	not supported	FF			
26	Maximum Data Access Time from Clock at CL=1	not supported	FF			
27	Minimum Row Precharge Time	20 ns	14			
28	Minimum Row Active to Row Active delay tRRD	16 ns	10			

Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -8	16Mx72 -8	32Mx64 -8	32Mx72 -8
29	Minimum RAS to CAS delay tRCD	20 ns	14			
30	Minimum RAS pulse width tRAS	45 ns	2D			
31	Module Bank Density (per bank)	128 MByte	20			
32	SDRAM input setup time	2 ns	20			
33	SDRAM input hold time	1 ns	10			
34	SDRAM data input hold time	2 ns	20			
35	SDRAM data input setup time	1 ns	10			
62-61	Superset information (may be used in future)		FF			
62	SPD Revision	Revision 1.2	12			
63	Checksum for bytes 0 - 62		71	83	72	84
64-125	Manufacturers information (optional) (FFh if not used)		XX	XX	XX	XX
126	Frequency Specification	100 MHz	64			
127	100 MHz support details		AF		FF	
128+	Unused storage locations		FF			

L-DIM-168-30
SDRAM DIMM Module package
HYS64/72V32220GU



L-DIM-168-33
SDRAM DIMM Module package
HYS64/72V16300GU



x) on ECC modules only

Update Releases:

June 1, 1999	Explanation for factory specific code in part numbers added
June 17, 1999	Byte 22 for PC100 modules changed from 06 to 0E
August 3, 1999	PC133 spec incorpoated
August 5, 1999	SPD tables added
August 23, 1999	Byte 126 changed to 64h for PC133 modules
Sept.30, 1999	Some errors corrected, checksums added
Dec. 2, 1999	Some timing parameters adjusted according to INTELs PC133 specification -8A speedsort removed