H1855
H1855C

1800 CMOS Microprocessor Family
Multiply/Divide Unit

HUGHES AIRCRAFT COMPANY

SEMICONDUCTOR DIVISION
Industrial Electronics Group

DESCRIPTION

Hughes 1855 is an 8 bit mode programmable multiply/divide unit which can be used to greatly increase the capabilities of 8 bit microprocessors. The 1855 interfaces directly to the 1802 microprocessor via the N-lines and can easily be configured to fit in either the memory or I/O space of generalized 8 bit microprocessors. The 1855 performs multiply and divide operations on unsigned, binary operators. It saves considerable memory space and execution time over the same functions as performed by coded multiply and divide software subroutines.

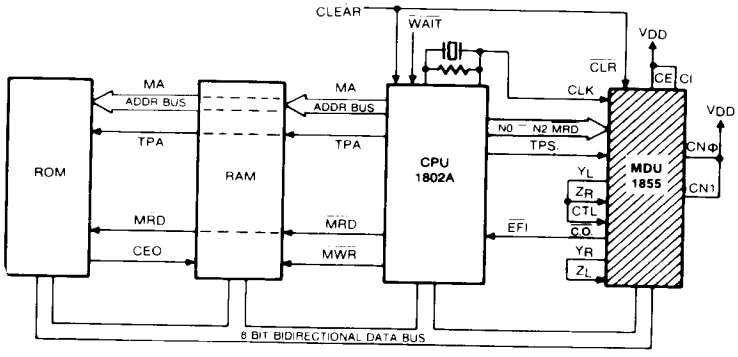
Add and shift right operations and subtract and shift left operations are used for multiply and divide functions respectively. The 1855 is cascadable up to 4 units for 32 x 32 bit multiply or 64 ÷ 32 bit divide functions.

The 1855 operates over a 4-10.5 voltage range while the 1855C operates over a 4-6.5 voltage range. The 1855 is available in a 28 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form are available upon request.

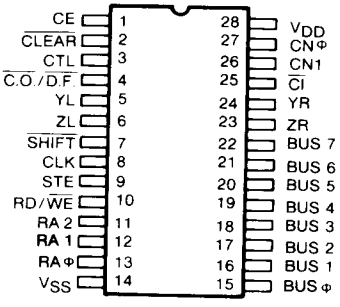
FEATURES

- Static silicon gate CMOS circuitry
- Interfaces directly to 1802A microprocessor without additional components.
- Easy interface to general 8 bit microprocessors.
- Low power dissipation
- Single non-critical voltage supply
- Cascadable up to 4 units for 32 bit by 32 bit multiply or 64 ÷ 32 bit divide
- 8 bit by 8 bit multiply or 16 ÷ 8 bit divide in 5 μs at 5V or 2.5 μs at 10V typical
- Significantly increased throughput of μp used for arithmetic calculations.

SYSTEM INTERCONNECT
Typical 1800 System with 1855



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

DC Supply-Voltage Range, (V_{CC}, V_{DD})
(All Voltage Values referenced to V_{SS} Terminal)
$V_{CC} \leq V_{DD}$:
1855 ..... −0.5 to + 13 Volts
1855C ..... −0.5 to + 7 Volts
Input Voltage Range, all inputs ..... −0.5 to V_{DD} + 0.5 Volts
DC Input Current, any one input ..... ± 10mA
Operating-Temperature Range (T_A)
Plastic Package ..... −40 to + 85°C
Ceramic Package ..... −55 to + 125°C
Storage Temperature Range (T_{stg}) .... −65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Range

CHARACTERISTICS	LIMITS				UNITS
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = − 40 to + 85°.

CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	1855 Min.	1855 Typ.[1]	1855 Max.	1855C Min.	1855C Typ.[1]	1855C Max.	
Quiescent Device Current, I_{DD}	−	0, 5	5	−	0.01	50	−	0.02	200	µA
	−	0, 10	10	−	1	200	−	−	−	
Output Low (Sink) Current, I_{OL}	0.4	0, 5	5	1.6	3.2	−	1.6	3.2	−	mA
	0.5	0, 10	10	2.6	5.2	−	−	−	−	
Output High (Source) Current, I_{OH}	4.6	0, 5	5	1.15	2.3	−	1.15	2.3	−	
	9.5	0, 10	10	2.6	5.2	−	−	−	−	
Output Voltage Low-Level, V_{OL}[2]	−	0, 5	5	−	0	0.1	−	0	0.1	V
	−	0, 10	10	−	0	0.1	−	−	−	
Output Voltage High-level, V_{OH}[2]	−	0, 5	5	4.9	5	−	4.9	5	−	
	−	0, 10	10	9.9	10	−	−	−	−	
Input Low Voltage, V_{IL}	0.5, 4.5	−	5	−	−	1.5	−	−	1.5	
	0.5, 9.5	−	10	−	−	3	−	−	−	
Input High Voltage, V_{IH}	0.5, 4.5	−	5	−	3.5	−	3.5	−	−	
	0.5, 9.5	−	10	−	7	−	−	−	−	
Input Current, I_{IN}	−	0, 5	5	−	± 10^{-4}	± 1	−	± 10^{-4}	± 1	µA
	−	0, 10	10	−	± 10^{-4}	± 1	−	−	−	
3-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	−	−	± 15	−	−	± 15	
	0, 10	0, 10	10	−	−	± 15	−	−	−	
Operating Current, I_{DD}[3]	−	0, 5	5	−	2	5	−	2	5	mA
	−	0, 10	10	−	4	10	−	−	−	
Input Capacitance, C_{IN}	−	−	−	−	5	7.5	−	5	7.5	pF
Output Capacitance, C_{OUT}	−	−	−	−	10	15	−	−	15	

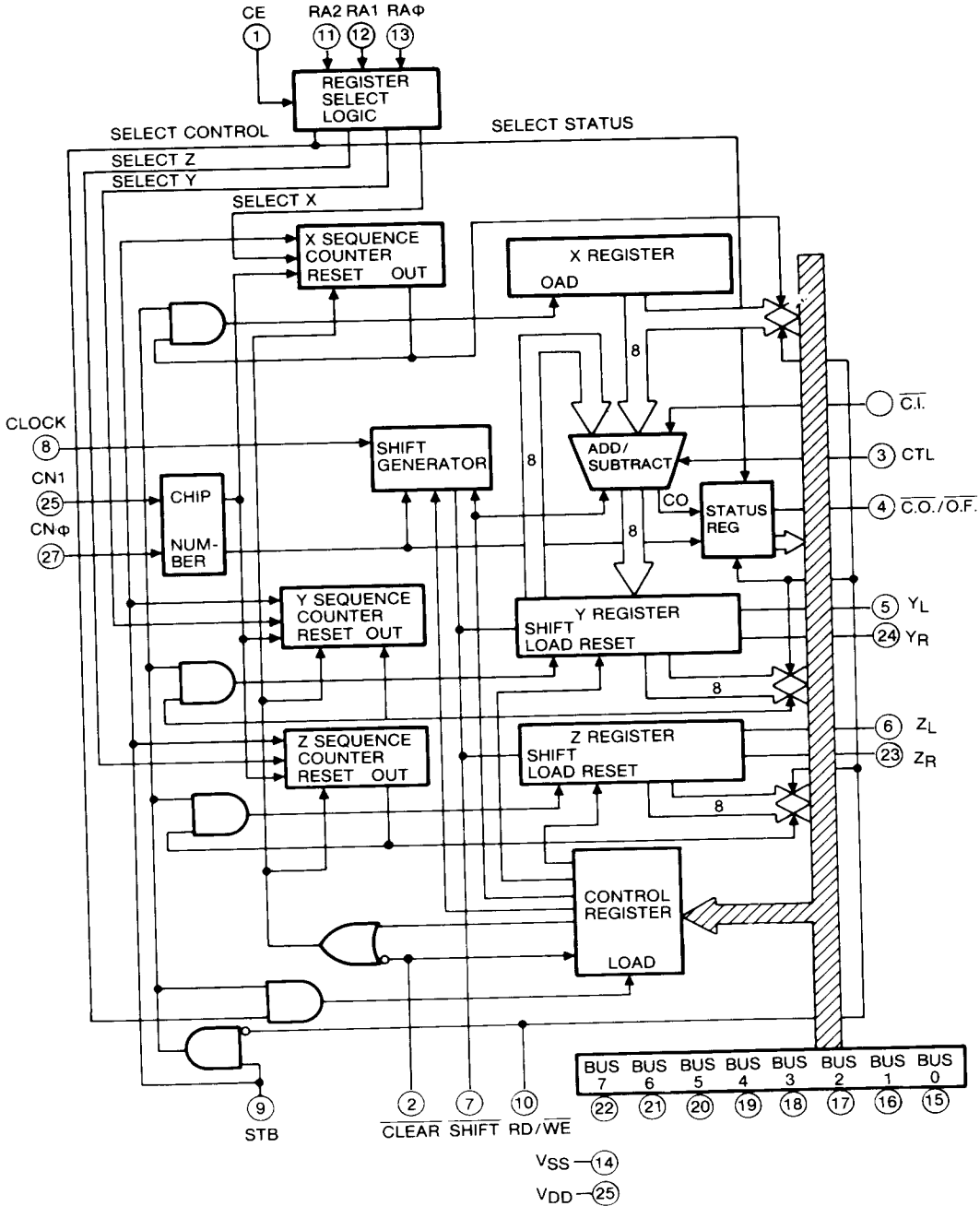
Notes: 1. Typical values are to T_A = + 25°C and nominal voltage.
2. I_{OL} = 1 µA.
3. Operating current measured in a 1802A at 2 MHz with outputs floating.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to + 85°C, V_{DD} ± 5% t_r, t_f = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Timing Diagram)

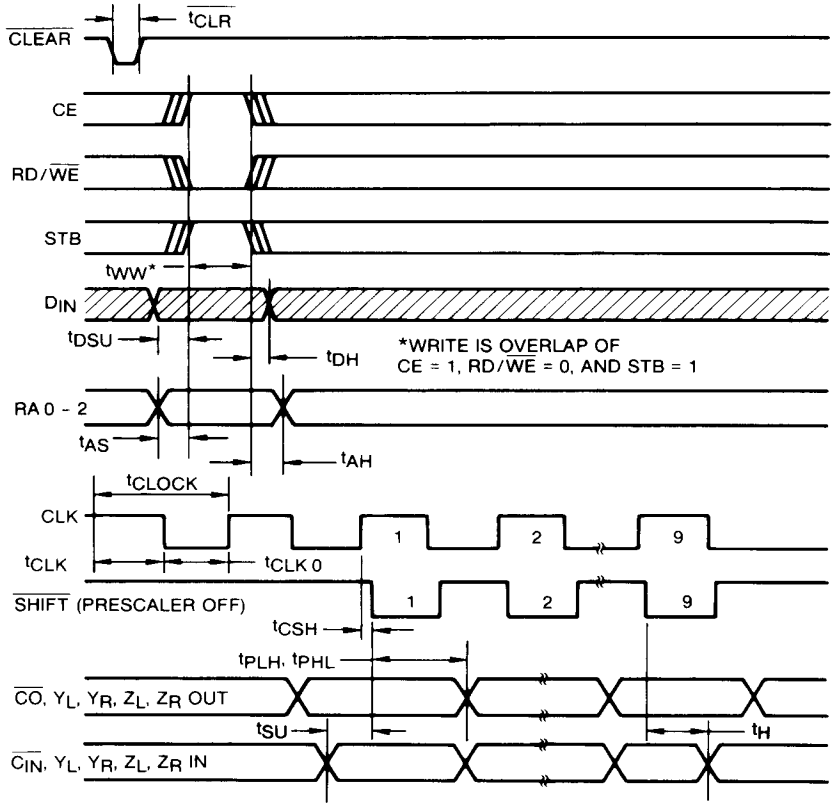
CHARACTERISTICS[1]	SYMBOL	V_{DD} (V)	25°C Min.	25°C Typ.[2]	25°C Max.	−40 to +85°C Min.	−40 to +85°C Typ.[2]	−40 to +85°C Max.	UNITS
WRITE CYCLE									
Minimum Clear Pulse Width	$t_{\overline{CLR}}$	5	–	50	75	–	50	75	ns
		10	–	25	40	–	–	–	
Minimum Write Pulse Width	t_{WW}	5	–	150	225	–	150	225	
		10	–	75	115	–	–	–	
Minimum Data-In Setup	t_{DSU}	5	–	−75	0	–	−75	0	
		10	–	−40	0	–	–	–	
Minimum Data-In Hold	t_{DH}	5	–	50	75	–	50	75	
		10	–	25	40	–	–	–	
Minimum Address to Write Setup	t_{ASU}	5	–	50	75	–	50	75	
		10	–	25	40	–	–	–	
Minimum Address after Write Hold	t_{AH}	5	–	50	75	–	50	75	
		10	–	25	40	–	–	–	
READ CYCLE									
CE to Data Out Active	t_{CDO}	5	–	200	300	–	200	300	ns
		10	–	100	150	–	–	–	
CE to Data Access	t_{CA}	5	–	300	450	–	300	450	
		10	–	150	225	–	–	–	
Address to Data Access	t_{AA}	5	–	300	450	–	300	450	
		10	–	150	225	–	–	–	
Data Out Hold After CE	t_{DOH}	5	50	150	225	50	150	225	
		10	25	75	115	–	–	–	
Data Out Hold After Read	t_{DOH}	5	50	150	225	50	150	225	
		10	25	75	115	–	–	–	
Read to Data Out Active	t_{RDO}	5	–	200	300	–	200	300	
		10	–	100	150	–	–	–	
Read to Data Access	t_{RA}	5	–	200	300	–	200	300	
		10	–	100	150	–	–	–	
Strobe to Data Access	t_{SA}	5	50	200	300	50	200	300	
		10	25	100	150	–	–	–	
Minimum Strobe Width	t_{SW}	5	–	150	225	–	150	225	
		10	–	75	115	–	–	–	
OPERATION TIMING									
Maximum Clock Frequency[3]	t_{CF}	5	3	4	–	3	4	–	MHz
		10	6	8	–	–	–	–	
Maximum Shift Frequency (1 Device)[4]	t_{SF}	5	1.5	2	–	1.5	2	–	
		10	3	4	–	–	–	–	
Minimum Clock Width	t_{CLK0} t_{CLK1}	5	–	100	150	–	100	150	ns
		10	–	50	75	–	–	–	
Minimum Clock Period	t_{CLK}	5	–	250	333	–	250	333	ns
		10	–	125	167	–	–	–	
Clock to Shift Prop. Delay	t_{CSH}	5	–	200	300	–	200	300	
		10	–	100	150	–	–	–	
Minimum C.I. to Shift Setup	t_{SU}	5	–	50	67	–	50	67	
		10	–	25	33	–	–	–	
C.O. from Shift Prog. Delay	t_{PLH} t_{PHL}	5	–	450	600	–	450	600	
		10	–	225	300	–	–	–	
Minimum C.I. from Shift Hold	t_H	5	–	50	75	–	50	75	
		10	–	25	40	–	–	–	
Minimum Register Input Setup	t_{SU}	5	–	−20	10	–	−20	10	
		10	–	−10	10	–	–	–	
Register after Shift Prop. Delay	t_{PLH} t_{PHL}	5	–	400	600	–	400	600	
		10	–	200	300	–	–	–	
Minimum Register after Shift Hold	t_H	5	–	50	100	–	50	100	
		10	–	25	50	–	–	–	
C.O. from C.I. Prop. Delay	t_{PLH} t_{PHL}	5	–	100	150	–	100	150	
		10	–	50	75	–	–	–	
Register from C.I. Prop. Delay	t_{PLH} t_{PHL}	5	–	80	120	–	80	120	
		10	–	40	60	–	–	–	

Notes
1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for T_A = + 25°C and nominal voltages.
3. Clock frequency and pulse width are given for systems using the internal clock option of the 1855. Clock frequency equals shift frequency for systems not using the internal clock option.
4. Shift period for cascading of devices is increased by an amount equal to the C.O. to C.I. Prop. Delay for each device added.

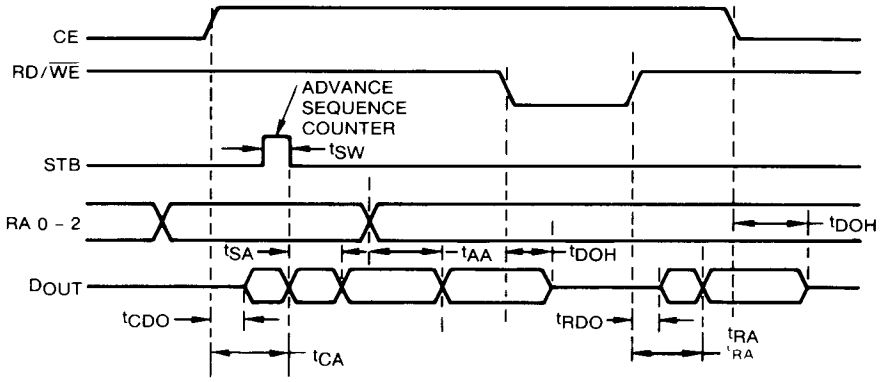
FUNCTIONAL DIAGRAM



Write Timing And Operation Timing



Read Timing



CONTROL TRUTH TABLE

INPUTS*						RESPONSE
CE	RA 2 (N 2)	RA 1 (N 1)	RA 0 (N 0)	RD/CE (WRD)	STB (TPB)	
0	X	X	X	X	X	NO ACTION (BUS FLOATS)
X	0	X	X	X	X	NO ACTION (BUS FLOATS)
1	1	0	0	1	X	X TO BUS } INCREMENT SEQUENCE
1	1	0	1	1	X	Z TO BUS } COUNTER WHEN
1	1	1	0	1	X	Y TO BUS } STB AND RD = 1
1	1	1	1	1	X	STATUS TO BUS
1	1	0	0	0	1	LOAD X FROM BUS } INCREMENT
1	1	0	1	0	1	LOAD Z FROM BUS } SEQUENCE
1	1	1	0	0	1	LOAD Y FROM BUS } COUNTER
1	1	1	1	0	1	LOAD CONTROL REGISTER
1	1	X	X	0	0	NO ACTION (BUS FLOATS)

*( ) = 1800 system signals. 1 = High Level, 0 = Low Level, X = High Level or Low Level

REGISTER BIT ASSIGNMENT CONTROL/REGISTER BIT ASSIGNMENT

BITS							
7	6	5	4	3	2	1	0
SHIFT RATE SELECT	RESET CONT. SEQUENCE COUNTER	NUMBER OF 1855		RESET CONT. Y REG.	RESET CONT. Z REG.	OPERATION	
0 = Clock frequency 1 = Select option*	1 = Reset sequence counters	00 = Four 1855's 01 = Three 1855's 10 = Two 1855's 11 = One 1855		1 = Reset Y register	1 = Reset Z register	00 = No Operation (except reset controls) 01 = Multiply 10 = Divide 11 = Invalid State	

*Select shift rate option:
One 1855 = shift rate = clock frequency ÷ 2
Two 1855's = shift rate = clock frequency ÷ 4
Three or four 1855's = shift rate = clock frequency ÷ 8

STATUS REGISTER BIT ASSIGNMENT

BIT	7	6	5	4	3	2	1	0
Output	0	0	0	0	0	0	0	O.F.

O.F. = 1 if overflow (only valid after a divide has been done).

FUNCTIONAL DESCRIPTION

The 1855 performs an 8N-bit by 8N-bit multiply with a 16N-bit results and 16N bit by 8N-bit divide yielding an 8N-bit result plus an 8 bit remainder. The N represents the number of cascaded 1855s from 1 through 4. All operations require 8N + 1 shift pulses.

The 1855 contains X, Y and Z registers for loading the operands and saving the results, the control register for initializing the multiply or divide operation, and a status register for storing an overflow flag. There are two register address lines (RA 0-RA 1) provided to select the appropriate register for loading or reading. The RD/$\overline{WE}$ and STB lines are used in conjunction with the RA lines to determine the exact MDU response (see Control Truth Table).

When multiple MDUs are cascaded, the loading of each register is done sequentially. The first selection of any register loads the most significant 1855, the second loads the next significant and so on. Registers are also read out sequentially. This is accomplished by internal counters on each 1855 which are decremented by STB during each register selection. When the counter matches the chip number (CN 1, CN 0 lines), the device is selected. These counters must be cleared with a clear pulse on pin 2 or with bit 6 in the control word (See Control Register Bit Assignment Table) in order to start each sequence of accesses with the most significant device.

The 1855 has a built-in clock prescaler which can be selected via bit 7 on the control register. The prescaler may be necessary in cascaded systems operating at high frequencies or in systems where a suitable exact frequency is not available. This need is to provide for propagation delay of the carry output signal. Without the prescaler select, the shift frequency is equal to the clock input frequency. With the prescaler selected, the rate depends on the number of MDUs as defined by bits 4 and 5 of the control word. For one MDU, the clock frequency is divided by two; the two MDUs the clock frequency is divided by four and for three or four MDUs the clock frequency is divided by eight.

OPERATION

A. Initialization and Controls:

The 1855 must be cleared by a low signal input on pin 2 during power on. This prevents bus contention problems at YL, YR and ZL, and ZR terminals. It also resets the sequence counters and shift pulse generator.

Prior to loading any other registers, the control register must be loaded to specify the number of 1855s being cascaded. Once the number of devices has been specified and sequence counters cleared with a clear pulse or bit 6 of the control word, the X, Y and Z registers can be loaded as defined in the control truth table. Registers can be loaded in any sequence. Successive loads to a given register will always proceed sequentially from the most significant byte to the least significant byte as described previously. Resetting the sequence counters selects the most significant MDU. In a four MDU system, loading all MDUs results in the sequence counter pointing to the first MDU again while in all other configurations it must be reset prior to each series or register reads or writes.

OPERATION, cont.

B. Multiply Operation:

(X) x (Z) + (Y) ⇒ (Y) (Z); (X) unchanged

The two numbers to be multiplied are loaded in the X and Z registers. The result will be in the Y and Z register with Y being the more significant half and Z the less significant half. The X register will be unchanged after the operation is completed.

The original contents of Y register are added to the product of X and Z. Bit 3 of the control word will reset register Y to zero if desired.

C. Divide Operation:

$\frac{(Y)\ (Z)}{(X)}$ ⇒ (Z) = quotient, (Y) = remainder; $\overline{C.O.}/\overline{O.F.}$ in status byte.

The divisor is loaded into the X register. The dividend is loaded in the Y and Z registers with the more significant half in the Y register and less significant half in the Z register. The X register will be unaltered by the operation. The quotient will be in the Z register while the remainder will be in the Y register. An overflow will be indicated by the $\overline{C.O.}/\overline{O.F.}$ of the most significant MDU and can also be determined by reading the status byte.

The overflow indicator will be set at the start of the divide operation if the resultant will exceed the size of the Z register (8N-bits).

The Z register can be reset using bit 2 of the control word and another divide can be performed in order to further divide the remainder.

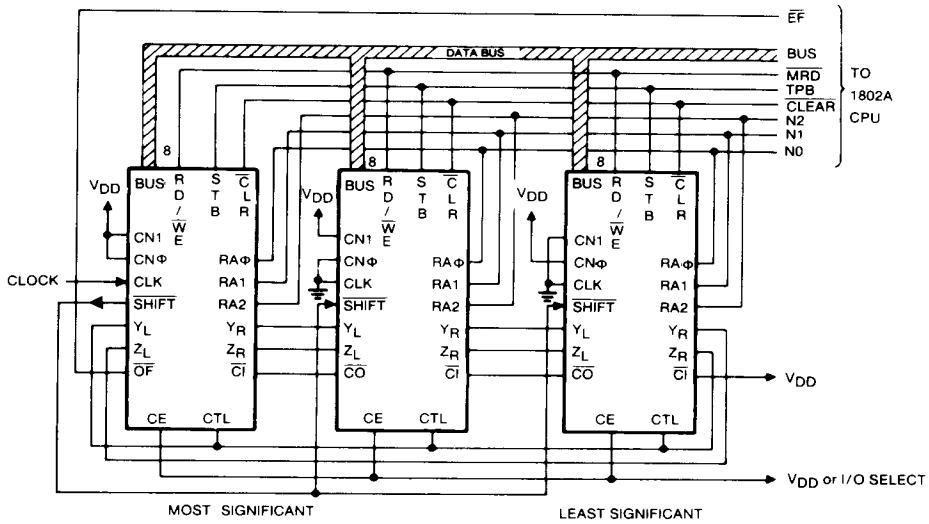
Programming Examples:

Connection to an 1802A Microprocessor in direct I/O mode (N lines connected to R inputs).

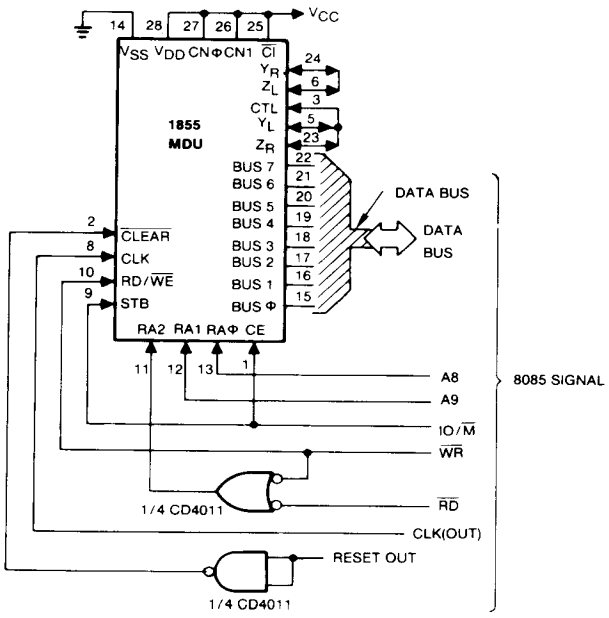
$F\Phi E1_{16}$ X $2D3C_{16}$ Multiply	
LDI #ΦΦ PLO R2 LDI #1Φ PHI R2	$R_2 = 1\Phi\Phi\Phi$
OUT 7, #60	Load control word with 2 MDUs and reset/sequence counters.
OUT 4, #FΦ OUT 4, #E1	Load MSB of X reg. Load LSB of X reg. (X) = FΦE1
OUT 5, #2D OUT 5, #3C	Load MSB of Z reg. Load LSB of Z reg. (Z) = 2D3C
OUT 7, #69	Load control word with 2 MDUs, reset y reg and seq counters and do multiply operation
SEX R2 INP 6; IRX INP 6; IRX INP 5; IRX INP 5; IRX	MSB of results from Y reg. to Location 1ΦΦΦ and 1ΦΦ1 LSB of result from Z reg. to Location 1ΦΦ2 and 1ΦΦ3

Divide $\frac{B4A5968_{16}}{4F3\Phi_{16}}$	
LDI #ΦΦ PLO R2 LDI #2Φ PHI R2	$R_2 = 2\Phi\Phi\Phi$
OUT 7, #60	load control word
OUT 6, #B4 OUT 6, #A5	= Y register (Y) = BYA5
OUT 5, #96 OUT 5, #85	= Z register (Z) = 9685
OUT 4, #4F OUT 4, #30	= X register (X) = 4F3Φ
OUT 7, #6A	Load control word for divide function
SEX R2 INP 5; IRX INP 5; IRX INP 6: IRX INP 6: IRX	Quotient for z register to mem. 2ΦΦΦ, 2ΦΦ3 Remainder from y register to mem. 2ΦΦ2, 2ΦΦ3

(A) Cascading 3 MDUs in 1802A system with MDU being accessed as an I/O port.



(B) Interfacing the 1855 to 8085 microprocessor as an I/O device.



SIGNAL DESCRIPTION

CE — CHIP ENABLE (Input):
A high on this pin enables the 1855 MDU to respond to the select lines. All cascaded MDUs must be enabled together. CE also controls the three state $\overline{C.O.}/\overline{O.F.}$ output of the most significant MDU.

$\overline{Clear}$ (Input):
The 1855 MDU(s) must be cleared upon power on with a low on this pin. The clear signal resets the sequence counters, the shift pulse generator, and bits 0 and 1 of the control register.

CTL-Control (Input):
This is an input pin. All CTL pins must be wired together and to the Y_L of the most significant 1855 MDU and the Z_R of the least significant 1855 MDU. This signal is used to indicate whether the registers are to be operated on or only shifted.

$\overline{C.O.}/\overline{O.F.}$ — $\overline{Carry\ Out}/\overline{Over\ Flow}$ (Output):
The three state 1855 Carry Out signal is connected to CI (Carry-In) of the next more significant 1855 MDU, except on the most significant MDU. On that MDU it is an overflow indicator and is enabled when a chip enable is true. A low on this pin indicates that an overflow has occurred. The overflow signal is latched each time the control register is loaded, but is only meaningful after a divide command.

Y_L, Y_R — Y-Left, Y-Right:
These are three state bi-directional pins for data transfer between the Y registers of cascaded 1855 MDUs. The Y_R pin in an output and Y_L is an input during a multiply and the reverse is true at all other times. The Y_L pin must be connected to the Y_R pin of the next more significant MDU. An exception is the Y_L pin of the most significant MDU must be connected to the Z_R pin of the least significant MDU and the CTL pins of all MDU's. Also the Y_R pin of the least significant MDU is tied to the Z_L pin of the most significant MDU.

Z_L, Z_R — Z-Left, Z-Right:
These are three state bi-directional pins for data transfers between the Z registers of cascaded MDUs. The Z_R pin is an output and Z_L is an input during a multiply and the reverse is true at all other times. the Z_L pin must be tied to the Y_R pin of the next most significant MDU. An exception is the Z_L pin of the most significant MDU must be connected to the Y_R pin of the lest significant MDU. Also, the Z_R pin of the least significant MDU is tied to the Y_L of the most significant MDU.

$\overline{Shift}$ — $\overline{Shift\ Clock}$:
This is a three state bi-directional pin. It is an output on the most significant MDU and an input on all other MDUs. It provides the MDU system's timing pulses. All $\overline{Shift}$ pins must be connected together for cascaded operation. A maximum of the 8N + 1 shifts are required for an operation where N equals the number of MDU devices cascaded.

Clk — Clock (Input):
This pin should be grounded on all but the most significant MDU. There is an optional reduction of clock frequency available on this pin, if so desired, controlled by bit 7 of the control byte.

Stb — Strobe (Input):
When RD/$\overline{WE}$, low data, is latched from bus lines on the falling edge of this signal, it may be asynchronous to the clock. Strobe also increments the selected register's sequence counter during reads and writes. TPB would be used in 1802A systems.

RD/$\overline{WE}$ — Read/$\overline{Write\ Enable}$ (Input):
This signal defines whether the selected register is to be read from or written to. In the 1802A systems use $\overline{MRD}$ if MDUs are addressed as I/O devices; $\overline{MWR}$ is used if MDUs are addressed as memory devices.

RAΦ, RA 1, RA 2 — Register Address (Input):
These input signals define which register is to be read from or written to. It can be seen in the Control Truth Table that RA 2 can be used as a chip enable. It is identical to the CE pin, except only CE controls the tristate $\overline{C.O.}/\overline{O.F.}$ on the most significant MDU. In the 1802A systems use N lines if MDUs are used as I/O devices; use address lines or function of address lines if MDUs are used as memory devices.

V_{SS} — Ground:
Power supply line.

BUS 0 — BUS 7 — Bus Lines:
Three state bidirectional bus for direct interface with 1802A series and other 8-bit microprocessors.

Z_R — Z-Right:
See signal Z_L

Y_R — Y-Right:
See signal Y_L

$\overline{CI}$-$\overline{Carry\text{-}In}$ (Input):
This is an input for the carry from the next less significant MDU. On the least significant MDU, it must be high (V_{DD}) on all others and connected to the $\overline{CO}$ pin of the next less significant MDU.

CNΦ, CN 1 — Chip Number (Input):
These two input pins are wired high or low to indicate the MDU position in the cascaded chain. Both are high for the most significant MDU regardless of how many 1855 MDUs are used. Then CN 1 = high and CN 0 = low for the next MDU and so forth.

V_{DD} — V+:
Power supply line.