

H1852 H1852C

1800 CMOS Microprocessor Family
Input/Output Port

HUGHES
AIRCRAFT COMPANY

MICROELECTRONICS CENTER

DESCRIPTION

Hughes 1852 is an 8 bit mode programmable CMOS Input or Output Port. The device acts as a buffer between the 1802A data bus and the peripheral data bus. It can also be used as an 8 bit address latch for multiplexed address buses.

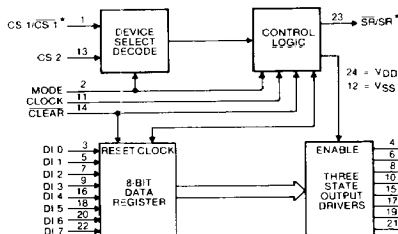
The Mode control signal programs the 1852 as an input port mode (mode = 0) or an output port (mode = 1). As an input port, data (DI 0-DI 7) is strobed from the peripheral into the 8 bit buffer register by a logic high on the Clock signal input; the negative clock transition sets the service request flip flop low (SR = 0) and latches data. When the CS1 and CS2 signals are enabled, the data (DO 0-DO 7) is read onto the microprocessor bus. The signal SR is then reset (SR = 1) on the negative transition CS1 • CS2. As an output port, data (DI 0-DI 7) is strobed into the buffer register by the microprocessor when CS1, CS2, and the Clock input are activated. The Service Request is set on the negative transition of CS1 • CS2, and will remain until the following negative transition of the clock. The Output driver is always enabled when the output mode is chosen. A Clear control allows asynchronous resetting of the port's register (DO 0-DO 7) and service request flip flop.

The 1852 operates over a 4—10.5 voltage range while the 1852C operates over a 4—6.5 voltage range. The 1852 is available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), or cerdip (Y suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

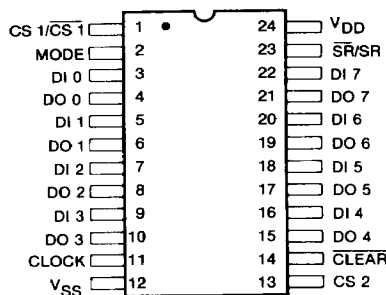
- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components.
- Parallel 8 Bit Data Register and Buffer
- Stored Service Request
- Asynchronous Register Clear
- Single Voltage Supply
- Low Quiescent and Operating Power

FUNCTIONAL DIAGRAM



* POLARITY DEPENDS ON MODE

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T _A)	
Ceramic Package	— 55 to + 125°C
Plastic Package	— 40 to + 85°C
DC Supply-Voltage Range (V _{DD})	
(All voltage values referenced to V _{SS} terminal)	
1852	—0.5 to + 11 Volts
1852C	— 0.5 to + 7 Volts
Input Voltage Range	V _{SS} —0.3V to V _{DD} + 0.3V
Storage Temperature Range (T _{stg})	— 65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range.

CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	1852		1852C				
Supply-Voltage Range (At T _A = Full Package Temperature Range)	—	—	—	4	—	10.5	4	—	6.5	V
Recommended Input Voltage Range	—	—	—	V _{SS}	—	V _{DD}	V _{SS}	—	V _{DD}	V
Static Electrical Characteristics at T _A = -55 to + 125°C, V _{DD} nominal										
Quiescent Device Current, I _{DD} ⁴	—	0.5	5	—	—	50	—	—	100	μA
	—	0.10	10	—	—	100	—	—	—	
Output Low Drive (Sink) Current, I _{OL}	0.4	0.5	5	1.2	3.2	—	1.2	3.2	—	mA
	0.5	0.10	10	2.7	6	—	—	—	—	
Output High Drive (Source) Current, I _{OH}	4.6	0.5	5	-1.2	-2.3	—	-1.2	-2.3	—	mA
	9.5	0.10	10	-2.7	-6	—	—	—	—	
Output Voltage Low Level, V _{OL} ^{1, 3}	—	0.5	5	—	0	0.1	—	0	0.1	V
	—	0.10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V _{OH} ³	—	0.5	5	4.9	5	—	4.9	5	—	V
	—	0.10	10	9.9	10	—	—	—	—	
Input Low Voltage, V _{IL}	2.5, 2.5	—	5	—	—	1.25	—	—	1.25	V
	5, 5	—	10	—	—	3	—	—	—	
Input High Voltage, V _{IH}	2.5, 2.5	—	5	3.5	—	—	3.5	—	—	V
	5, 5	—	10	7	—	—	—	—	—	
Input Current, I _{IN} ⁴	—	0.5	5	—	—	±1	—	—	±1	μA
	—	0.10	10	—	—	±1	—	—	—	
3-State Output Leakage Current, I _{OUT} ⁴	0.5	0.5	5	—	—	±1	—	—	±1	μA
	0.10	0.10	10	—	—	±1	—	—	—	
Operating Current, I _{DD1} ^{2, 3}	—	0.5	5	—	.1	2	—	.1	5	mA
	—	0.10	10	—	.4	5	—	—	—	
Input Capacitance C _{IN} ³	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C _{OUT} ²	—	—	—	—	5	7.5	—	—	—	pF
DYNAMIC ELECTRICAL CHARACTERISTICS at T _A = -55 to 125°C, V _{DD} = 5, 10v, V _{IH} = V _{DD} , V _{IL} = V _{SS} , C _L = 50pF, LIMITS AT V _{DD} = + 10V APPLY TO THE 1852 ONLY.										
Required Write Pulse Width, t _{WW}	—	—	5	—	130	250	—	130	250	ns
	—	—	10	—	65	130	—	—	—	
Required Data Setup Time, t _{DS}	—	—	5	—	-10	0	—	-10	0	ns
	—	—	10	—	-5	0	—	—	—	
Required Data Hold Time, t _{PH}	—	—	5	—	75	195	—	75	195	ns
	—	—	10	—	35	97	—	—	—	

*Typical values are for T_A = —25° C and nominal V_{DD}.

NOTE 1: I_{OL} = I_{OH} = 1 μA.

NOTE 2: Operating current is measured at 2MHz in an 1802 system with open outputs and a program of alternating 1 and 0 data pattern.

NOTE 3: Design assured but not tested.

NOTE 4: Parameters guaranteed by other tests at —55° C.

DYNAMIC ELECTRICAL CHARACTERISTICS, cont.

H1852/1852C

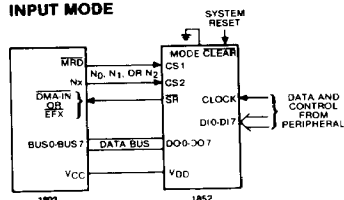
Propagation Delay Times, tPLH, tPHL										
Service Request:	—	—	5	—	170	340	—	170	340	ns
Clear to SR, tRSR ³	—	—	10	—	85	170	—	—	—	
Clock to SR, tCSR ³	—	—	5	—	120	240	—	120	240	
Select to SR, tSSR ³	—	—	10	—	60	120	—	—	240	
Input Mode:	—	—	5	30	185	370	30	185	370	ns
Data Output Hold Time, tDOH ^{1,3}	—	—	10	15	100	200	—	—	—	
Select to Data Output, tSDO ^{1,3}	—	—	5	30	185	370	30	185	370	
Output Mode:	—	—	5	—	140	280	—	140	280	ns
Clear to Data Output, tRDO ³	—	—	10	—	70	140	—	—	—	
Write to Data Output, tWDO ³	—	—	5	—	220	440	—	220	440	
Data Input to Data Output, tDDO ³	—	—	10	—	110	220	—	—	—	
	—	—	5	—	100	200	—	100	200	
	—	—	10	—	50	100	—	—	—	

* Typical Values are for T_A = + 25°C and nominal V_{DD}

NOTE 1: Minimum value is measured from CS 2; maximum value is measured from CS 1.

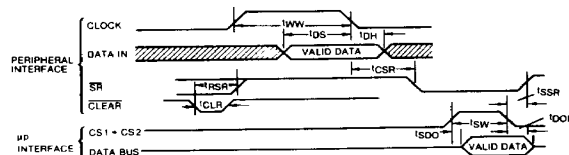
SYSTEM INTERCONNECT

INPUT MODE



INPUT MODE

CS1•CS2 is the overlap of CS1 = 1 and CS2 = 1



MODE = V_{SS} MODE 0 (INPUT)

CLOCK	CS1•CS2	CLEAR	DATA OUTPUT
X	0	X	HIGH IMPEDANCE
0	1	0	0
0	1	1	DATA LATCH
1	1	X	DATA INPUT

SR=0 CLOCK \downarrow (CLEAR = 1, CS1•CS2 = 0)

SR=1 (CS1•CS2) \downarrow OR (CLEAR) \downarrow

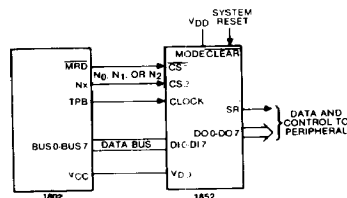
MODE = V_{DD} MODE 1 (OUTPUT)

CLOCK	CS1•CS2	CLEAR	DATA OUTPUT
0	X	0	0
0	X	1	DATA LATCH
X	0	1	DATA LATCH
1	1	X	DATA INPUT

SR=1 CS1•CS2 \downarrow (CLEAR = 1)

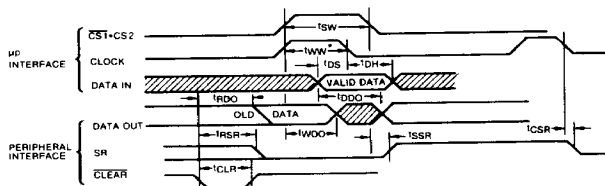
SR=0 CLOCK \downarrow (CLEAR = 1, CS1•CS2 = 0) OR (CLEAR) \downarrow

OUTPUT MODE



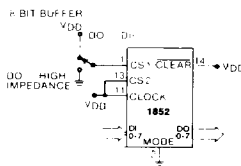
OUTPUT MODE

CS1•CS2 is the overlap of CS1 = 0 and CS2 = 1



*Write is the overlap of CS1•CS2 and Clock

Address Latch



This figure shows 1852 connected as a non-inverting, three state, 8 bit buffer, with $\text{MODE} = 0$, $\text{CLOCK} = 1$ and $\text{CS } 2 = 1$, $\text{CS } 1$ can be used as a tri-state control. When $\text{CS } 1 = 0$, the output is a high impedance, but when $\text{CS } 1 = 1$ data output equals data input. If a high impedance state is not required, the $\text{CS } 1$ input can be tied high ($\text{CS } 1 = 1$).

DI0-DI7: These 8 input lines are strobed into an internal buffer by a high level on the Clock input line and latched by the negative transition of the Clock input.

DO0-DO7: These 8 output lines reflect the information from the internal buffer when the three state drivers are enabled by CS1 • CS2 in the input mode or, at all times, in the output mode.

MODE: This control input sets the 1852 in the input mode with a V_{SS} applied or in the output mode with V_{DD} applied.

CLEAR: This asynchronous reset control clears the buffer register and resets the SR flip flop.

CLOCK: Input Mode: This input strobes data into the buffer when it is activated (high) and sets the SR flip flop (SR = 0) while latching data on its negative transition.

Output Mode: This input along with the chip selects ($\overline{\text{CS1}} \bullet \text{CS2} \bullet \text{Clock} = 1$) strobes data into the buffer. The service request ($\overline{\text{SR}}$) is set high on the termination of $\text{CS1} \bullet \text{CS2} = 1$ and reset low on the next negative transition of the clock.

CS1/CS1, CS2: These chip select controls enable device selection.

SR/SR: This output signal is used as a service request transfer control between the microprocessor and peripheral buses.

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