

GD4053B

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION — The 4053B is a Triple 2-Channel Analog Multiplexer/Demultiplexer with a common Enable Input ($\bar{E}$). Each Multiplexer/Demultiplexer has two Independent Inputs/Outputs (Y_0, Y_1), a Common Input/Output (Z), and a Select Input (S). Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0, Y_1) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\bar{E}$) LOW, one of the two switches is selected (low impedance, ON state) by the Select Input (S). With the Enable Input ($\bar{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Select Inputs (S_a, S_b, S_c).

V_{DD} and V_{SS} are the two supply voltage connections for the Digital Control Inputs ($S_a, S_b, S_c, \bar{E}$). Their voltage limits are the same as for all other digital CMOS. The analog Inputs/Outputs (Y_0, Y_1, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER
- COMMON ENABLE INPUT (ACTIVE LOW)

PIN NAMES

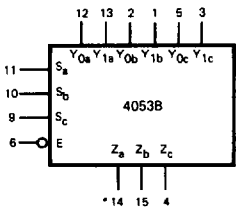
Y_0a-Y_0c, Y_1a-Y_1c	Independent Input/Outputs
S_a-S_c	Select Inputs
$\bar{E}$	Enable Input (Active LOW)
Z_a-Z_c	Common Input/Outputs

TRUTH TABLE

INPUTS		CHANNELS	
$\bar{E}$	S	Y_0-Z	Y_1-Z
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF

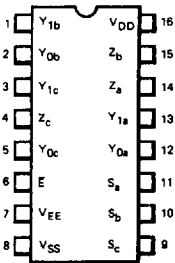
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC SYMBOL



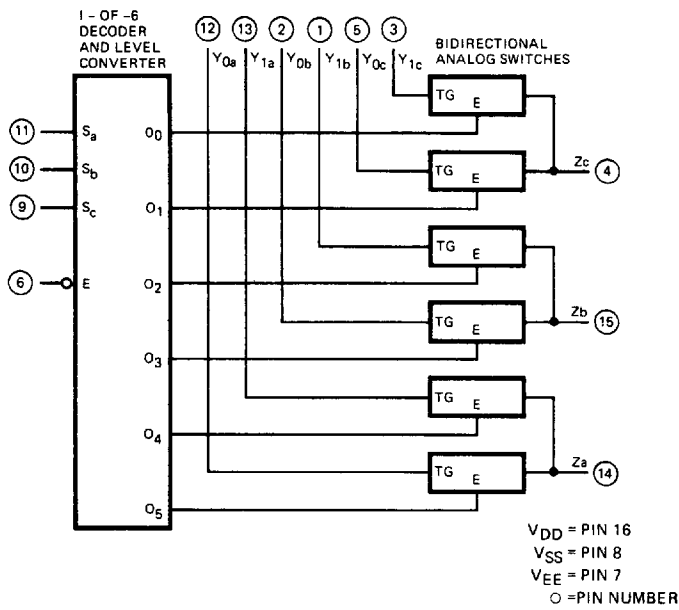
V_{DD} = Pin 16
 V_{SS} = Pin 8
 V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL LOGIC DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, $V_{EE} = 0\text{ V}$ (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V _{DD} = 5 V			V _{DD} = 10 V			V _{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R _{ON}	ON Resistance	XC		95	900		55	380		35	210	Ω	MIN 25°C MAX	V _{is} = V _{DD} to V _{EE} Note 2
				100	1000		65	500		40	280			
				125	1100		100	600		65	340			
		XM		90	850		50	340		30	190	Ω	MIN 25°C MAX	
	100		1000		65	500		40	280					
	150		1150		110	660		70	370					
ΔR _{ON}	"Δ" ON Resistance Between Any Two Channels			25		10			5		Ω	25°C	Note 2	
I _Z	OFF State Leakage	XC					800				nA	25°C	$\bar{E} = V_{DD}$, V _{SS} = V _{DD} /2 V _{is} = V _{DD} or V _{EE} V _{os} = V _{EE} or V _{DD}	
	Current, All Channels OFF		XM					80						
	Any Channel OFF	XC						100						
			XM					10						
I _{DD}	Quiescent Power	XC			20		40		80	μA	MIN, 25°C MAX	V _{SS} = V _{EE} All inputs at 0 V or V _{DD}		
				150		300		600						
	Supply Dissipation	XM		5		10		20	MIN, 25°C MAX					
				150		300		600						

Notes are on the following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{EE} = 0$ V, $T_A = 25^\circ\text{C}$ (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V _{DD} = 5 V			V _{DD} = 10 V			V _{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t _{PLH}	Propagation Delay, Input to Output		25			10			6		ns	C _L = 50 pF R _L = 200 kΩ E̅ = V _{SS} = V _{EE} .
t _{PHL}	Propagation Delay, Select to Output		170			95			80		ns	S _n or V _{is} = V _{DD} or V _{EE} Note 5
t _{PZL}	Output Enable Time		210			125			95		ns	
t _{PZH}	Output Disable Time		185			95			75		ns	C _L = 50 pF , R _L = 1 kΩ E̅ or S _n = V _{SS} = V _{EE}
t _{PLZ}	Output Disable Time		205			105			85		ns	V _{is} = V _{DD} or V _{EE} Note 5
t _{PHZ}	Output Disable Time		1250			1130			1080		ns	
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	R _L = 10 kΩ V _{SS} = V _{DD} /2, E̅ = V _{EE} . V _{is} = V _{DD} /2 (sine wave) p-p f _{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R _L = 1 kΩ E̅ = V _{EE} V _{is} = V _{DD} /2 (sine wave) p-p at -40 dB V _{SS} = V _{DD} /2, 20 Log ₁₀ (V _{OS} /V _{is}) = -40 dB
	OFF State Feedthrough					1					MHz	R _L = 1 kΩ, V _{SS} = V _{DD} /2 E̅ = V _{DD} V _{is} = V _{DD} /2 (sine wave) p-p 20 Log ₁₀ (V _{OS} /V _{is}) = -40 dB
f _{MAX}	ON State Frequency Response		13			40			70		MHz	R _L = 1 kΩ, E̅ = V _{SS} V _{is} = V _{DD} /2 (sine wave) p-p V _{SS} = V _{DD} /2 20 Log ₁₀ (V _{OS} /V _{OS} @ 1 kHz) = -3 dB

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. $\bar{E} = V_{SS}$, $R_L = 10$ k Ω , any channel selected and $V_{SS} = V_{EE}$ or $V_{DD}/2$.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
5. $V_{IN} = V_{DD}$ (Square Wave), Input transition times ≤ 20 ns.
6. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 2, 3, 5, 12, or 13 the voltage drop across the bidirectional switch must not exceed 0.5 V at $T_A \leq 25^\circ\text{C}$, or 0.3 V at $T_A > 25^\circ\text{C}$. No V_{DD} current will flow through R_L if the switch current flows into terminals 4, 14, or 15.