PRELIMINARY

LH28F800SG
8-MBIT (512 KB x 16)
SmartVoltage FLASH MEMORY

FEATURES

- SmartVoltage Technology
  - 3.0V or 5V V_{CC}
  - 3.0V, 5V or 12V V_{PP}
- High-Performance
  - 70 ns (5V V_{CC}) Read Access Time
  - 100 ns (2.7V V_{CC}) Read Access Time
- Enhanced Automated Suspend Options
  - Word Write Suspend to Read
  - Block Erase Suspend to Word Write
  - Block Erase Suspend to Read
- Enhanced Data Protection Features
  - Absolute Protection with V_{PP} = GND
  - Flexible Block Locking
  - Block Erase/Write Lockout during Power Transitions
- Industry Standard Packaging
  - 48-Lead TSOP, 44-Lead PSOP
- Chip Size Packaging
  - 48-Ball CSP
- SRAM-Compatible Write Interface
- High-Density Symmetrically Blocked Architecture
  - Sixteen 32k-word Erasable Blocks
- Extended Cycling Capability
  - 100,000 Block Erase Cycles
  - 1.6 Million Block Erase Cycles/ Device
- Low Power Management
  - Deep Power-Down Mode
  - Automatic Power Savings Mode Decreases I_{CC} in Static Mode
- Automated Word Write and Block Erase
  - Command User Interface
  - Status Register
- ETOX™* V Nonvolatile Flash Technology
- Not designed or rated as radiation hardened

SHARP's LH28F800SG Flash memory with SmartVoltage technology is a high-density, low-cost, nonvolatile, read/ write storage solution for a wide range of applications. LH28F800SG can operate at V_{CC} = 2.7V and V_{PP} = 2.7V. Its low voltage operation capability realize longer battery life and suits for cellular phone application. Its symmetrically-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F800SG offers three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F800SG is manufactured on SHARP's 0.4 µm ETOX™ V process technology. It comes in industry-standard packages: the 48-lead TSOP and 48-ball CSP, ideal for board constrained applications, and the rugged 44-lead PSOP.

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* ETOX is a trademark of Intel Corporation.

1.0 INTRODUCTION

This datasheet contains LH28F800SG specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 New Features

Key enhancements of LH28F800SG SmartVoltage Flash memory are:

- SmartVoltage Technology
- Enhanced Suspend Capabilities
- In-System Block Locking
- Permanent Lock Capability

Please note following important differences:

- V_{PPLK} has been lowered to 1.5V to support 3.3V and 5V block erase, word write, and lock-bit configuration operations. Designs that switch V_{PP} off during read operations should make sure that the V_{PP} voltage transitions to GND.
- To take advantage of SmartVoltage technology, allow V_{PP} connection to 2.7V, 3.3V or 5V.
- Once set the permanent lock bit, the blocks which have been set block lock-bit can not be erased, written forever.

1.2 Product Overview

The LH28F800SG is a high-performance 8-Mbit SmartVoltage Flash memory organized as 512 Kword of 16 bits. The 512 Kword of data is arranged in sixteen 32-Kword blocks which are individually erasable, lockable, and unlockable in-system. The memory map is shown in Figure 6.

SmartVoltage technology provides a choice of V_{CC} and V_{PP} combinations, as shown in Table 1, to meet system performance and power expectations. 3.3V V_{CC} consumes approximately one-fifth the power of 5V V_{CC}. But, 5V V_{CC} provides the highest read performance. V_{PP} at 3.3V and 5V eliminates the need for a separate 12V converter, while V_{PP} = 12V maximizes block erase and word write performance. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 1. V_{CC} and V_{PP} Voltage Combinations Offered by SmartVoltage Technology

V_{CC} Voltage	V_{PP} Voltage
2.7V (1)	2.7V,(2) 3.3V, 5V, 12V
3.3V	3.3V, 5V, 12V
5V	5V, 12V

NOTES:

1. Block erase, word write and lock-bit configuration operations with V_{CC} < 2.7V are not supported.
2. Block erase, word write and lock-bit configuration operations with V_{PP} < 2.7V are not supported.

Internal V_{CC} and V_{PP} detection circuitry automatically configures the device for optimized read and write operations.

A command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timing necessary for block erase, word write, and lock-bit configuration operations.

A block erase operation erases one of the device's 32-Kword blocks typically within 1.2 second (5V V_{CC}, 12V V_{PP}) independent of other blocks. Each block can be independently erased 100,000 times (1.6 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word increments typically within 7.5 µs (5V V_{CC}, 12V V_{PP}). Word write suspend mode enables the system to read data or execute code from any other flash memory array location.

The selected block can be locked or unlocked individuary by the combination of sixteen block lock bits and the WP#. Block erase or word write must not be carried out by setting block lock bits and setting WP# to Low or RP# to V_{IH}. Even if WP# is High state or RP# is set to V_{HH}, block erase and word write to locked blocks is prohibited by setting permanent lock bit. In PSOP, block lock is controlled by RP# since WP# is grounded internally.

The status register indicates when the WSM's block erase, word write, or lock-bit configuration operation is finished.

The RY/BY# output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase, word write, or lock-bit configuration. RY/BY#-high indicates that the WSM is ready for a new command, block erase is suspended (and word write is inactive), word write is suspended, or the device is in deep power-down mode.

The access time is 80 ns (t_{AVAV}) over the commercial temperature range (0°C to +70°C) and V_{CC} supply voltage range of 4.5V-5.5V). At lower V_{CC} voltages, the access times are 85 ns (3.0V-3.6V), 100 ns (2.7V-3.0V).

The Automatic Power Saving (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 1 mA at 5V V_{CC}.

When CE# and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the RP# pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

The device is available in 48-lead TSOP (Thin Small Outline Package, 1.2 mm thick), 44-lead PSOP (Plastic Small Outline Package) and 48-ball CSP (Chip Size Package). Pinouts are shown in Figures 2, 3, 4 and 5.

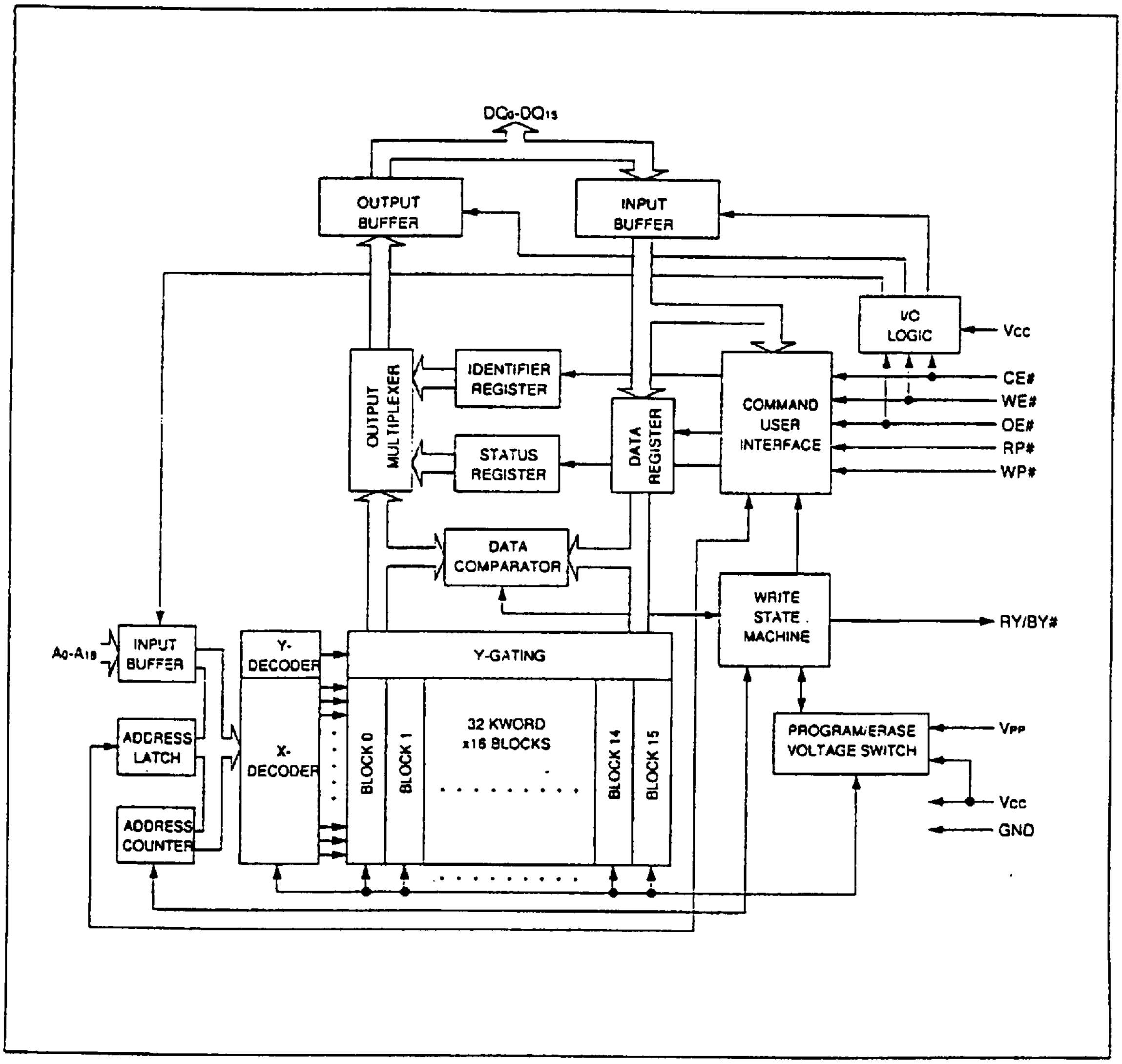

DQ0-DQ15
OUTPUT BUFFER
INPUT BUFFER
I/O LOGIC
Vcc
IDENTIFIER REGISTER
OUTPUT MULTIPLEXER
STATUS REGISTER
DATA REGISTER
COMMAND USER INTERFACE
CE#
WE#
OE#
RP#
WP#
DATA COMPARATOR
WRITE STATE MACHINE
RY/BY#
A0-A18
INPUT BUFFER
Y-DECODER
Y-GATING
ADDRESS LATCH
X-DECODER
32 KWORD x16 BLOCKS
BLOCK 0
BLOCK 1
BLOCK 14
BLOCK 15
ADDRESS COUNTER
PROGRAM/ERASE VOLTAGE SWITCH
VPP
Vcc
GND

Figure 1. Block Diagram

Table 2. Pin Descriptions

Symbol	Type	Name and Function
A_0 - A_{18}	INPUT	**ADDRESS INPUTS:** Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle.
DQ_0 - DQ_{15}	INPUT/OUTPUT	**DATA INPUT/OUTPUTS:** Inputs data and commands during CUI write cycles; outputs data during memory array, status register, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Puts the device in deep power-down mode and resets internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. RP# at V_{HH} allows to set permanent lock-bit. Block erase, word write, or lock-bit configuration with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.
OE#	INPUT	**OUTPUT ENABLE:** Gates the device's outputs during a read cycle.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	**WRITE PROTECT:** Master control for block locking. When V_{IL}, locked blocks cannot be erased and programmed, and block lock-bits can not be set and reset.
RY/BY#	OUTPUT	**READY/BUSY#:** Indicates the status of the internal WSM. When low, the WSM is performing an interml operation (block erase, word write, or lock-bit configuration). RY/BY#-high indicates that the WSM is ready for new commands, block erase is suspended, and word write is inactive, word write is suspended, or the device is in deep power-down mode. RY/BY# is always active and does not float when the chip is deselected or data outputs are disabled.
V_{PP}	SUPPLY	**BLOCK ERASE, WORD WRITE, LOCK-BIT CONFIGURATION POWER SUPPLY:** For erasing array blocks, writing words, or configuration lock-bits. With $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. Block erase, word write, and lock-bit configuration with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY:** Internal detection configured the device for 3.3V or 5V operation. To switch from one voltage to another, ramp V_{CC} down to GND and then ramp V_{CC} to the new voltage. Do not float any power pins.With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	**GROUND:** Do not float any ground pins.
NC		**NO CONNECT:** Lead is not internal connected: it may be driven or floated.

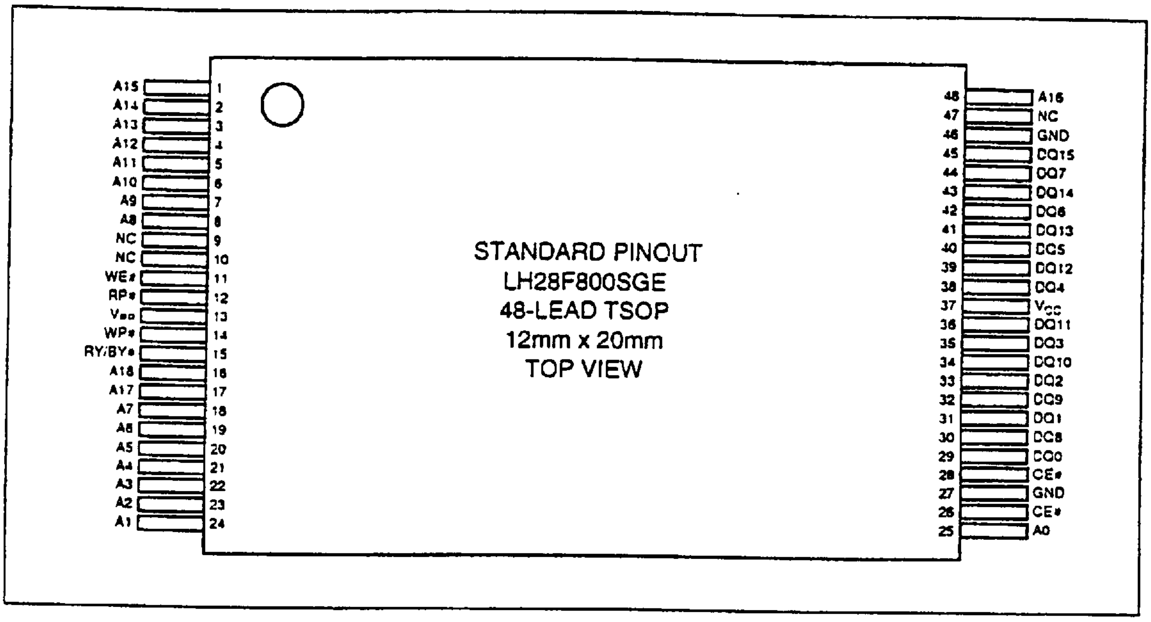

STANDARD PINOUT
LH28F800SGE
48-LEAD TSOP
12mm x 20mm
TOP VIEW
A15 1
A14 2
A13 3
A12 4
A11 5
A10 6
A9 7
A8 8
NC 9
NC 10
WE# 11
RP# 12
VPP 13
WP# 14
RY/BY# 15
A18 16
A17 17
A7 18
A6 19
A5 20
A4 21
A3 22
A2 23
A1 24
48 A16
47 NC
46 GND
45 DQ15
44 DQ7
43 DQ14
42 DQ6
41 DQ13
40 DQ5
39 DQ12
38 DQ4
37 VCC
36 DQ11
35 DQ3
34 DQ10
33 DQ2
32 DQ9
31 DQ1
30 DQ8
29 DQ0
28 CE#
27 GND
26 CE#
25 A0

Figure 2. 48-Lead TSOP Standard Pinout Configuration

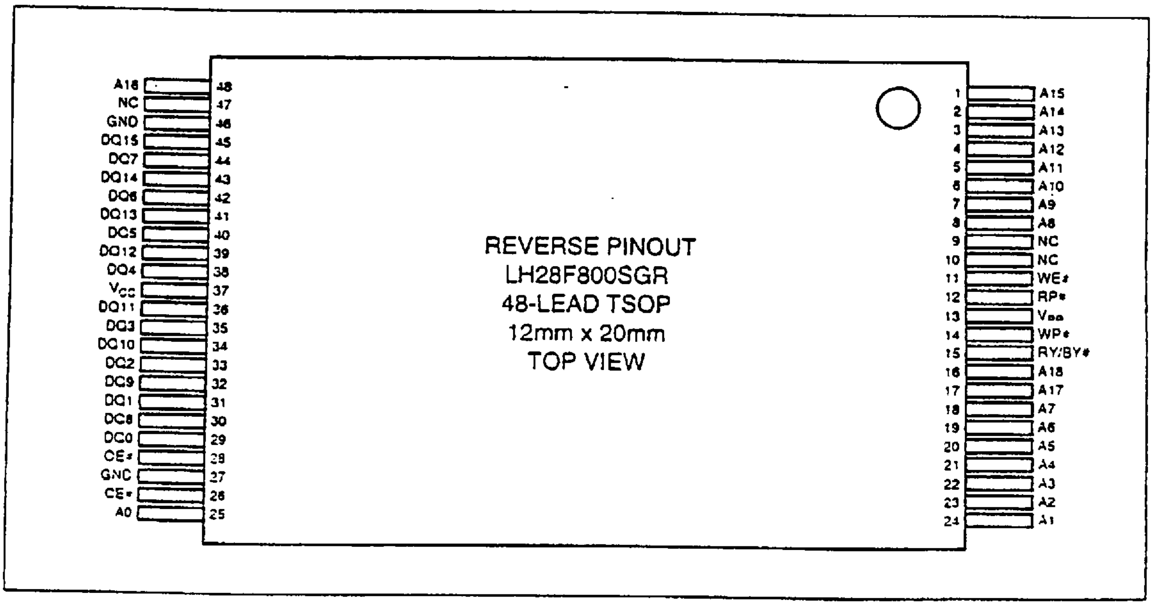

REVERSE PINOUT
LH28F800SGR
48-LEAD TSOP
12mm x 20mm
TOP VIEW
A16 48
NC 47
GND 46
DQ15 45
DQ7 44
DQ14 43
DQ6 42
DQ13 41
DQ5 40
DQ12 39
DQ4 38
VCC 37
DQ11 36
DQ3 35
DQ10 34
DQ2 33
DQ9 32
DQ1 31
DQ8 30
DQ0 29
CE# 28
GND 27
CE# 26
A0 25
1 A15
2 A14
3 A13
4 A12
5 A11
6 A10
7 A9
8 A8
9 NC
10 NC
11 WE#
12 RP#
13 VPP
14 WP#
15 RY/BY#
16 A18
17 A17
18 A7
19 A6
20 A5
21 A4
22 A3
23 A2
24 A1

Figure 3. 48-Lead TSOP Reverse Pinout Configuration

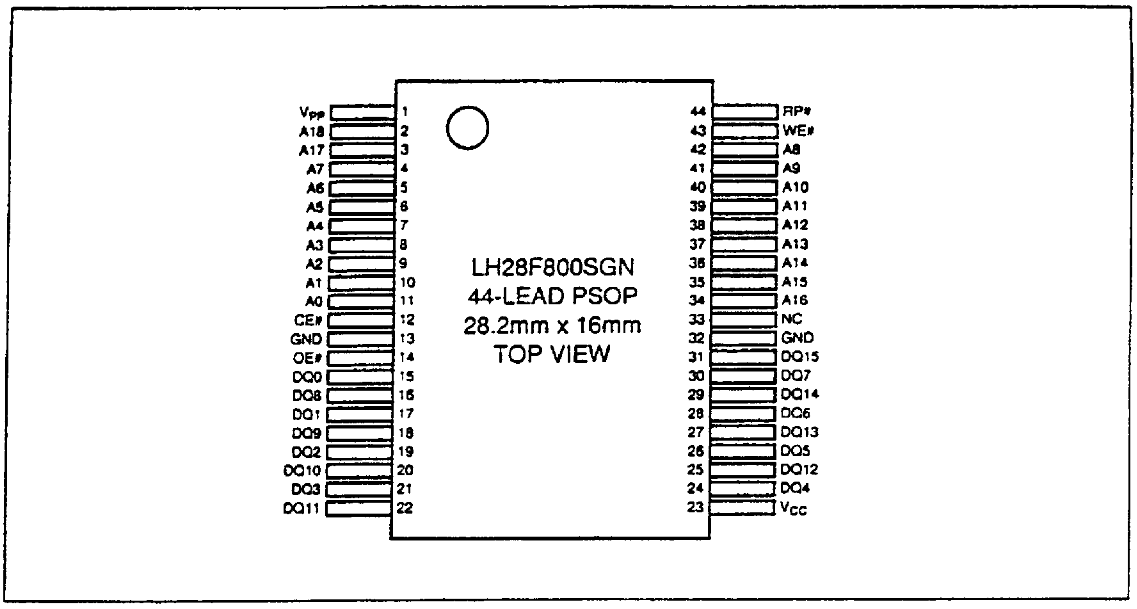

LH28F800SGN
44-LEAD PSOP
28.2mm x 16mm
TOP VIEW
VPP 1
A18 2
A17 3
A7 4
A6 5
A5 6
A4 7
A3 8
A2 9
A1 10
A0 11
CE# 12
GND 13
OE# 14
DQ0 15
DQ8 16
DQ1 17
DQ9 18
DQ2 19
DQ10 20
DQ3 21
DQ11 22
44 RP#
43 WE#
42 A8
41 A9
40 A10
39 A11
38 A12
37 A13
36 A14
35 A15
34 A16
33 NC
32 GND
31 DQ15
30 DQ7
29 DQ14
28 DQ6
27 DQ13
26 DQ5
25 DQ12
24 DQ4
23 VCC

Figure 4. 44-Lead PSOP Pinout Configuration

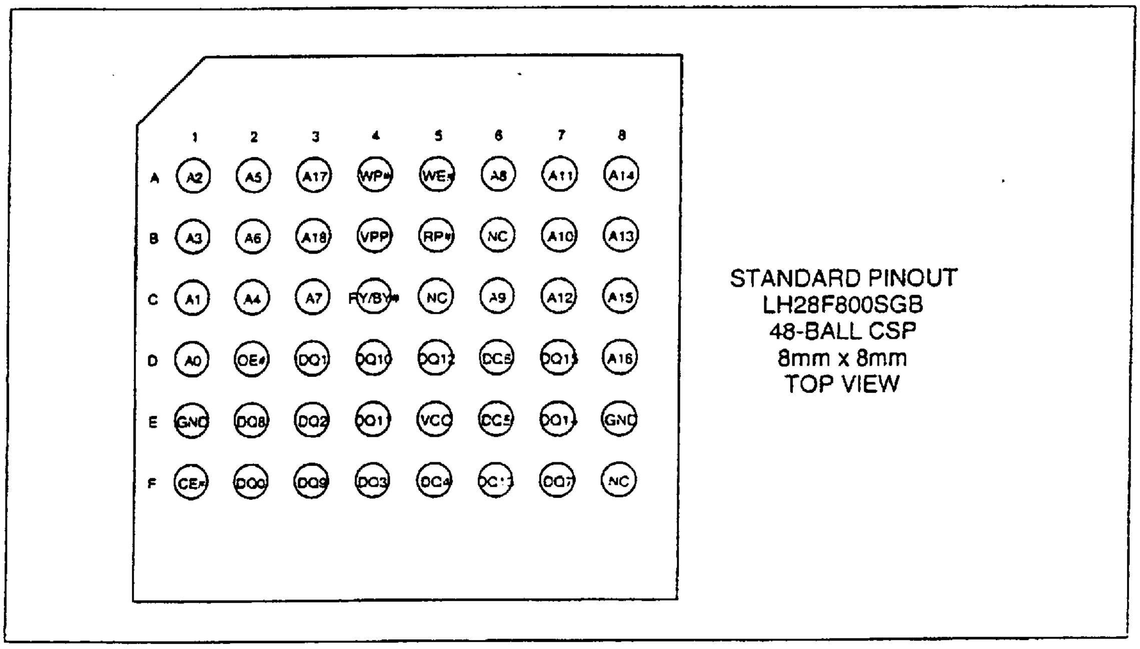

1
2
3
4
5
6
7
8
A
A2
A5
A17
WP#
WE#
A8
A11
A14
B
A3
A6
A18
VPP
RP#
NC
A10
A13
C
A1
A4
A7
RY/BY#
NC
A9
A12
A15
D
A0
OE#
DQ1
DQ10
DQ12
DQ6
DQ13
A16
E
GND
DQ8
DQ2
DQ11
VCC
DQ5
DQ14
GND
F
CE#
DQ0
DQ9
DQ3
DQ4
DQ15
DQ7
NC
STANDARD PINOUT
LH28F800SGB
48-BALL CSP
8mm x 8mm
TOP VIEW

Figure 5. 48-Ball CSP Pinout Configuration

2.0 PRINCIPLES OF OPERATION

The LH28F800SG SmartVoltage Flash memory includes an on-chip WSM to manage block erase, word write, and lock-bit configuration functions. It allows for 100% TTL-level control inputs, fixed power supplies during block erasure, word write, and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erasure, word writing, and lock-bit configuration. All functions associated with altering memory contents — block erase, word write, lock-bit configuration, status, and identifier codes — are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, word write, and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase, word write, and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Word write suspend allows system software to suspend a word write to read data from any other flash memory array location.

7FFFF	78000	32 Kword Block	15
77FFF	70000	32 Kword Block	14
6FFFF	68000	32 Kword Block	13
67FFF	60000	32 Kword Block	12
5FFFF	58000	32 Kword Block	11
57FFF	50000	32 Kword Block	10
4FFFF	48000	32 Kword Block	9
47FFF	40000	32 Kword Block	8
3FFFF	38000	32 Kword Block	7
37FFF	30000	32 Kword Block	6
2FFFF	28000	32 Kword Block	5
27FFF	20000	32 Kword Block	4
1FFFF	18000	32 Kword Block	3
17FFF	10000	32 Kword Block	2
0FFFF	08000	32 Kword Block	1
07FFF	00000	32 Kword Block	0

Figure 6. Memory Map

2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erases, word writes, or lock-bit configurations are required) or hardwired to $V_{PPH1/2/3}$. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase, word write, or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating erase and word write operations.

3.0 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes, or status register independent of the V_{PP} voltage. RP# can be at either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component: CE#, OE#, WE#, RP# and WP#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and when active drives the selected memory data onto the I/O bus. WE# must be at V_{IH} and RP# must be at V_{IH} or V_{HH}. Figure 18 illustrates read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins DQ_0-DQ_{15} are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0-DQ_{15} outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, word write, or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, word write, or lock-bit configuration modes, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, word write, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block, and the permanent lock configuration code (see Figure 7). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and permanent lock configuration codes identify locked and unlocked blocks and permanent lock-bit setting.

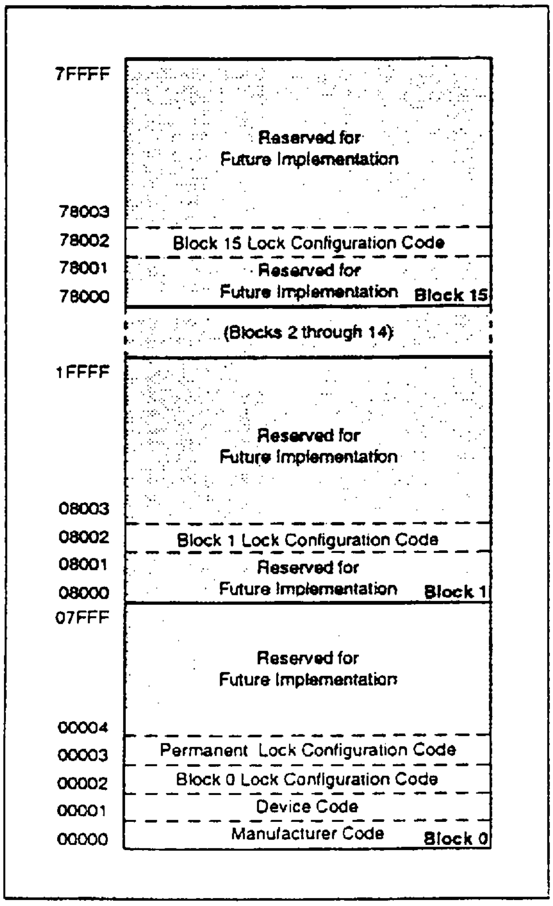

7FFFF
Reserved for Future Implementation
78003
78002
Block 15 Lock Configuration Code
78001
Reserved for Future Implementation
78000
Block 15
(Blocks 2 through 14)
1FFFF
Reserved for Future Implementation
08003
08002
Block 1 Lock Configuration Code
08001
Reserved for Future Implementation
08000
Block 1
07FFF
Reserved for Future Implementation
00004
00003
Permanent Lock Configuration Code
00002
Block 0 Lock Configuration Code
00001
Device Code
00000
Manufacturer Code
Block 0

Figure 7. Device Identifier Code Memory Map

3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word Write command requires the command and address of the location to be written. Set Permanent and Block Lock-Bit commands require the command and address within the device (Permanent Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 19 and 20 illustrate WE# and CE# controlled write operations.

4.0 COMMAND DEFINITIONS

When the $V_{PP} \leq V_{PPLK}$, Read operations from the status register, identifier codes, or blocks are enabled. Placing $V_{PPH1/2/3}$ on V_{PP} enables successful block erase, word write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

Table 3. Bus Operations

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{PP}	DQ_{0-15}	RY/BY#
Read	1, 2, 3, 8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable	3	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	3	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	X
Deep Power-Down	4	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Read Identifier Codes	8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 7	X	Note 5	V_{OH}
Write	3, 6, 7, 8	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2/3}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2/3}$ voltages.
3. RY/BY# is V_{OL} when the WSM is executing internal block erase, word write, or lock-bit configuration algorithms. It is V_{OH} during when the WSM is not busy, in block erase suspend mode (with word write inactive), word write suspend mode, or deep power-down mode.
4. RP# at GND ± 0.2V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.

6V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.

7. Refer to Table 4 for valid D_{IN} during a write operation.
8. Never hold OE# low and WE# low at the same timing.

Table 4. Command Definitions (9)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper (1)	Addr (2)	Data (3)	Oper (1)	Addr (2)	Data (3)
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥ 2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Word Write	2	5, 6	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word Write Suspend	1	5	Write	X	B0H			
Block Erase and Word Write Resume	1	5	Write	X	D0H			
Set Block Lock-Bit	2	7	Write	BA	60H	Write	BA	01H
Set Permanent Lock-Bit	2	7	Write	X	60H	Write	X	F1H
Clear Block Lock-Bits	2	8	Write	X	60H	Write	X	D0H

NOTES:

1. Bus operations are defined in Table 3.
2. X = Any valid address within the device.
   IA = Identifier Code Address: see Figure 7.
   BA = Address within the block being erased or locked.
   WA = Address of memory location to be written.
3. SRD = Data read from status register. See Table 7 for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID = Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and permanent lock codes. See Section 4.2 for read identifier code data.
5. If the block is locked, WP# must be at V_{IH} or RP# must be at V_{HH} to enable block erase or word write operations. Attempts to issue a block erase or word write to a locked block while WP# is V_{IH} or RP# is V_{IH}.
6. Either 40H or 10H are recognized by the WSM as the word write setup.
7. If the permanent lock-bit is set, WP# must be at V_{IH} or RP# must be at V_{HH} to set a block lock-bit. RP# must be at V_{HH} to set the permanent lock-bit. If the permanent lock-bit is set, a block lock-bit cannot be set. Once the permanent lock-bit is set, permanent lock-bit reset is unable.
8. If the permanent lock-bit is set, clear block lock-bits operation is unable. The clear block lock-bits operation simultaneously clears all block lock-bits. If the permanent lock-bit is not set, the Clear Block Lock-Bits command can be done while WP# is V_{IH} or RP# is V_{HH}.
9. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, word write or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 7 retrieve the manufacturer, device, block lock configuration and permanent lock configuration codes (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes

Code		Data	Address
Manufacture Code		0080H	00000H
Device Code		0050H	00001H
Block Lock[2] Configuration	Block is Unlocked	$DQ_0 = 0$	X0002H[1]
	Block is Locked	$DQ_0 = 1$	
Permanent Lock[2] Configuration	Device is Unlocked	$DQ_0 = 0$	00003H
	Device is Locked	$DQ_0 = 1$	

NOTE:

1. X selects the specific block lock configuration code to be read. See Figure 5 for the device identifier code memory map.
2. Block lock status and permanent lock status are output by DQ_0. DQ_1-DQ_{15} are reserved for future enhancement.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, word write, or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. RP# can be V_{IH} or V_{HH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 7). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several words in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} voltage. RP# can be V_{IH} or V_{HH}. This command is not functional during block erase or word write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect block erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when $V_{CC} = V_{CC1/2/3/4}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase requires that the corresponding block lock-bit be cleared or, if set, that WP# = V_{IH} or RP# = V_{HH}. If block erase is attempted when the corresponding block lock-bit is set and WP# = V_{IL} or RP# = V_{IH}, SR.1 and SR.5 will be set to "1". Once permanent lock-bit is set, the blocks which have been set block lock-bit are unable to erase forever. Block erase operations with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.

4.6 Word Write Command

Word write is executed by a two-cycle command sequence. Word write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word write and write verify algorithms internally. After the word write sequence is written, the device automatically outputs status register data when read (see Figure 9). The CPU can detect the completion of the word write event by analyzing the RY/BY# pin or status register bit SR.7.

When word write is complete, status register bit SR.4 should be checked. If word write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word writes can only occur when $V_{CC} = V_{CC1/2/3/4}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, memory contents are protected against word writes. If word write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word write requires that the corresponding block lock-bit be cleared or, if set, that WP# = V_{IH} or RP# = V_{HH}. If word write is attempted when the corresponding block lock-bit is set and WP# = V_{IL} or RP# = V_{IH}, SR.1 and SR.4 will be set to "1". Once permanent lock-bit is set, the blocks which have been set block lock-bit are unable to write forever. Word write operations with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.

4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word-write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word Write Suspend command (see Section 4.8), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 10). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for block erase). WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for block erase). Block erase cannot resume until word write operations initiated during block erase suspend have completed.

4.8 Word Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the word write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word write operation has been suspended (both will be set to "1"). RY/BY# will also transition to V_{OH}. Specification t_{WHRH1} defines the word write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After Word Write Resume command is written to the flash memory, the WSM will continue the word write process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Word Write Resume command is written, the device automatically outputs status register data when read (see Figure 11). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for word write) while in word write suspend mode. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for word write). WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for word write).

4.9 Set Block and Permanent Lock-Bit Commands

The combination of the software command sequence and hardware WP#, RP# pin provides most flexible block lock (write protection) capability. The word write/ block erase operation is restricted by the status of block lock-bit, WP# pin, RP# pin and permanent lock-bit. The status of WP# pin, RP# pin and permanent lock-bit restricts the set block bit. When the permanent lock-bit has not been set, and when WP# = V_{IH} or RP# = V_{HH}, the block lock bit can be set with the status of the RP#pin. When RP# = V_{HH} the permanent lock-bit can be set with the the permanent lock-bit set command. After the the permanent lock-bit has been set, the write/erase operation to the block lock bit can never be accepted. Please refer to the Table 6 for the hardware and the software write protection.

Set block lock-bit and permanent lock-bit are executed by a two-cycle command sequence. The set block or permanent lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set permanent lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 12). The CPU can detect the completion of the set lock-bit event by analyzing the RY/BY# pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Permanent Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when $V_{CC} = V_{CC1/2/3/4}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the permanent lock-bit be cleared and WP# = V_{IH} or RP# = V_{HH}. If it is attempted with the permanent lock-bit set, SR.1 and SR.4 will be set to "1" and the operation will fail. Set block lock-bit operations while V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted. A successful set permanent lock-bit operation requires that RP# = V_{HH}. If it is attempted with RP# = V_{IH}, SR.1 and SR.4 will be set to "1" and the operation will fail. Set permanent lock-bit operations with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.

4.10 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the permanent lock-bit not set and WP# = V_{IH} or RP# = V_{HH}, block lock-bits can be cleared using the Clear Block Lock-Bits command. If the permanent lock-bit is set, clear block lock-bits operation is unable. See Table 6 for a summary of hardware and software write protection options.

Clear block lock-bits option is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 13). The CPU can detect completion of the clear block lock-bits event by analyzing the RY/BY# pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when $V_{CC} = V_{CC1/2/3/4}$ and $V_{PP} = V_{PPH1/2/3}$. In a clear block lock-bits operation is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the permanent lock-bit is not set and WP# = V_{IH} or RP# = V_{HH}. If it is attempted with the permanent lock-bit set or WP# = V_{IL} or RP# = V_{IH}, SR.1 and SR.5 will be set to "1" and the operation will fail. A clear block lock-bits operation with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to V_{PP} or V_{CC} transitioning out of valid range or RP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the permanent lock-bit is set, it cannot be cleared.

Table 6. Write Protection Alternatives

Operation	Permanent Lock-Bit	Block Lock-Bit	WP#	RP#	Effect
Word Write or Block Erase	X	0	X	V_{IH} or V_{HH}	Block Erase and Word Write Enabled
	0	1	V_{IH}	V_{IH} or V_{HH}	Block Lock-Bit Override. Block Erase and Word Write Enabled
			V_{IL}	V_{HH}	Block Lock-Bit Override. Block Erase and Word Write Enabled
				V_{IH}	Block is Locked. Block Erase and Word Write Disabled
	1		X	X	Permanent Lock-Bit is set. Block Erase and Word Write Disabled
Set Block Lock-Bit	0	X	V_{IH}	V_{IH} or V_{HH}	Set Block Lock-Bit Enabled
			V_{IL}	V_{HH}	Set Block Lock-Bit Enabled
			V_{IL}	V_{IH}	Set Block Lock-Bit Disabled
	1		X	X	Permanent Lock-Bit is set. Set Block Lock-Bit Disabled
Set Permanent Lock-Bit	X	X	X	V_{HH}	Set Permanent Lock-Bit Enabled
				V_{IH}	Set Permanent Lock-Bit Disabled
Clear Block Lock-Bits	0	X	V_{IH}	V_{IH} or V_{HH}	Clear Block Lock-Bits Enabled
			V_{IL}	V_{HH}	Clear Block Lock-Bits Enabled
			V_{IL}	V_{IH}	Clear Block Lock-Bits Disabled
	1		X	X	Permanent Lock-Bit is set. Clear Block Lock-Bits Disabled

Table 7. Status Register Definition

WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 = ERASE SUSPEND STATUS
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR LOCK-BITS STATUS
1 = Error in Block Erasure or Clear Lock-Bits
0 = Successful Block Erase or Clear Lock-Bits

SR.4 = WORD WRITE AND SET LOCK-BIT STATUS
1 = Error in Word Write or Set Permanent/Block Lock-Bit
0 = Successful Word Write or Set Permanent/Block Lock-Bit

SR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

SR.2 = WORD WRITE SUSPEND STATUS
1 = Word Write Suspended
0 = Word Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
1 = Permanent Lock-Bit, Block Lock-Bit and/or WP#/RP# Lock Detected, Operation Abort
0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

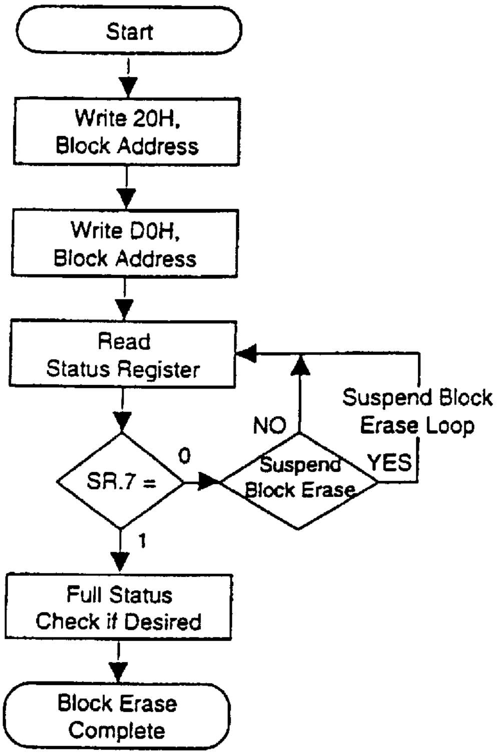
Check RY/BY# or SR.7 to determine block erase, word write, or lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0".

If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Word Write, Set Block/ Permanent Lock-Bit, or Clear Block Lock-Bits command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} = V_{PPH1/2/3}$.

SR.1 does not provide a continuous indication of permanent and block lock-bit values. The WSM interrogates the permanent lock-bit, block lock-bit, WP# and RP# only after Block Erase, Word Write, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set, and/ or WP# is not V_{IH}, RP# is not V_{HH}. Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status.

SR.0 is reserved for future use and should be masked out when polling the status register.


Start
Write 20H, Block Address
Write D0H, Block Address
Read Status Register
SR.7 =
0
1
NO
Suspend Block Erase
YES
Suspend Block Erase Loop
Full Status Check if Desired
Block Erase Complete

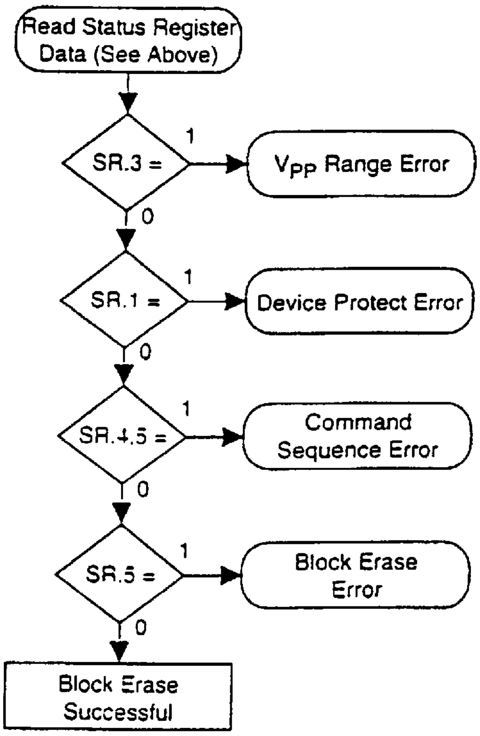
Bus Operation	Command	Comments
Write	Erase Setup	D = 20H A = Within Block to be Erased
Write	Erase Confirm	D = D0H A = Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.

Full status check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

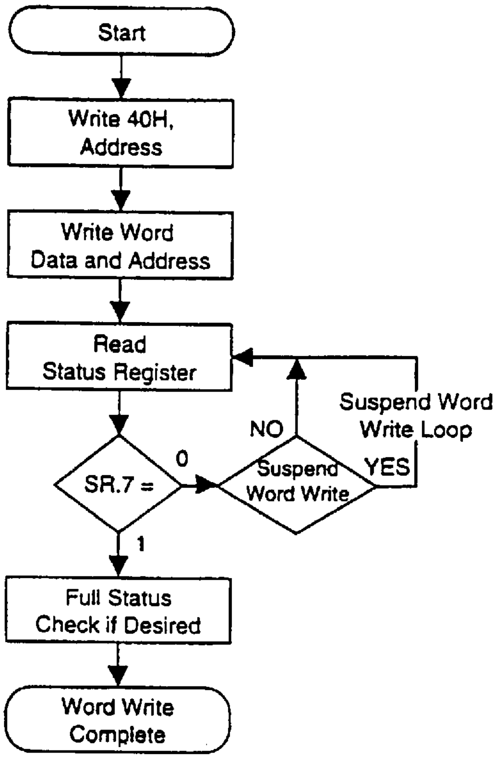

Read Status Register Data (See Above)
SR.3 =
1
V_{PP} Range Error
0
SR.1 =
1
Device Protect Error
0
SR.4.5 =
1
Command Sequence Error
0
SR.5 =
1
Block Erase Error
0
Block Erase Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH}, Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4.5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 8. Automated Block Erase Flowchart


Start
Write 40H, Address
Write Word Data and Address
Read Status Register
SR.7 =
0
1
Suspend Word Write
NO
YES
Suspend Word Write Loop
Full Status Check if Desired
Word Write Complete

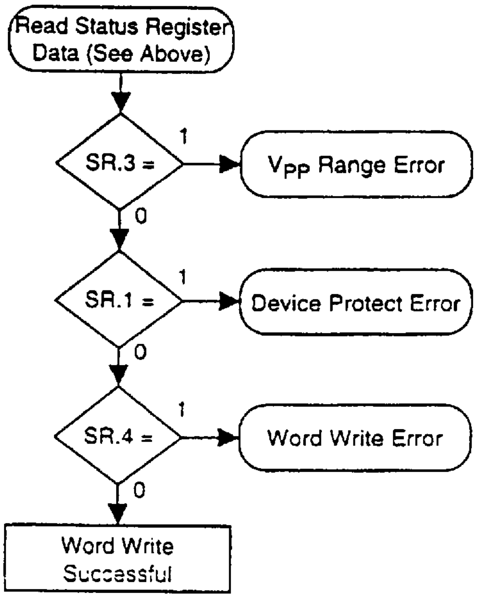
Bus Operation	Command	Comments
Write	Setup Word Write	D = 40H A = Location to Be Written
Write	Word Write	D = Data to Be Written A = Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent word writes.

SR full status check can be done after each word write, or after a sequence of word writes.

Write FFH after the last word write operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

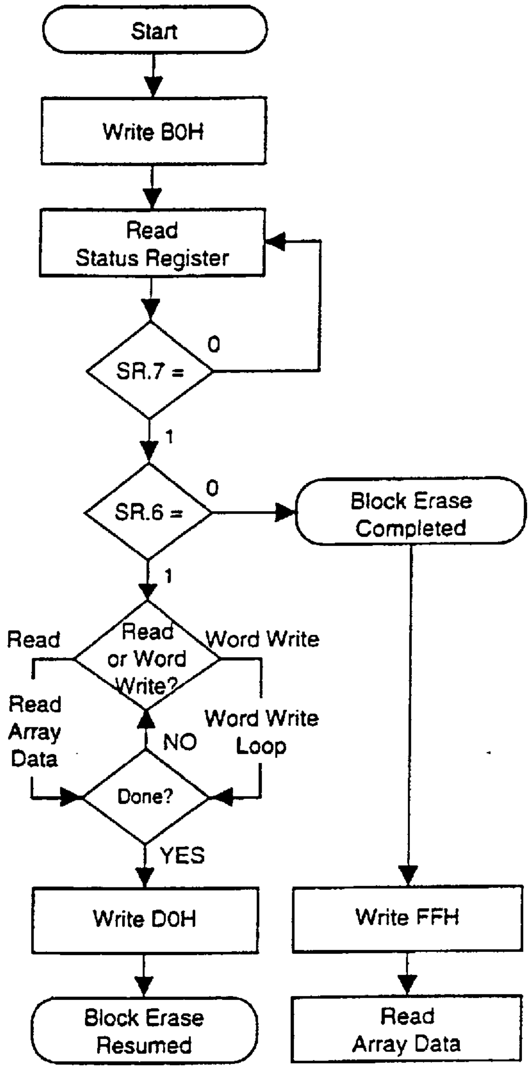

Read Status Register Data (See Above)
SR.3 =
1
0
V_PP Range Error
SR.1 =
1
0
Device Protect Error
SR.4 =
1
0
Word Write Error
Word Write Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH}, Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4 1 = Data Write Error

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.

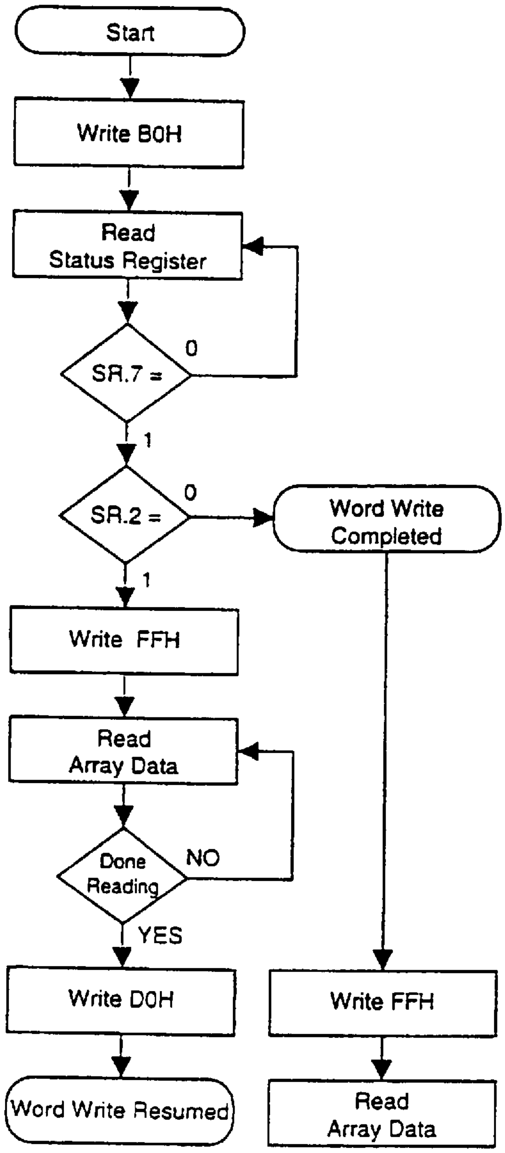
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 9. Automated Word Write Flowchart


Start
Write B0H
Read
Status Register
SR.7 =
0
1
SR.6 =
0
Block Erase
Completed
1
Read
or Word
Write?
Read
Word Write
Read
Array
Data
NO
Word Write
Loop
Done?
YES
Write D0H
Write FFH
Block Erase
Resumed
Read
Array Data

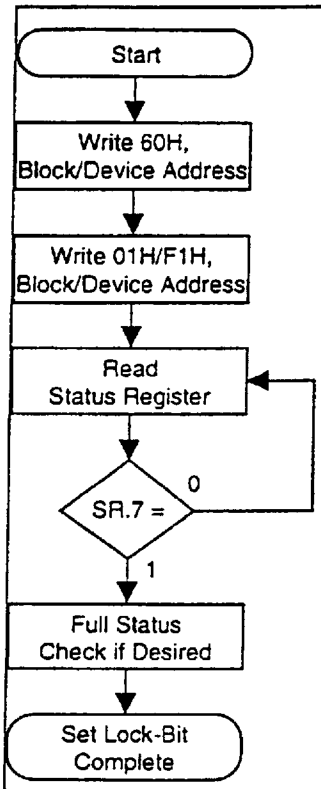
Bus Operation	Command	Comments
Write	Erase Suspend	D = B0H A = X
Read		Status Register Data A = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	D = D0H A= X

Figure 10. Block Erase Suspend/Resume Flowchart


Start
Write B0H
Read Status Register
SR.7 =
0
1
SR.2 =
0
1
Word Write Completed
Write FFH
Read Array Data
Done Reading
NO
YES
Write D0H
Word Write Resumed
Write FFH
Read Array Data

Bus Operation	Command	Comments
Write	Word Write Suspend	D = B0H A = X
Read		Status Register Data A = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Word Write Suspended 0 = Word Write Completed
Write	Read Array	D = FFH A= X
Read		Read array locations other than that being written
Write	Word Write Resume	D = D0H A = X

Figure 11. Word Write Suspend/Resume Flowchart


Start
Write 60H,
Block/Device Address
Write 01H/F1H,
Block/Device Address
Read
Status Register
SR.7 =
0
1
Full Status
Check if Desired
Set Lock-Bit
Complete

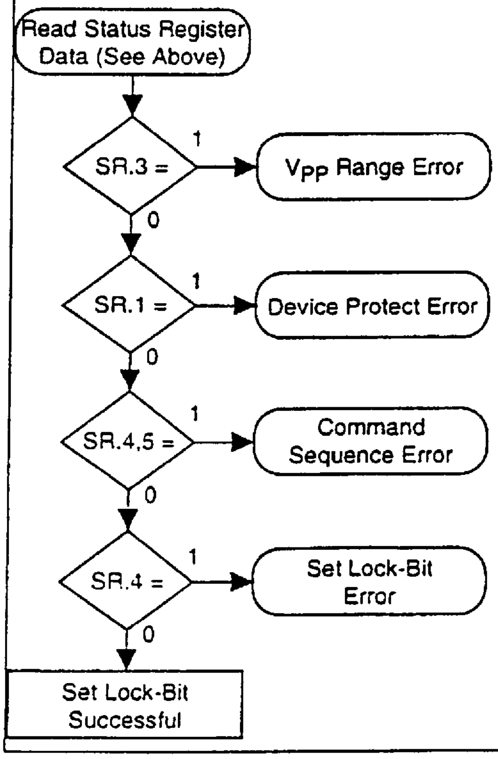
Bus Operation	Command	Comments
Write	Set Block/Permanent Lock-Bit Setup	D = 60H A = Block Address (Block), Device Address (Permanent)
Write	Set Block or Permanent Lock-Bit Confirm	D = 01H (Block), F1H (Permanent) A = Block Address (Block), Device Address (Permanent)
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent lock-bit set operations.

Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations.

Write FFH after the last lock-bit set operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

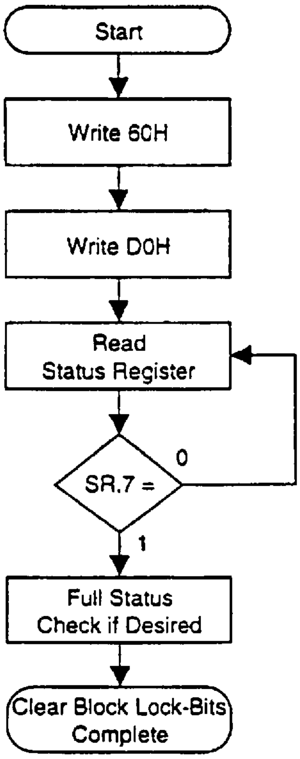

Read Status Register
Data (See Above)
SR.3 =
1
Vpp Range Error
0
SR.1 =
1
Device Protect Error
0
SR.4,5 =
1
Command
Sequence Error
0
SR.4 =
1
Set Lock-Bit
Error
0
Set Lock-Bit
Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH} (Set Permanent Lock-Bit Operation) WP# = V_{IL}, Permanent Lock-Bit is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Lock-Bit Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked.

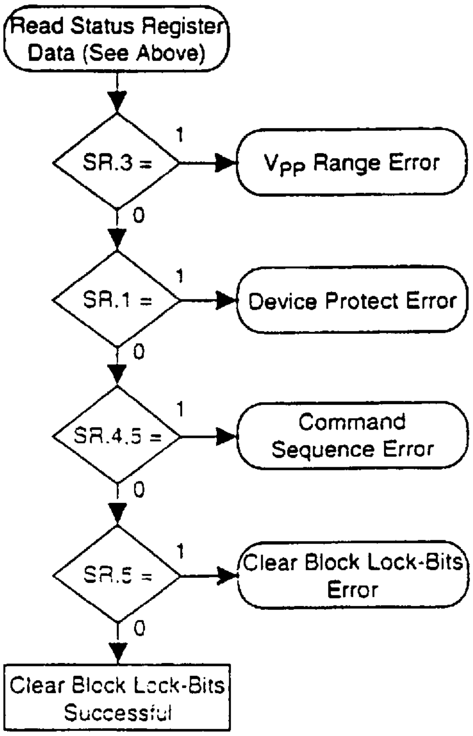
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 12. Set Block and Permanent Lock-Bit Flowchart


Start
Write 60H
Write D0H
Read Status Register
SR.7 =
0
1
Full Status Check if Desired
Clear Block Lock-Bits Complete

Bus Operation	Command	Comments
Write	**Clear Block Lock-Bits Setup**	D = 60H A = X
Write	**Clear Block Lock-Bits Confirm**	D = D0H A = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE


Read Status Register Data (See Above)
SR.3 =
1
V_PP Range Error
0
SR.1 =
1
Device Protect Error
0
SR.4,5 =
1
Command Sequence Error
0
SR.5 =
1
Clear Block Lock-Bits Error
0
Clear Block Lock-Bits Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect WP# = V_{IL} and RP# = V_{IH} or Permanent Lock-Bit is Set
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 13. Clear Block Lock-Bits Flowchart

5.0 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a. Lowest possible memory power dissipation.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 RY/BY# and Block Erase, Word Write, and Lock-Bit Configuration Polling

RY/BY# is a full CMOS output that provides a hardware method of detecting block erase, word write and lock-bit configuration completion. It transitions low after block erase, word write, or lock-bit configuration commands and returns to V_{OH} when the WSM has finished executing the internal algorithm.

RY/BY# can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/BY# is also V_{OH} when the device is in block erase suspend (with word write inactive), word write suspend or deep power-down modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for word writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

5.5 V_{CC}, V_{PP}, RP# Transitions

Block erase, word write and lock-bit configuration are not guaranteed if V_{PP} falls outside of a valid $V_{PPH1/2/3}$ range, V_{CC} falls outside of a valid $V_{CC2/3/4}$ range, or RP# ≠ V_{IH} or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to V_{IL} during block erase, word write, or lock-bit configuration, RY/BY# will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase, word write, or lock-bit configuration, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure, word writing, or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while RP# = V_{IL} regardless of its control inputs state.

5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after RP# is first raised to V_{IH}. See AC Characteristics — Read Only and Write Operations and Figures 18, 19 and 20 for more information.

6.0 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

<Operating Temperature>
Commercial Products
During Read, Block Erase, Word Write,
and Lock-Bit Configuration .... 0°C to + 70°C
Temperature under Bias .... -10°C to + 80°C
Extended temperature Products
During Read, Block Erase, Word Write,
and Lock-Bit Configuration .... -40°C to + 85°C
Temperature under Bias .... -40°C to + 85°C
<Storage Temperature> .... - 65°C to + 125°C
<Voltage On Any Pin>
except V_{CC}, V_{PP}, and RP# .... -2.0V to + 7.0V (1)
V_{CC} Supply Voltage .... -2.0V to + 7.0V (1)
V_{PP} Update Voltage during
Block Erase, Word Write, and
Lock-Bit Configuration .... -2.0V to + 14.0V (1,2)
RP# Voltage with Respect to
GND during Lock-Bit
Configuration Operations ..... -2.0V to + 14.0V (1,2)
<Output Short Circuit Current> .... 100 mA (3)

NOTICE: This datasheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local SHARP Sales office that you have the latest datasheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is - 0.5V on input/output pins and - 0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to - 2.0V for periods < 20 ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods < 20 ns.
3. Maximum DC voltage on V_{PP} and RP# may overshoot to +14.0V for periods < 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T_A	Operating Temperature Commercial Products		0	+ 70	°C	Ambient Temperature
T_A	Operating Temperature Extended temperature Products		-40	+ 85	°C	Ambient Temperature
V_{CC1}	V_{CC} Supply Voltage (2.7V - 3.6V)		2.7	3.6	V	
V_{CC2}	V_{CC} Supply Voltage (3.3V ± 0.3V)		3.0	3.6	V	
V_{CC3}	V_{CC} Supply Voltage (5.0V ± 5%)		4.75	5.25	V	
V_{CC4}	V_{CC} Supply Voltage (5.0V ± 10%)		4.50	5.50	V	

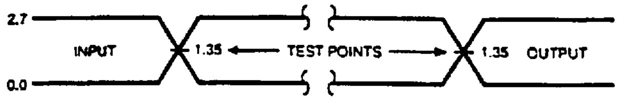
6.2.1 Capacitance (1)

T_A = + 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0V

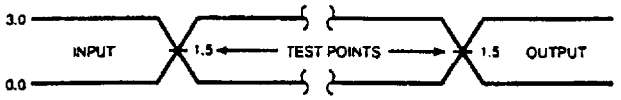
NOTES:
1. Sampled, not 100% tested.

6.2.2 AC Input/Output Test Conditions


2.7
0.0
INPUT
1.35
TEST POINTS
1.35
OUTPUT

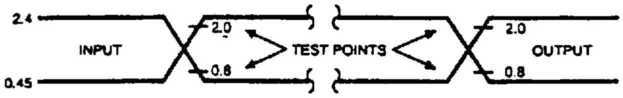
AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) < 10 ns.

Figure 14. Transient Input/Output Reference Waveform for $2.7V \leq V_{cc} < 3.0V$


3.0
0.0
INPUT
1.5
TEST POINTS
1.5
OUTPUT

AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10 ns.

Figure 15. Transient Input/Output Reference Waveform for $3.0V \leq V_{cc} \leq 3.6V$ and $4.75V \leq V_{cc} \leq 5.25V$
(High Speed Testing Configuration)


2.4
0.45
INPUT
2.0
0.8
TEST POINTS
2.0
0.8
OUTPUT

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) < 10 ns.

Figure 16. Transient Input/Output Reference Waveform for $4.5V \leq V_{cc} \leq 5.5V$
(Standard Testing Configuration)

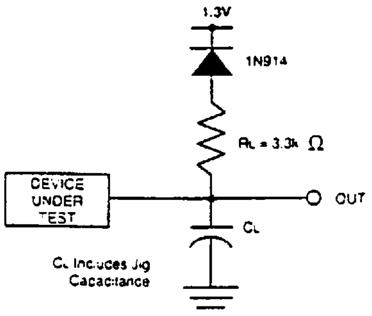

1.3V
1N914
$R_L = 3.3k\ \Omega$
DEVICE UNDER TEST
OUT
C_L
C_L Includes Jig Capacitance

Figure 17. Transient Equivalent Testing Load Circuit

Test Configuration	C_L (pF)
V_{CC} = 2.7V - 3.6V	50
V_{CC} = 5V ± 5%	30
V_{CC} = 5V ± 10%	100

6.2.3 DC Characteristics

DC Characteristics

Symbol	Parameter	Notes	V_{CC} = 2.7V - 3.6V		V_{CC} = 5V ± 10%		Unit	Test Conditions
			Typ	Max	Typ	Max		
I_{LI}	Input Load Current	1		± 0.5		± 1	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1		± 0.5		± 10	µA	V_{CC} = V_{CC} Max, V_{OUT} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,3,6		100		100	µA	CMOS Inputs V_{CC} = V_{CC} Max CE# = RP# = V_{CC} ± 0.2V
				2		2	mA	TTL Inputs V_{CC} = V_{CC} Max CE# = RP# = V_{IH}
I_{CCD}	V_{CC} Deep Power-Down Current	1		12		16	µA	RP# = GND ± 0.2V I_{OUT} (RY/BY#) = 0 mA
I_{CCR}	V_{CC} Read Current	1,5,6		25		50	mA	CMOS Inputs V_{CC} = V_{CC} Max, CE# = GND f = 5 MHz (3.3V, 2.7V), 8 MHz (5V) I_{OUT} = 0 mA
				30		65	mA	TTL Inputs V_{CC} = V_{CC} Max, CE# = GND f = 5 MHz (3.3V, 2.7V), 8 MHz (5V) I_{OUT} = 0 mA
I_{CCW}	V_{CC} Byte Write or Set Lock-Bit Current	1,7		17	-	-	mA	V_{PP} = 2.7V - 3.6V
				17		35	mA	V_{PP} = 5V ± 10%
				12		30	mA	V_{PP} = 12V ± 5%
I_{CCE}	V_{CC} Block Erase or Clear Block Lock-Bits Current	1,7		17	-	-	mA	V_{PP} = 2.7V - 3.6V
				17		30	mA	V_{PP} = 5V ± 10%
				12		25	mA	V_{PP} = 12V ± 5%
I_{CCWS} I_{CCES}	V_{CC} Byte Write or Block Erase Suspend Current	1,2		6		10	mA	CE# = V_{IH}
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current	1		± 15		± 15	µA	$V_{PP} \leq V_{CC}$
				200		200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		5		5	µA	RP# = GND ± 0.2V
I_{PPW}	V_{PP} Byte Write or Set Lock-Bit Current	1,7		80	-	-	mA	V_{PP} = 2.7V - 3.6V
				80		80	mA	V_{PP} = 5V ± 10%
				30		30	mA	V_{PP} = 12V ± 5%
I_{PPE}	V_{PP} Block Erase or Set Lock-Bit Current	1,7		40	-	-	mA	V_{PP} = 2.7V - 3.6V
				40		40	mA	V_{PP} = 5V ± 10%
				30		30	mA	V_{PP} = 12V ± 5%
I_{PPWS} I_{PPES}	V_{PP} Byte Write or Block Erase Suspend Current	1		200		200	µA	V_{PP} = $V_{PPH1/2/3}$

DC Characteristics (Continued)

Symbol	Parameter	Notes	V_{CC} = 2.7V - 3.6V		V_{CC} = 5V ± 10%		Unit	Test Conditions
			Min	Max	Min	Max		
V_{IL}	Input Low Voltage	7	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	7	2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage	3,7		0.4		0.45	V	$V_{CC} = V_{CC}$ Min, I_{OL} = 5.8mA(V_{CC}=5V) I_{OL} = 2.0mA(V_{CC}=3.3V)
V_{OH1}	Output High Voltage (TTL)	3,7	2.4		2.4		V	$V_{CC} = V_{CC}$ Min, I_{OH} = -2.5mA(V_{CC}=5V) I_{OH} = -2.0mA(V_{CC}=3.3V)
V_{OH2}	Output High Voltage (CMOS)	3,7	0.85 V_{CC}		0.85 V_{CC}		V	$V_{CC} = V_{CC}$ Min, I_{OH} = - 2.5 µA
			V_{CC} - 0.4		V_{CC} - 0.4		V	$V_{CC} = V_{CC}$ Min, I_{OH} = - 100 µA
V_{PPLK}	V_{PP} Lockout during Normal Operations	4,7		1.5		1.5	V	
V_{PPH1}	V_{PP} during Byte Write, Block Erase, or Lock-Bit Operations		2.7	3.6	-	-	V	
V_{PPH2}	V_{PP} during Byte Write, Block Erase, or Lock-Bit Operations		4.5	5.5	4.5	5.5	V	
V_{PPH3}	V_{PP} during Byte Write, Block Erase, or Lock-Bit Operations		11.4	12.6	11.4	12.6	V	
V_{LKO}	V_{CC} Lockout Voltage		2.0		2.0		V	
V_{HH}	RP# Unlock Voltage	8	11.4	12.6	11.4	12.6	V	Set Permanent Lock-Bit Override Block Lock-Bit

NOTES:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (package and speeds). Contact your local sales office for information about typical specifications.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes RY/BY#.
4. Block erases, word writes, and lock-bit configurations are inhibited when $V_{PP} \le V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (max) and V_{PPH1} (min), between V_{PPH1} (max) and V_{PPH2} (min), between V_{PPH2} (max) and V_{PPH3} (min), and above V_{PPH3} (max).
5. Automatic Power Saving (APS) reduces typical I_{CCR} to 1 mA at 5V V_{CC} and 3 mA at 3.3V V_{CC} in static operation.
6. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.
8. Permanent lock-bit set operations are inhibited when RP# = V_{IH}. Block lock-bit configuration operations are inhibited when the permanent lock-bit is set or RP# = V_{IH} or WP# = V_{IL}. Block erases and word writes are inhibited when the corresponding block-lock bit is set and RP# = V_{IH} or WP# = V_{IL} or the permanent lock-bit is set. Block erase, word write, and lock-bit configuration operations are not guaranteed with V_{CC} < 2.7V or V_{IH} < RP# < V_{HH} and should not be attempted.

6.2.4 AC Characteristics - Read Only Operations (1)

V_{CC} = 2.7V - 3.6V, T_A = -40°C to + 85°C

Versions (4)			LH28F800SG-L70		LH28F800SG-L100		
Symbol	Parameter	Notes	Min	Max	Min	Max	Unit
t_{AVAV}	Read Cycle Time		100		120		ns
t_{AVQV}	Address to Output Delay			100		120	ns
t_{ELQV}	CE# to Output Delay	2		100		120	ns
t_{PHQV}	RP# High to Output Delay			600		600	ns
t_{GLQV}	OE# to Output Delay	2		45		50	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# High to Output in High Z	3		45		55	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# High to Output in High Z	3		20		25	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns

V_{CC} = 3.3V ± 0.3V, T_A = -40°C to + 85°C

Versions (4)			LH28F800SG-L70		LH28F800SG-L100		
Symbol	Parameter	Notes	Min	Max	Min	Max	Unit
t_{AVAV}	Read Cycle Time		85		100		ns
t_{AVQV}	Address to Output Delay			85		100	ns
t_{ELQV}	CE# to Output Delay	2		85		100	ns
t_{PHQV}	RP# High to Output Delay			600		600	ns
t_{GLQV}	OE# to Output Delay	2		40		45	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# High to Output in High Z	3		40		45	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# High to Output in High Z	3		15		20	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns

6.2.4 AC Characteristics - Read Only Operations (Cont.) (1)

V_{CC} = 5.0V ± 10%, 5.0V ± 5%, T_A = -40°C to + 85°C

Versions[4]		Vcc ± 5%	LH28F800SG-L70[5]						
		Vcc ± 10%			LH28F800SG-L70[6]		LH28F800SG-L100[6]		
Symbol	Parameter	Notes	Min	Max	Min	Max	Min	Max	Unit
t_{AVAV}	Read Cycle Time		70		80		100		ns
t_{AVQV}	Address to Output Delay			70		80		100	ns
t_{ELQV}	CE# to Output Delay	2		70		80		100	ns
t_{PHQV}	RP# High to Output Delay			400		400		400	ns
t_{GLQV}	OE# to Output Delay	2		40		45		50	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		0		ns
t_{EHQZ}	CE# High to Output in High Z	3		55		55		55	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		0		ns
t_{GHQZ}	OE# High to Output in High Z	3		10		10		15	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		0		ns

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. See Ordering Information for device speeds (valid operational combinations).
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Speed Configuration) for testing characteristics.
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.

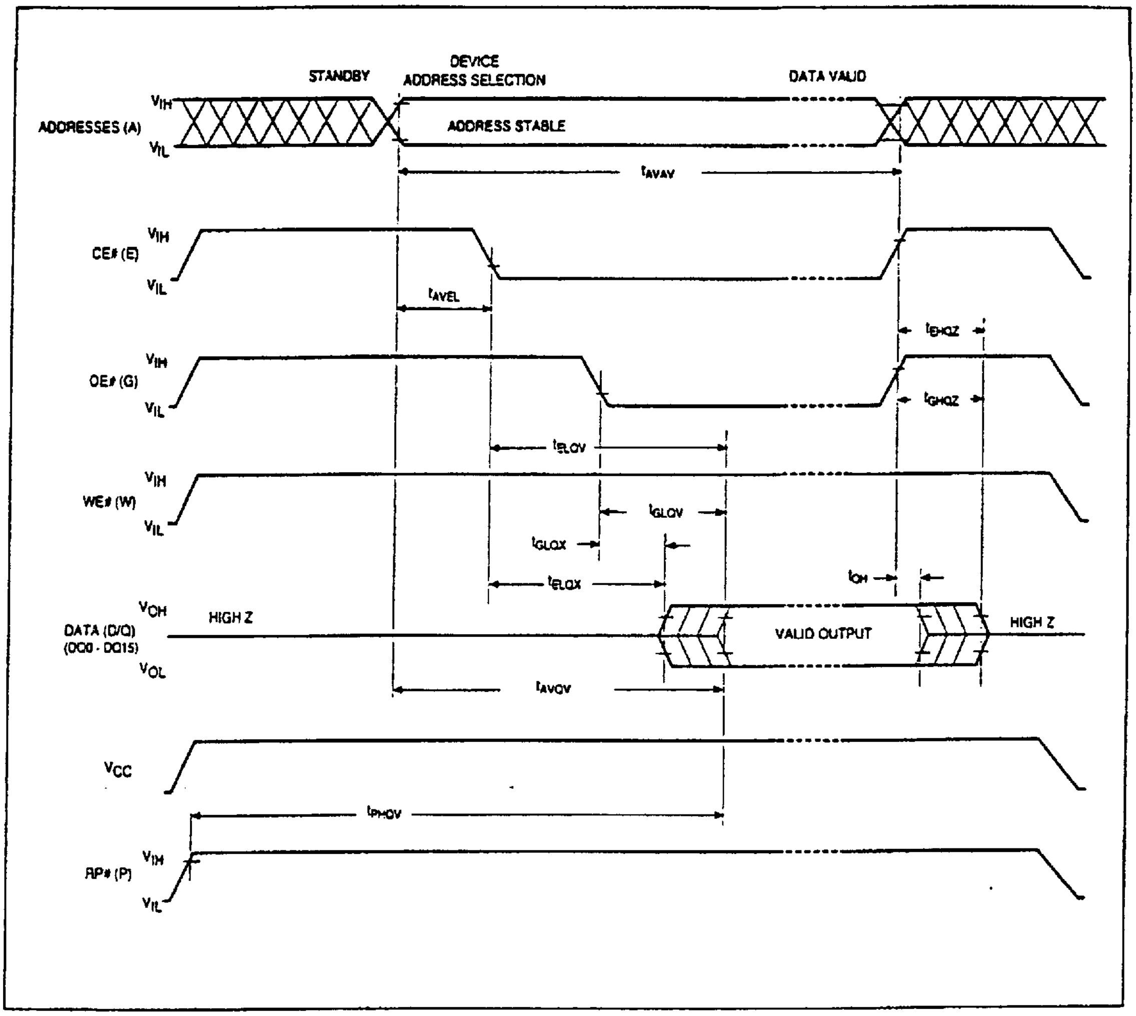

STANDBY
DEVICE ADDRESS SELECTION
DATA VALID
ADDRESSES (A)
VIH
VIL
ADDRESS STABLE
tAVAV
CE# (E)
VIH
VIL
tAVEL
tEHQZ
OE# (G)
VIH
VIL
tGHQZ
tELQV
WE# (W)
VIH
VIL
tGLQV
tGLQX
tELQX
tOH
DATA (D/Q)
(DQ0 - DQ15)
VOH
VOL
HIGH Z
VALID OUTPUT
HIGH Z
tAVQV
VCC
tPHQV
RP# (P)
VIH
VIL

Figure 18. AC Waveform for Read Operations

6.2.5 AC Characteristics for WE#- Controled Write Operations (1)

V_{CC} = 2.7V - 3.6V, T_A = -40°C to + 85°C

Versions (5)			LH28F800SG-L70		LH28F800SG-L100		
Symbol	Parameter	Notes	Min	Max	Min	Max	Unit
t_{AVAV}	Write Cycle Time		100		120		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		10		ns
t_{WLWH}	WE# Pulse Width		50		50		ns
t_{PHHWH}	RP# V_{HH} Setup to WE# Going High	2	100		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		50		ns
t_{WHDX}	Data Hold from WE# High		5		5		ns
t_{WHAX}	Address Hold from WE# High		5		5		ns
t_{WHEH}	CE# Hold from WE# High		10		10		ns
t_{WHWL}	WE# Pulse Width High		30		30		ns
t_{WHRL}	WE# High to RY/BY# Going Low			100		100	ns
t_{WHGL}	Write Recovery before Read		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns

V_{CC} = 3.3V ± 0.3V, T_A = -40°C to + 85°C

Versions (5)			LH28F800SG-L70		LH28F800SG-L100		
Symbol	Parameter	Notes	Min	Max	Min	Max	Unit
t_{AVAV}	Write Cycle Time		85		100		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		10		ns
t_{WLWH}	WE# Pulse Width		50		50		ns
t_{PHHWH}	RP# V_{HH} Setup to WE# Going High	2	100		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		50		ns
t_{CVWH}	Data Setup to WE# Going High	3	50		50		ns
t_{WHDX}	Data Hold from WE# High		5		5		ns
t_{WHAX}	Address Hold from WE# High		5		5		ns
t_{WHEH}	CE# Hold from WE# High		10		10		ns
t_{WHWL}	WE# Pulse Width High		30		30		ns
t_{WHRL}	WE# High to RY/BY# Going Low			100		100	ns
t_{WHGL}	Write Recovery before Read		0		0		ns
t_{CVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2.4	0		0		ns
t_{CVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2.4	0		0		ns

6.2.5 AC Characteristics for WE# - Controled Write Operations (Cont.)[1]

V_{CC} = 5V ± 10%, 5V ± 5%, T_A = -40°C to + 85°C

Versions[5]		Vcc ± 5%	LH28F800SG-L70[6]						
		Vcc ± 10%			LH28F800SG-L70[7]		LH28F800SG-L100[7]		
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		70		80		100		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		1		1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		10		10		ns
t_{WLWH}	WE# Pulse Width		40		40		40		ns
t_{PHHWH}	RP# V_{HH} Setup to WE# Going High	2	100		100		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		100		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	40		40		40		ns
t_{DVWH}	Data Setup to WE# Going High	3	40		40		40		ns
t_{WHDX}	Data Hold from WE# High		5		5		5		ns
t_{WHAX}	Address Hold from WE# High		5		5		5		ns
t_{WHEH}	CE# Hold from WE# High		10		10		10		ns
t_{WHWL}	WE# Pulse Width High		30		30		30		ns
t_{WHRL}	WE# High to RY/BY# Going Low			90		90		90	ns
t_{WHGL}	Write Recovery before Read		0		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		0		0		ns

NOTES:

1. Read timing characteristics during block erase, word write and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, word write, or lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2/3}$ (and if necessary RP# should be held at V_{HH}) until determination of block erase, word write, or lock-bit configuration success (SR.1/3/4/5 = 0).
5. See Ordering Information for device speeds (valid operational combinations).
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Speed Configuration) for testing characteristics.
7. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.

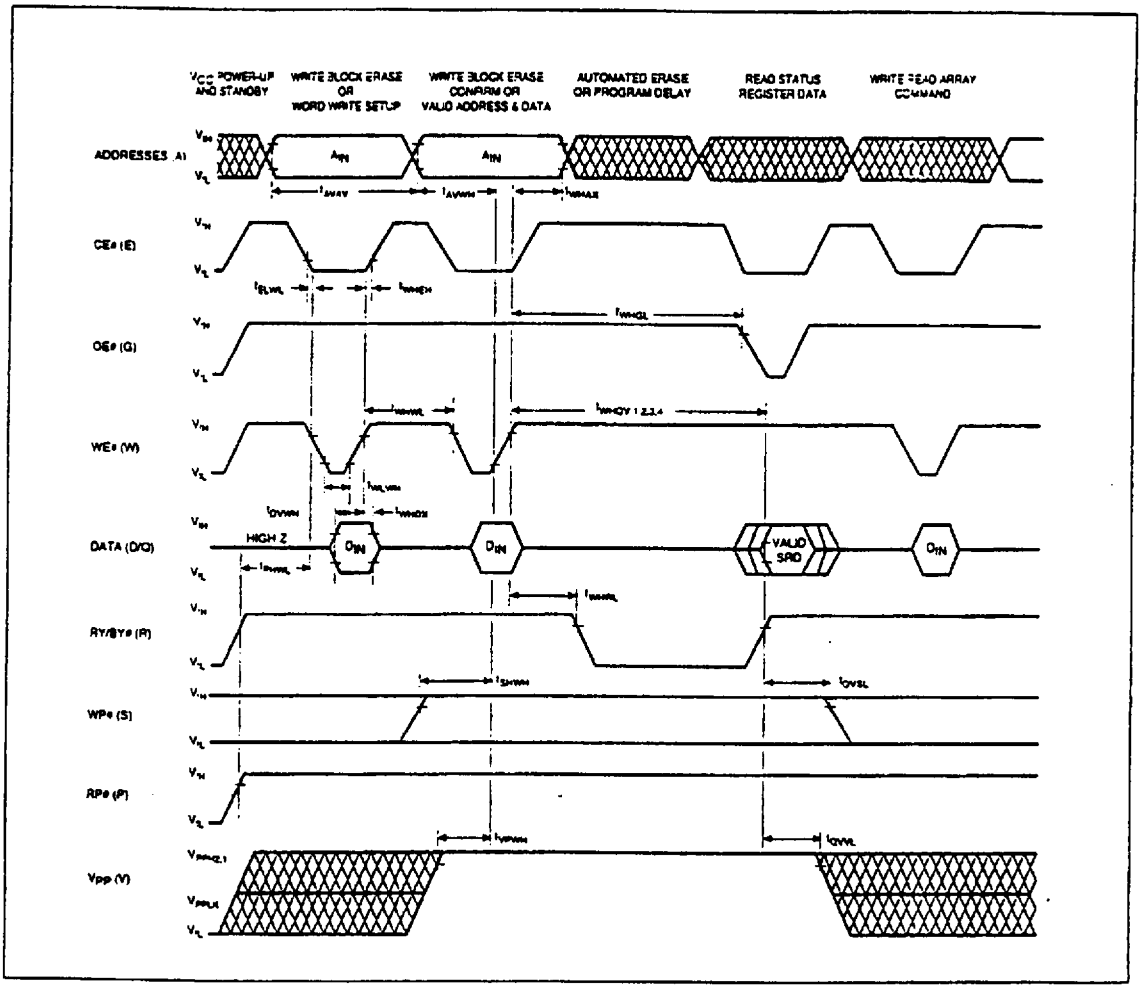

VCC POWER-UP AND STANDBY
WRITE BLOCK ERASE OR WORD WRITE SETUP
WRITE BLOCK ERASE CONFIRM OR VALID ADDRESS & DATA
AUTOMATED ERASE OR PROGRAM DELAY
READ STATUS REGISTER DATA
WRITE READ ARRAY COMMAND
ADDRESSES (A)
CE# (E)
OE# (G)
WE# (W)
DATA (D/Q)
RY/BY# (R)
WP# (S)
RP# (P)
VPP (V)
VIH
VIL
VPPH2,1
VPPLK
AIN
DIN
HIGH Z
VALID SRD
tAVAV
tAVWH
tWHAX
tELWL
tWHEH
tWHGL
tWHWL
tWHQV1,2,3,4
tWLWH
tDVWH
tWHDX
tPHWL
tWHRL
tSHWH
tQVSL
tVPWH
tQVVL

Figure 19. AC Waveform for WE#-Controlled Write Operations

6.2.6 AC Characteristics for CE#-Controlled Writes Operations (1)

V_{CC} = 2.7V - 3.6V, T_A = -40°C to + 85°C

Versions (5)			LH28F800SG-L70		LH28F800SG-L100		
Symbol	Parameter	Notes	Min	Max	Min	Max	Unit
t_{AVAV}	Write Cycle Time		100		120		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		0		ns
t_{ELEH}	CE# Pulse Width		70		70		ns
t_{PHHEH}	RP# V_{HH} Setup to CE# Going High	2	100		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		50		ns
t_{EHDX}	Data Hold from CE# High		5		5		ns
t_{EHAX}	Address Hold from CE# High		5		5		ns
t_{EHWH}	WE# Hold from CE# High		0		0		ns
t_{EHEL}	CE# Pulse Width High		25		25		ns
t_{EHRL}	CE# High to RY/BY# Going Low			100		100	ns
t_{EHGL}	Write Recovery before Read		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns

V_{CC} = 3.3V ± 0.3V, T_A = -40°C to + 85°C

Versions (5)			LH28F800SG-L70		LH28F800SG-L100		
Symbol	Parameter	Notes	Min	Max	Min	Max	Unit
t_{AVAV}	Write Cycle Time		85		100		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		0		ns
t_{ELEH}	CE# Pulse Width		70		70		ns
t_{PHHEH}	RP# V_{HH} Setup to CE# Going High	2	100		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		50		ns
t_{EHDX}	Data Hold from CE# High		5		5		ns
t_{EHAX}	Address Hold from CE# High		5		5		ns
t_{EHWH}	WE# Hold from CE# High		0		0		ns
t_{EHEL}	CE# Pulse Width High		25		25		ns
t_{EHRL}	CE# High to RY/BY# Going Low			100		100	ns
t_{EHGL}	Write Recovery before Read		0		0-		ns
t_{QVVL}	V_{PP} Hold from Valid SRD. RY/BY# High	2,4	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns

6.2.6 AC Characteristics for CE#-Controlled Writes Operations (Cont.) [1]

V_{CC} = 5V ± 10%, 5V ± 5%, T_A = -40°C to + 85°C

Versions [5]		V_{CC} ± 5%	LH28F800SG-L70 [6]						
		V_{CC} ± 10%			LH28F800SG-L70 [7]		LH28F800SG-L100 [7]		
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		70		80		100		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		1		1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		0		0		ns
t_{ELEH}	CE# Pulse Width		50		50		50		ns
t_{PHHEH}	RP# V_{HH} Setup to CE# Going High	2	100		100		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		100		100		ns
t_{AVEH}	Address Setup to CE# Going High	3	40		40		40		ns
t_{DVEH}	Data Setup to CE# Going High	3	40		40		40		ns
t_{EHDX}	Data Hold from CE# High		5		5		5		ns
t_{EHAX}	Address Hold from CE# High		5		5		5		ns
t_{EHWH}	WE# Hold from CE# High		0		0		0		ns
t_{EHEL}	CE# Pulse Width High		25		25		25		ns
t_{EHRL}	CE# High to RY/BY# Going Low			90		90		90	ns
t_{EHGL}	Write Recovery before Read		0		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		0		0		ns

NOTES:

1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold, and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, word write, or lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2/3}$ (and if necessary RP# should be held at V_{HH}) until determination of block erase, word write, or lock-bit configuration success (SR.1/3/4/5 = 0).
5. See Ordering Information for device speeds (valid operational combinations).
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Speed Configuration) for testing characteristics.
7. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.

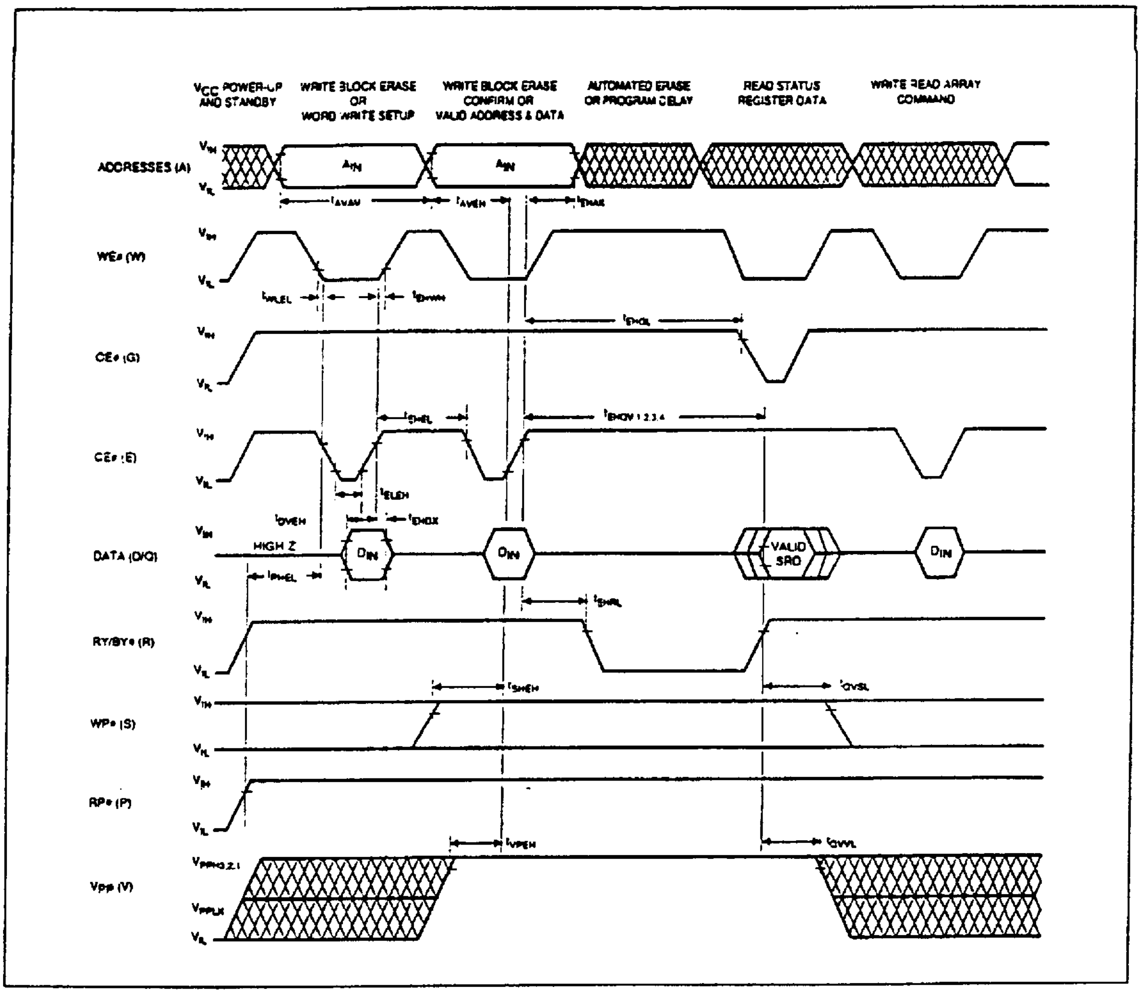
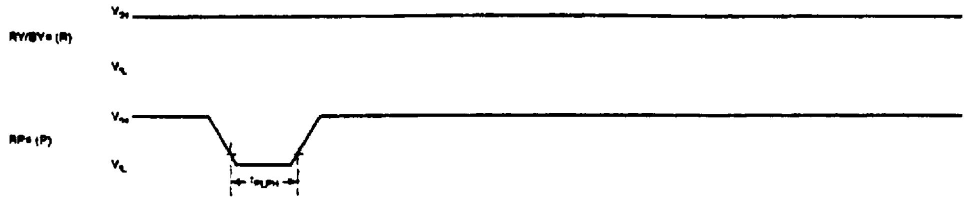
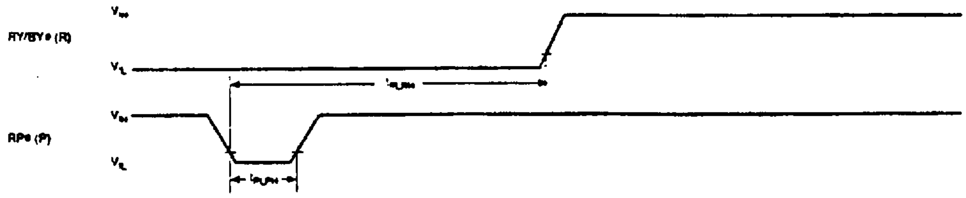

VCC POWER-UP AND STANDBY
WRITE BLOCK ERASE OR WORD WRITE SETUP
WRITE BLOCK ERASE CONFIRM OR VALID ADDRESS & DATA
AUTOMATED ERASE OR PROGRAM DELAY
READ STATUS REGISTER DATA
WRITE READ ARRAY COMMAND
ADDRESSES (A)
WE# (W)
OE# (G)
CE# (E)
DATA (D/Q)
RY/BY# (R)
WP# (S)
RP# (P)
VPP (V)
VIH
VIL
VPPH2,1
VPPLK
AIN
tAVAV
tAVEH
tEHAX
tWLEL
tEHWH
tEHGL
tEHEL
tEHQV1,2,3,4
tELEH
tDVEH
tEHDX
HIGH Z
DIN
tPHEL
VALID SRD
tEHRL
tSHEH
tQVSL
tVPEH
tQVVL

Figure 20. AC Waveform for CE#-Controlled Write Operations

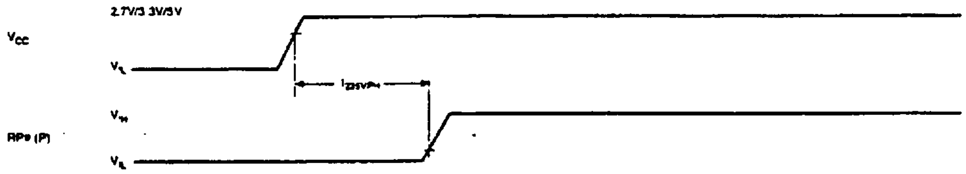
6.2.7 Reset Operations



(A) Reset During Read Array Mode



(B) Reset During Block Erase, Word Write, or Lock-Bit Configuration



(C) RP# Rising Timing

Figure 21. AC Waveform for Reset Operation

Reset AC Specifications (1)

Symbol	Parameter	Notes	V_{CC} = 2.7V - 3.6V		V_{CC} = 5V ± 10%		Unit
			Min	Max	Min	Max	
t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)		100		100		ns
t_{PLRH}	RP# Low to Reset during Block Erase, Word Write, or Lock-Bit Configuration	2,3		20		12	μs
t_{235VPH}	V_{CC} 2.7V to RP# High V_{CC} 3.0V to RP# High V_{CC} 4.5V to RP# High	4	100		100		ns

NOTES:

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, word write, or lock-bit configuration operation is not executing, the reset will complete within 100 ns.
3. A reset time, t_{PHQV}, is required from the latter of RY/BY# or RP# going high until outputs are valid.
4. When the device power-up, holding RP# low minimum 100 ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.8 Block Erase, Word Write and Lock-Bit Configuration Performance [3,4]

V_{CC} = 3.3V ± 0.3V, T_A = -40°C to +85°C

Symbol	Parameter	Notes	Vpp = 3.0 - 3.6V			Vpp = 5.0V ± 10%			Vpp = 12.0V ± 5%			Unit
			Min	Typ[1]	Max	Min	Typ[1]	Max	Min	Typ[1]	Max	
t_{WHQV1} t_{EHQV1}	Word Write Time	2	35	45		14	20			11		µs
	Block Write Time	2	1.2	1.5		0.5	0.7			0.4		sec
t_{WHQV2} t_{EHQV2}	Block Erase Time	2		2.1			1.4			1.3		sec
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time	2		31			20			17.4		µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	2		2.7			1.8			1.6		sec
t_{WHRH1} t_{EHRH1}	Word Write Suspend Latency Time to Read			9			7.5			7.5		µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read			24.3			14.4			14.4		µs

V_{CC} = 5V ± 10%, 5V ± 5%, T_A = -40°C to +85°C

Symbol	Parameter	Notes	Vpp = 5V ± 10%			Vpp = 12V ± 5%			Unit
			Min	Typ[1]	Max	Min	Typ[1]	Max	
t_{WHQV1} t_{EHQV1}	Word Write Time	2	10	14			7.5		µs
	Block Write Time	2	0.4	0.5			0.25		sec
t_{WHQV2} t_{EHQV2}	Block Erase Time	2		1.3			1.2		sec
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time	2		18			15		µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	2		1.6			1.5		sec
t_{WHRH1} t_{EHRH1}	Word Write Suspend Latency Time to Read			7.5			6		µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read			14.4			14.4		µs

NOTES:

1. Typical values measured at T_A = +25°C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.

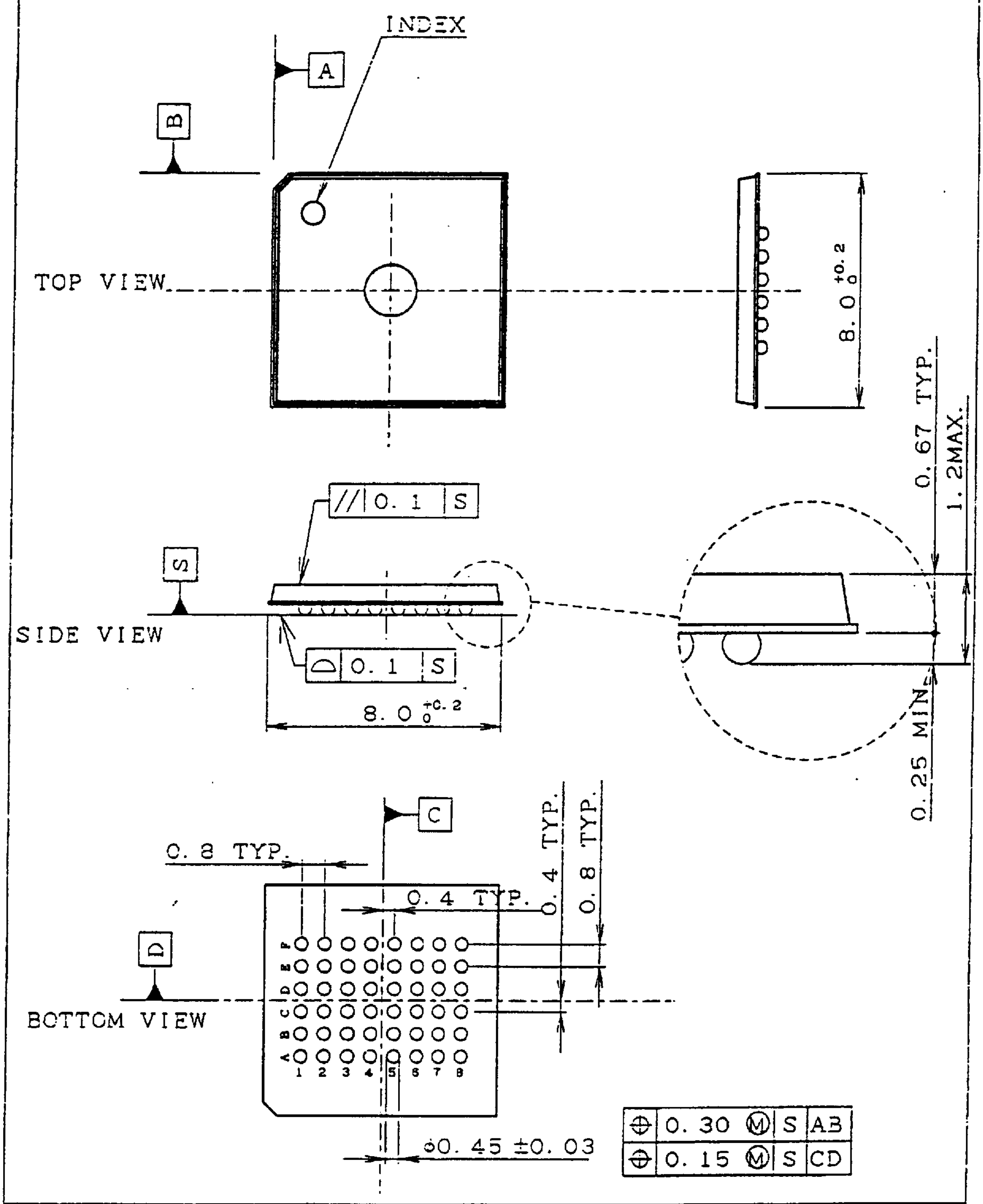
V_{CC} = 2.7V -3.0V, T_A = - 40°C to + 85°C

Symbol	Parameter	Notes	V_{PP} = 2.7 ~3.0V			V_{PP} = 5.0V ± 10%			V_{PP} = 12.0V ± 5%			Unit
			Min	Typ[(1)]	Max	Min	Typ[(1)]	Max	Min	Typ[(1)]	Max	
t_{WHQV1} t_{EHQV1}	Word Write Time	2	49	63		20	28			15.4		µs
	Block Write Time	2	1.7	2.1		0.7	1.0			0.56		sec
t_{WHQV2} t_{EHQV2}	Block Erase Time	2		3.0			2.0			1.9		sec
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time	2		44			28			24.4		µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	2		3.8			2.6			2.3		sec
t_{WHRH1} t_{EHRH1}	Word Write Suspend Latency Time to Read			12.6			10.5			10.5		µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read			34.1			20.2			20.2		µs

NOTES:

1. Typical values measured at T_A = + 25°C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.

SHARP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A
B
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0.67 TYP.
1.2MAX.
//0.1 S
S
SIDE VIEW
⌓ 0.1 S
8.0 +0.2 0
0.25 MIN.
C
0.8 TYP.
0.4 TYP.
0.4 TYP.
0.8 TYP.
D
BOTTOM VIEW
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φ0.45 ±0.03
⊕ 0.30 Ⓜ S AB
⊕ 0.15 Ⓜ S CD

改訂日 DATE	改訂記事 REVISE	担当 CHARGE

日付 DATE	1997. 1. 14			
設計 DESIGN	製図 DRAW	写図 TRACE	検図 CHECK	承認 APPROVS
Y. Sota	Y. Kimura			

尺度 SCALE	5/1
単位 UNIT	1=1/1mm
適用機種 APPLICABLE MODEL	8M FLASH (SV)(X16)
端子マトリクス MATRIX	8 × 6
端子数 COUNTS	48
端子ピッチ PITCH	0.8
名称 NAME	CSP048-P-0808 (FBGA048-P-0808)
コード CODE	CSP-GR-048-1-0808
図番 DRAWING No.	AA2009

シャープ株式会社 SHARP CORPORATION
IC 天理事業本部 TENRI IC GROUP
超LSI開発研究所 VLSI DEVELOPMENT LABORATORIES
生産技術開発部 PRODUCTION ENGINEERING DEPT.

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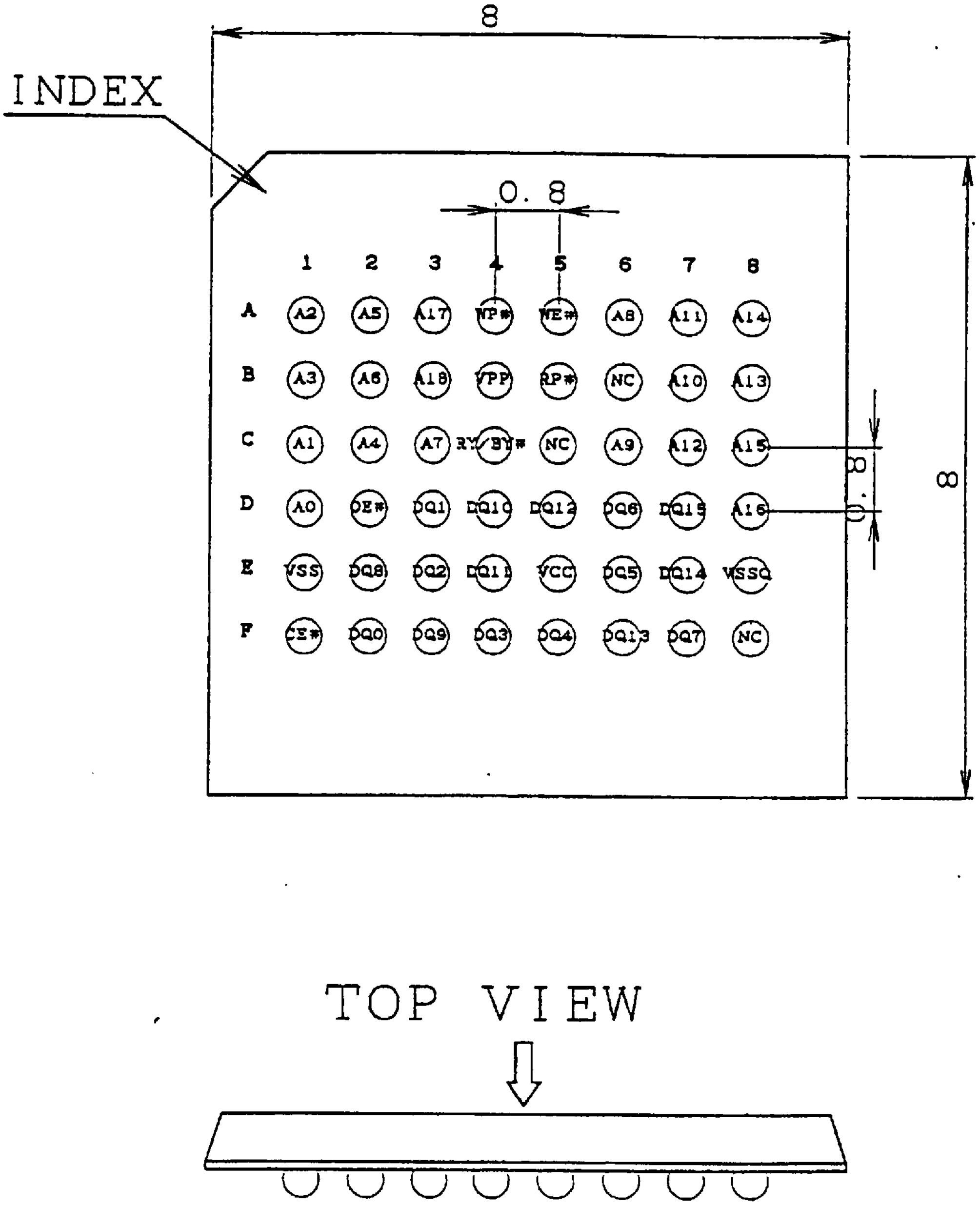
SHARP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A14
B
A3
A6
A18
VPP
RP#
NC
A10
A13
C
A1
A4
A7
RY/BY#
NC
A9
A12
A15
D
A0
OE#
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DQ6
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DQ2
DQ11
VCC
DQ5
DQ14
VSSQ
F
CE#
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DQ9
DQ3
DQ4
DQ13
DQ7
NC
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8
TOP VIEW

適応機種名	8M FLASH MEMORY (X 16)	尺度 SCALE	単位 UNIT			
		12/1	1=1/1mm			
日付 DATE	1996. 12. 26			改訂日 DATE	改訂記事 REVISE	担当 CHARGE

設計 DESIGN	製図 DRAW	写図 TRACE	検図 CHECK	承認 APPROVE	シャープ株式会社 IC天理事業本部 超LSI開発研究所生産技術開発部 SHARP CORPORATION	名称 NAME	CSP48-P-0808 (0. 8PITCH)(端子位置)

CSP-T-48-1-8mqc