LSI LOGIC

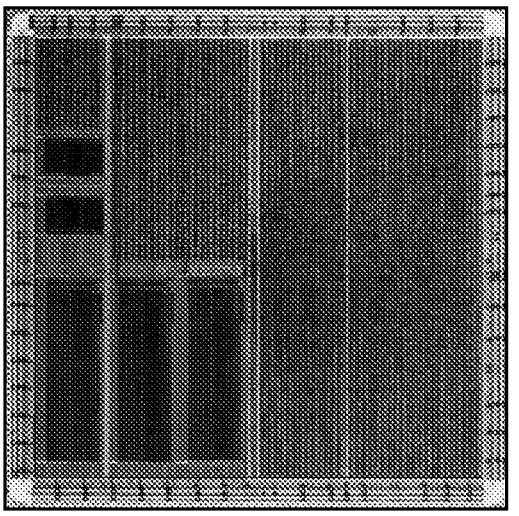
L64710
8-Error Correcting Reed-Solomon Codec

Description

The L64710 contains an RS (Reed-Solomon) encoder and a RS decoder. This pipelined, high-speed, error-correction device implements an RS code as specified in CMTT (Committee for Mixed Telephone and Television, joint CCITT/CCIR (Consultative Committee on International Telephones and Telegraphs/ Consultative Committee on International Radio)) recommendation CCIR723. The encoder appends 16 redundant check bytes to every K message bytes. The message length K is user-programmable between 38 and 239. Each RS codeword consists of N = K + 16 bytes of data. Thus the codeword length N may range between 54 and 255 bytes.

The decoder is capable of correcting up to 8-byte errors per codeword. Sustained throughput data rates up to 40 Mbytes per second (commercial) are supported for both the encoder and decoder

The L64710 is ideally suited for ensuring data integrity in high-performance storage media,



L64710 Chip

communication channels and digital television transmission (CCIR723). The device is implemented in a 1.0 micron drawn gate length (0.7 micron effective channel length) HCMOS technology.

Introduction

The L64710 codec has two new operating modes: the Error Pattern mode and the Error Count mode. These two modes allow the L64710 to give the exact position, type and number of errors.

Error Pattern Mode

When the Error Pattern mode is enabled, the DDO bus outputs error patterns rather than corrected data. These patterns give the exact position of errors in a codeword. Each bit of the pattern corresponds to one bit of the codeword. If a bit in the error pattern is set, the corresponding bit of the codeword is in error. The Error Pattern mode is ideal for channel characterization in a development environment.

The Error Pattern mode is enabled when the EPTRN register is equal to one. See the subsection entitled "Loading the Control Inputs" on how to set this register.

Error Count Mode

When the Error Count mode is enabled, the DDO bus outputs an error count during the check period. (The check period is the time during which the L64710 outputs redundant bytes on the DDO bus.) The L64710 outputs the number of bit errors during the last cycle of the check period. The L64710 outputs the number of byte errors during the next to the last clock cycle of the check period. The eight-bit DDO bus carries each error count as a binary number. The L64710 reports byte error counts between zero and eight, and it reports bit error counts between zero and 64. When error counts exceed these maximum values, the L64710 drives the DFAIL output HIGH. The Error Count mode allows the user to monitor the number of errors without the loss of corrected message data.

Loading the Control Inputs

Two control words control the operation of the L64710. The codec latches the data on the eight-bit CI (Control Input) bus into the register specified by the state of REGSEL when WE is LOW. Table 2a is a memory map that shows which registers. Table 2a replaces Table 2 on page 8 of the databook. All registers shown in Table 2a, except EPTRN and ECNT, are described on page 8 of the databook.

When EPTRN is equal to one, the Error Pattern mode is enabled. When ECTN is equal to one, the Error Count mode is enabled. The preceding two subsections describe these modes.

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Introduction (Contiuned)

No more than one of the following registers- may be set to one at the same time: CORRDIS, EPTRN or ECNT. If the DFAIL signal is HIGH, more than eight byte errors exist in a code-word. The data and any error information on that particular codeword are unreliable.

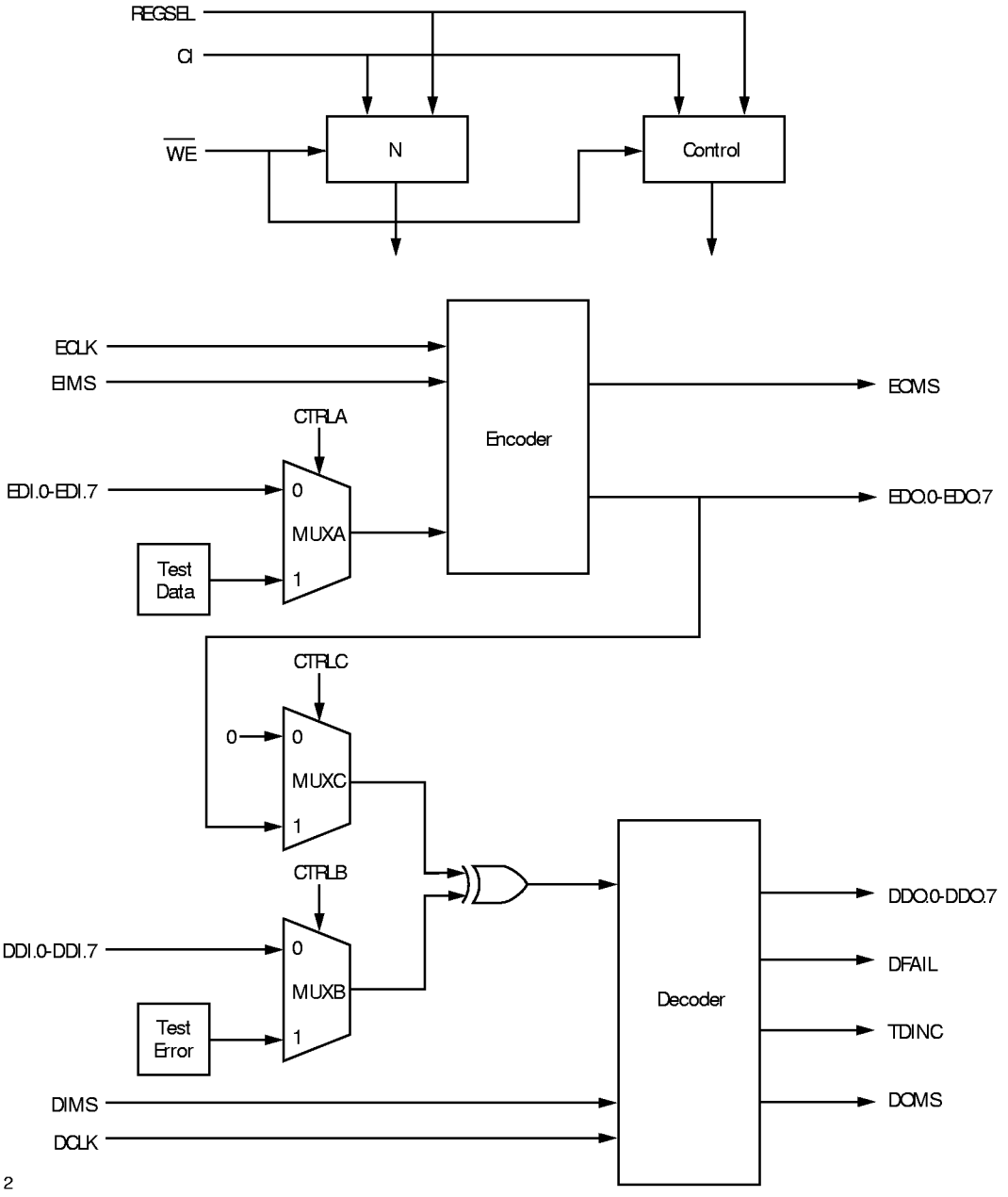
Features

- Eight bits (1 byte) per code symbol
- Sixteen bytes of redundancy per codeword
- Percentage redundancy as low as 6.7%
- Corrects up to 8 byte errors per codeword
- Corrects single burst up to 57 bits long
- Systematic Reed-Solomon code for easy retrieval of message data
- User-selectable codeword length of between 54 and 255 bytes
- Separate encoder and decoder for full duplex operation
- Complies with CCIR723
- Pipelined architecture with high data rate

Commercial	Military
40 MHz	40 MHz
30 MHz	30 MHz

- Fully static design with no minimum speed requirement
- Built-in test modes
- Available in a 68-pin CPGA (Ceramic Pin Grid Array) package

Block Diagram



Pin Listing and Description

The descriptions given in the following table assumes normal mode operation. For details of the test modes of operations, see the section entitled Test Mode Operations.

CI.0-CI.7
Control input bus. The bus is used to load the codeword length and other control information.

$\overline{WE}$
Active-LOW write enable for the CI inputs. When $\overline{WE}$ is LOW, new data is written into the register specified by the REGSEL pin.

REGSEL
Control register select. Determines whether the N register or the CONTROL register is loaded with the data on the CI bus when WE goes LOW.

ECLK
Encoder system clock, active at the rising edge. All encoder inputs (EDI and EIMS) are clocked into the encoder with the rising edge of ECLK. All encoder outputs (EDO and EOMS) are clocked out from the encoder with the rising edge of ECLK.

EDI.0-EDI.7
Eight-bit wide encoder data input bus. The data on this bus is clocked into the encoder with the rising edge of ECLK. Each block of K contiguous bytes of messages must be followed by 16 cycles of check time for insertion of redundant check bytes. The data on the input data bus is ignored during check time. The check time is then followed by a variable number of bytes (possibly zero) of optional intercodeword information. The intercodeword information could be sync patterns or frame numbers.

EIMS
Indicates the start of encoder input message. EIMS is clocked into the encoder with the rising edge of ECLK. A HIGH on EIMS indicates that the first of the K bytes of messages in a codeword will appear on the EDI bus in the following clock cycle.

EDO.0-EDO.7
Eight-bit wide encoder data output bus. The data on this bus is clocked out from the encoder with the rising edge of ECLK. The output message data is delayed from the input message data by three clock cycles. The 16 bytes of redundancy generated by the encoder follow the K bytes of message data. Any optional intercodeword information present on the EDI bus is not altered by the encoder. It is delayed by three clock cycles before being output on the EDO bus.

EOMS
Indicates the start of encoder output message. EOMS is clocked out from the encoder with the rising edge of ECLK. A HIGH on EOMS indicates that the first of the K bytes of messages in a codeword will appear on the EDO bus in the following clock cycle. EOMS is delayed from EIMS by three clock cycles.

DCLK
Decoder system clock, active at the rising edge. All decoder inputs (DDI and DIMS) are clocked into the decoder with the rising edge of DCLK. All decoder outputs (DDO, DOMS, DFAIL, TDINC) are clocked out from the decoder with the rising edge of DCLK.

DDI.0-DDI.7
Eight-bit wide decoder data input bus. The data on this bus is clocked into the decoder with the rising edge of DCLK. Each block of N contiguous bytes of codeword data may be followed by any number (possibly zero) of clock cycles of intercodeword information. The intercodeword information has no effect on the operation of the decoder.

DIMS
Indicates the start of decoder input message. DIMS is clocked into the decoder with the rising edge of DCLK. A HIGH on DIMS indicates that the first of the K bytes of messages in a codeword will appear on the DDI bus in the following clock cycle.

DDO.0-DDO.7
Eight-bit wide decoder data output bus. The data on this bus is clocked out from the decoder with the rising edge of DCLK. The output decoded data is delayed from the input codeword data by N + 91 clock cycles. Any optional intercodeword information present on the DDI bus is not altered by the decoder. It is delayed by N + 91 clock cycles before being output on the DDO bus.

Pin Listing and Description (Continued)

DOMS
Indicates the start of decoder output message. DOMS is clocked out from the decoder with the rising edge of DCLK. A HIGH on DOMS indicates that the first of the K bytes of messages in a codeword will appear on the DDO bus in the following clock cycle. DOMS is delayed from DIMS by N + 91 clock cycles.

DFAIL
Decoding failure flag. DFAIL is valid only on the clock cycle during which the last byte of a codeword comes out on the DDO bus. A HIGH indicates that there are more than 8 byte errors in the codeword. When this happens, the RS code fails to correct the errors. The data in that particular codeword should not be trusted.

TDINC
A HIGH indicates incorrect output test data on the DDO bus in test modes B and D. This signal should be ignored during normal mode operation.

RESET
Reset pin used for LSI Logic internal testing. RESET should be held LOW by the user.

TOUT
LSI Logic internal output test pin. TOUT should be left unconnected by the user.

L64710 Pin Description Summary

L64710 Pin Description Summary

Pin	No. of Pins	I/O	Description
DDI.0-DDI.7	8	I	Decoder data input
DDO.0-DDO.7	8	O	Decoder data output
EDI.0-EDI.7	8	I	Encoder data input
EDO.0-EDO.7	8	O	Encoder data output
CI.0-CI.7	8	I	Control input bus
REGSEL	1	I	Register select
$\overline{WE}$	1	I	Write enable
DCLK	1	I	Decoder system clock
ECLK	1	I	Encoder system clock
DIMS	1	I	Decoder input message start
DOMS	1	O	Decoder output message start
EIMS	1	I	Encoder input message start
EOMS	1	O	Encoder output message start
DFAIL	1	O	Decoder failure flag
TDINC	1	O	Test failure flag
RESET	1	I	Internal reset - always low
TOUT	1	O	Internal test output - no connect

Architecture

The L64710's two main sections, the encoder and the decoder, run on two separate clocks. The encoder accepts message data from either the encoder input data bus or the internal test data generator. This selection is controlled by MUXA. The data input to the decoder is the exclusive OR of the following two buses:

1. Decoder input data bus or data from internal test error generator (controlled by MUXB),
2. Zero or encoder output data bus (controlled by MUXC)

The codeword length N and other control signals are stored in the N register and the CONTROL register respectively. The signals stored in the CONTROL register include the select signals CTRLA, CTRLB, and CTRLC for MUXA, MUXB, and MUXC respectively. These signals define the various modes of operation as described in Table 1.

Table 1. Modes of Operations

CTRLA	CTRLB	CTRLC	Description
0	0	0	Normal mode Independent encoder and decoder External data (EDI and DDI) for both encoder and decoder inputs
1	0	0	Invalid combination
0	1	0	Invalid combination
1	1	0	Invalid combination
0	0	1	Test mode A External data for encoder input Encoder output fed internally to decoder DDI bus used to input noise into decoder
1	0	1	Test mode B Internal test data for encoder input Encoder output fed internally to decoder DDI bus used to input noise into decoder
0	1	1	Test mode C External data for encoder input Encoder output fed internally to decoder Internally generated test errors
1	1	1	Test mode D Internal test data for encoder input Encoder output fed internally to decoder Internally generated test errors

Normal Mode Operation

The encoder and decoder operate independently. The encoder clock ECLK and decoder clock DCLK are asynchronous with respect to each other.

The encoder appends 16 redundant check bytes following every K message byte to form a codeword of length N = K + 16 bytes. The data on the EDI bus during the 16 bytes of check time is ignored by the encoder. It is replaced by the redundant check bytes on the EDO bus. Both the message bytes and the optional inter-codeword information are left unchanged. The delay through the encoder is three clock cycles.

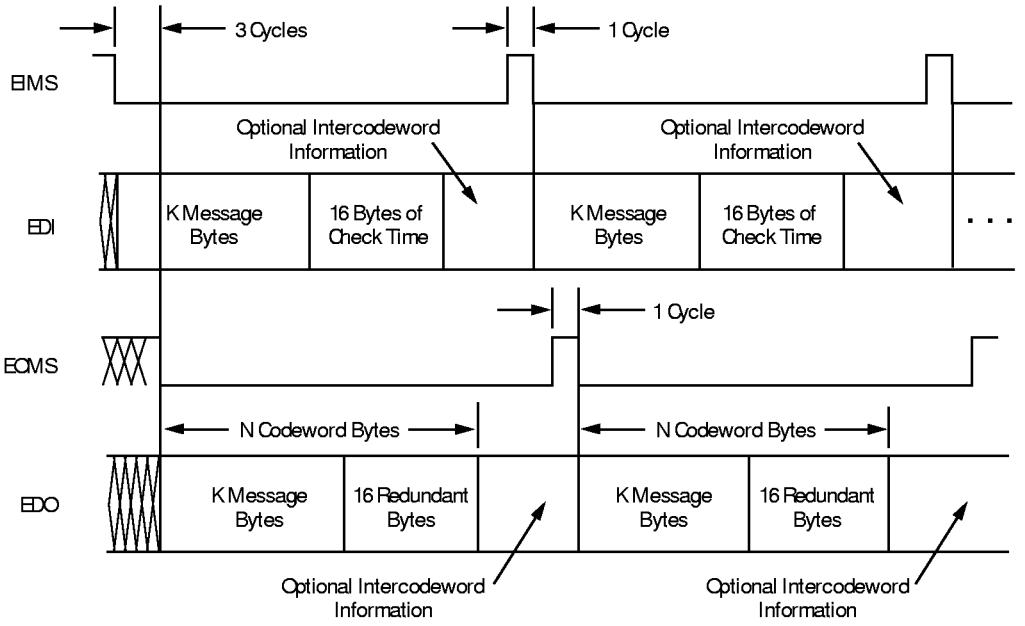
The decoder processes N bytes of codeword data and outputs the decoded data on the DDO bus. When the control signal CORRDIS is LOW, the error-correction mode in the decoder is activated. If there are 8 byte-errors or less among the N-byte codeword, errors are corrected and the output signal DFAIL is LOW. A HIGH on DFAIL indicates that more than 8 byte-errors exist in the codeword.

When the control signal CORRDIS is HIGH, error correction is disabled. When this happens, the decoder passes data through unchanged.

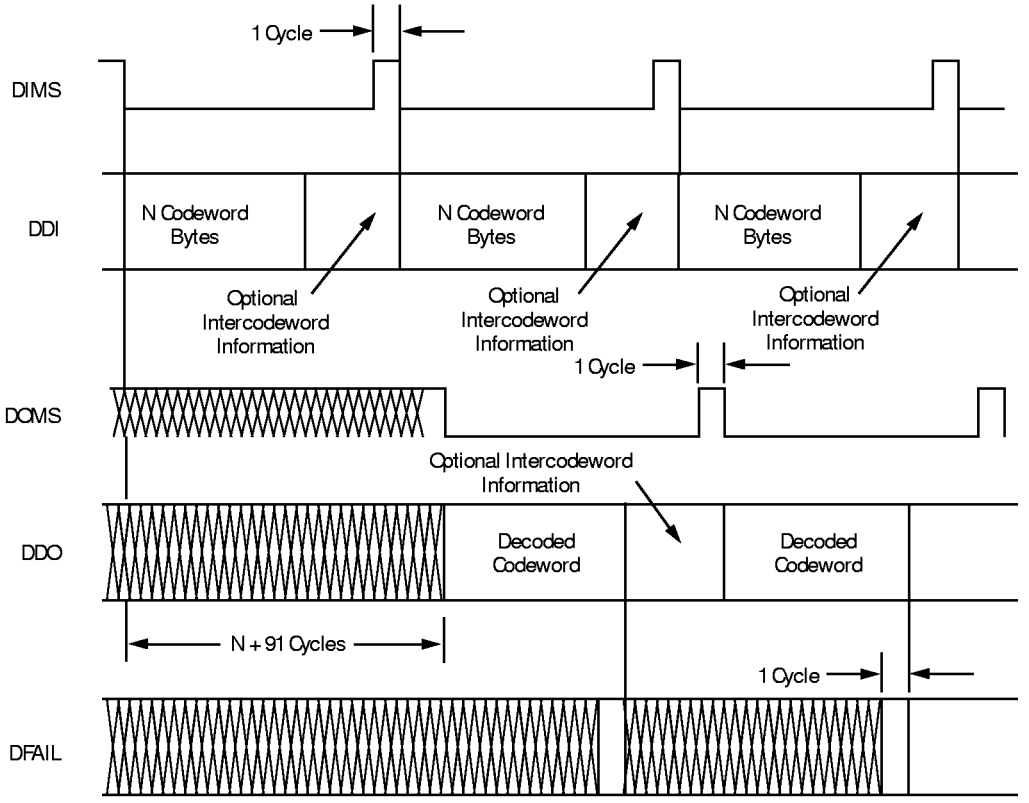
The delay through the decoder is N + 91 clock cycles.

Normal Mode Operation
(Continued)

Encoder Functional Timing Diagram



Decoder Functional Timing Diagram



Test Mode Operations

When the device operates in the test mode, noise is added to the encoded data. The noisy data is then fed into the decoder to test the error-correction capability of the RS code. Due to the interaction between the encoder and decoder, the two clocks ECLK and DCLK must be tied together. The input signal DIMS is ignored during test mode operations.

Test Mode A

The encoder obtains its message data from the EDI bus. The DDI bus is used to add noise to the encoded data. The output signal TDINC should be ignored during this mode of operation.

Test Mode B

The encoder uses internally generated test data as messages. No intercodeword information is inserted. The input signals EDI and EIMS are both ignored. The DDI bus is used to add noise to the encoded data. A HIGH on the TDINC signal indicates incorrect output test data on the DDO bus. The logic level of TDINC depends on how much noise is added to the encoded data through the DDI bus and whether correction is turned off using the CORRDIS signal.

Test Mode C

The encoder obtains its message data from the EDI bus. The noise is internally generated. A test error is inserted into the encoded data stream once every 15 clock cycles. The DDI bus is ignored by the device. The user should ignore the output TDINC signal.

Test Mode D

The encoder uses internally generated data as messages. No intercodeword information is inserted. The input signals EDI and EIMS are both ignored. The noise is internally generated. A test error is inserted into the encoded data stream once every 15 clock cycles. The DDI bus is ignored by the device. A HIGH on the TDINC signal indicates incorrect output test data on the DDO bus. Since the frequency of error is fixed at once every 15 cycles, the logic level of TDINC depends on the codeword length N. For example, with N = 54, the number of errors per codeword is either three or four. All such errors should be corrected and TDINC should remain LOW (assuming CORRDIS is LOW). With N = 135, the number of errors per codeword is always nine. The decoder fails to correct such errors. TDINC should not always remain LOW. This test mode is the most convenient diagnostic check for the device. The procedure consists only of loading the control information and observing the TDINC signal.

Test Data

The internally generated test data is obtained from a periodic pseudo-random sequence of period 2047. The pseudo-random sequence is generated by the recursion $x_n = x_{n-9} + x_{n-11}$ over the binary field. The TDINC signal indicates whether the output test data still satisfies the same recursion.

Test Error

The internally generated test errors occur once every 15 clock cycles. The error pattern is 11111111.

Loading the Control Inputs

The operation of the device is controlled by two internally latched control words. The data on the 8-bit CI bus is latched into the register specified by REGSEL when WE is LOW. The memory map for this device is given in Table 2.

Table 2. Memory Map

REGSEL	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
0	N.7	N.6	N.5	N.4	N.3	N.2	N.1	N.0
1	ECNT	EPTRN	BTST	ATST	CORRDIS	CTRLC	CTRLB	CTRLA

N.0-N.7 controls the length N of the code-words. N is restricted to lie between 54 and 255 bytes. N.0-N.7 contain the bits of N expressed in binary. For example, with N = 255, the signals N.0-N.7 are all HIGH.

CTRLA, CTRLB, and CTRLC are the selects for the multiplexers MUXA, MUXB, and MUXC respectively. They select the various modes of operations.

CORRDIS is the correction disable signal. A HIGH on CORRDIS internally turns off correction in the decoder. When this happens, the decoder serves as a delay line of N + 91 clock cycles.

ATST and BTST are controls for internal LSI Logic tests. They should always be set LOW by the user.

Initialization

To properly initialize the decoder, after the control inputs are loaded, DCLK needs to be active for at least 512 cycles before the first code word is input on the DDI bus.

Algebraic Description of the Reed-Solomon Code*

This section is intended for those mathematically inclined users who are interested in the algebraic aspects of the implemented RS code. It may be ignored by other users who are only interested in the functionality of the device.

The generator polynomial of the RS code is given by

$$\prod_{i=0}^{15} (x+\alpha^i)$$

where α is a root of the binary primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$. A data byte $(d_7,d_6,...,d_1,d_0)$ is identified with the element $d_7\alpha^7 = d_6\alpha^6 + \ldots + d_1\alpha + d_0$ in GF(256), the finite field with 256 elements.

* Recommended code for the transmission of contribution-quality digital television signals (CCIR723).

Application Example

This section describes an example of utilizing the L64710 for ensuring data integrity in a data storage or communication system. The noisy channel may be a storage device (magnetic tape, magnetic disk, optical disk) or a communication channel. Although this example does not correspond to a particular real-life system, it illustrates the role played by the L64710 in the implementation of highly reliable systems. The following description assumes that the noisy channel is a storage device. However, the same principles also apply to a communication channel.

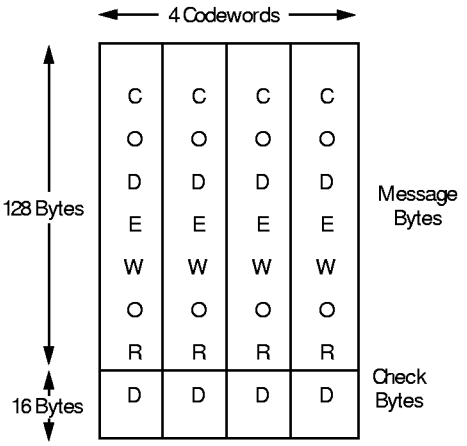
Sector Format

The data on the storage media is organized into sectors. Each sector contains a sync pattern followed by 512 bytes of message data and 64 bytes of redundant check data.

Sync Pattern	512 Message Bytes	64 Check Bytes

There are four Reed-Solomon codewords per sector. Each column in the following diagram is an RS codeword (128 message bytes followed by 16 check bytes). The data in this diagram is written onto the storage media row by row, instead of codeword by codeword (column by column). Thus two consecutive data bytes in an RS codeword are separated by three other data bytes on the storage media. A 32-byte long error burst within a sector on the media corrupts 8 bytes in each of the four codewords in the sector. Since the RS code is capable of correcting up to 8-byte errors per codeword, the error burst is corrected by the coding system. This technique is called interleaving. It increases the burst correction capability of the code.

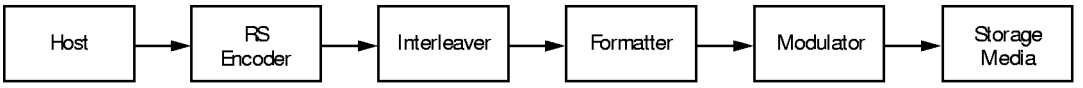
Interleaver/Deinterleaver Memory



Recording Operation

The RS encoder appends 16 bytes of check data to every 128 bytes of message data to form an RS codeword. Four such codewords constitute the data bytes in a sector. The four codewords are written in the interleaver memory column by column and read out row by row. The formatter inserts sync patterns at the beginning of sectors. The formatted data is then modulated and written onto the storage media.

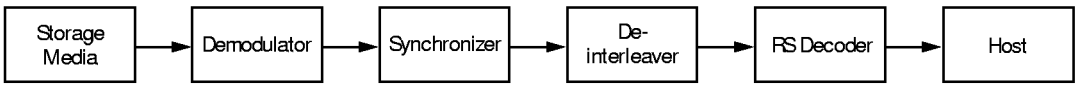
Recording Operation Data Flow



Playback Operation

The signals from the storage media are first demodulated. The synchronizer looks for the sync pattern in the demodulated signals to identify the beginning of a sector. This sync information is needed for the operation of the deinterleaver. Data is written in the deinterleaver memory row by row and read out column by column. Deinterleaved data passes into the RS decoder for error correction. The input DIMS signal for the RS decoder (indicates the start of decoder input message) is derived from the sync information produced by the synchronizer.

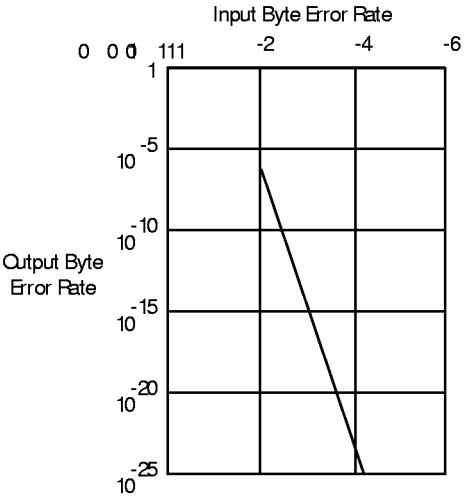
Playback Operation Data Flow



Application Example (Continued)

Performance

The percentage redundancy of the RS code in this example is 16/128 = 12.5%. With this modest amount of overhead, the coding system corrects error bursts up to 32 bytes long. The random error-correction capability of the code is summarized in the following chart. For a random input byte error rate of 10^{-3}, the corresponding output byte error rate is less than 10^{-14}.

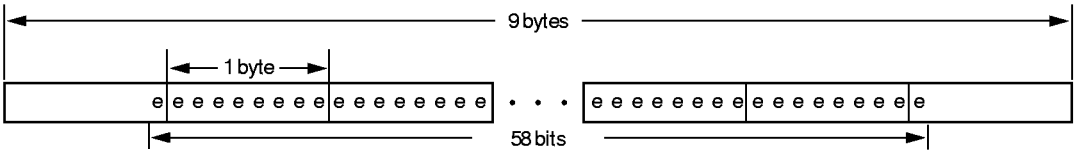


Performance Analysis

Data entering the L64710 decoder may be corrupted. A bit error occurs when a transmitted "0" is received as a "1" or vice versa. A byte error occurs when one or more bits in the byte have errors. For example, a byte with only one bit error is counted as one byte error, and a byte with 8 bit-errors (all bits are flipped) is also counted as one byte error. As long as there are no more than 8 byte-errors in a codeword, the RS decoder corrects all these errors.

Since a 58-bit burst may corrupt as many as 9 consecutive bytes, as shown in the following figures, the maximum guaranteed correctable burst length is 57 bits.

58-Bit Burst Example: (Each "e" represents one bit-error)



The performance of the code against independent random byte errors can be computed using the

$$q = \sum_{i=9}^{N} \frac{i}{N} \binom{N}{i} p^i (1-p)^{N-i}$$

where N denotes the codeword length, p denotes the input byte error rate, q denotes the output byte error rate and N/i is the binomial coefficient which represents the number of ways of choosing i items from a collection of N distinct items.

When there are more than 8 byte-errors in a codeword, the RS decoder usually detects the presence of excessive errors and notifies the user by asserting the DFAIL signal HIGH. However, there is a small probability that the erroneous decoded codeword remains undetected. The undetected erroneous codeword rate is given by:

$$\frac{1}{8!} \left(\frac{N}{255}\right)^8 \sum_{i=9}^{N} \binom{N}{i} p^i (1-p)^{N-i}$$

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Units
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD +0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC supply voltage	VDD	+3 to +6	V
Operating ambient Temperature range			
Military	TA	-55 to +125	°C
Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges(1)

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIL	Low level input voltage				0.8	V
VIH	High level input voltage					
	Commercial temperature range		2.0			V
	Military temperature range		2.25			V
IIN	Input current	VIN = VDD	-370		400	µA
VOH	High level output voltage	Comm and Mil				
		IOH = -4 mA	2.4	4.5		V
VOL	Low level output voltage	Comm and Mil				
		IOL = 4 mA		0.2	0.4	V
IOS	Output short circuit current (2)	VDD = Max, VO = VDD	30	75	140	mA
		VDD = Max, VO = 0V	-25	-70	-140	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS			10	mA
IDD	Operating supply current (3)	tECYCLE, tDCYCLE = 33 ns		300		mA
CIN	Input capacitance	Any Input		2.5		pF
COUT	Output capacitance	Any Output		2.0		pF

Notes:
1. Commercial temperature range is 0°C to +70°C, ±5% power supply; military temperature range is -55°C to +125°C, ±10% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. For 30 MHz device.

AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

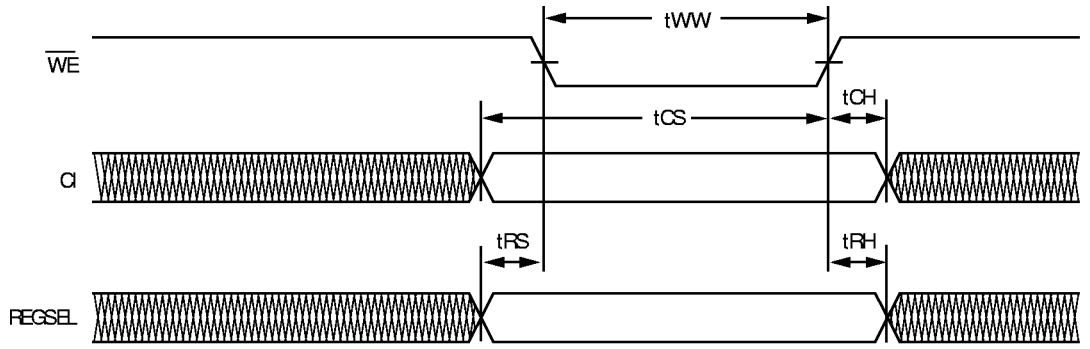
Symbol	Parameter	L64710-40		L64710-30	
		Min	Max	Min	Max
tWW	$\overline{WE}$ pulse width, LOW	13		17	
tCS	CI, input setup time	7		8	
tCH	CI, input hold time	0		0	
tRS	REGSEL input setup time	7		8	
tRH	REGSEL input hold time	0		0	
tECYCLE	ECLK cycle time	25		33	
tEPH	ECLK pulse width, HIGH	10		12	
tEPL	ECLK pulse width, LOW	10		12	
tES	EIMS, EDI input setup time	7		8	
tEH	EIMS, EDI input hold time	0		0	
tED	EOMS, EDO output delay		19		25
tDCYCLE	DCLK cycle time	25		33	
tDPH	DCLK pulse width, HIGH	10		12	
tDPL	DCLK pulse width, LOW	10		12	
tDS	DIMS, DDI input setup time	7		8	
tDH	DIMS, DDI input hold time	0		0	
tDD	DOMS, DDO, DFAIL, TDINC output delay		19		25

AC Switching Characteristics: Military (TA = -55°C to 125°C, VDD = 4.75 V to 5.25 V)

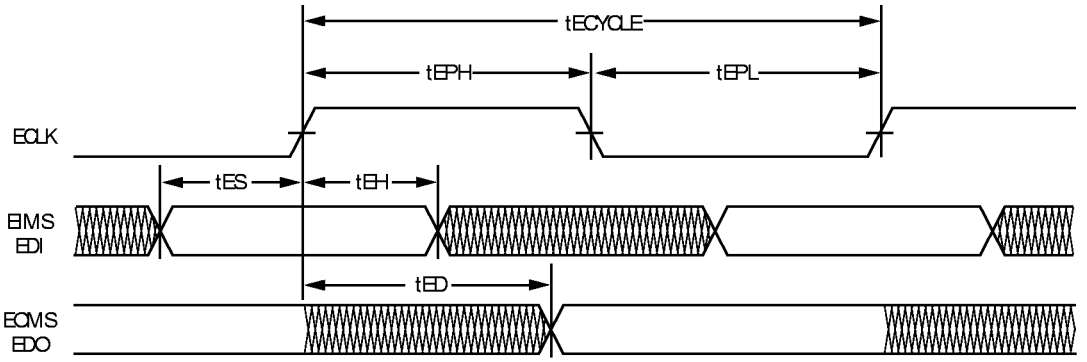
Symbol	Parameter	L64710-30		L64710-25	
		Min	Max	Min	Max
tWW	$\overline{WE}$ pulse width, LOW	17		20	
tCS	CI, input setup time	8		10	
tCH	CI, input hold time	0		0	
tRS	REGSEL input setup time	8		10	
tRH	REGSEL input hold time	0		0	
tECYCLE	ECLK cycle time	33		40	
tEPH	ECLK pulse width, HIGH	12		15	
tEPL	ECLK pulse width, LOW	12		15	
tES	EIMS, EDI input setup time	8		10	
tEH	EIMS, EDI input hold time	0		0	
tED	EOMS, EDO output delay		25		30
tDCYCLE	DCLK cycle time	33		40	
tDPH	DCLK pulse width, HIGH	12		15	
tDPL	DCLK pulse width, LOW	12		15	
tDS	DIMS, DDI input setup time	8		10	
tDH	DIMS, DDI input hold time	0		0	
tDD	DOMS, DDO, DFAIL, TDINC output delay		25		30

AC Timing Waveforms

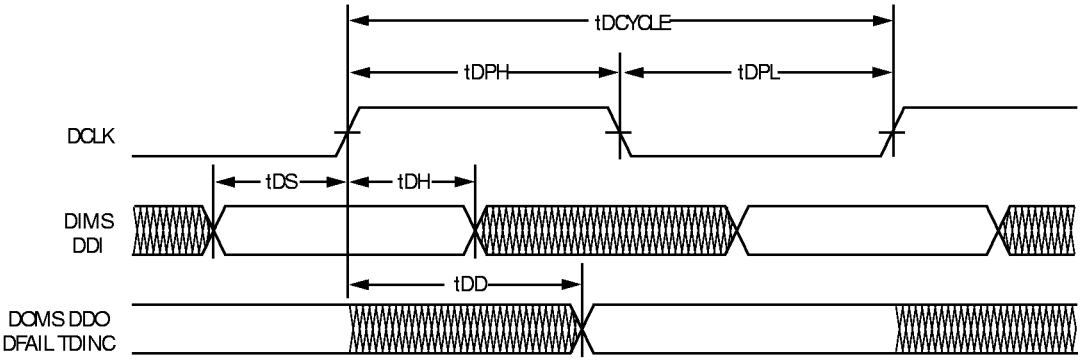
Control Section



Encoder Section



Decoder Section



Pinout Diagram

68-Pin Ceramic Pin Grid Array (CPGA)

	1	2	3	4	5	6	7	8	9
A		EDI.1	EDI.0	ECLK	EDO.6	EDO.4	VDD	EDO.2	EDO.1	DDI.7	
B	EDI.2	VDD	EOMS	EDO.7	EDO.5	VSS	EDO.3	VSS	EDO.0	VDD	DDI.6
C	VSS	EDI.3								DDI.4	DDI.5
D	EDI.5	EDI.4								DDI.2	DDI.3
E	VDD	EDI.6								DDI.0	DDI.1
F	EDI.7	VSS			Top View Cavity Up					VSS	VDD
G	RESET/ VSS	EIMS								DIMS	DCLK
H	$\overline{WE}$	REGSEL								VSS	DDO.7
J	CI.1	CI.O								DDO.5	DDO.6
K	CI.2	VDD	CI.4	CI.6	TCUT/ NC	VSS	DFAIL	DDO.0	DDO.1	VDD	DDO.4
L		CI.3	CI.5	CI.7	TDINC	VDD	DOMS	VSS	DDO.2	DDO.3	

Packaging

68-Pin Ceramic Pin Grid Array: See NB Package in Package Selector Guide

Ordering Information

L64710 G M -XX

- -XX — Speed MHz
- M — Temperature Range/Flow Option
  - C = Commercial (0°C to 70°C)
  - M = Military (-55°C to 125°C), Processed to MIL-STD-883C Level B
- G — Package Code
  - G = 68-Pin Ceramic Pin Grid Array
- L64710 — Device Type
  - Reed-Solomon Codec

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