HARRIS HSP45106/883

T-77-09

May 1991

16 Bit Numerically Controlled Oscillator

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1
- 25.6MHz and 33MHz Versions
- 32-Bit Center and Offset Frequency Control
- 16-Bit Phase Control
- 8 Level PSK Supported Through Three Pin Interface
- Simultaneous 16 Bit Sine and Cosine Outputs
- Output in Two's Complement or Offset Binary
- <0.01Hz Tuning Resolution at 33MHz
- Serial or Parallel Outputs
- Spurious Frequency Components < -90dBc
- 16 Bit Microprocessor Compatible Control Interface
- 85 Pin PGA

Applications

- Direct Digital Synthesis
- Quadrature Signal Generation
- Modulation - FM, FSK, PSK (BPSK, QPSK, 8PSK)
- Precision Signal Generation

Description

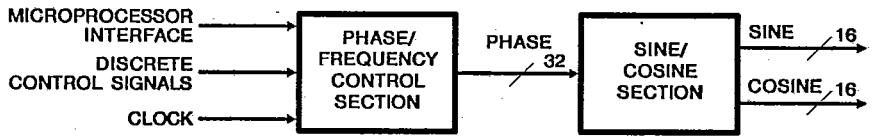
The Harris HSP45106/883 is a high performance 16-bit quadrature numerically controlled oscillator (NCO16). The NCO16 simplifies applications requiring frequency and phase agility such as frequency-hopped modems, PSK modems, spread spectrum communications, and precision signal generators. As shown in the block diagram, the HSP45106/883 is divided into a Phase/Frequency Control Section (PFCS) and a Sine/Cosine Section.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The frequency resolution is 32 bits, which provides for resolution of better than 0.01Hz at 33MHz. User programmable center frequency and offset frequency registers give the user the capability to perform phase coherent switching between two sinusoids of different frequencies. Further, a programmable phase control register allows for phase control of better than 0.006°. In applications requiring up to 8 level PSK, three discrete inputs are provided to simplify implementation.

The output of the PFCS is a 32-bit phase argument which is input to the sine/cosine section for conversion into sinusoidal amplitude. The outputs of the sine/cosine section are two 16-bit quadrature signals. The spurious free dynamic range of this complex vector is greater than 90dBc.

For added flexibility when using the NCO16 in conjunction with DAC's, a choice of either parallel of serial outputs with either two's complement or offset binary encoding is provided. In addition, a synchronization signal is available which signals serial word boundaries.

Block Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 2815

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output Voltage Applied ..... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic PGA Package	36.0°C/W	11.6°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package ..... 1.39 Watt
Gate Count ..... 18,750 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. HSP45106/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Output Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V, (Note 4)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 25.6MHz V_{CC} = 5.5V (Notes 2, 4)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	256	mA
Functional Test	FT	(Note 3)	7, 8	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 10mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, V_{OH} ≥ 1.5V, V_{OL} ≤ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.
4. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS -25 (25.6MHz) MIN	LIMITS -25 (25.6MHz) MAX	LIMITS -33 (33MHz) MIN	LIMITS -33 (33MHz) MAX	UNITS
CLK Period	T_{CP}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	39	-	30	-	ns
CLK High	T_{CH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	12	-	ns
CLK Low	T_{CL}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	12	-	ns
WR# Period	T_{WP}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	39	-	30	-	ns
WR# High	T_{WH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	12	-	ns
WR# Low	T_{WL}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	12	-	ns
Set-up Time A0-2, CS# to WR# going high	T_{AWS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	13	-	13	-	ns
Hold Time A0-2, CS# from WR# going high	T_{AWH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2	-	2	-	ns
Set-up Time C0-15 to WR# going high	T_{CWS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	15	-	ns
Hold Time C0-15 from WR# going high	T_{CWH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	1	-	1	-	ns
Set-up Time WR# high to CLK high	T_{WC}	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	16	-	12	-	ns
Set-up Time MOD0-2 to CLK going high	T_{MCS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	15	-	ns
Hold Time MOD0-2 from CLK going high	T_{MCH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	1	-	1	-	ns
Set-up Time ENPOREG#, ENOFREG#, ENCFREG#, ENPHAC#, ENTIREG#, INHOFR#, PMSEL#, INITPAC#, BINFMT#, TEST, PAR/SER#, PACI#, INITTAC# to CLK going high	T_{ECS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	12	-	12	-	ns
Hold Time ENPOREG#, ENOFREG#, ENCFREG#, ENPHAC#, ENTIREG#, INHOFR#, PMSEL#, INITPAC#, BINFMT#, TEST, PAR/SER#, PACI#, INITTAC# from CLK going high	T_{ECH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	1	-	1	-	ns
CLK to Output Delay SIN0-15, COS0-15, TICO#	T_{DO}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	18	-	15	ns
CLK to Output Delay DACSTRB#	T_{DSO}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2	18	2	15	ns
Output Enable Time	T_{OE}	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	12	-	12	ns

NOTES:

1. A.C. Testing: Inputs are driven to 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". Inputs driven at 1V/ns. CLK is driven at 4.0V and 0V and measured at 2.0V. Output load per test load circuit with switch closed and C_L = 40pF.
2. Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and C_L = 40pF.
3. If ENOFRCTL#, ENCFRCTL#, ENTICTL# or ENPHREG# are active, care must be taken to not violate set-up and hold times to these registers when writing data into the chip via the C0-15 port.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS -25 (25.6MHz) MIN	LIMITS -25 (25.6MHz) MAX	LIMITS -33 (33MHz) MIN	LIMITS -33 (33MHz) MAX	UNITS
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	T_A = +25°C	-	10	-	10	pF
Output Capacitance	C_{OUT}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	T_A = +25°C	-	10	-	10	pF
Output Disable Delay	T_{OEZ}		1,2	-55°C ≤ T_A ≤ +125°C	-	15	-	15	ns
Output Rise Time	T_{OR}	From 0.8V to 2.0V	1,2	-55°C ≤ T_A ≤ +125°C	-	8	-	8	ns
Output Fall Time	T_{OF}	From 2.0V to 0.8V	1,2	-55°C ≤ T_A ≤ +125°C	-	8	-	8	ns

NOTES:

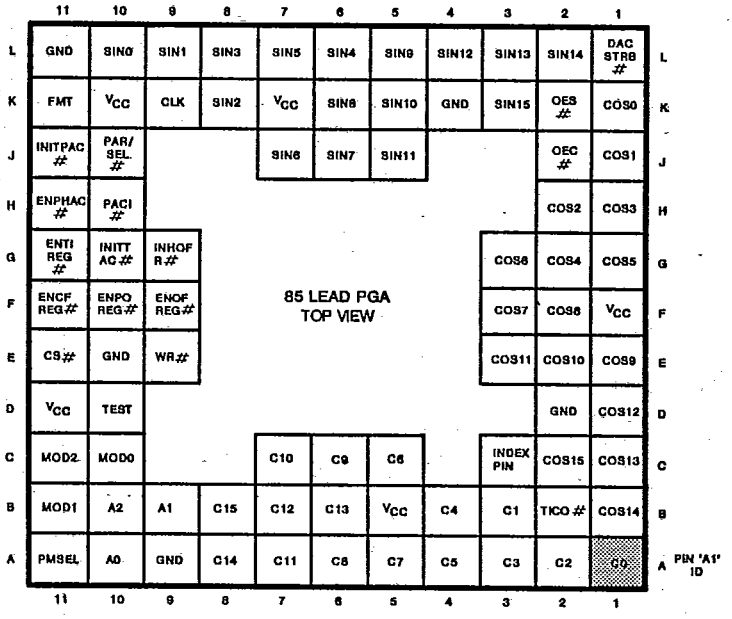
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with switch closed and C_L = 40pF.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

HSP45106/883 PIN GRID ARRAY (PGA)



PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	C0	F7	B11	MOD1	F13	F9	ENOFREG#	F8	K2	OES#	F14
A2	C2	F7	C1	COS13	$V_{CC}/2$	F10	ENPOREG#	F4	K3	SIN15	$V_{CC}/2$
A3	C3	F7	C2	COS15	$V_{CC}/2$	F11	ENCFREG#	F7	K4	GND	GND
A4	C5	F8	C5	C6	F8	G1	COS5	$V_{CC}/2$	K5	SIN10	$V_{CC}/2$
A5	C7	F8	C6	C9	F10	G2	COS4	$V_{CC}/2$	K6	SIN8	$V_{CC}/2$
A6	C8	F10	C7	C10	F10	G3	COS6	$V_{CC}/2$	K7	VCC	VCC
A7	C11	F10	C10	MOD0	F12	G9	INHOFR#	F11	K8	SIN2	$V_{CC}/2$
A8	C14	F11	C11	MOD2	F14	G10	INITTAC#	F13	K9	CLK	F0
A9	GND	GND	D1	COS12	$V_{CC}/2$	G11	ENTIREG#	F12	K10	VCC	VCC
A10	A0	F8	D2	GND	GND	H1	COS3	$V_{CC}/2$	K11	BINFMT#	F6
A11	PMSEL	F14	D10	TEST	F14	H2	COS2	$V_{CC}/2$	L1	DACSTRB#	$V_{CC}/2$
B1	COS14	$V_{CC}/2$	D11	VCC	VCC	H10	PACI#	F11	L2	SIN14	$V_{CC}/2$
B2	TICO#	$V_{CC}/2$	E1	COS9	$V_{CC}/2$	H11	ENPHAC#	F10	L3	SIN13	$V_{CC}/2$
B3	C1	F7	E2	COS10	$V_{CC}/2$	J1	COS1	$V_{CC}/2$	L4	SIN12	$V_{CC}/2$
B4	C4	F8	E3	COS11	$V_{CC}/2$	J2	OEC#	F14	L5	SIN9	$V_{CC}/2$
B5	VCC	VCC	E9	WR#	F4	J5	SIN11	$V_{CC}/2$	L6	SIN4	$V_{CC}/2$
B6	C13	F11	E10	GND	GND	J6	SIN7	$V_{CC}/2$	L7	SIN5	$V_{CC}/2$
B7	C12	F11	E11	CS#	F6	J7	SIN6	$V_{CC}/2$	L8	SIN3	$V_{CC}/2$
B8	C15	F11	F1	VCC	VCC	J10	PAR/SER#	F13	L9	SIN1	$V_{CC}/2$
B9	A1	F7	F2	COS8	$V_{CC}/2$	J11	INITPAC#	F12	L10	SIN0	$V_{CC}/2$
B10	A2	F10	F3	COS7	$V_{CC}/2$	K1	COS0	$V_{CC}/2$	L11	GND	GND

NOTES:

1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5V ±0.5V.
4. 0.1µF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2 . . . , F11 = F10/2, 40% - 60% Duty Cycle.
6. Input voltage limits: V_{IL} = 0.8V Max V_{IH} = 4.5V ±10%

Die Characteristics

DIE DIMENSIONS:
251 x 240 x 19 ±1 mils

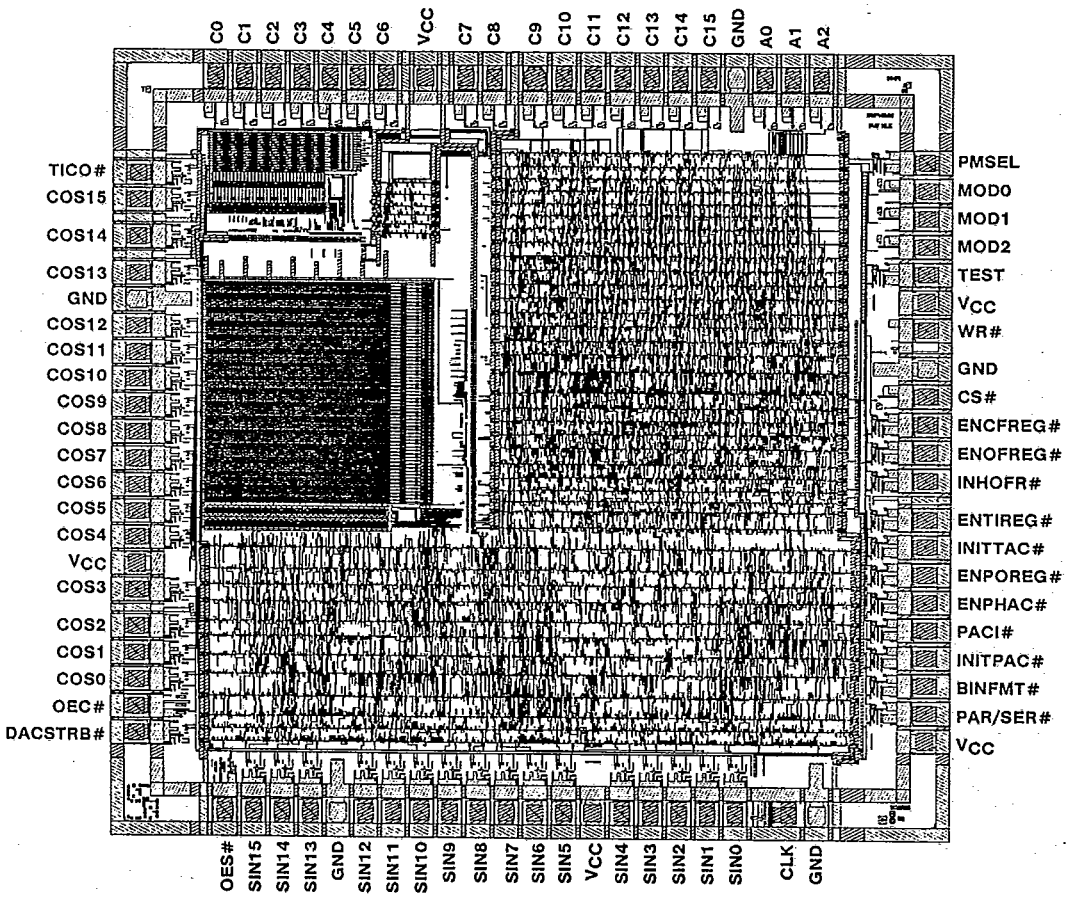
METALLIZATION:
Type: Si-Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

DIE ATTACH:
Material: Silver Glass

Metallization Mask Layout

HSP45106/883

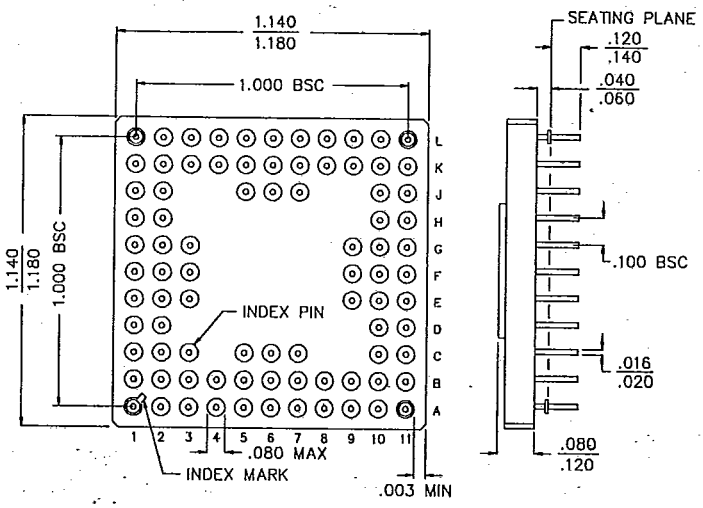


5 SIGNAL SYNTHESIZERS

T-77-09

Packaging†

85 PIN GRID ARRAY (PGA)



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Ceramic, Al_2O_3 90%
PACKAGE SEAL:
Material: Gold/Tin
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Wedge
COMPLIANT OUTLINE: 38510 P-AC

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†MIL-M-38510 Compliant Materials, Finishes, and Dimensions.