GT-64012/A

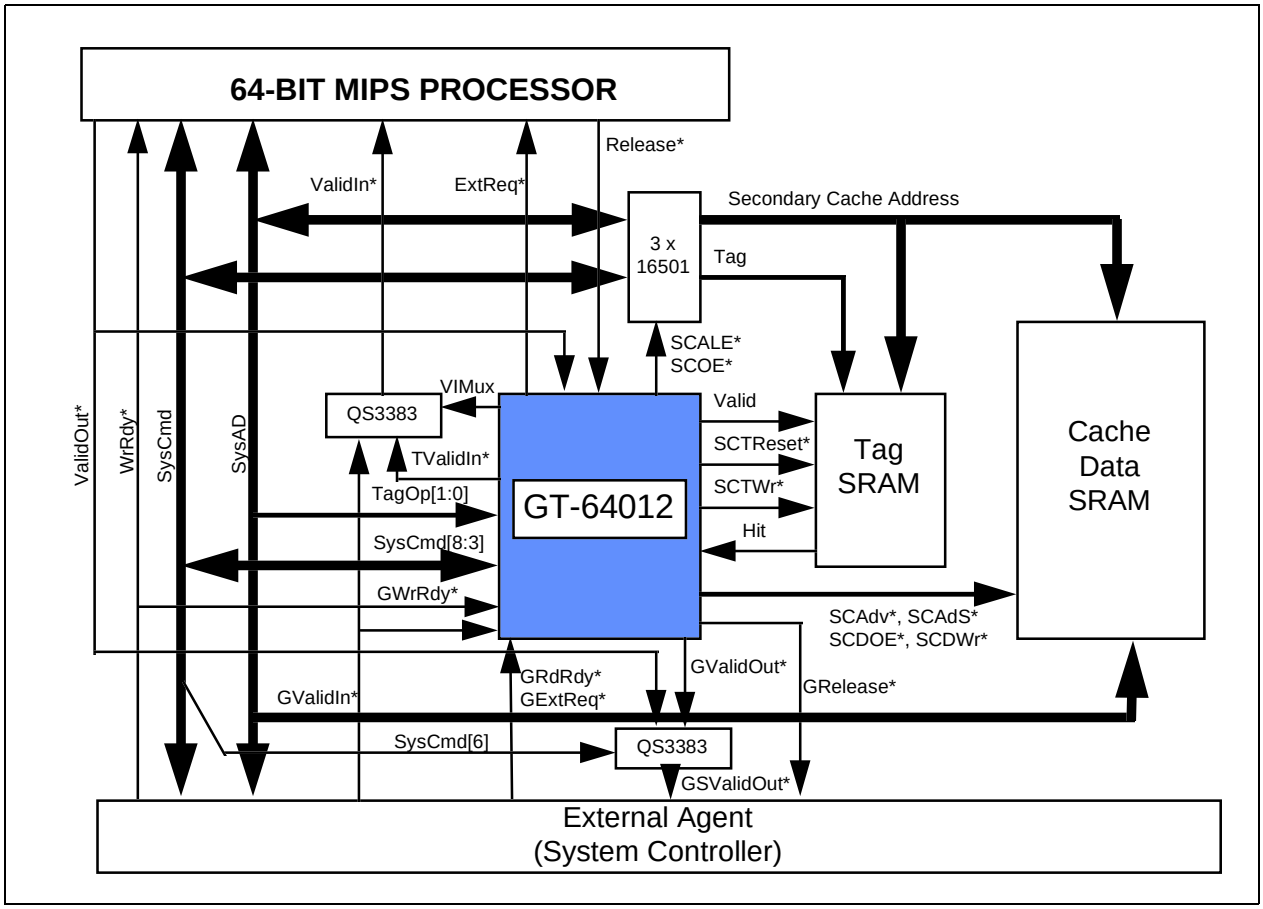
Secondary Cache Controller for R4600/4650/4700/5000

Final
Revision 3.0
10/22/97

Please contact Galileo Technology for possible updates before finalizing a design.

FEATURES

- Secondary cache controller for the 64-bit MIPS R4600/4650/4700/5000 microprocessors
- Large cache size support
  - 256KByte
  - 512KByte
- Fixed line size
  - 4 double-words (32 bytes)
- Write-through policy
- Direct mapping
- Physical address and tag
- Zero wait-states for cache hit
- Supports industry standard synchronous burst SRAMs
  - 32Kx18
  - 64Kx18
  - 32Kx36
- Moderate Data SRAM speed required
  - 12ns for 50MHz
- Supports de-facto standard cache tags
  - 8Kx8 tag (IDT71B74)
  - 16Kx15 tag (IDT71215)
- Read burst latency of 3-1-1-1
- Supports all write patterns (DDDD or slower)
- Supports the R4700's special write modes
  - Pipeline
  - Re-issue
- "Transparent" architecture
  - Design with no logic changes into existing systems
- Easy evaluation via Galileo-2 CPU module
  - Fits into existing CPU sockets with no board changes to R4600/R4700 system
- Compatible with Galileo GT-64010 System Controller
- Minimizes use of external logic components
  - Only 4 standard logic components needed besides memory
- Simple way to boost CPU performance
  - Typical improvement range of 20%-100% depending on system architecture and code
- 5 Volt operation
  - Easy to incorporate into a 3.3V environment
- Works with GT-64010A and GT-64120 System Controllers
- 44-pin PLCC package



1. OVERVIEW

The GT-64012 is a secondary cache controller for the MIPS R4600/4650/4700/5000, which can help system performance increase by anywhere between 20% and 100%, depending on the system architecture and the nature of the software run by it. The GT-64012 is also compatible with the R4400PC and R4000PC.

The architecture of the GT-64012 enables the addition of a secondary cache to an existing system without changes to the system ASICs or controller logic, for a cost-effective increase in system performance. Brand new designs can attain further optimizations.

The GT-64012 is designed with BiCMOS technology to ensure support of fast processor speeds, and to reduce the speed requirement of the tag and data SRAMs, thus reducing system cost. The GT-64012 supports up to 50MHz clock speeds in the bus with no wait-states, which means that it supports the R4600/R4700-100MHz in up to divide-by-2 mode, the R4600/R4700-133MHz, and R4600/R4700-150MHz in up to divide-by-3 mode, and the R4700-166MHz and R4700-175MHz in up to divide-by-4 mode.

The GT-64012 supports industry standard synchronous SRAMs with a sub-block ordering burst sequence like the one found in Intel processors, thus taking advantage of the economies of scale associated with the PC industry. By supporting synchronous SRAMs, zero wait-state is attained without the need for interleaving, thus reducing component count, board space, and loading, while improving granularity. Only 2 or 4 data SRAMs are needed to build a 256KByte or 512KByte cache. At the maximum speed of 50MHz, the GT-64012 only requires the 12ns version of these SRAMs, thus keeping system cost at reasonable levels.

The GT-64012 is designed to work with de-facto standard cache tags, very fast SRAMs that include the tag comparison logic on-board. This simplifies the design and ensures no wait-state operation. For a 256KByte cache, a depth of 8K is needed in the cache tag, whereas for a 512KByte cache a tag depth of 16K is necessary. The required speed for the address-to-match comparison is 10ns, which is not the fastest tag SRAM speed available. The tag SRAM requirement can be reduced to a single chip in the case of the IDT71215 16Kx15 device if a 512KB cache is used, or two IDT71B74 8Kx8 devices if a 256KB cache is used.

The GT-64012 operates as a direct mapped, write-through cache, with a fixed line size of 32 bytes. It supports no wait-state operation and a burst read hit pattern of 3-1-1-1. Furthermore, it supports the special write modes of the R4600, including pipeline and re-issue. It supports the DDDD write pattern, as well as any other slower patterns. The miss "penalty" of the secondary cache is 0 clock cycles for write transactions, 1 clock cycle for non-cacheable read transactions, and 2 clock cycles for cacheable read transactions.

The GT-64012 is housed in a low-cost surface mounted 44-pin PLCC package.

1.1 REFERENCE DESIGN

A system can be easily retrofitted in one of two ways. First, the R4700 CPU can be replaced by a CPU module that contains all the secondary cache components. An example of this is the Galileo-2 module, which is available for evaluation, and the reference design of which is available for free (please request your copy). Secondly, a motherboard can be easily redesigned to incorporate the cache subsystem knowing that no changes are necessary to the existing controller logic or ASICs. In either case, all that is needed is to adjust the software or firmware to recognize the presence of the secondary cache.

Brand new designs can use the schematics of the Galileo-2 module as a reference, to facilitate the design process. New designs can reduce the "miss" penalty to 0 clock cycles for writes and non-cacheable read transactions, and 1 clock cycle for cacheable reads. This can be achieved by connecting the system controller to the CPU's ValidOut* signal and the Tag SRAM's Hit signal.

The Galileo-2 module consists of a small PC board that is plugged into an existing R4600 or R4700 179-PGA socket, replacing the CPU. The CPU is then plugged into a similar 179-PGA socket on the Galileo-2 module. The module contains the GT-64012 secondary cache controller, a 16Kx15 Tag SRAM, four 32Kx18 or 64Kx18 burst SRAMs, and 4 standard logic components. A block diagram of it appears on the cover.

1.2 DESIGNING A NEW SYSTEM WITH THE GT-64012

When a new System ASIC is being designed and the GT-64012 is used, it is possible to improve system performance during reads.

The GT-64012 distinguishes between two types of Reads: uncacheable (partial reads) and cacheable (block reads).

All partial reads (SysCmd[7:5] = 0 and SysCmd[3] = 1), are forwarded to the System a cycle later than the issue cycle on the CPU bus. As both the SysAD and SysCmd buses are point-to-point connections between the CPU and the System, a newly designed System ASIC may monitor SysCmd, ValidOut*, TagOp0, and TagOp1 to detect a partial read request. When a partial read is detected, with both TagOp0 and TagOp1 inactive, the System ASIC may start processing the transaction immediately, knowing that a cycle later it should ignore the GValidOut* generated by the GT-64012. One cycle is therefore saved.

Block reads are checked by the GT-64012 for Hit or Miss in the Tag SRAM. The lookup is done one cycle after ValidOut* is asserted. No action is taken by the GT-64012 until the CPU bus is released (read issue cycle). One cycle after the CPU bus is released the GT-64012 asserts GValidOut* if the lookup turned to be a Miss so as to forward the request to the system.

A newly designed System ASIC may monitor the Hit signal during the look-up phase to determine in advance if the request will be forwarded to the system or not. If a Hit occurs, no action should be taken as data will be returned from the secondary cache. If a Miss occurs, the System ASIC may start processing the request ignoring the GValidOut* which will be generated by the GT-64012 at least a cycle later. Care should be taken to keep track over CPU bus status (released or not) before SysAD and SysCmd get driven by the System; i.e., GRelease* should be monitored for assertion before SysCmd and SysAD are truly released. In systems where RdRdy* is constantly asserted, GRelease* will be asserted two cycles after the issue cycle.

In most systems, RdRdy* is constantly asserted or even tied to ground so the same cycle in which ValidOut* is firstly asserted is also the issue cycle. Such systems may simplify the decision making involved in this process.

The GT-64010 System Controller from Galileo takes advantage of this methodology to provide a system designer with maximum performance when also using the GT-64012 Secondary Cache Controller.

1.3 DETERMINATION OF SECONDARY CACHE PRESENCE VIA SOFTWARE

It is possible to utilize a simple software mechanism to determine if a GT-64012 is present in the system or not. The sequence of transactions to be made is as follows (all are addressed to the same cache line):

1. cacheable read (block);
2. first level cache invalidate (cache operation) *or* two first level cache line replacements;
3. uncacheable write;
4. cacheable read.

If the returned data from step 4 is updated by the written data in step 3, the GT-64012 is not present in the system, and vice versa.

1.4 COMPATIBILITY WITH 3.3V SYSTEMS

It is easy to interface the 5V GT-64012 to a 3.3V CPU subsystem. The block diagram that appears on the cover needs to be augmented only by one component. The existing components are already 3.3V-compatible.

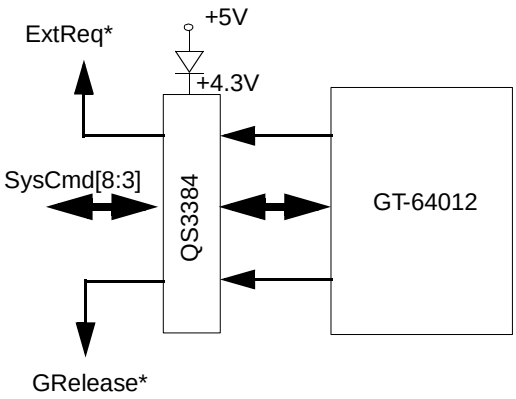
The burst synchronous SRAMs are available in 3.3V Vcc versions with 5V-tolerant inputs and thus can interface directly to the GT-64012.

Tag SRAMs like the IDT71215 can have their I/Os working from a 5V or 3.3V source, while the supplied Vcc is 5V, and thus can work in a mixed voltage environment.

The FCT163501 3.3V bidirectional latches can be used instead of the 5V version, since their inputs are still 5V tolerant.

The QuickSwitches used to gate the ValidOut and ValidIn signals provide an effective mechanism to interface between 5V and 3.3V.

Consequently, the only extra component needed is another QuickSwitch to interface the GT-64012 outputs ExtReq* and GRelease*, plus the I/Os SysCmd[8:3], to the 3.3V subsystem. The QS3384 when supplied with 4.3V works as an effective 5V to 3.3V converter with zero delay. This is illustrated in the figure below.



1.5 GT-64012 and GT-64012A

The original GT-64012 is being augmented in late 1997/early 1998 by the GT-64012A. The GT-64012 is manufactured at Temic on a BiCMOS process. The GT-64012A by comparison, is manufactured at Samsung on a high-volume.5 micron CMOS process. The GT-64012A is pin compatible and a drop in replacement for all systems using the GT-64012.

The table below lists the specification changes between the GT-64012 and GT-64012A. Reductions in drive strength and test load are not expected to affect any production systems as the signals affected drive lightly loaded nodes.

Table 1: Drive Strength Differences

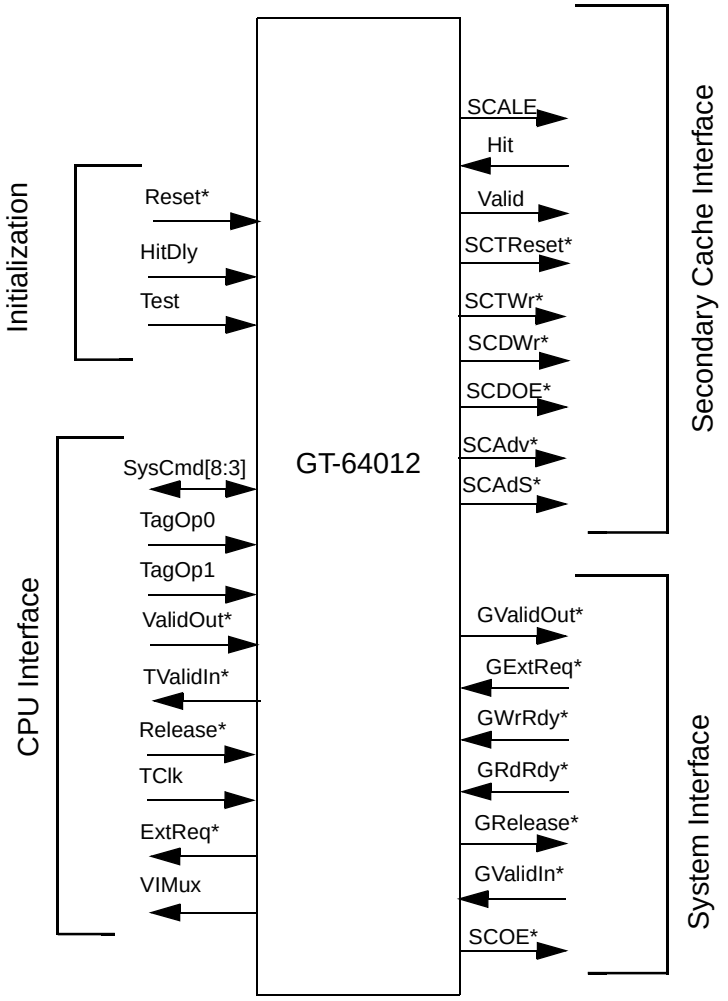
Parameter	GT-64012	GT-64012A
SysCmd[8:3] drive strength	32mA	16mA
TValidIn* drive strength	32mA	8mA
ExtReq* drive strength	32mA	2mA
VIMux drive strength	32mA	12mA
GRelease*, GValidOut* drive strength	32mA	20mA
SCOE* drive strength	32mA	12mA
Valid, SCTReset*, SCTWr* drive strength	32mA	2mA
SCDOE*, SCAdv*, SCDWr* drive strength	32mA	12mA
SCAds* drive strength	32mA	16mA

Table 2: AC Test Load Differences

Parameter	GT-64012	GT-64012A
ExtReq* AC test load	50pF	20pF
Valid, SCTReset*, SCTWr* AC test load	50pF	20pF

2. PIN INFORMATION

2.1 Logic Symbol



3. Pin Assignment Table

Pin name	Sync to	Type	Drive	Description
Initialization				
Reset*	---------	I		**Reset:** Initializes the internal state of the GT-64012.
HitDly	TClk	I		**Hit Delay:** Configuration bit for the R4600 versions. '0': zero wait states during hits (R4600 version 2.0 or higher) '1': one wait state during hits (R4600 version 1.7)
Test		I		**Test:** Tri-states all outputs. "0": normal functioning "1": tri-state outputs
CPU Bus				
Release*	TClk	I		**Release:** In response to the assertion of ExtReq* or a CPU Read request, the CPU asserts Release*, signaling to the GT-64012 that the System interface is available
TagOp1	TClk	I		**Tag RAM Operations 1:** A HIGH during a partial read address space causes a Tag SRAM flush. This input typically connects to a high order address bit (e.g. SysAD[31]).
TagOp0	TClk	I		**Tag RAM Operations 0:** A HIGH during a partial read address space invalidates a specific Tag SRAM entry. This input typically connects to a high order address bit (e.g. SysAD[30]). The entry to be invalidated is defined by the address of the transaction. Note that TagOp1 and TagOp0 should not be high simultaneously during a partial read address phase.
SysCmd[8:3]	TClk	I/O	16mA (32mA)[1]	**System Command:** Upper 6 bits of command and data identifier.
TValidIn*	TClk	O	8mA (32mA)	**Valid In:** Asserted when the GT-64012 drives valid data onto the SysAD bus and valid data identifier onto the SysCmd bus during block read Hit or Tag SRAM operations.
ValidOut*	TClk	I		**Valid Out:** Used by the GT-64012 as an indication that the CPU is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ExtReq*	TClk	O	2mA (32mA)	**External Request:** The GT-64012 asserts this signal to request use of the System interface.
TClk	---------	I		**Transmit Clock:** System clock input.
VIMux	TClk	O	12mA (32mA)	**ValidIn Multiplexing:** Controls the no-delay external multiplexer (QS3383Q) selecting the source of CPU ValidIn* from the TValidIn* signal supplied by the GT-64012 or the GValidIn* signal supplied by the system controller.
System Bus				
GExtReq*	TClk	I		**System External Request:** Provided by the system controller, it controls the ExtReq* output of the GT-64012. Only external Write and external Null requests are supported.

Pin name	Sync to	Type	Drive	Description
GRdRdy*	TClk	I		**System Read Ready:** When asserted by the system controller, it indicates that the system can accept a CPU Read request.
GRelease*	TClk	O	20mA (32mA)	**System Release:** In response to the assertion of GExtReq* or a CPU Partial Read or Block Read Miss, the GT-64012 asserts GRelease*, signaling to the system controller that the System interface is available.
GValidIn*	TClk	I		**System Valid In:** Asserted when the system controller drives valid address or data onto the SysAD bus and valid data identifier onto the SysCmd bus, during CPU Reads or external requests.
GValidOut*	(1)	O	20mA (32mA)	**System Valid Out:** Indicates to the system controller that the CPU or the GT-64012 is driving a valid address or data onto the SysAD bus and a valid command or data identifier onto the SysCmd bus.
GWrRdy*		I		**System Write Ready:** Indicates that the system controller can accept a CPU Write request.
SCOE*	TClk	O	12mA (32mA)	**Secondary Cache Output Enable:** Provides output enable control of the external bidirectional latches (FCT16501). Active during Partial Reads and Block Read Misses to drive address and command onto the system controller.
Cache Interface				
SCALE	(2)	O	8mA (32mA)	**Secondary Cache Address Latch Enable:** Provides latch enable control to the external bidirectional latches (FCT16501). It is used to latch the address and command at issue.
Hit	TClk	I		**Hit:** Indicates a valid match in the Tag RAM.
Valid	TClk	O	2mA (32mA)	**Valid:** Validates tag entry during Block Write and Block Read Miss (line fill). Invalidates tag entry during Tag Invalidate operation.
SCTReset*	TClk	O	2mA (32mA)	**Secondary Cache Tag Reset:** A reset signal to the Tag RAM, asserted during a Tag Flush operation.
SCTWr*	TClk	O	2mA (32mA)	**Secondary Cache Tag Write:** Controls writes to the Tag RAM.
SCDWr*	TClk	O	12mA (32mA)	**Secondary Cache Data Write:** Enables data Writes to the cache data SRAMs. Activated during Block Write and Block Read Miss (line fill).
SCDOE*	TClk	O	12mA (32mA)	**Secondary Cache Data Output Enable:** Enables data output from the cache data SRAMs. Activated during Block Read Hit.
SCAdv*	TClk	O	12mA (32mA)	**Secondary Cache Advance:** Synchronously advances the cache data SRAM internal burst address.
SCAdS*	(3)	O	16mA (32mA)	**Secondary Cache Address Strobe:** Synchronously latches the burst start address in the cache data SRAMs.

1. All drive strengths in parentheses (e.g. (32mA)) refer to the original GT-64012 as opposed to the new GT-64012A.

3.1 Notes on Pinout

(1) Flow-through signal for Writes; Registered Signal for Reads

(2) Latched-out on the falling edge of TClk

(3) Flow-through signal

4. FUNCTIONAL DESCRIPTION

4.1 Initialization Interface

Reset* initializes the internal state of the GT-64012. It does not initialize the Tag RAM entries. The configuration pin (HitDly) is sampled during reset to determine whether to have zero or one wait-state in read hit cycles. This is designed to accommodate Rev. 1.7 versions of the R4600. The pin is sampled during the last four TClk cycles in which Reset* is asserted. When HitDly is sampled HIGH, there is one wait-state during read hits to support Rev. 1.7 R4600's. When HitDly is sampled LOW, there are no wait-states on read hits. Reset* and TClk must be connected to the CPU Reset input and TClk output.

4.2 CPU Interface

- **Block Read Request**

In a block read request and a hit in the secondary cache, the data will be supplied from the cache and the GT-64012 will not forward the request to the system interface (GValidOut* is not asserted).

In a miss in the secondary cache, the GT-64012 forwards the request to the system by asserting GValidOut* and GRelease* two TClks after receiving the request from the CPU. The address and the command, which are no longer available from the CPU, are driven onto the SysAD and SysCmd buses from the bi-directional latches (16501), by means of the GT-64012 asserting SCOE*. When the data is returned from the system to the CPU, the GT-64012 writes the line into the secondary cache (performs a line fill).

- **Uncached Read Requests**

In an uncached read request the GT-64012 forwards the request to the system one TClk cycle after receiving the request. When the system returns the data, the GT-64012 forwards it to the CPU without writing it to the secondary cache.

- **Block Write Request**

In a block write request the GT-64012 forwards the request to the system by asserting GValidOut* in the same TClk the request is issued by the CPU (ValidOut* is asserted). Concurrently the GT-64012 writes the line to the cache and updates the tag and Valid bit in the Tag RAM. The GT-64012 supports all write patterns of the R4600 (DDDD, DXDXDXDX, etc.).

- **Uncached Write Request**

In an uncached write request, the GT-64012 forwards the request to the system in the same TClk that the request is issued from the CPU. The cache is not updated.

- **Flush**

The CPU can flush the secondary cache by executing an uncached read request with TagOp0 LOW and TagOp1 HIGH. The GT-64012 will not forward this cycle to the system bus. It will reset the entire Tag RAM and return undefined data to the CPU three TClks from ValidOut*. This means that the entire Tag RAM is cleared (flushed).

- **Cache Entry Invalidate**

The CPU can invalidate an entry in the secondary cache Tag RAM by performing an uncached read with TagOp0 HIGH and TagOp1 LOW. The entry pointed by the address on SysAD[5:17/18] will be invalidated (17 or 18 as a function of the size of the data SRAMs used). Note that both Flush and Cache Entry Invalidate operations return undefined data. The GT-64012 always drives SysCmd[4] to check parity. Thus if the system is parity-protected, the CPU's parity checking should be turned off when executing cache operations.

- **External Requests**

The GT-64012 supports external write requests and external null requests. It does not support external read requests. All external requests are forwarded to the CPU without GT-64012 intervention.

- **Read Ready**

The CPU's RdRdy* pin is connected to VSS (always active). The external agent drives the GT-64012's GRdRdy* signal.

- **Write Ready**

The external agent drives WrRdy* to both the GT-64012 and the CPU.

4.3 System Interface

The system interface transfers CPU cycles to the system bus. It transfers read responses and external requests from the system bus to the CPU via the 16501s.

4.4 Cache Interface

The GT-64012 supports industry standard synchronous burst SRAMs. Examples of this are the IDT 71420 32Kx18 and the Motorola 67B618 64Kx18.

Synchronous Burst SRAM	Number of Tag Entries	Number of SRAMs	Cache size
32K x 18	8K	4	256KB
32K x 36	8K	2	256KB
64K x 18	16K	4	512KB

5. PINOUT TABLES

5.1 44 pin PLCC (Sorted Alphabetically)

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
40	ExtReq*	39	Release*	35	SCTWr*	9	TClk
25	GExtReq*	15	Reset*	3	SysCmd[3]	16	Test
27	GRdRdy*	28	SCAdS*	4	SysCmd[4]	32	Valid
20	GRelease*	29	SCAdv*	5	SysCmd[5]	42	TValidIn*
24	GValidIn*	37	SCALE	6	SysCmd[6]	41	ValidOut*
21	GValidOut*	31	SCDOE*	7	SysCmd[7]	14	VIMux
26	GWrRdy*	30	SCDWr*	8	SysCmd[8]		
38	Hit	13	SCOE*	2	TagOp0		
17	HitDly	36	SCTReset*	43	TagOp1		

VSS pins - 11, 18, 19, 22, 33, 44

VDD pins - 1, 10, 12, 23, 34

5.2 44 pin PLCC (Sorted By Pin Position)

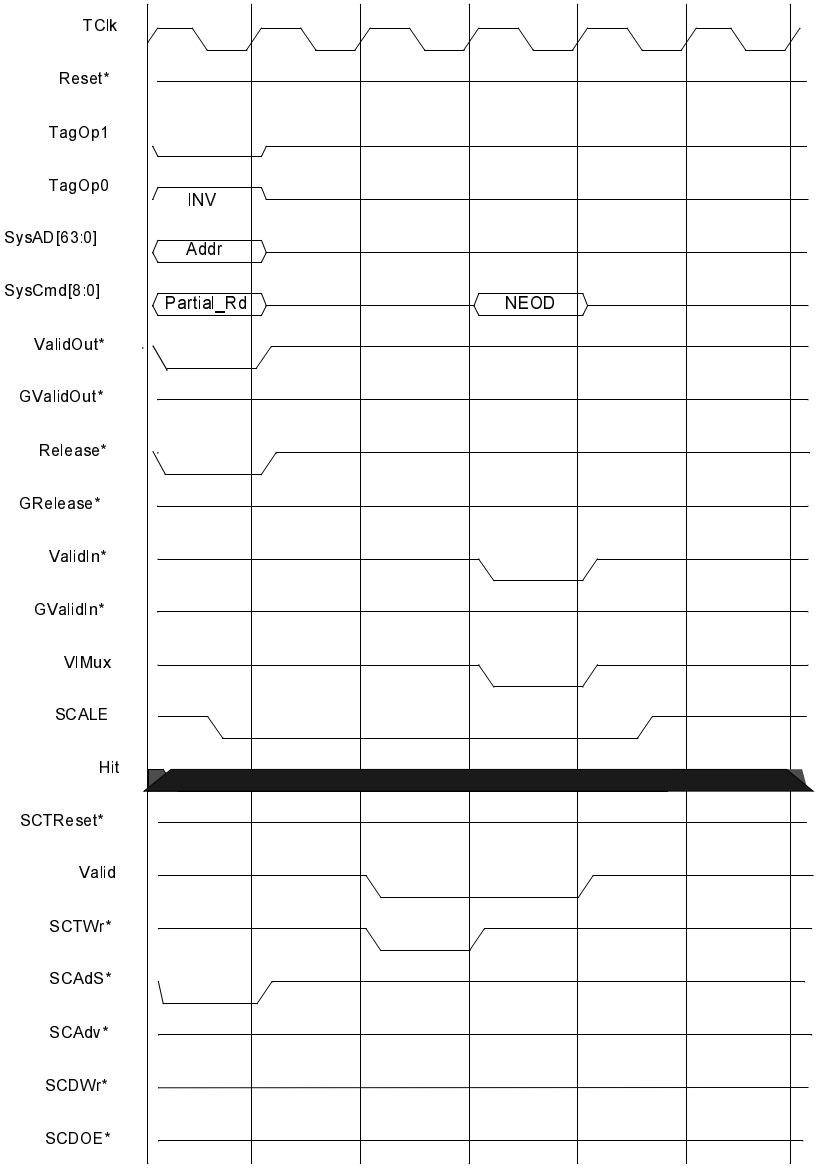
Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	VDD	12	VDD	23	VDD	34	VDD
2	TagOp0	13	SCOE*	24	GValidIn*	35	SCTWr*
3	SysCmd[3]	14	VIMux	25	GExtReq*	36	SCTReset*
4	SysCmd[4]	15	Reset*	26	GWrRdy*	37	SCALE
5	SysCmd[5]	16	Test	27	GRdRdy*	38	Hit
6	SysCmd[6]	17	HitDly	28	SCAdS*	39	Release*
7	SysCmd[7]	18	VSS	29	SCAdv*	40	ExtReq*
8	SysCmd[8]	19	VSS	30	SCDWr*	41	ValidOut*
9	TClk	20	GRelease*	31	SCDOE*	42	TValidIn*
10	VDD	21	GValidOut*	32	Valid	43	TagOp1
11	VSS	22	VSS	33	VSS	44	VSS

6. AC TIMING CHARACTERISTICS

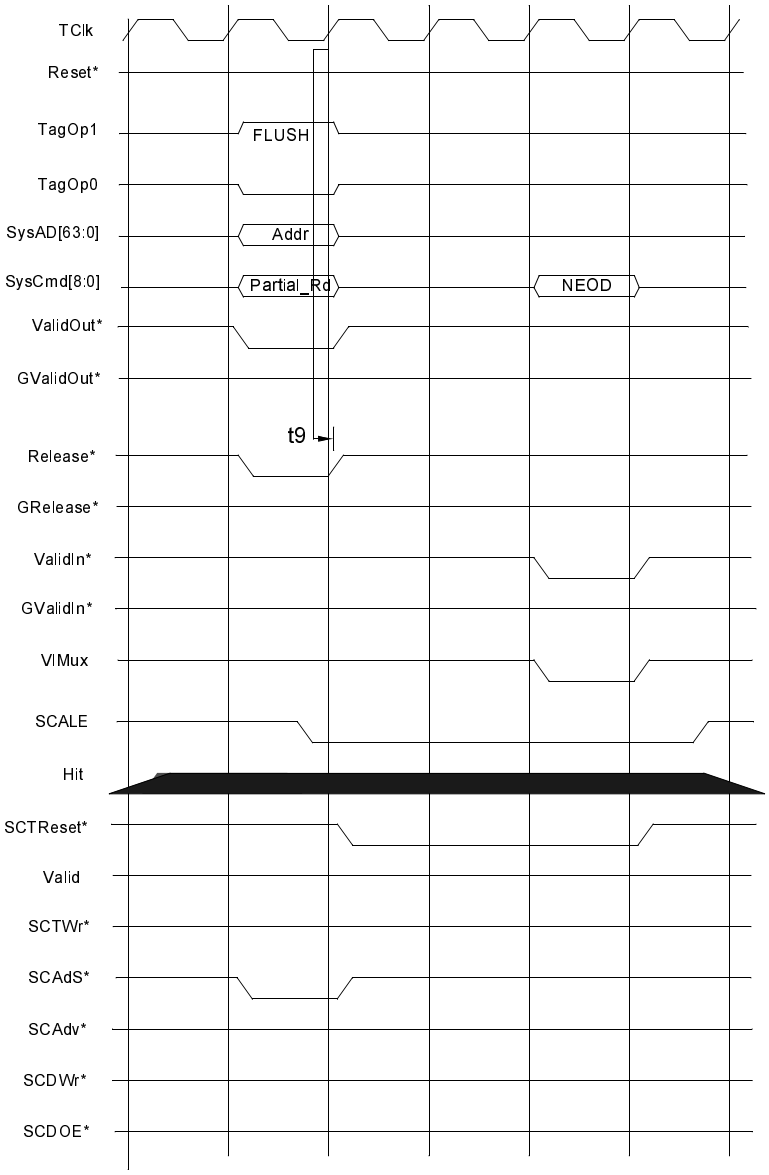
(TC= 0-70^{0}C; VDD= +5V, +/- 5%, 50 pF except where noted)

			GT-64012A		GT-64012		
Symbol	**Signals**	**Description**	**Min**	**Max**	**Min**	**Max**	**Unit**
t1	TClk	Pulse Width High	8		8		ns
t2	TClk	Pulse Width Low	8		8		ns
t3	TClk	Clock period	20		20		ns
t3a	TClk	Rise time		2		2	ns
t3b	TClk	Fall time		2		2	ns
t4a	SysCmd[8:3] System Driven	Setup to TClk	3.5		3.5		ns
t4b	SysCmd[8:3] CPU Driven	Setup to TClk	8		8		ns
t5	ValidOut*, Release*, TagOp1, TagOp0	Setup to TClk	8		8		ns
t6	Hit	Setup to TClk	7		7		ns
t7	GWrRdy*, GValidIn*, GExtReq*	Setup to TClk	4		4		ns
t8	GRdRdy*	Setup to TClk	4		4		ns
t9	SysCmd[8:3], Validout*, Release*, TagOp1, TagOp0, GExtreq*, GWrRdy*, GRdRdy*, GValidIn*, Hit	Hold from TClk	1		1		ns
t10	GRelease*	Delay from TClk	2	8	2	8.5	ns
	GValidout* [1]	Delay from TClk	2	8	2	8	
t11	SCALE	Delay from TClk falling edge	3	8	3	8	ns
t12	SCTReset*[5], SCTWr*[5], Valid[5], SCDWr*, SCAdv*	Delay from TClk	2	10	2	10	ns
t13	ExtReq*[5], SysCmd[8:6]	Delay from TClk	2	12	2	12	ns
t14	VIMux[5,6]	Delay from TClk rising edge	2	9	2	9	ns
t15	GValidOut* [2]	Delay from SysCmd[6]	2	8	2	8	ns
t16	SCAdS* [3]	Delay from ValidOut*	2	6	2	7	ns
t17	SCAdS* [4]	Delay from SysCmd[8]	2	6	2	6	ns
t20	SCOE* Rising	Delay from TClk	2	8.5	2	8.5	ns
t21	SCOE* Falling	Delay from TClk	2	6.5	2	6.5	ns
t22	SCDOE* Rising	Delay from TClk	2	9	2	9	ns
t23	SCDOE* Falling	Delay from TClk	2	8	2	8	ns
t24	ValidIn*[5,6]	Delay from TClk	2	9.5	2	9.5	ns

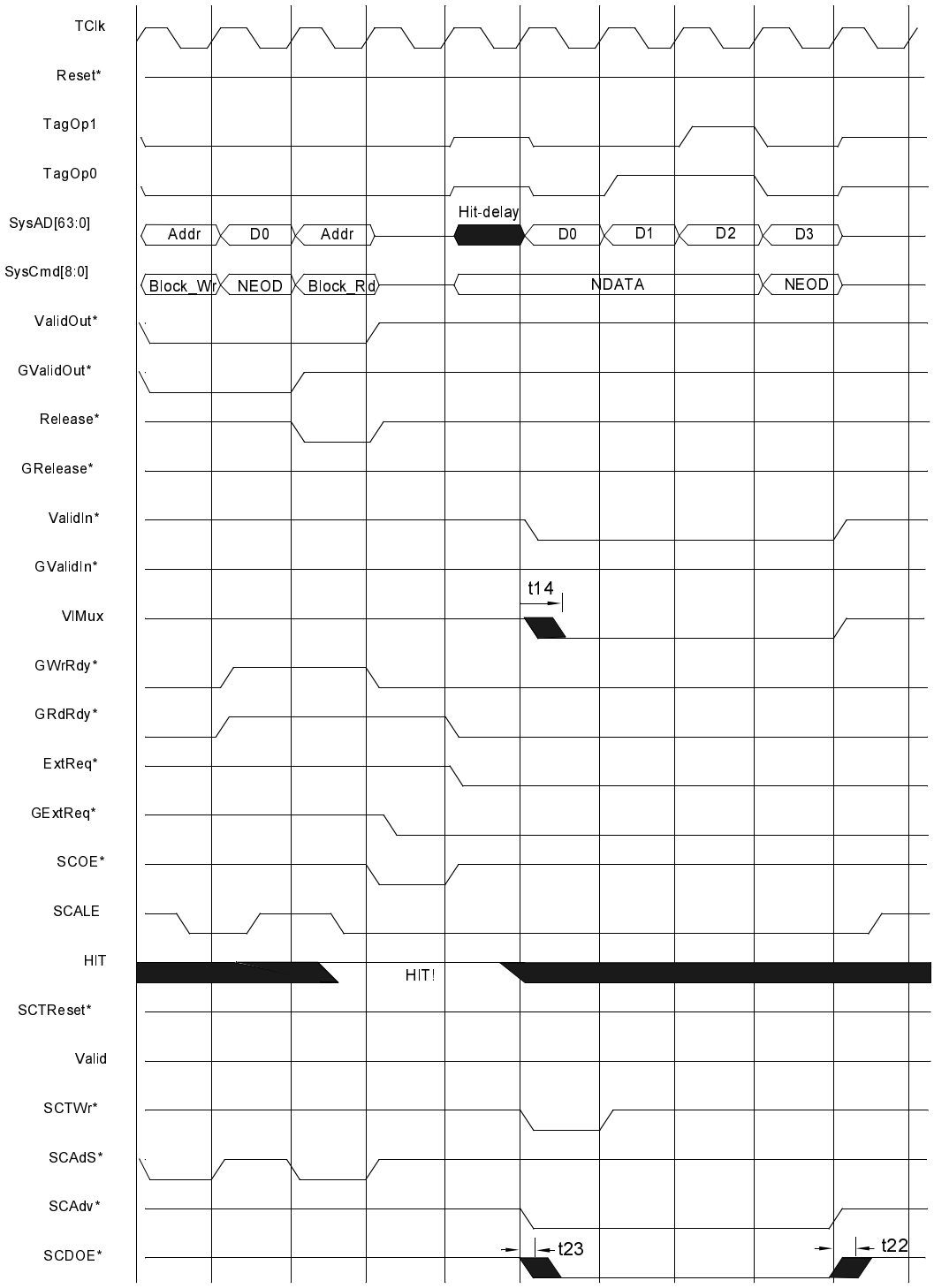
Notes:
1. Reads Only
2. Writes Only
3. Deassertion
4. Assertion
5. 20pf load for GT-64012A (Samsung)
6. 20pf load for GT-64012 (Temic)



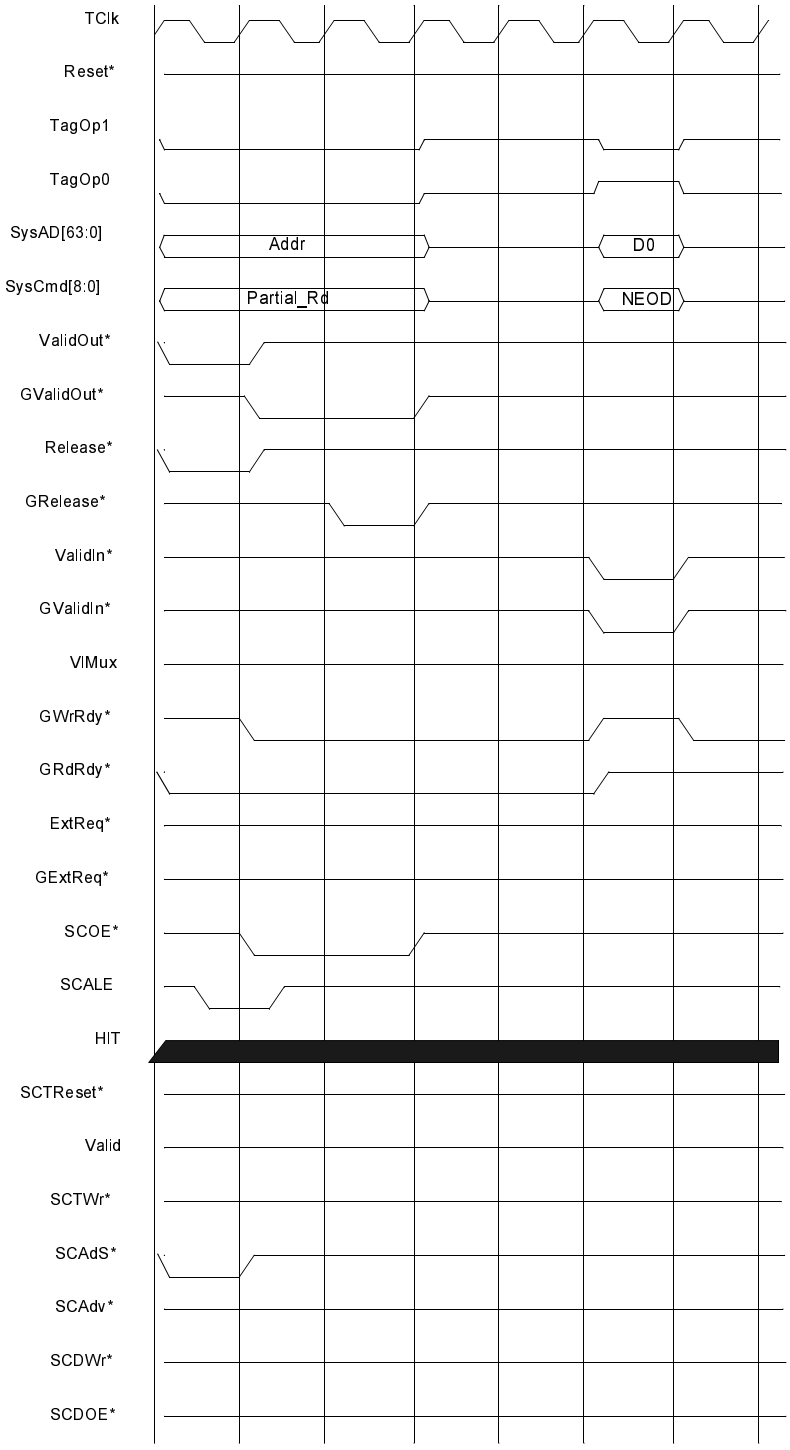
Cache Entry Invalidate


TClk
Reset*
TagOp1
FLUSH
TagOp0
SysAD[63:0]
Addr
SysCmd[8:0]
Partial_Rd
NEOD
ValidOut*
GValidOut*
t9
Release*
GRelease*
ValidIn*
GValidIn*
VlMux
SCALE
Hit
SCTReset*
Valid
SCTWr*
SCAdS*
SCAdv*
SCDWr*
SCDOE*

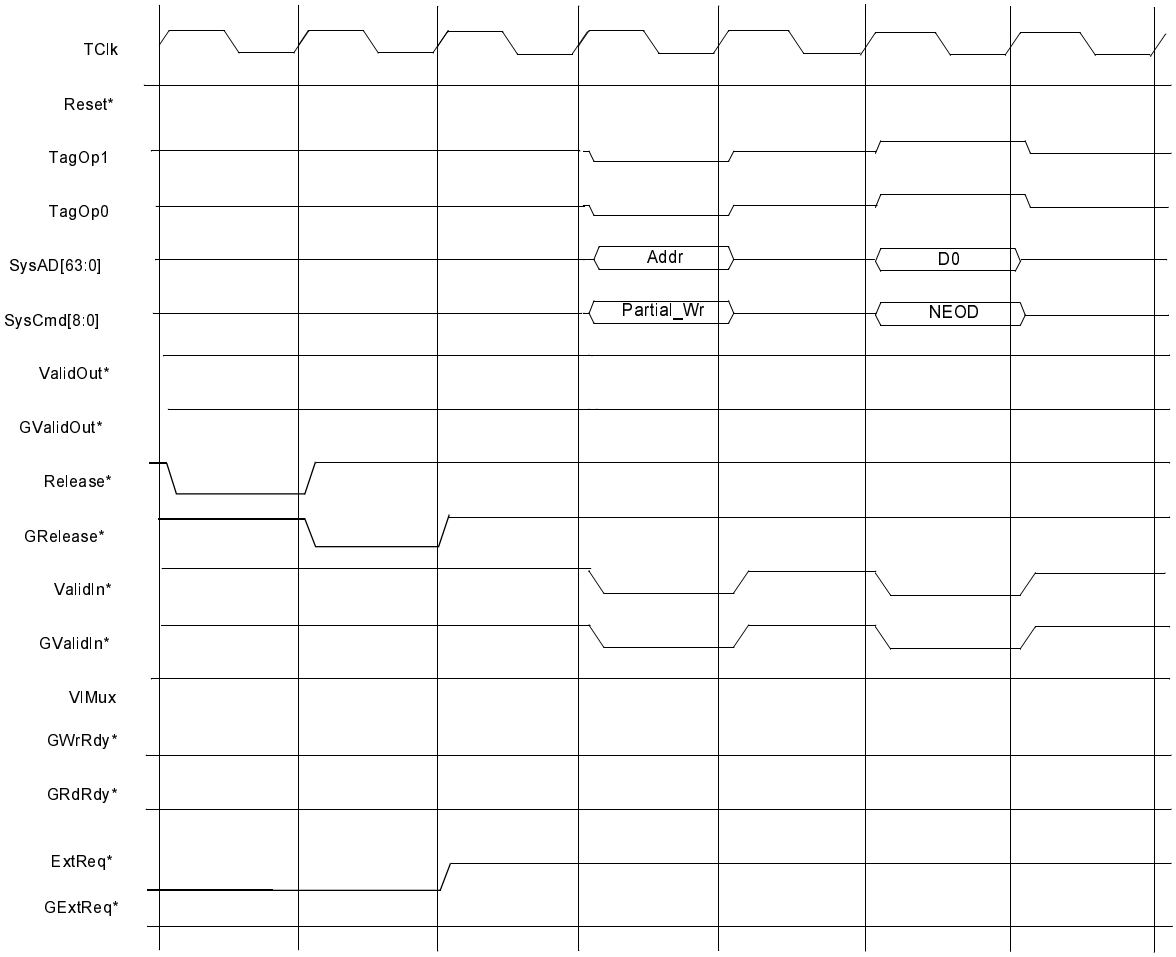
Tag Flush



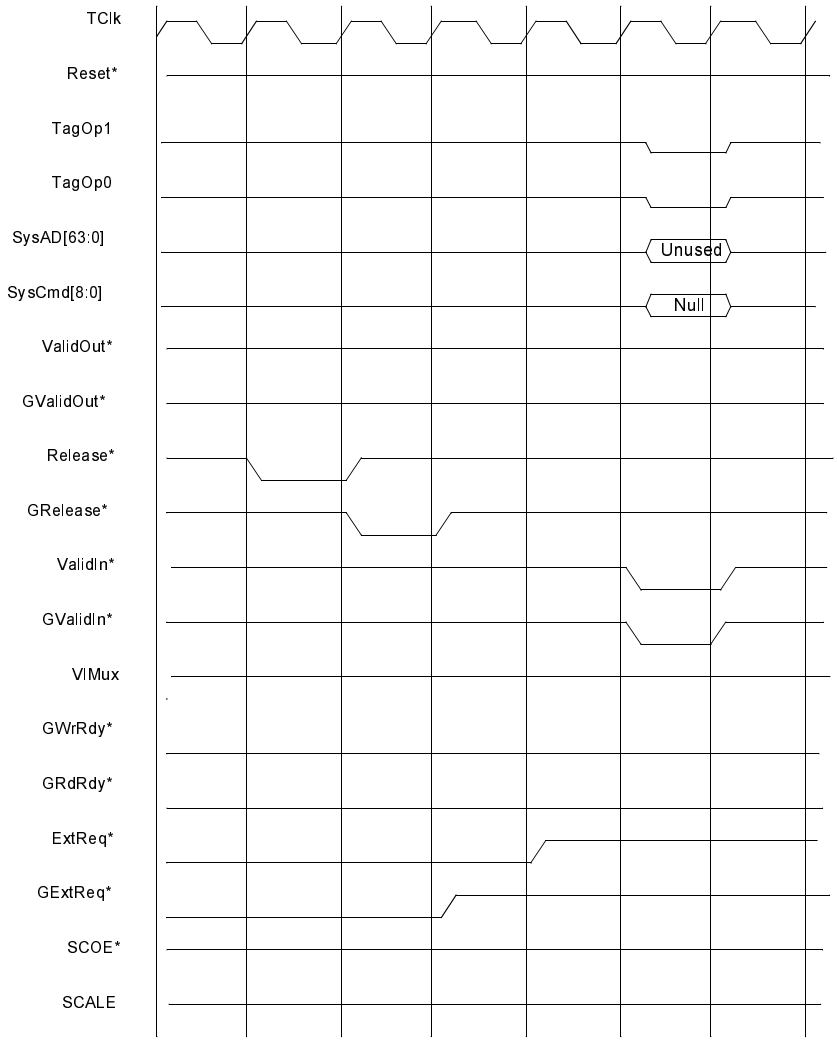
Partial Write + Block Read Hit



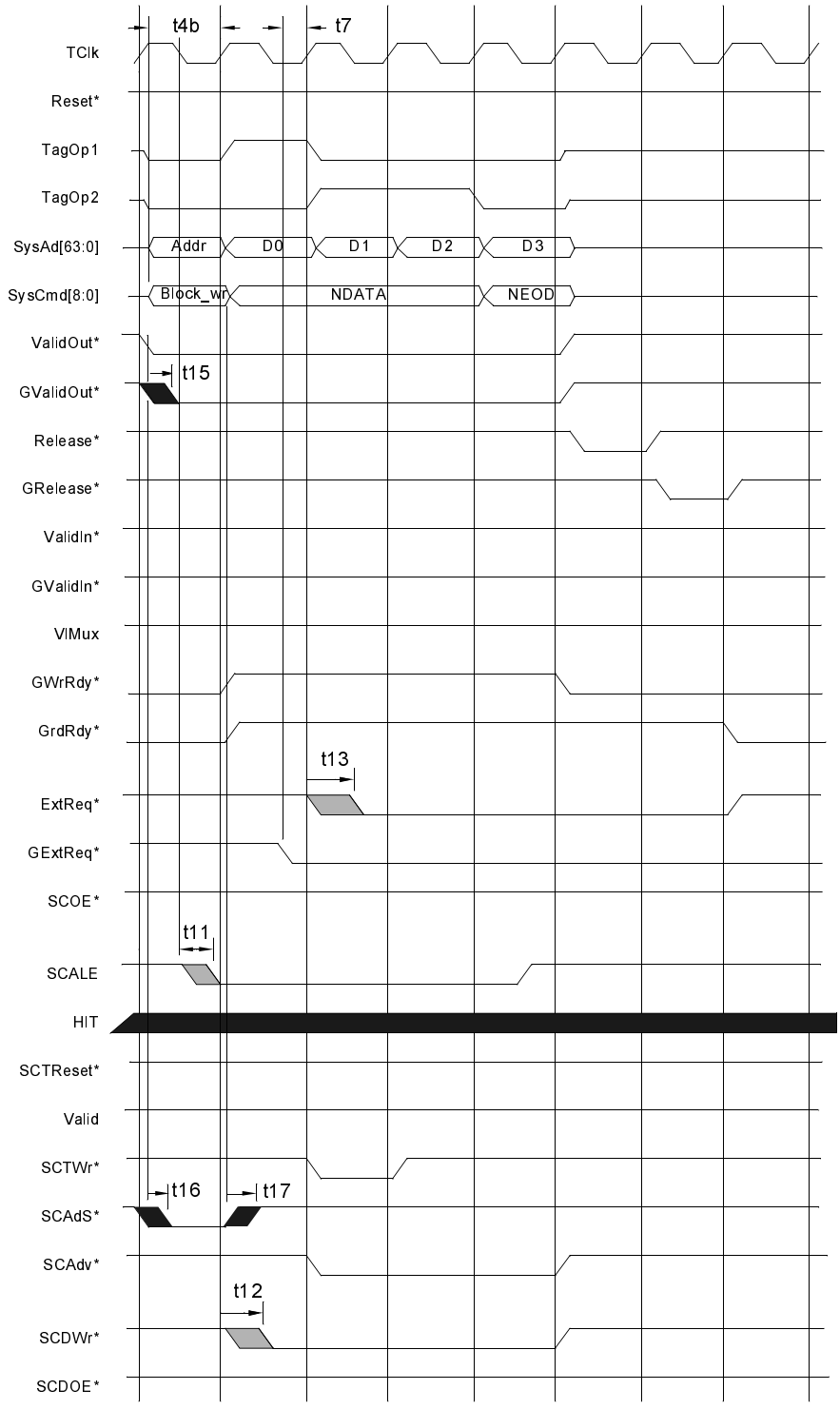
Partial Read



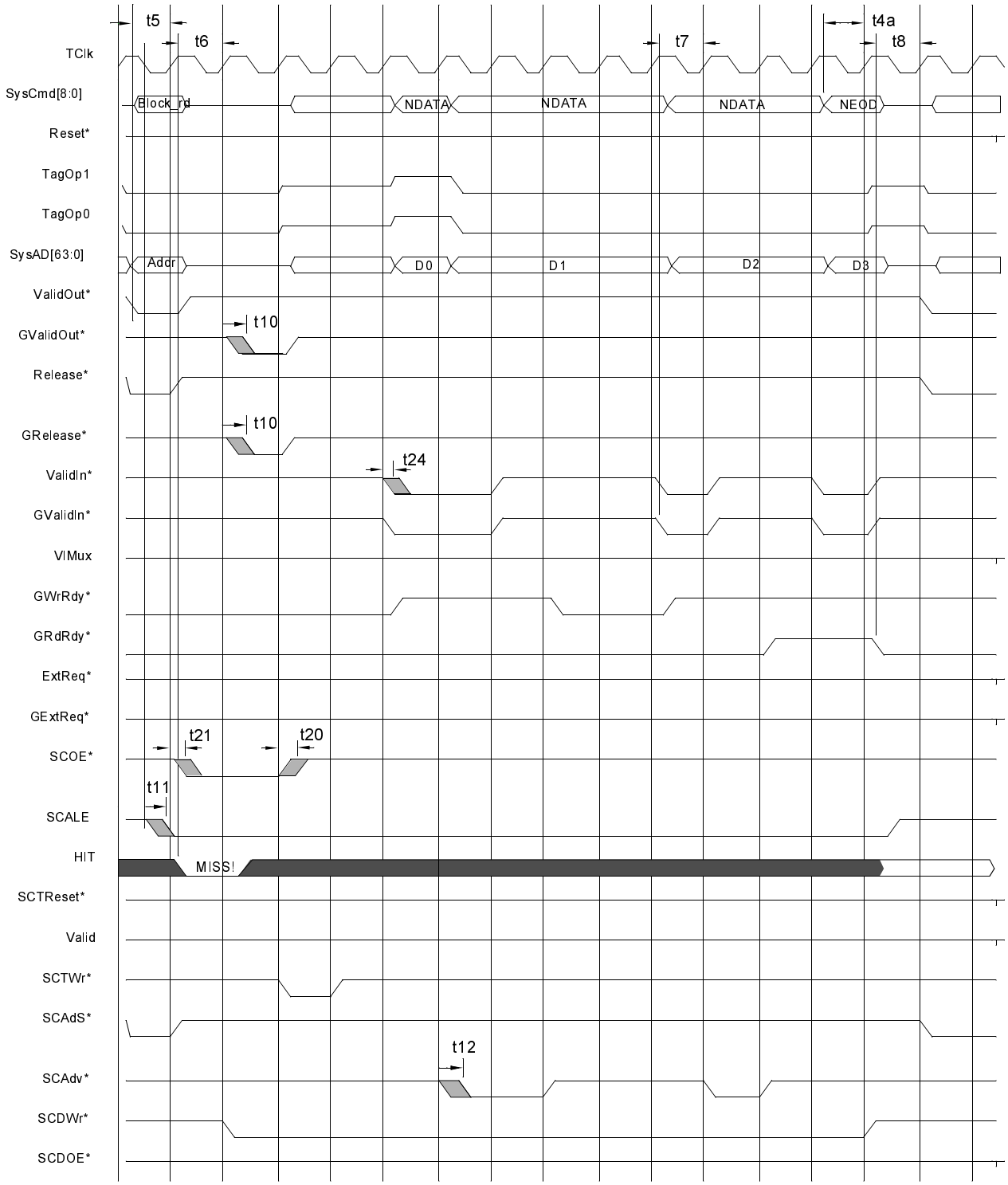
External Write



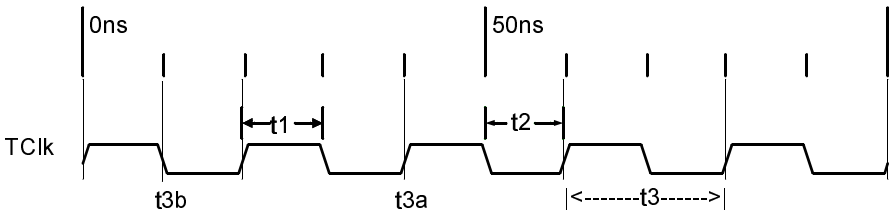
External Null


t4b
t7
TClk
Reset*
TagOp1
TagOp2
SysAd[63:0]
Addr
D0
D1
D2
D3
SysCmd[8:0]
Block_wr
NDATA
NEOD
ValidOut*
t15
GValidOut*
Release*
GRelease*
ValidIn*
GValidIn*
VlMux
GWrRdy*
GrdRdy*
t13
ExtReq*
GExtReq*
SCOE*
t11
SCALE
HIT
SCTReset*
Valid
SCTWr*
t16
t17
SCAdS*
SCAdv*
t12
SCDWr*
SCDOE*

Block Write



Block Read Miss



TClk Timing

7. DC ELECTRICAL SPECIFICATIONS

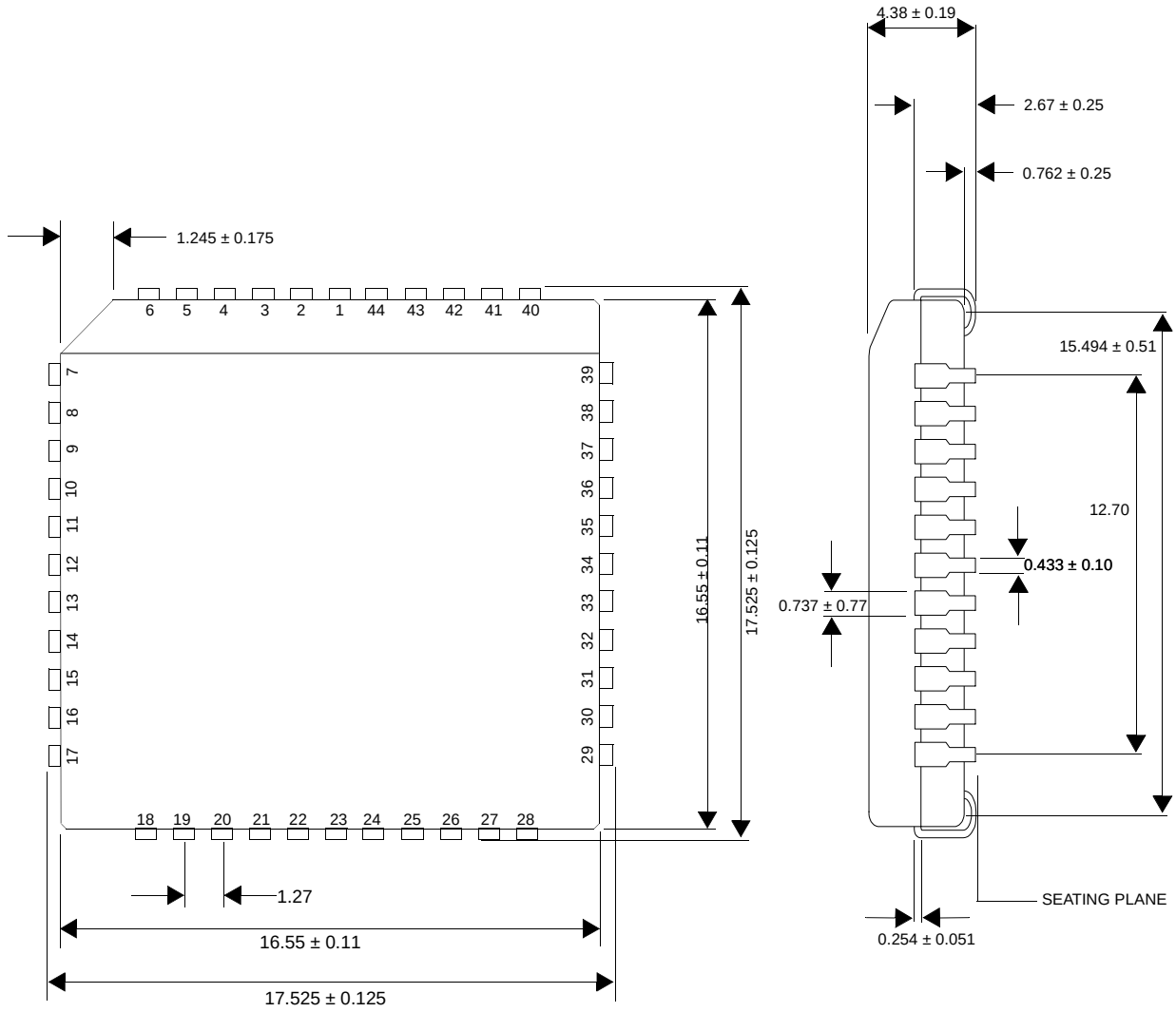
(TC= 0-70^{0}C; VDD= +5V, +/- 5%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	
VIL	Input LOW Voltage	-0.5	0.8	V	
VOH	Output HIGH Voltage	2.4		V	
VOL	Output LOW Voltage		0.4	V	
IIN	Input Leakage Current	-10	10	uA	VIN = VDD or GND
IOZ	3-State Output Leakage Current	-10	10	uA	VOUT = VDD or GND
ICC	Operating Current		100	mA	VDD = 5V, Ta=25C
CinClk	CLK Input Capacitance		7.5	pF	
Cin	Input Capacitance		5	pF	
Cout	Output Capacitance		5	pF	

6) PACKAGING

6.1 44-Pin PLCC

(all dimensions given in millimeters)



8. REVISION HISTORY

Revision History For Rev. 2 vs. Rev. 1:

Note: These are documentation revisions, the GT-64012's chip has not changed, but some AC parameters have been tightened.

1. AC Timing Characteristics have been changed, reclassified, or split as follows:

   a) The minimum values of TClk's pulse width high and pulse width low (t1 and t2) have changed from 7 to 8ns.
   b) The minimum value of SCALE (t11) has changed from 2 to 3ns.
   c) The maximum values for SCAdS* (t16 and t17) have been tightened from 8 to 6ns.
   d) SCOE* has been removed from t12, and has been given the symbols t20 and t21 for Rising and Falling values, respectively. The maximum value for SCOE* Rising (t20) has been tightened from 10 to 8.5ns. The maximum value for SCOE* Falling (t21) has been tightened from 10 to 6.5ns.
   e) SCDOE* has been removed from t12, and has been given the symbols t22 and t23 for Rising and Falling values, respectively. The maximum value for SCDOE* Rising (t22) has been tightened from 10 to 9ns. The maximum value for SCDOE* Falling (t23) has been tightened from 10 to 8ns.
   f) ValidIn* has been removed from t13 and has been given the symbol t24. The maximum value for ValidIn* has been tightened from 12 to 9.5ns.

2. Clarification has been added on the test load conditions of the AC Timing Characteristics

3. A package profile drawing has been added.

Revision History For Rev. 3 (October 1997) vs. Rev. 2:

1. GT-64012A device information added.

2. t10 for GRelease* increased from 8ns to 8.5ns for GT-64012 only.

3. t16 for SCAds* increased from 6ns to 7ns for GT-64012 only.