FM 1008/1108/1208/1308/1408 FRAM®

1,024-16,384-Bit Nonvolatile Static RAM Family

Product Preview

Features

- Nonvolatile CMOS Static RAM with >10 Year Data Retention Without Power
- Endurance Rated at $>10^{10}$ Read/Write Cycles
- Fully Synchronous Operation with Latched Address and Data
  - 100ns Maximum Read Access Time
  - 200ns Minimum Read/Write Cycle Times
- Single 5 Volt ±10% Supply with CMOS/TTL Compatible I/O
- Low Power Operation
  - 88mW Maximum Active Dissipation
  - 220µW Maximum Static Dissipation
- On-Chip Low Voltage Data Protection
- Fully Compatible and Upgradable Family in JEDEC Standard 24-Pin Packaging
  - 128 x 8
  - 256 x 8
  - 512 x 8
  - 1024 x 8
  - 2048 x 8

Description

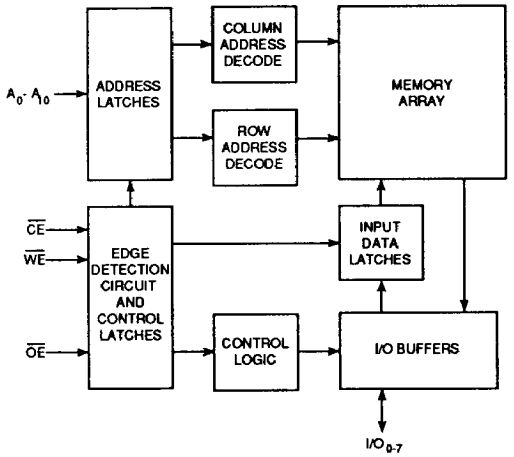
The FM 1008, 1108, 1208, 1308 and 1408 are a family of nonvolatile 128 x 8, 256 x 8, 512 x 8, 1024 x 8 and 2048 x 8 CMOS synchronous static Ferroelectronic Random Access Memories (FRAM®). Nonvolatility, the retention of data without power, is achieved by utilizing the ability of a ferroelectric material to maintain a stable polar state after removal of an applied electric field. Ramtron incorporates a proprietary lead-zirconate-titanate (PZT) ceramic thin film to fabricate the nonvolatile bistable ferroelectronic storage cells used in all its FRAM products.

The FRAM memory functions as a conventional CMOS synchronous static RAM with the sole exception that upon a loss of power, data is retained virtually indefinitely. No store or recall cycles are required since the ferroelectric storage cells are updated on each access cycle with a minimum endurance of 10^{10} read/write cycles before a bit failure.

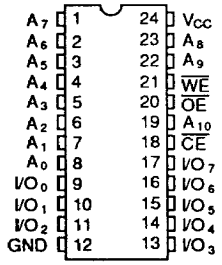
The memories are intended for application in a broad range of commercial, industrial, aerospace and defense systems, wherein a limited amount of writeable, nonvolatile memory is required and the performance limitations of EEPROM technology, magnetics or battery back-up of volatile memory are not acceptable.

The memories operate from a single 5 volt supply with ±10% tolerance and are TTL/CMOS compatible at all inputs and outputs. An on-chip data protection circuit disables the memory operation when V_{CC} is below +3.0 volts. Operation is fully synchronous with all operations initiated by a high-to-low transition at the $\overline{CE}$ input. Read and write cycles are symmetrical at 200ns minimum with a maximum read access time of 100ns. Power dissipation is very low since no power is consumed to retain data other than the normal leakage currents of the CMOS circuitry. The memories utilize JEDEC approved byte-wide pinouts and are offered in industry standard 24-pin DIP packaging as well as 24-pin SOP packaging.

Functional Diagram



Pin Configuration



This document contains information on a product under development. Ramtron reserves the right to change or discontinue this product without notice.

Pin Assignments

Part	Organization	Pin 1	Pin 23	Pin 22	Pin 19
FMx 1008	128 x 8	NC	NC	NC	NC
FMx 1108	256 x 8	A_7	NC	NC	NC
FMx 1208	512 x 8	A_7	A_8	NC	NC
FMx 1308	1024 x 8	A_7	A_8	A_9	NC
FMx 1408	2048 x 8	A_7	A_8	A_9	A_{10}

Pin Names

Pin Names	Function
A_0 - A_{10}	Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	+5 Volts
GND	Ground
NC	No Connect

Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	0 to +70°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V

AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	0 to 3V
Input Rise and Fall Time	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF

E.S.D. Characteristics

Symbol	Parameter	Value
V_{ZAP} (1)	E.S.D. Tolerance	> 2,000 Volts

(1) Characterized to MIL-STD-883 test method 3015. Not tested.

DC Operating Conditions

T_A = 0° to 70°C, V_{CC} = 5V ± 10% Unless Otherwise Noted

Symbol	Parameters	Min	Max	Test Condition
I_{CC}	Power Supply Current — Standby		40µA	$\overline{CE}$ High, All Inputs Stable at V_{CC} or V_{SS} , $I_{I/O}$ = 0mA
I_{CC}	Power Supply Current — Active		16mA	V_{CC} = Max, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{IL}	Input Load Current		10µA	V_{IN} = GND to V_{CC}
I_{OL}	Output Leakage Current		10µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	-1V	0.8V	
V_{IH}	Input High Voltage	2.0V	V_{CC} +1V	
V_{OL}	Output Low Voltage		0.4V	I_{OL} = 4.2mA
V_{OH}	Output High Voltage	2.4V		I_{OH} = -2mA

Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Mode
H	X	X	Output High-Z	Non-Selected
L	L	L	Output Data	Read
L	H	L	Output Data	Read
L	L	H	Input Data	Write
L	H	H	Output High-Z	Tri-State

Capacitance

T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Parameter	Description	Max	Test Condition
$C_{I/O}$ (1)	Input/Output Capacitance	8pF	$V_{I/O}$ = 0V
C_{IN} (1)	Input Capacitance	6pF	$V_{I/O}$ = 0V

(1) This Parameter is periodically sampled and not 100% tested.

Theory of Operation

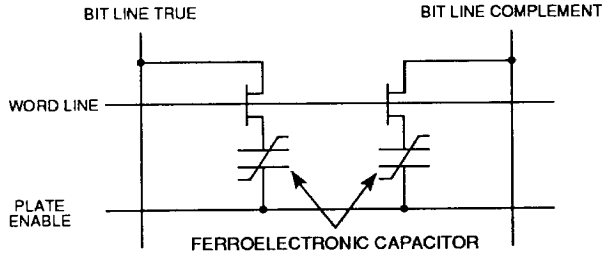
The FM 1008, 1108, 1208, 1308 and 1408 FRAM memories use a two transistor, two capacitor memory cell structure illustrated below.

During a write operation, data is transferred from the I/O pins to the bit lines (true and complement). When the word line pass transistor is enabled, the data at the selected address is applied to the ferroelectronic capacitor. The plate enable signal is pulsed to polarize the data in one of the two stable states of the ferroelectric material. The information stored in the polarized capacitor is retained until the next memory reference to this cell without refreshing or maintaining the power supply. Therefore, the FRAM acts as a nonvolatile static RAM.

To read the memory, the selected memory cell address pass transistors connect the ferroelectronic capacitor to the bit lines. The memory sense amplifier differentially senses the difference in charge between polarized and unpolarized cells to detect the data value. The data value is transferred to the I/O buffer. Since the memory reference is destructive, the data is automatically restored to the cell by re-polarizing the capacitors.

The amount of polarization energy stored by the capacitor decreases as a function of the number of polarization cycles. After a minimum of 10^{10} cycles, the energy level can no longer be reliably detected and the memory bit can fail. It is important that the read and write statistics of the memory application be understood so that a memory bit failure does not occur during the normal lifetime of the system.

Dual Memory Capacitor Cell



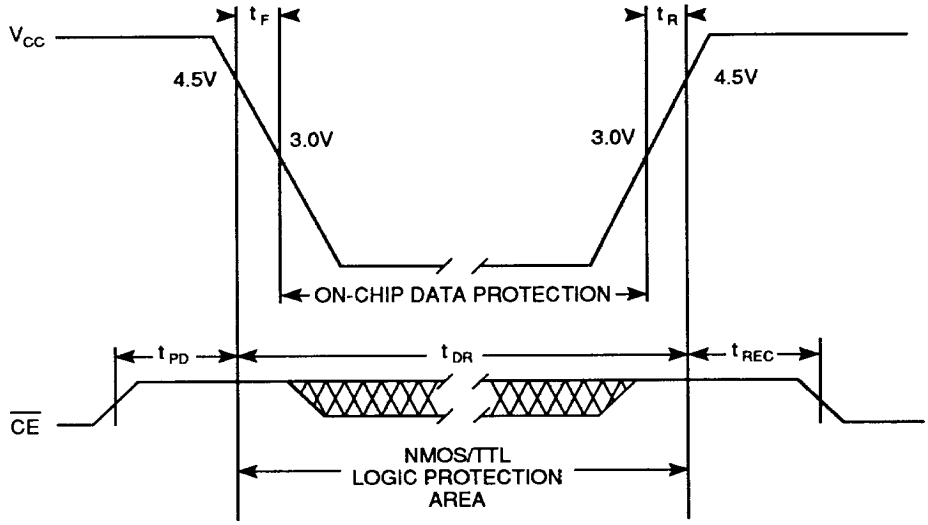
Power-Down/Power-Up Conditions

The memory stores data in its nonvolatile ferroelectronic memory cells during normal operation. Therefore, no special store or recall operations are required. Care must be taken during power sequencing to prevent data loss resulting from memory operations during out of spec voltage conditions. This is managed by detecting power failure with sufficient time to disable memory operation time t_{PD} prior to V_{CC} reaching its lower specification, +4.5 volts. During power-up, the memory operation should be disabled until time t_{REC} after V_{CC} reaches its operating voltage, +4.5 volts.

The memory has an on-chip data protection circuit which prevents memory operation when V_{CC} is less than +3.0 volts. This will protect the data in CMOS systems where the system control logic continues to function to +3.0 volts. However, external circuitry is required in systems with NMOS or TTL control logic to force $\overline{CE}$ to a high level between V_{CC} = +4.5 - +3.0 volts to prevent false memory operations from being initiated by the system control logic during this unspecified voltage range. There are a number of precision DC voltage detector circuits available to implement this function.

Times t_F and t_R are the typical rise and fall times used during memory retention testing. Time t_{DR} is the data retention time of the nonvolatile memory. The memory will retain its information during power losses of this duration. Data retention time is periodically sampled during production but is not tested on each part.

Power-Down/Power-Up Conditions



Power-Down/Power-Up AC Parameters [1]

Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
		-100		-150		-200		
t_{PD}	Chip Enable Stable to Power-Down	100		150		200		ns
t_{REC}	Power-Up to Chip Enable	100		150		200		ns
t_F	Power Supply Fall Time (+4.5 to 3.0 Volts)	10		10		10		µs
t_R	Power Supply Rise Time (3.0 to +4.5 Volts)	10		10		10		µs

For test purposes t_F and t_R (power supply slew rate) = 200µs/V

(1) These parameters are guaranteed by design and are not 100% tested.

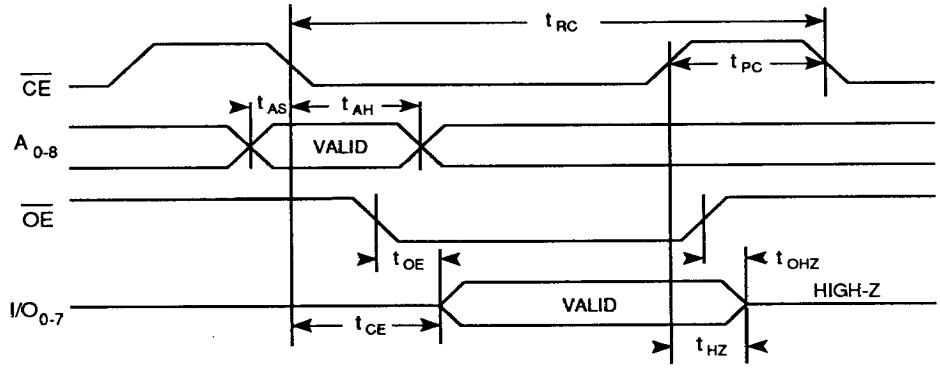
Read Cycle Operation

The memory operates synchronously using the $\overline{CE}$ signal as the clock. The memory read cycle time t_{RC} is measured between falling edges of $\overline{CE}$. The memory requires a minimum precharge time t_{PC} to precharge the internal busses between operations.

The memory latches the address internally on the falling edge of $\overline{CE}$. The address data must meet a minimum setup time t_{AS} and hold time t_{AH} relative to a clock edge. Read data is valid a maximum access time t_{CE} after the beginning of the read cycle. The $\overline{OE}$ signal is used to gate the data to the I/O pins. It must be enabled time t_{OE} prior to the time data is required on the I/O pins. Output data remains valid on the outputs until disabled by either the rising edge of $\overline{OE}$ or $\overline{CE}$. The output becomes high-Z after time t_{HZ} from the $\overline{CE}$ signal and time t_{OHZ} from the $\overline{OE}$ signal. The $\overline{WE}$ signal is high during the entire read operation.

Read Cycle Timing

$\overline{WE} = V_{IH}$



Read Cycle AC Parameters

T_A = 0° to 70°C, V_{CC} = 5V ± 10% Unless Otherwise Noted

Symbol	Parameter	JEDEC Symbol	Min	Max	Min	Max	Min	Max
			-100		-150		-200	
t_{RC}	Read Cycle Time	t_{ELEL}	200		300		400	
t_{PC}	Precharge Time	t_{EHEL}	100		150		200	
t_{AS}	Address Setup Time	t_{AVEL}	0		0		0	
t_{AH}	Address Hold Time	t_{ELAX}	20		30		40	
t_{CE}	Chip Enable Access Time	t_{ELQV}		100		150		200
t_{OE}	Output Enable Access Time	t_{OLQV}	20		30		40	
t_{HZ}	Chip Enable to Output High-Z	t_{EHQZ}	20		30			40
t_{OHZ}	Output Enable to Output High-Z	t_{OHQZ}	20		30			40

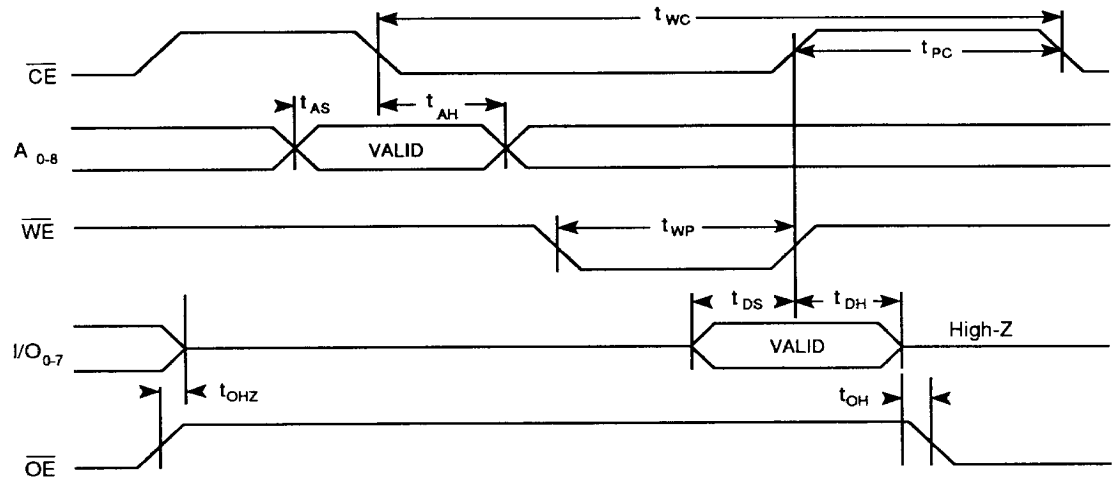
Write Cycle Operation

The memory operates synchronously using the $\overline{CE}$ signal as a clock. The memory write cycle time t_{WC} is measured between falling edges of $\overline{CE}$. The memory requires a minimum precharge time t_{PC} to precharge the internal busses between operations.

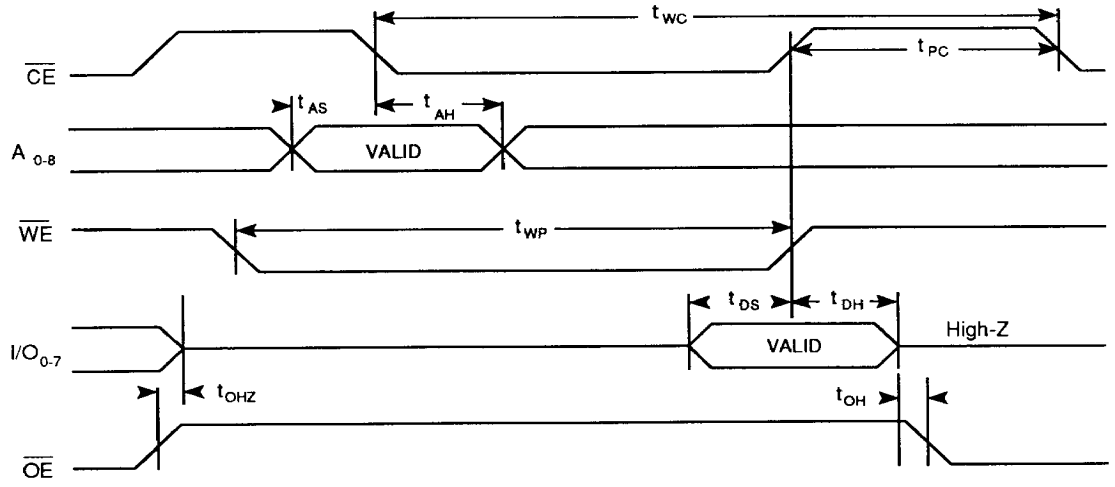
The memory latches the addresses internally on the falling edge of $\overline{CE}$. The address data must meet a minimum setup time t_{AS} and hold time t_{AH} relative to the clock edge.

The data must be valid on the I/O pins time t_{DS} prior to the rising edge of $\overline{WE}$ and held time t_{DH} after $\overline{WE}$. $\overline{WE}$ must be stable time t_{WP} prior to the rising edge of $\overline{CE}$. The $\overline{OE}$ signal must disable the chip outputs time t_{OHZ} prior to placing data on the I/O pins to prevent a data conflict. $\overline{OE}$ must remain disabled until time t_{OH} after the data is removed from the bus.

$\overline{WE}$ Controlled Write Timing



$\overline{CE}$ Controlled Write Timing



Write Cycle AC Parameters

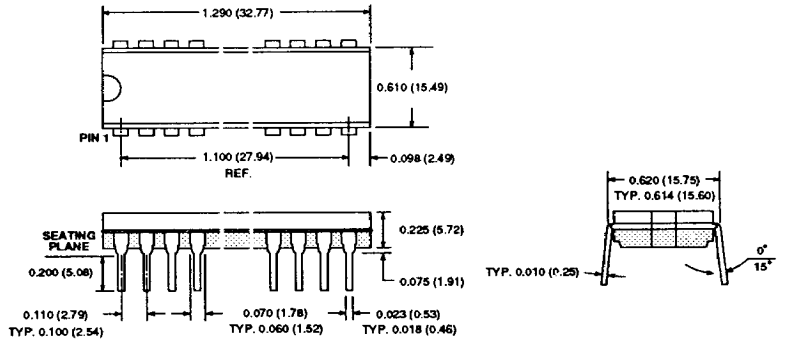
T_A = 0° to 70°C, V_{CC} = 5V ± 10% Unless Otherwise Noted

Symbol	Parameter	JEDEC Symbol	Min	Max	Min	Max	Min	Max
			-100		-150		-200	
t_{WC}	Write Cycle Time	t_{ELEL}	200		300		400	
t_{PC}	Precharge Time	t_{EHEL}	100		150		200	
t_{AS}	Address Setup Time	t_{AVEL}	0		0		0	
t_{AH}	Address Hold Time	t_{ELAX}	20		30		40	
t_{WP}	Write Pulse Width	t_{WLWH}	100		150		200	
t_{DS}	Data Setup Time	t_{DVWH}	0		0		0	
t_{DH}	Data Hold Time	t_{WHDX}		20		30		40
t_{OHZ}	Output Enable to Output High-Z	t_{OHQZ}		20		30		40
t_{OH}	Output Enable Hold Time	N/A	0		0		0	

Packaging Information

Maximum dimensions in inches. Metric dimensions in millimeter shown in parenthesis.

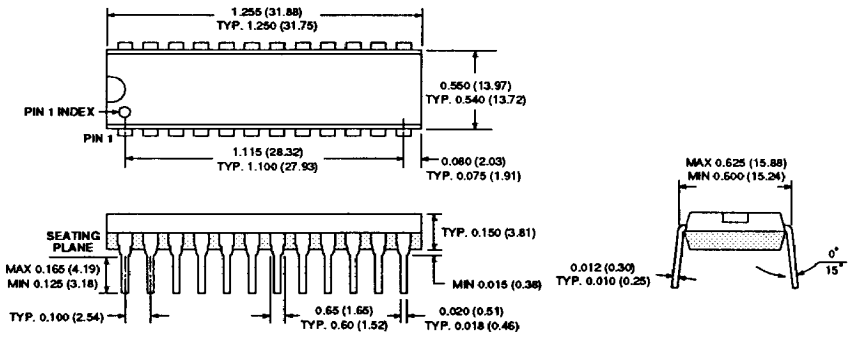
24 Lead Ceramic Dual In-Line Package Type D



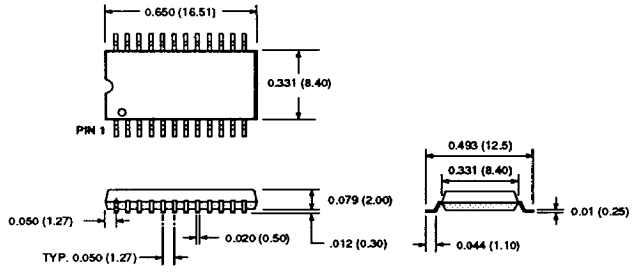
Packaging Information

Maximum dimensions in inches. Metric dimensions in millimeter shown in parenthesis.

24 Lead Plastic Dual In-Line Package Type P



24 Lead Plastic Small Outline Package Type S



Ordering Information

FMx 1408 - 200 D C

Commercial Temperature Range (0-70°C)

Package Type
- D - CerDip (24-Pin)
- P - Plastic Dip (24-Pin)
- S - Plastic Small Outline Package (24-Pin)

Access Time (ns)
- 100
- 150
- 200

Memory Configuration
- 1008 - 128 x 8
- 1108 - 256 x 8
- 1208 - 512 x 8
- 1308 - 1024 x 8
- 1408 - 2048 x 8

Ramtron Ferroelectronic Memory

015108