Features

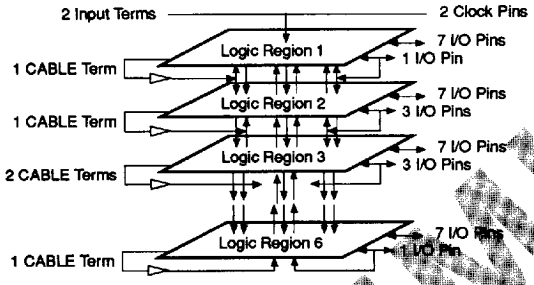
- High Through-Put Programmable Logic Device
- High Speed - 83.3 MHz System Clock Rate Operation
- Low Power - 0.5 mA Typical (ATH3000L)
- Flexible Interconnect Architecture - Universal Routing
- 56 Logic Cells - 56 Flip-Flops - 56 I/O Pins
- Multiple Flip-Flop Types - Synchronous or Asynchronous Registers
- Complete Third Party Software Support
  - No Placement, Routing or Layout Software Required
- Proven and Reliable High Speed CMOS EPROM Process
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Reprogrammable - Tested 100% for Programmability
- Commercial, Industrial and Military Temperature Grades

High Throughput UV Erasable Programmable Logic Device

Preliminary

7

Block Diagram



Description

The Atmel ATH3000/L is an easy to use, high through-put programmable logic device. Its simple, regular architecture translates into increased utilization and high performance.

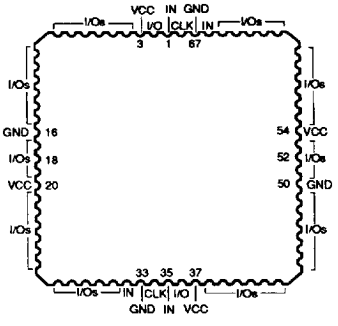
The Atmel ATH3000/L has one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. Sum terms, which are easy-to-use blocks of gates, provide combinatorial AND-OR logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. To expand the levels of logic, buried sum terms feed back into the logic array. A register or a sum term can drive each of the 56 I/O pins.

All 56 registers are configurable as D- or T-types without using extra logic gates. Individual sum terms and clocks give each flip-flop added flexibility. A direct "clock from pin" option guarantees synchronization and fast clock to output performance.

Standard off-the-shelf third party software tools and programmers support the ATH3000/L. This minimizes startup investment and improves product support.

Chip Carrier Pin Configuration

Pin Name	Function
IN	Logic Inputs
Clk	Register Clocks 1,2
I/O	Bidirectional Buffers
VCC	+5 V Supply



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Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V[1]
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V[1]
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Range

		ATH3000-15	ATH3000/L-20	ATH3000/L-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} =- 0.1 V to V_{CC}+0.1 V				10	µA
I_{CC}	Power Supply Current ATH3000	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		150	225	mA
			Ind.,Mil.		150	270	mA
I_{CC}	Power Supply Current ATH3000L	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		0.5	5	mA
			Ind.,Mil.		0.5	10	mA
I_{CC2}	Clocked Power Supply Current, ATH3000L Only	f = 1 MHz, V_{CC} = MAX Outputs Open	Com.		10	15	mA
			Ind.,Mil.		10	20	mA
I_{OS} [1]	Output Short Circuit Current	V_{OUT} = 0.5 V		-10		-90	mA
V_{IL}	Input Low Voltage			-0.6		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH}/V_{IL}, I_{OL} = 12 mA Com,Ind; 8 mA Mil.				0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3			V
		I_{OH} = -4.0 mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 seconds.

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Functional Logic Diagram Description

There are 56 identical Input/Ouput logic cells in the ATH3000. Each I/O cell has one flip-flop, six product terms divided into two sum terms, a clock term and one output enable term.

Each logic cell drives one signal (56 total) into the logic array. This signal can come from the pin, the flip-flop or the sum term. Each signal is either regional or universal.

The ATH3000/L has six regions. The Universal Bus routes signals to all six regions. It contains six Complement Array Buried Logic Extender (CABLE) terms, the true and false signals from ten universal I/O pins and the true and false signals from the two input-only pins. Regional buses route regional true and false signals.

Each I/O Logic Cell contains two sum terms, one flip-flop, a feedback buffer and an I/O buffer. Output enable and clock options have one product term each per I/O Cell.

The ATH3000/L has six CABLE terms. These terms provide wide-input NAND gate structures or universal routing.

Register preload simplifies testing. All registers automatically clear at power up.

ATH3000/L Block Diagram

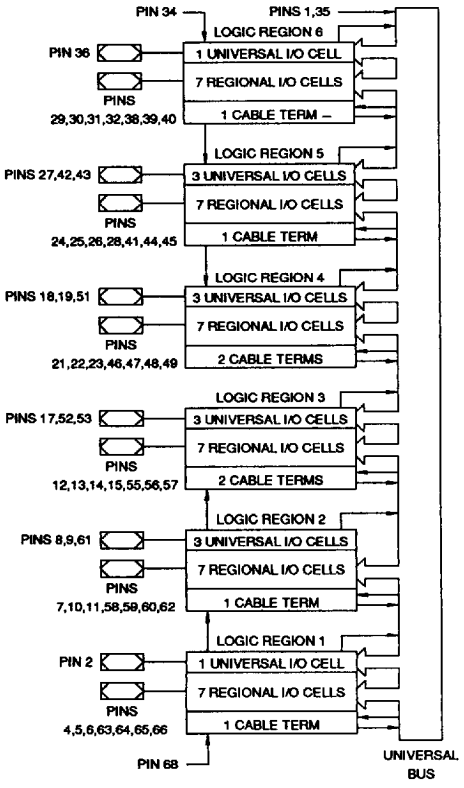

Figure 2

Functional Logic Diagram, ATH3000/L Logic Region

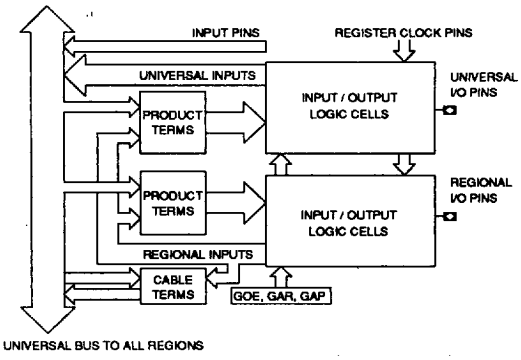

Figure 1

Logic Region Description

The ATH3000/L has six regions containing a total of 56 identical input/output logic cells (figure 2). The Universal Bus routes signals from ten universal I/O logic cells, Pins 1 and 35, and the CABLE terms. Regional buses route the remaining regional I/O logic cell signals.

CABLE Terms

CABLE terms in each ATH3000/L logic block provide a wide-input NAND function. This function is useful for logic expansion and for universal routing. CABLE terms route any signal or product of signals into the universal bus. Universal bus signals are available to every logic cell in the ATH3000/L.

CABLE terms provide two functions: 1) the ability to collect common logical expressions into one gate, and 2) the ability to route this signal to the entire chip. CABLE terms are useful for routing regional signals to the universal bus for use elsewhere.

CABLE Term Schematic

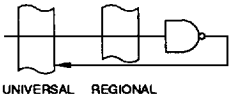

Figure 3

Group Resource Assignments

Regions I/O Pins	1,2,3 2-17	1,2,3 52-66	4,5,6 18-32	4,5,6 36-51
Register Clock Pin	68	68	34	34
Group OE Term	1	4	2	3
Group AR Term	1	4	2	3
Group AP Term	1	4	2	3

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Logic Cell Options

The ATH3000/L logic cells contain most of the chip's logic options. The block diagram in figure 4 shows the eight product terms, one array input buffer and an I/O buffer. Figures 6, 7 and 8 show the product term groupings. Each logic cell also contains one flip-flop, two sum terms, and clock and OE options. Combining the two sum terms provides three to six product terms. Combining neighboring sum terms provides up to 12 product terms in a single sum term.

The I/O buffer outputs the combinatorial input or registered output of Q1. The array input buffer transmits Q1, the pin or the 'E' node to the array. The flip-flop stores B, E or the pin input.

The clock and OE options each have one product term. Each of four group OE terms is OR'ed with blocks of 14 I/O logic cells. Group AR and AP terms each feed one-quarter of all flip-flops.

Logic Region Structure

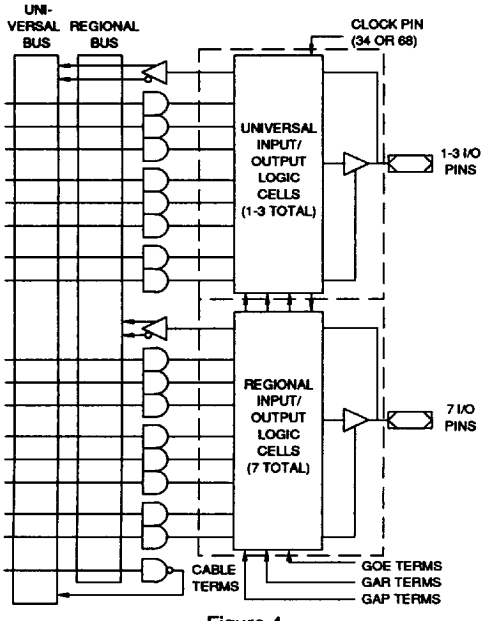

Figure 4

Clock Option

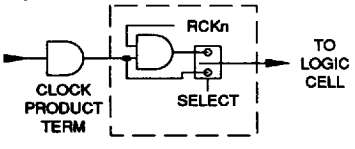

Figure 5

Node Feedbacks

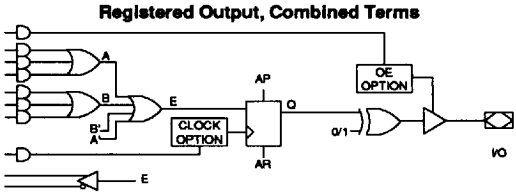

Figure 6a

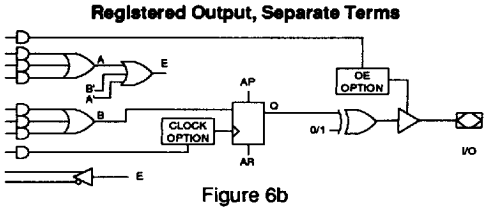

Figure 6b

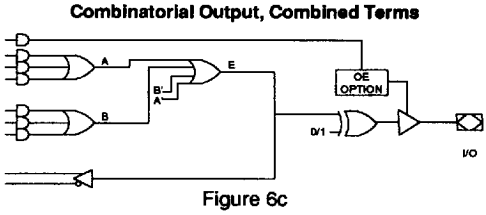

Figure 6c

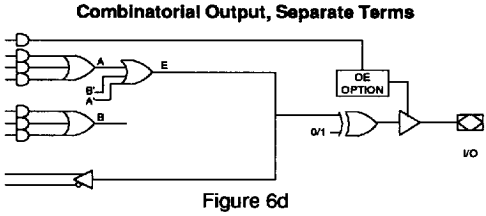

Figure 6d

Flip-Flop Clock Options

Each register can be connected to a clock pin to provide fast clock to output timing (see Figure 5). In this "synchronous" mode, the clock is one of two input pins, a unique clock pin for each chip half. One product term defines each flip-flop's clock in the "asynchronous" mode.

In the "synchronous" mode, the register clock pin is ANDed with the product term. This provides the fast timing of a synchronous clock with the local control of the product term.

Flip-Flop Types

Each flip-flop in the ATH3000/L may be configured as either a T- or D-type flip-flop. A T-type flip-flop can also easily be configured into a JK or SR flip-flop.

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Register Feedbacks

Register Output, Combined Terms

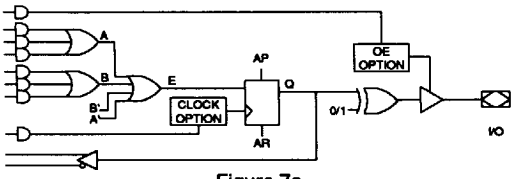

Figure 7a

Register Output, Separate Terms

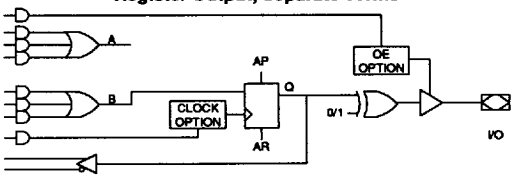

Figure 7b

Combinatorial Output, Combined Terms

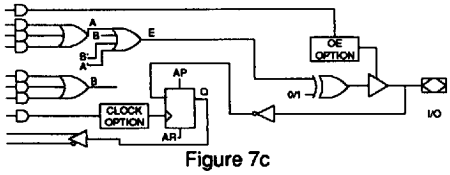

Figure 7c

Combinatorial Output, Separate Terms

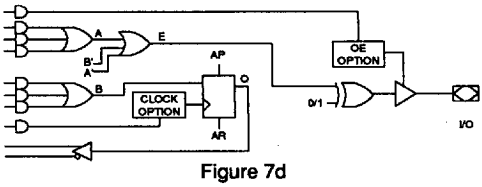

Figure 7d

Pin Feedbacks

Register Output, Combined Terms

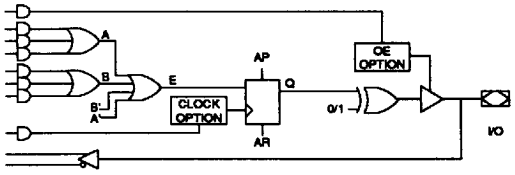

Figure 8a

Register Output, Separate Terms

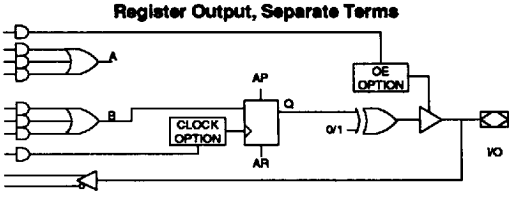

Figure 8b

Combinatorial Output, Combined Terms

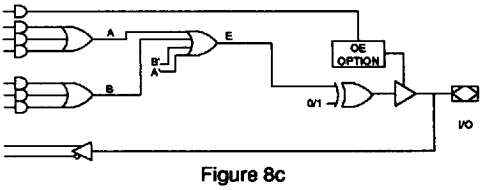

Figure 8c

Combinatorial Output, Separate Terms

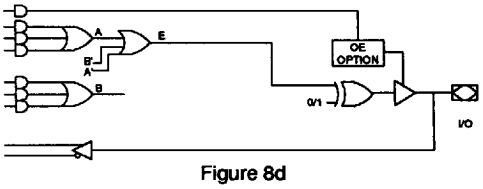

Figure 8d

Output Enable Options

Each output of the ATH3000/L functions as a bidirectional buffer. The OE option in each I/O logic cell controls the signal direction. In the default condition, the output driver is controlled by the product term in each I/O cell (OEPT). When selected, the output control is the logical OR of the product term and a product term from each quadrant of the chip (GOE). I/O pins 2-17 in regions 1, 2, and 3 use group OE term 1. I/O pins 52-66 in regions 1, 2, and 3 use group OE term 4. I/O pins 18-32 in regions 4, 5, and 6 use group OE term 2. I/O pins 36-51 in regions 4, 5, and 6 use group OE term 3.

OE Option

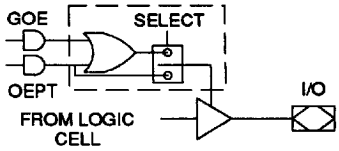

Figure 9

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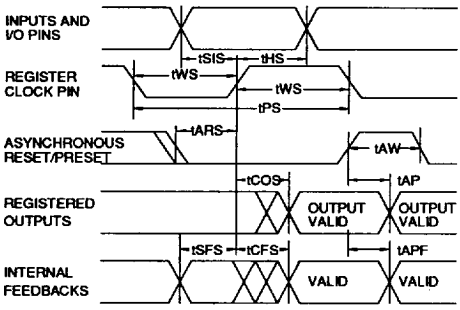
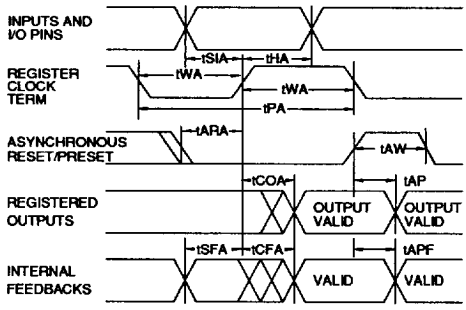
A.C. Waveforms [1] Input Pin Clock



A.C. Waveforms [1] Product Term Clock



Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

Register A.C. Characteristics, Input Pin Clock

Symbol	Parameter	ATH3000-15 Min	ATH3000-15 Max	ATH3000/L-20 Min	ATH3000/L-20 Max	ATH3000/L-25 Min	ATH3000/L-25 Max	Units
t_{COS}	Clock Pin to Registered Output Pin	4	12	4	15	4	20	ns
t_{CFS}	Clock Pin to Registered Feedback	2	6	2	7	2	10	ns
t_{SIS}	Pin Input Setup Time	12		15		18		ns
t_{SFS}	Feedback Setup Time	6		8		10		ns
t_{HS}	Hold Time	0		0		0		ns
t_{WS}	Clock Width	6		7		9		ns
t_{PS}	Clock Period	12		15		20		ns
F_{MAXS}	Maximum Frequency 1/(t_{CFS}+ t_{SFS})		83.3		66.7		50	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

Register A.C. Characteristics, Product Term Clock

Symbol	Parameter	ATH3000-15 Min	ATH3000-15 Max	ATH3000/L-20 Min	ATH3000/L-20 Max	ATH3000/L-35 Min	ATH3000/L-35 Max	Units
t_{COA}	Clock Input to Registered Output Pin	5	15	5	20	5	25	ns
t_{CFA}	Clock Input to Registered Feedback	2	9	5	12	5	15	ns
t_{SIA}	Pin Input Setup Time	10		12		15		ns
t_{SFA}	Feedback Setup Time	5		6		10		ns
t_{HA}	Hold Time	2		5		5		ns
t_{WA}	Clock Width	7		9		12		ns
t_{PA}	Clock Period	14		18		25		ns
F_{MAXA}	Maximum Frequency 1/(t_{CFA}+ t_{SFA})		71		55		40	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

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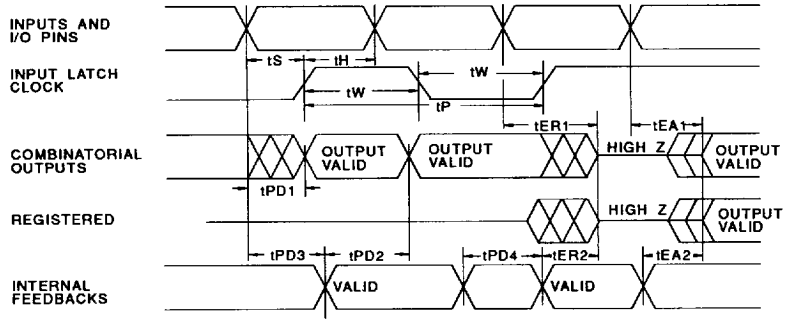
A.C. Waveforms [1]

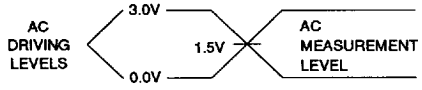


Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

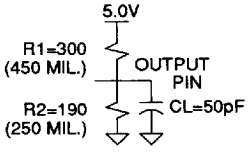
Symbol	Parameter	ATH3000-15 Min	ATH3000-15 Max	ATH3000/L-20 Min	ATH3000/L-20 Max	ATH3000/L-25 Min	ATH3000/L-25 Max	Units
t_{PD1}	Input to Non-Registered Output		15		20		25	ns
t_{PD2}	Feedback to Non-Registered Output		12		15		20	ns
t_{PD3}	Input to Non-Registered Feedback		12		15		20	ns
t_{PD4}	Feedback to Non-Registered Feedback		10		12		17	ns
t_{EA1}	Input to Output Enable		15		20		25	ns
t_{ER1}	Input to Output Disable		15		20		25	ns
t_{EA2}	Feedback to Output Enable		12		15		20	ns
t_{ER2}	Feedback to Output Disable		12		15		20	ns
t_S	Input Latch Setup Time	5		6		7		ns
t_H	Input Latch Hold Time	5		5		5		ns
t_W	Input Latch Clock Width	6		7		9		ns
t_P	Input Latch Clock Period	12		15		20		ns
F_{MAX}	Maximum Frequency ($1/t_P$)		83.3		66.7		50	MHz
t_{AW}	Asynchronous Reset/Preset Width	15		20		25		ns
t_{AP}	Asynchronous Reset/Preset to Registered Output		20		25		30	ns
t_{APF}	Asynchronous Reset/Preset to Registered Feedback		15		20		25	ns

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



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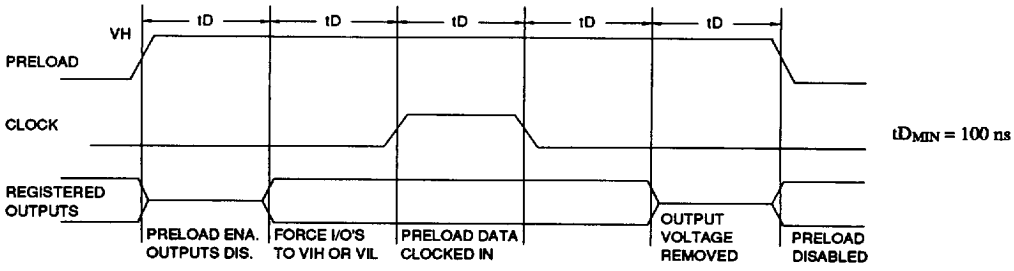
Preload of Registered Outputs

The ATH3000/L's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register low; a V_{IL} will force it high, independent of the polarity setting. The PRELOAD state is entered by placing an 11 V to 14 V signal on pin 35 on SMPs. When the clock (pin 1) is pulsed high, the data on the I/O pin is placed into the associated register.

Level forced on registered output pin during PRELOAD cycle.	Register state After Cycle
V_{IH}	High
V_{IL}	Low



Operating Modes

Mode	68 Lead LCC Pin 1	2	36	34	68	35	Vcc (3,20,37,54)	I/Os
"EPLD"	X (1)	X	X	X	X	X	5V	I/O
Program	V_{PP}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	6V	ADD/D_{IN}
PGM Verify	V_{PP}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	X	6V	ADD/D_{OUT}
PGM Inhibit	V_{PP}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	6V	High Z
Preload	⎍	X	X	X	X	V_H (2)	5V	D_{IN}

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0 V to 14.0 V

Power Up Reset

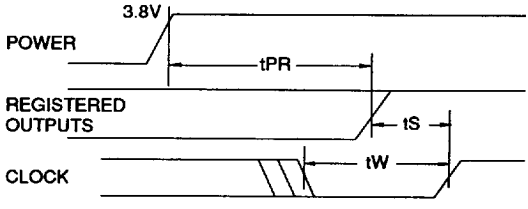
The registers in the ATH3000/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

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ATH3000 PLCC/PGA Pin Assignments

PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name
1	B6	IN	18	F2	I/O	35	K6	IN	52	F10	I/O
2	A6	I/O	19	F1	I/O	36	L6	I/O	53	F11	I/O
3	B5	VCC	20	G2	VCC	37	K7	VCC	54	E10	VCC
4	A5	I/O	21	G1	I/O	38	L7	I/O	55	E11	I/O
5	B4	I/O	22	H2	I/O	39	K8	I/O	56	D10	I/O
6	A4	I/O	23	H1	I/O	40	L8	I/O	57	D11	I/O
7	B3	I/O	24	J2	I/O	41	K9	I/O	58	C10	I/O
8	A3	I/O	25	J1	I/O	42	L9	I/O	59	C11	I/O
9	A2	I/O	26	K1	I/O	43	L10	I/O	60	B11	I/O
10	B2	I/O	27	K2	I/O	44	K10	I/O	61	B10	I/O
11	B1	I/O	28	L2	I/O	45	K11	I/O	62	A10	I/O
12	C2	I/O	29	K3	I/O	46	J10	I/O	63	B9	I/O
13	C1	I/O	30	L3	I/O	47	J11	I/O	64	A9	I/O
14	D2	I/O	31	K4	I/O	48	H10	I/O	65	B8	I/O
15	D1	I/O	32	L4	I/O	49	H11	I/O	66	A8	I/O
16	E2	GND	33	K5	GND	50	G10	GND	67	B7	GND
17	E1	I/O	34	L5	CLK	51	G11	I/O	68	A7	CLK

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Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	6	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATH3000/L fuse patterns. Once programmed, all outputs appear programmed during verify. The security fuse should be programmed last.

The security fuse inhibits Preload.

Erasure Characteristics

The entire memory array of an ATH3000/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W\text{-}sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

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Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
15	12	83.3	ATH3000-15JC ATH3000-15KC ATH3000-15UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000-15JI ATH3000-15KI ATH3000-15UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
20	15	66.7	ATH3000-20JC ATH3000-20KC ATH3000-20UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000-20JI ATH3000-20KI ATH3000-20UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
			ATH3000-20KM ATH3000-20UM	68KW 68UW	Military (-55°C to 125°C)
			ATH3000-20KM/883 ATH3000-20UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
25	20	50	ATH3000-25JC ATH3000-25KC ATH3000-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000-25JI ATH3000-25KI ATH3000-25UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
			ATH3000-25KM ATH3000-25UM	68KW 68UW	Military (-55°C to 125°C)
			ATH3000-25KM/883 ATH3000-25UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

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Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
20	15	66.7	ATH3000L-20JC ATH3000L-20KC ATH3000L-20UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000L-20JI ATH3000L-20KI ATH3000L-20UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
25	20	50	ATH3000L-25JC ATH3000L-25KC ATH3000L-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATH3000L-25JI ATH3000L-25KI ATH3000L-25UI	68J 68KW 68UW	Industrial (-40°C to 85°C)
			ATH3000L-25KM ATH3000L-25UM	68KW 68UW	Military (-55°C to 125°C)

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Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

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