Features

- **Single 2.7V - 3.6V Supply**
- **Sequential Access, Parallel I/O Architecture**
- **Page Program Operation**
  - **Single Cycle Reprogram (Erase and Program)**
  - **4096 Pages (264 Bytes/Page) Main Memory**
- **Two 264-Byte Data Buffers – Allows Receiving of Data while Reprogramming of Non-Volatile Memory**
- **Internal Program and Control Timer**
- **Fast Page Program Time – 7 ms Typical**
- **120 µs Typical Page to Buffer Transfer Time**
- **Low Power Dissipation**
  - **4 mA Active Read Current Typical**
  - **2 µA CMOS Standby Current Typical**
- **2 MHz Max Clock Frequency**
- **Hardware Data Protection Feature**
- **Synchronous Clocking (Two Modes)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Commercial and Industrial Temperature Ranges**

Description

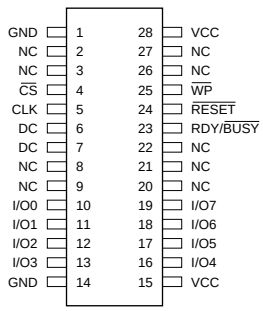
The AT45DB080 is a 2.7-volt only, sequential access, parallel interface Flash memory suitable for in-system reprogramming. Its 8,650,752 bits of memory are organized as 4096 pages of 264-bytes each. In addition to the main memory, the AT45DB080 also contains two data buffers of 264-bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface,

(continued)

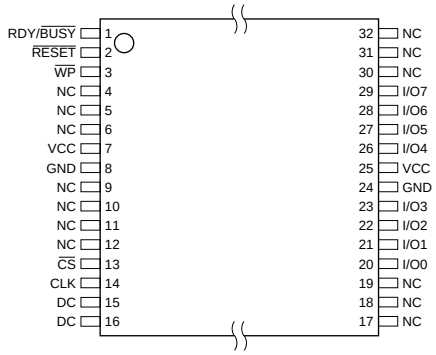
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
CLK	Clock
I/O7-I/O0	Input/Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

SOIC



TSOP Top View
Type 1



Note: SOIC pins 6 and 7 and TSOP pins 15 and 16 are DON'T CONNECT.

8-Megabit 2.7-volt Only Sequential Access Parallel I/O DataFlash®

AT45DB080 Preliminary

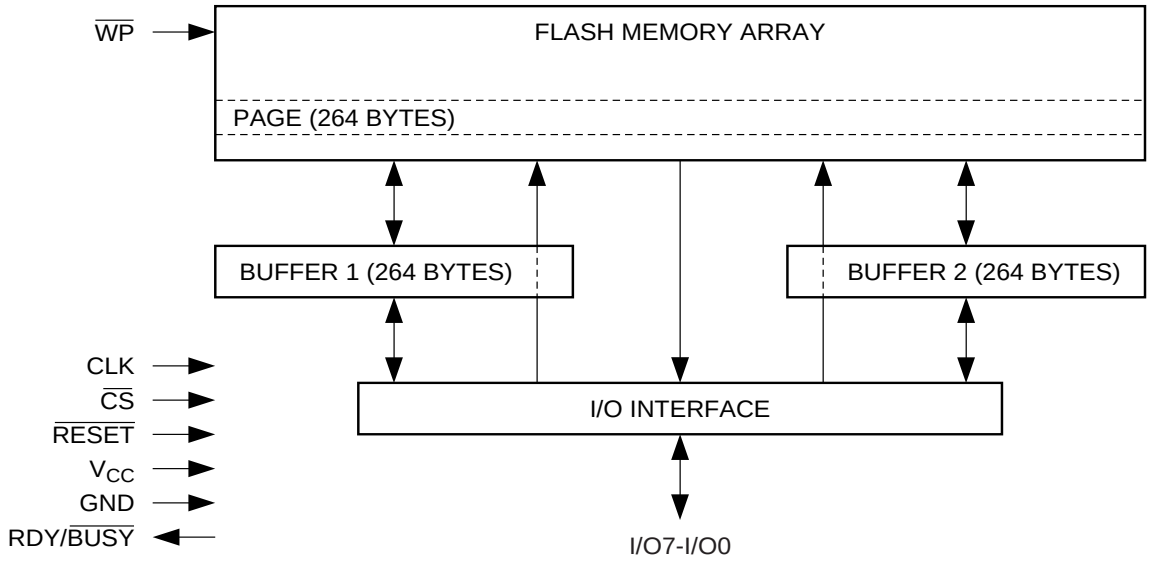
Rev. 1075B–06/98

the DataFlash uses a parallel interface to sequentially access its data. The simple sequential access facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 2 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB080 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB080 is enabled through the chip select pin ($\overline{CS}$) and accessed via an interface consisting of the parallel input/output (I/O7-I/O0) pins and the clock (CLK) pin.

All programming cycles are self-timed, and no separate erase cycle is required before programming.

Block Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 1 and Table 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 1-byte opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the CLK pin controls the loading of the opcode and the desired buffer or main memory address location through the input pins (I/O7-I/O0).

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 4096 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 1-byte opcode, 52H, is followed by 3 address bytes (which comprise the 24 page and byte address bits) and 60 don't care bytes. In the AT45DB080, the first three address bits are reserved for larger density devices (see Notes on page 8), the next 12 address bits (PA11-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 60 don't care bytes which follow the 3 address bytes are sent to initialize the read operation. Following the 60 don't care bytes, additional pulses on CLK result in data being output on the output pins (I/O7-I/O0). The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from

buffer 2. To perform a buffer read, the 1-byte opcode must be followed by the three address bytes comprised of 15 don't care bits and nine address bits. Following the three address bytes, an additional don't care byte must be clocked in to initialize the read operation. Since the buffer size is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. A 1-byte opcode, 53H for buffer 1 and 55H for buffer 2, is followed by the three address bytes comprised of the three reserved bits, 12 address bits (PA11-PA0) which specify the page in main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the CLK pin to load the opcode and the address bytes from the input pins. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. A 1-byte opcode, 60H for buffer 1 and 61H for buffer 2, is followed by three address bytes consisting of three reserved bits, 12 address bits (PA11-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the CLK pin to load the opcode and the address bytes from the input pins. On the low to high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be clocked in from the input pins into either buffer 1 or buffer 2. To load data into either buffer, a 1-byte opcode, 84H for buffer 1 or 87H for buffer 2, is followed by the three address bytes comprised of 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. A 1-byte opcode, 83H for buffer 1 or 86H for buffer 2, is followed by the three address bytes consisting of three reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. A 1-byte opcode, 88H for buffer 1 or 89H for buffer 2, is followed by three address bytes consisting of three reserved bits, 12 address bits (PA11-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously programmed to all 1s (erased state). The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first clocked into buffer 1 or buffer 2 from the input pins and then programmed into a specified page in the main memory. A 1-byte opcode, 82H for buffer 1 or 85H for buffer 2, is followed by three address bytes comprised of three reserved bits and 21 address bits. The 12 most significant address bits (PA11-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bytes are clocked in, the part will take data from the input pins and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. A 1-byte opcode, 58H for buffer 1 or 59H for buffer 2, is followed by the three address bytes comprised of three reserved bits, 12 address bits (PA11-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If the main memory is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in the main memory, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the opcode is clocked in, the 1-byte status register will be clocked out on the output pins during the next clock cycle. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After the one byte of the status register has been clocked out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and CLK is being toggled). The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register on I/O7 by stopping CLK once bit 7 has been output on I/O7. The status of bit 7 will continue to be output on the I/O7 pin, and once the device is no longer busy, the state of I/O7 will change from 0 to 1. There are six operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45DB080, the three bits are 1, 0, and 0. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	1	0	0	X	X	X

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main memory page read
2. Main memory page to buffer 1 (or 2) transfer
3. Main memory page to buffer 1 (or 2) compare
4. Buffer 1 (or 2) to main memory page program with built-in erase
5. Buffer 1 (or 2) to main memory page program without built-in erase
6. Main memory page program
7. Auto page rewrite

Group B modes consist of:

1. Buffer 1 (or 2) read
2. Buffer 1 (or 2) write
3. Status read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data

can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{WP}$ pin is internally pulled high; therefore, in low pin count applications, connection of the $\overline{WP}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{WP}$ pin be driven high externally whenever possible.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, in low pin count applications, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to the "Inactive Clock Polarity High" mode. In addition, the output pins (I/O_7 - I/O_0) will be in a high impedance state, and a high to low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The Clock Polarity mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB081
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

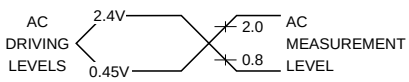
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		2	10	µA
I_{CC1}	Active Current, Read Operation	f = 2 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/Erase Operation			15	35	mA
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

AC Characteristics

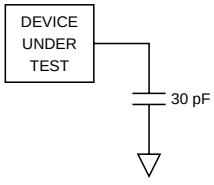
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			2	MHz
t_{WH}	SCK High Time	200			ns
t_{WL}	SCK Low Time	200			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	20			ns
t_H	Data In Hold Time	50			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			150	ns
t_V	Output Valid			180	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		120	250	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	14	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

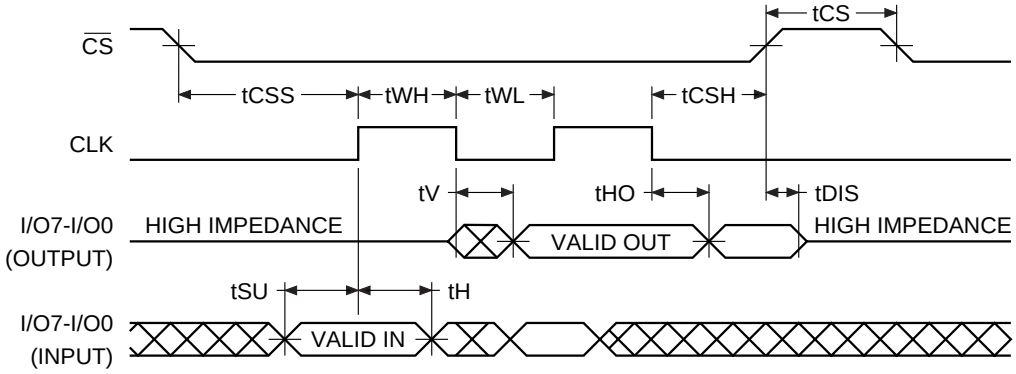
Output Test Load



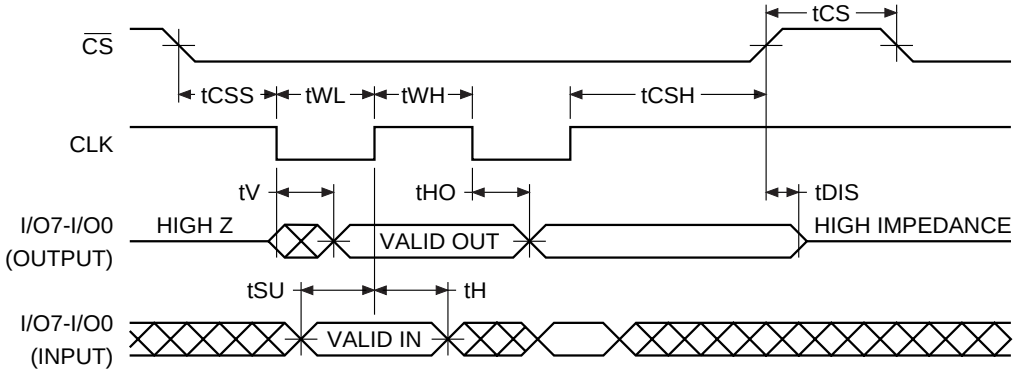
AC Waveforms

Two different timing diagrams are shown below. Waveform 1 shows the CLK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the CLK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the CLK signal.

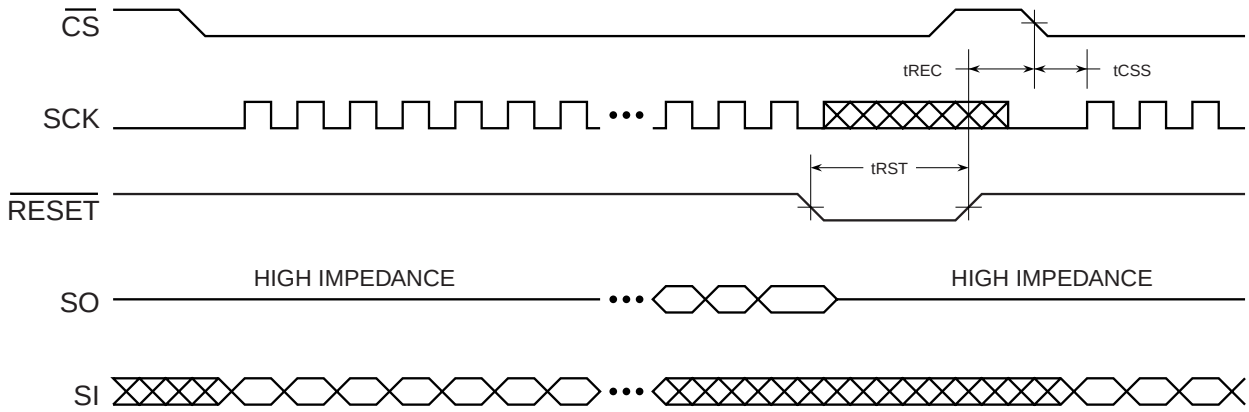
Waveform 1 – Inactive Clock Polarity Low



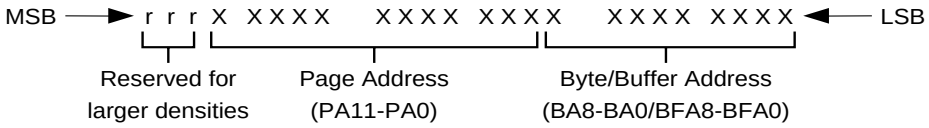
Waveform 2 – Inactive Clock Polarity High



Reset Timing (Inactive Clock Polarity Low Shown)



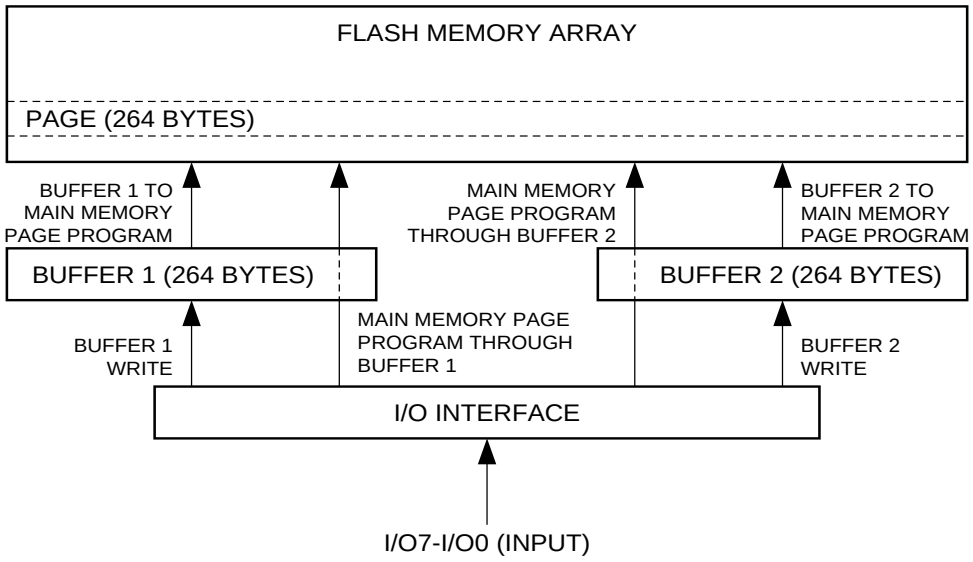
Command Sequence for Read/Write Operations (Except Status Register Read)



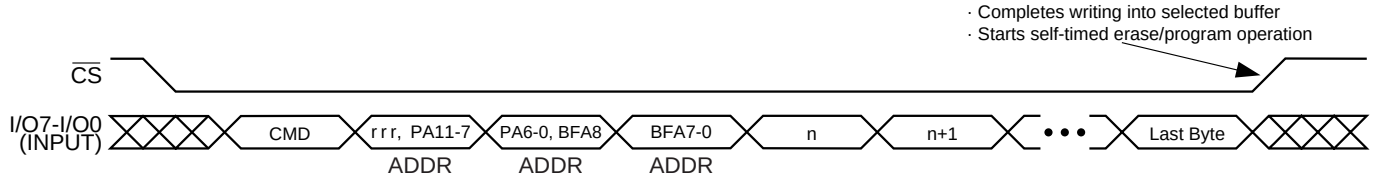
Notes: 1. “r” designates bits reserved for larger densities.
2. It is recommended that “r” be a logical “0” for densities of 8M bit or smaller.
3. For densities larger than 8M bit, the “r” bits become the most significant Page Address bit for the appropriate density.

Write Operations

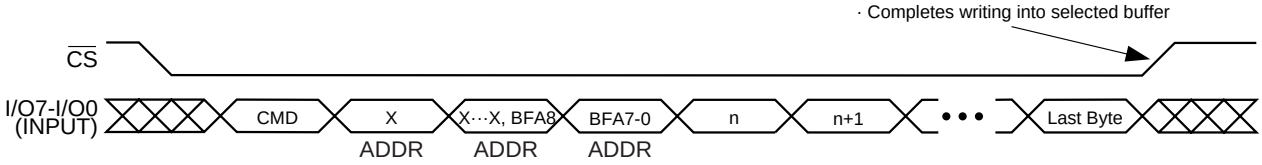
The following block diagram and waveforms illustrate the various write sequences available.



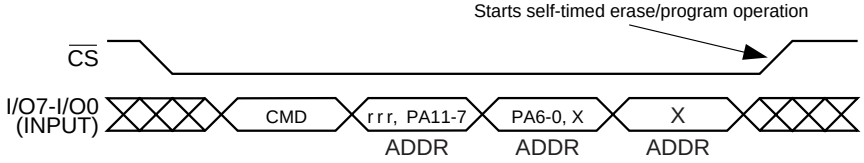
Main Memory Page Program through Buffers



Buffer Write

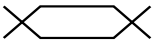


Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)



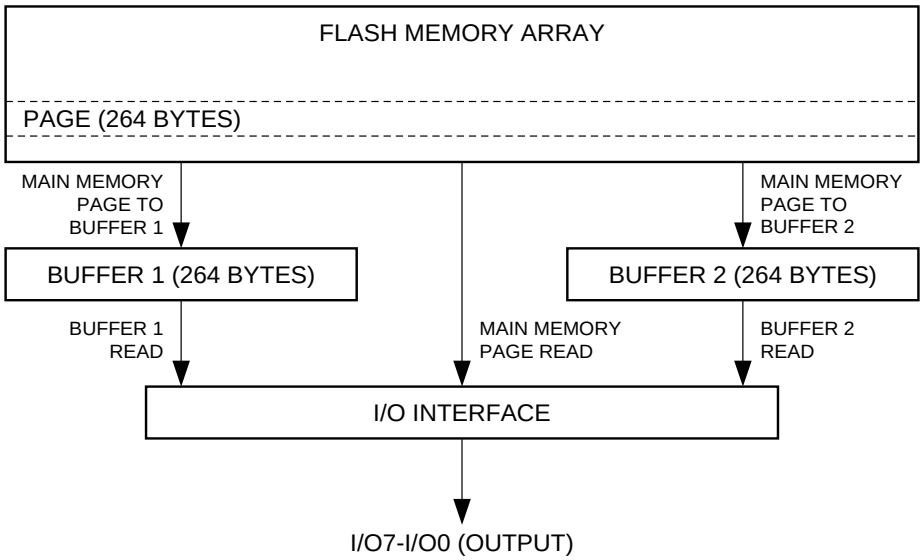
n = 1st byte written

n+1 = 2nd byte written

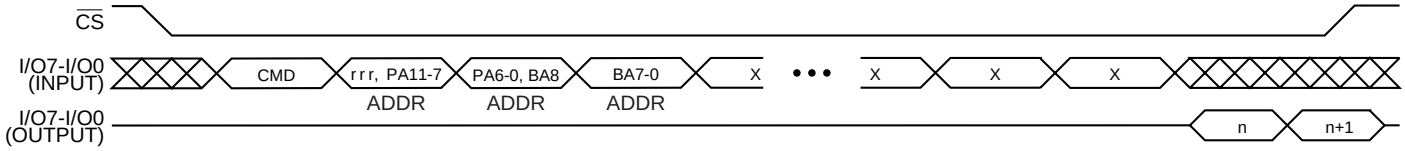
Each transition represents 8 bits and 1 clock cycle 

Read Operations

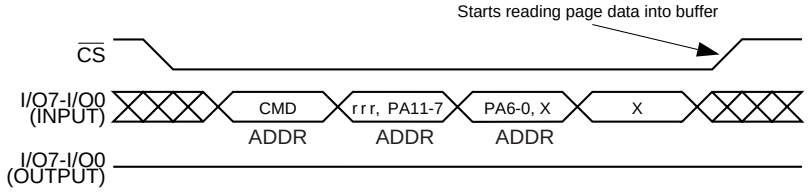
The following block diagram and waveforms illustrate the various read sequences available.



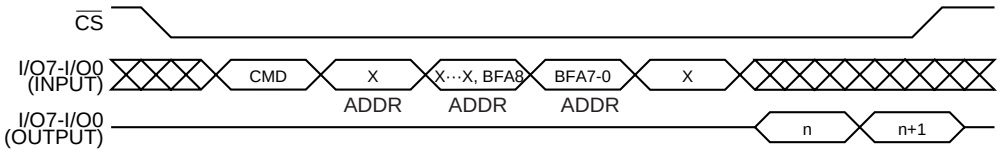
Main Memory Page Read



Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read



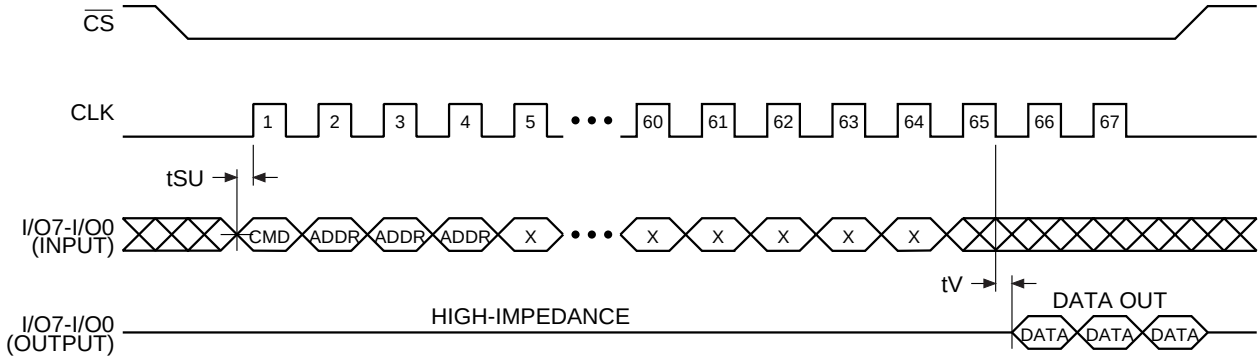
Each transition represents 8 bits and 1 clock cycle

n = 1st byte written

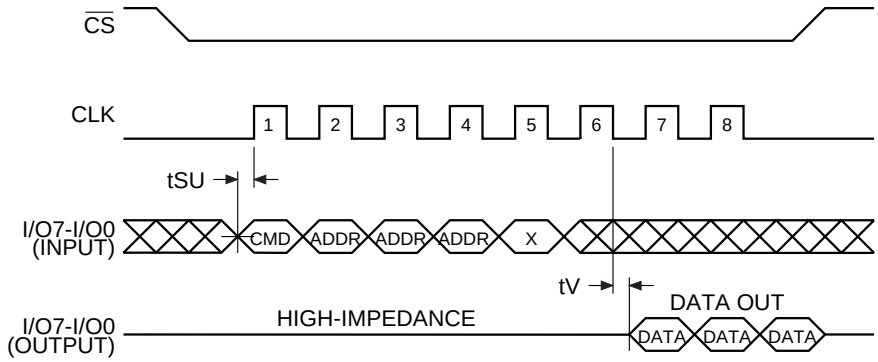
n+1 = 2nd byte written

Detailed Read Timing – Inactive Clock Polarity Low

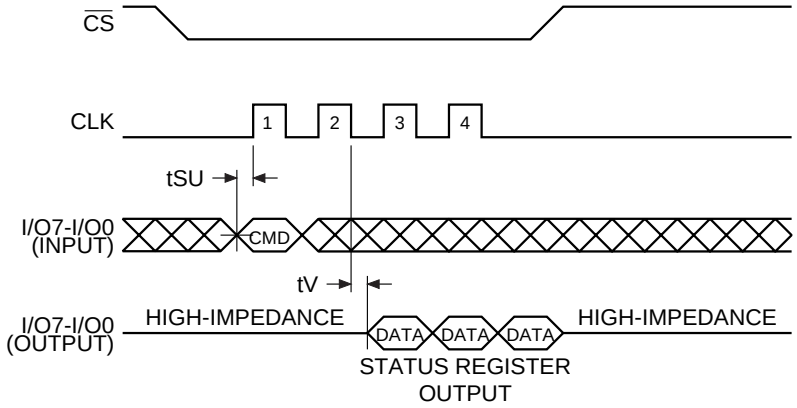
Main Memory Page Read



Buffer Read

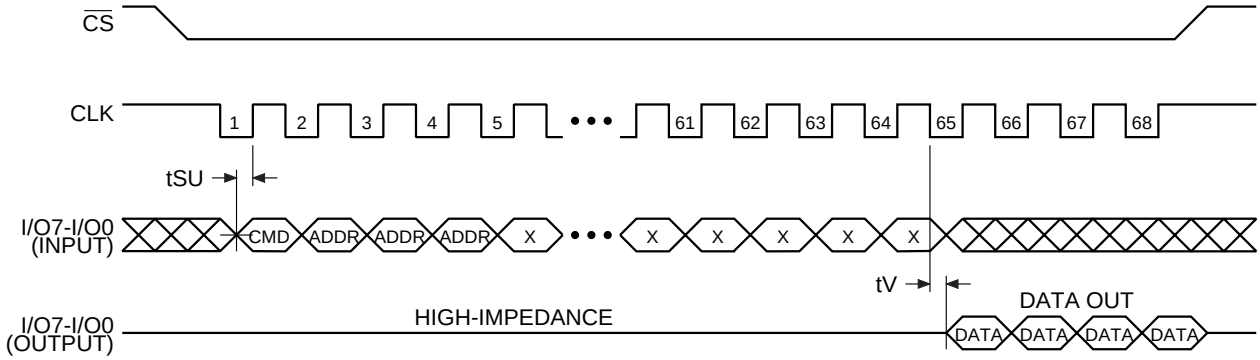


Status Register Read

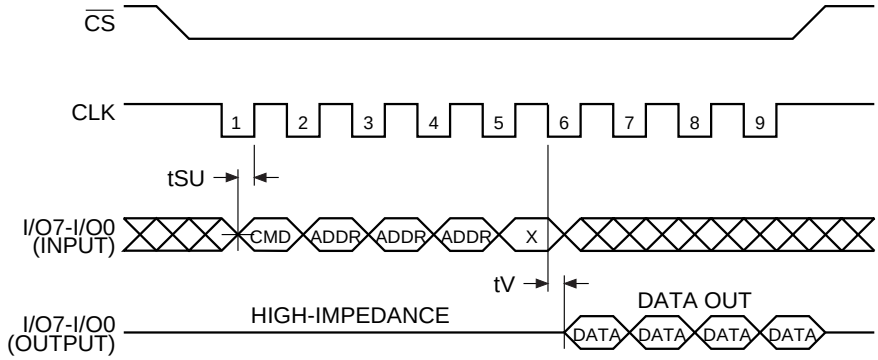


Detailed Read Timing – Inactive Clock Polarity High

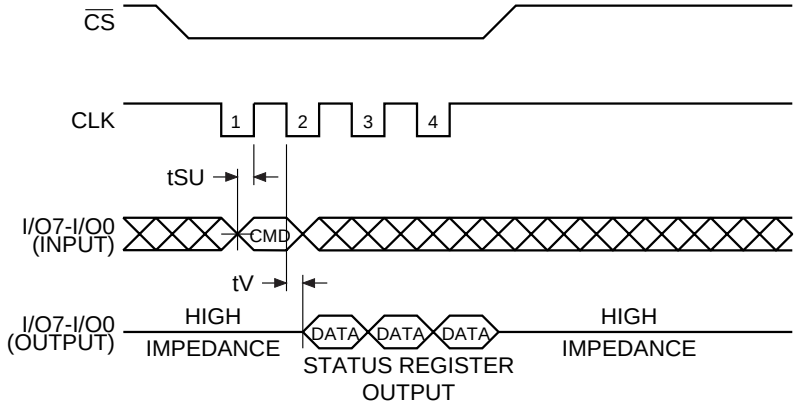
Main Memory Page Read



Buffer Read



Status Register Read



X (Don't Care)
r (reserved bits)

Table 1.

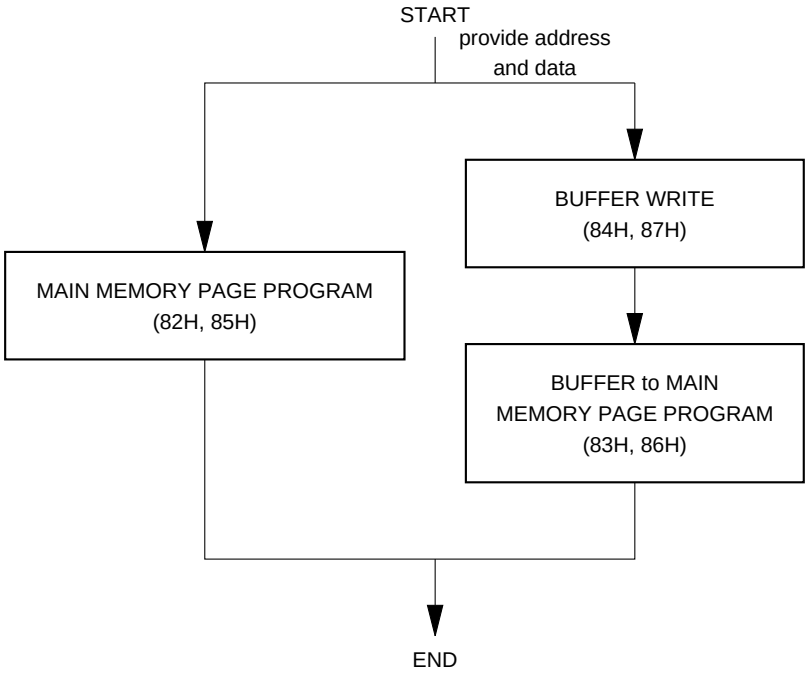
		Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
		Opcode								
CLK	I/O	52H	54H	56H	53H	55H	60H	61H	84H	87H
1	7	0	0	0	0	0	0	0	1	1
	6	1	1	1	1	1	1	1	0	0
	5	0	0	0	0	0	1	1	0	0
	4	1	1	1	1	1	0	0	0	0
	3	0	0	0	0	0	0	0	0	0
	2	0	1	1	0	1	0	0	1	1
	1	1	0	1	1	0	0	0	0	1
	0	0	0	0	1	1	0	1	0	1
2	7	r	X	X	r	r	r	r	X	X
	6	r	X	X	r	r	r	r	X	X
	5	r	X	X	r	r	r	r	X	X
	4	PA11	X	X	PA11	PA11	PA11	PA11	X	X
	3	PA10	X	X	PA10	PA10	PA10	PA10	X	X
	2	PA9	X	X	PA9	PA9	PA9	PA9	X	X
	1	PA8	X	X	PA8	PA8	PA8	PA8	X	X
	0	PA7	X	X	PA7	PA7	PA7	PA7	X	X
3	7	PA6	X	X	PA6	PA6	PA6	PA6	X	X
	6	PA5	X	X	PA5	PA5	PA5	PA5	X	X
	5	PA4	X	X	PA4	PA4	PA4	PA4	X	X
	4	PA3	X	X	PA3	PA3	PA3	PA3	X	X
	3	PA2	X	X	PA2	PA2	PA2	PA2	X	X
	2	PA1	X	X	PA1	PA1	PA1	PA1	X	X
	1	PA0	X	X	PA0	PA0	PA0	PA0	X	X
	0	BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
4	7	BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
	6	BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
	5	BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
	4	BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
	3	BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
	2	BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
	1	BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
	0	BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
5	7	X	X	X						
	6	X	X	X						
	5	X	X	X						
	4	X	X	X						
	3	X	X	X						
	2	X	X	X						
	1	X	X	X						
	0	X	X	X						
• • •		• • •								
64	7	X								
	6	X								
	5	X								
	4	X								
	3	X								
	2	X								
	1	X								
	0	X								

X (Don't Care)
r (reserved bits)

Table 2.

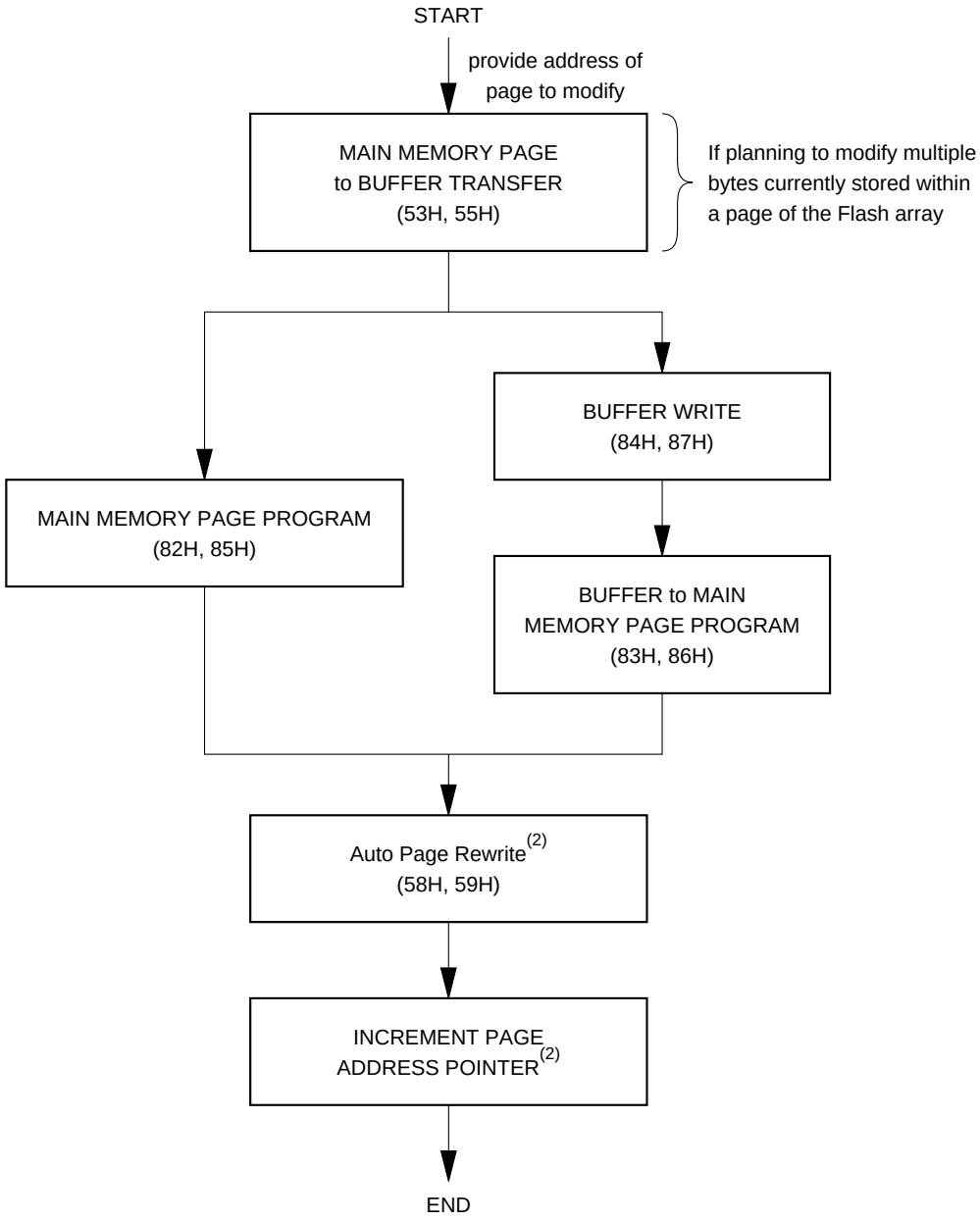
		Buffer 1 to Main Memory Page Program with Built-In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
		Opcode								
CLK	**I/O**	**83H**	**86H**	**88H**	**89H**	**82H**	**85H**	**58H**	**59H**	**57H**
1	7	1	1	1	1	1	1	0	0	0
	6	0	0	0	0	0	0	1	1	1
	5	0	0	0	0	0	0	0	0	0
	4	0	0	0	0	0	0	1	1	1
	3	0	0	1	1	0	0	1	1	0
	2	0	1	0	0	0	1	0	0	1
	1	1	1	0	0	1	0	0	0	1
	0	1	0	0	1	0	1	0	1	1
2	7	r	r	r	r	r	r	r	r	
	6	r	r	r	r	r	r	r	r	
	5	r	r	r	r	r	r	r	r	
	4	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	
	3	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
	2	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
	1	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
	0	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
3	7	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
	6	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
	5	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
	4	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
	3	PA2	PA2	PA2	PA2	PA2	PA2	PA2	PA2	
	2	PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1	
	1	PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0	
	0	X	X	X	X	BA8	BA8	X	X	
4	7	X	X	X	X	BA7	BA7	X	X	
	6	X	X	X	X	BA6	BA6	X	X	
	5	X	X	X	X	BA5	BA5	X	X	
	4	X	X	X	X	BA4	BA4	X	X	
	3	X	X	X	X	BA3	BA3	X	X	
	2	X	X	X	X	BA2	BA2	X	X	
	1	X	X	X	X	BA1	BA1	X	X	
	0	X	X	X	X	BA0	BA0	X	X	

Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 2. Algorithm for Randomly Modifying Data



Note:
1. To preserve data integrity, each page of the DataFlash memory array must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the Flash array. See application note AN-4 (“Using Atmel’s Serial DataFlash”) for more details.

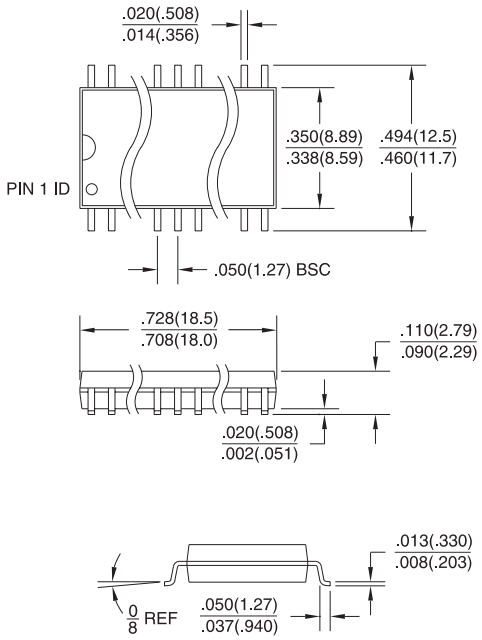
Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
2	10	0.01	AT45DB080-RC AT45DB080-TC	28R 32T	Commercial (0°C to 70°C)
2	10	0.01	AT45DB080-RI AT45DB080-TI	28R 32T	Industrial (-40°C to 85°C)

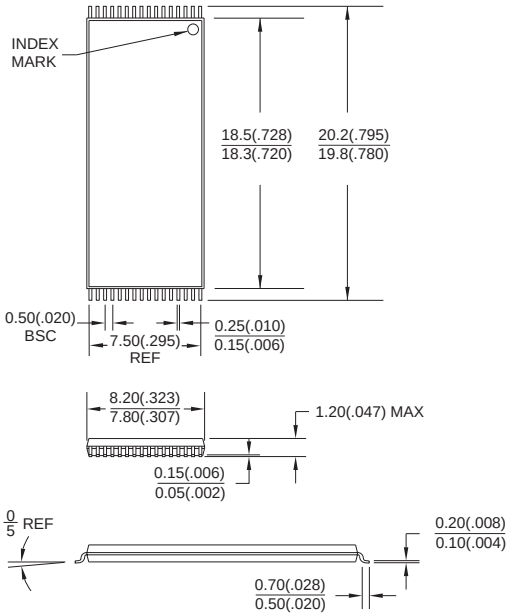
Package Type	
28R	28-Lead, 0.330" Wide, Plastic Gull-Wing Small Outline Package (SOIC)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Packaging Information

28R, 28-Lead, 0.330" Wide,
Plastic Gull Wing Small Outline Package (SOIC)
Dimensions in Inches and (Millimeters)



32T, 32-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters