ASAHI KASEI® =PRELIMINARY= AK2392

π/4 Shift QPSK MODEM for Digital Cordless Telephone

General Description

The AK2392 is a MODEM LSI for a digital cordless telephone which conforms to the second generation cordless telephone system standard (STD-28) of RCR (Japan). The modulator is configured from a baseband filter (Root Nyquist roll off filter) for band limitation, sum logical circuit and D/A converter, etc. The demodulator is configured from a differential demodulation circuit, preamble detection circuit, timing recovery circuit, etc.

Features

Modulator

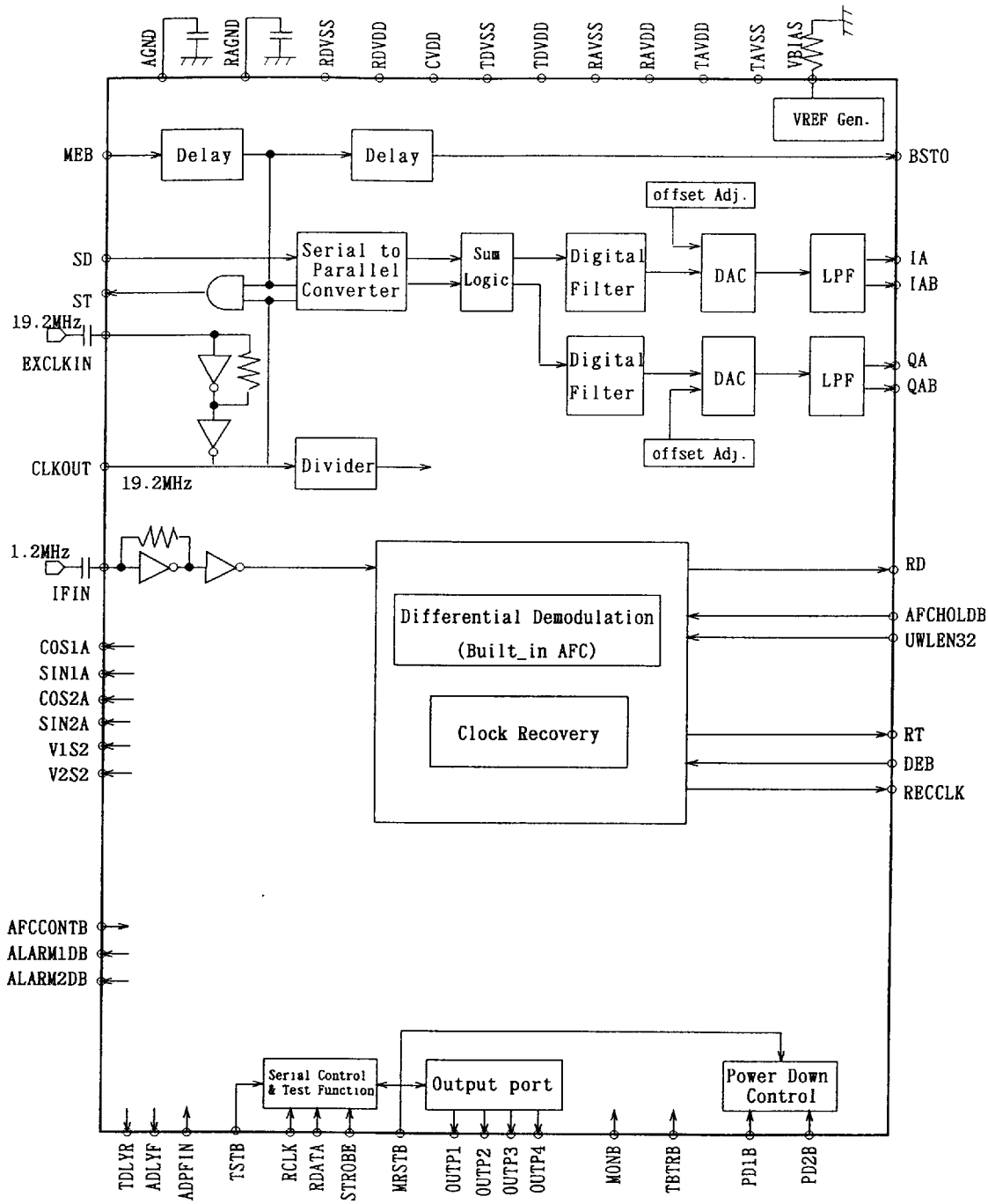
- ☐ Transmission Speed 384 kbps
- ☐ Roll off Filter (Digital filter + Analog filter)
  - *Root Nyquist Frequency Response
  - *Roll-off Rate $\alpha = 0.5$
  - *Passband (3 dB) 96 kHz
  - *Stop band attenuation 60 dB or greater (600 kHz Detuning)
    65 dB or greater (900 kHz or higher)
- ☐ Modulation Accuracy 3% rms or lower.
- ☐ Built-in ramp response circuit.
- ☐ Built-in D/A converter.
- ☐ Built-in output level adjusting circuit.
- ☐ Built-in DC offset voltage adjustment circuit.
- ☐ Built-in differential logical circuit conforming to the π/4 shift QPSK modulation system.

Demodulator

- ☐ IF input frequency (Amplitude) 1.2 MHz (1.5 V p-p)
- ☐ Differential demodulation
- ☐ Built-in AFC circuit
- ☐ Built-in preamble detection circuit.
- ☐ Handles continuous and burst receiving modes.

- ☐ Current consumption During conversation 5.75 mA Typ. (during 3V operation)
  During full power down 50 μA Typ.
- ☐ Power supply voltage Single 2.7 - 5.5 V power supply
- ☐ Package 64 pin VQFP

■ Block Diagram



Block Description

① Modulator

Generates the I and Q signals from digital data input from the SD pin. This block is configured from a delay circuit, S/P converter, SUM Logic, digital filter, DAC, LPF, divider and analog ground AMP.

Block	Function
Delay	Controls the send operation timing based on the MEB input signal.
Serial to parallel Converter	Divides 384 kbps serial data input from the SD pin into two 192 kbps parallel data.
Sum Logic	Performs differential encoding of data from the S/P converter.
Digital Filter	This is a root Nyquist filter.
DAC	This is a DAC which converts signals from the digital filter to analog signals. 6-bit offset adjustments and 4-bit gain adjustments are made possible through the control register.
Divider	Generates a clock for 384 kHz transmission data based on the 19.2MHz clock.

② Demodulator

Performs clock recovery and data demodulation from the IFIN input signal. This block is configured from the following blocks.

Block	Function
Differential Demodulation Circuit	Demodulates the 1.2 MHz, 1.5 V p-p IF signal input from IFIN and outputs 384 kbps serial data from RD.
AFC Circuit	The AFC circuit operates to prevent deterioration of the bit error rate . (AFC can perform normally for the receive signal whose deviation is within ± 12kHz.)
Timing Recovery	Recovers the 384 kHz clock from receiving data and outputs it from RT. The output data from RD are synchronized with the falling edge of the 384 kHz recovered clock.

There are two receiving modes to select from, the burst receiving mode and the continuous receiving mode.

Mode	Operation
Burst Receiving Mode	In the burst receiving mode, the demodulator operates during 122.75 ±0.25 symbols after the falling edge of DEB. Demodulation starts from the IF signal which is input after the 9.25 ±0.25 symbols from the falling edge of DEB, and demodulated data are output from RD after the 2.25 symbol following IF signal input. The detection enable interval is 110 symbols, from the 9.25 symbol after the falling edge of DEB to the 119.25 symbol. After 3.5 symbols from detection circuit is disabled, the operation of the entire demodulator is disabled. (Fig.2.1)
Continuous Receiving Mode	In the continuous receiving mode, demodulator operates while DEB is "L". Operation of the internal DPLL circuit is enabled from the falling edge of the RT clock immediately after DEB goes "L" until the falling edge of the RT clock immediately after DEB goes "H". (Fig. 2.2).

③Data Registers

The various internal registers in the IC undergo rewriting in accordance with input data, causing each register's setting conditions to change.
This block is configured from S/P converters.

④Output Ports

Values set in the address (11000) control registers are output in parallel.
This block is configured from 4-bit registers.

⑤Reference Voltage Source

This supplies the voltage and current used for reference in the IC.

Pin/Function Descriptions

Pin#	Pin Name	I/O	Function	Remark
			Modulator I/O pins	
54	SD	DI	Send data input pin. The status of the SD pin is fetched at the falling edge of ST clock.	
52	ST	DO	Clock output pin for send data. Outputs the 384 kHz clock 225 times in accordance with the falling edge of MEB.	
38	MEB	DI	Modulator enable input pin. The burst signal transmission is triggered by MEB signal.	
1	EXCLKIN	AI	Main clock input pin. The 19.2 MHz clock (0.7 V p-p) undergoes DC cutting and is input.	
7	CLKOUT	DO	Main clock output pin. The 19.2 MHz clock is output at the DVSS-DVDD level.	
51	BSTO	DO	Burst indicator signal output pin. Indicates the burst position during I and Q analog output. Outputs the "H" level during sending of the burst signal.	
27 28	IA IAB	AO	Quadradure modulator in-phase component output pins. These signal pair is a differential output. They have high impedance except when the burst signals are transmitted.	
34 33	QA QAB	AO	Quadradure modulator quadra component output pins. These signal pair is a differential output. They have high impedance except when the burst signals are transmitted.	
			Demodulator I/O pins	
62	RT	DO	Demodulator receiving clock output pin. Outputs the 384 kHz clock.	
63	RD	DO	Demodulator receiving data output pin. Outputs data synchronous with the falling edge of RT	
11	DEB	DI	Demodulator enable input pin. Operation of the demodulator is enabled from the falling edge.	
13	UWLEN32	DI	Unique word length setting signal input pin. Preamble detection is enabled by "H" level input.	
15	BURSTB	DI	Receiving mode setting pin. Through the polarity of this signal when the DEB signal falls, the receiving mode is set as follows. * When the "L" level is input, burst receiving mode. * When the "H" level is input, continuous receiving mode.	
14	AFCCONTB	DI	AFC control enable input pin. AFC is enabled by inputting the "L" level. This pin includes pull down MOS.	

Pin#	Pin Name	I/O	Function	Remark
16	IFIN	AI	IF signal input pin. Inputs a 1.2 MHz (1.5 V p-p) signal.	
10	ALARM1DB	DO	Differential demodulation circuit alarm output 1. Outputs the "L" level when an alarm is detected.	
9	ALARM2DB	DO	Differential demodulation circuit alarm output 2. Outputs the "L" level when an alarm is detected.	
64	RECCLK	DO	Recover clock output pin. Outputs the recovered 192 kHz clock.	
17	V1S2	AO	Differential demodulation test pin 1.	
18	V2S2	AO	Differential demodulation test pin 2.	
22	COS1A	AI/O	Differential demodulation test pin 3.	
21	SIN1A	AI/O	Differential demodulation test pin 4.	
24	COS2A	AI/O	Differential demodulation test pin 5.	
23	SIN2A	AI/O	Differential demodulation test pin 6.	
19	TLPFIN	AI	Differential demodulation test pin 7.	
4	TDLYR	DO	Differential demodulation test pin 8.	
3	TDLYF	DO	Differential demodulation test pin 9.	
46	TSTB	DI	Test mode control pin 1. Normally, set this pin permanently at the "H" level.	
40	TBTRB	DI	Test mode control pin 2. Normally, set this pin permanently at the "H" level.	
39	MONB	DI	Monitor mode control pin. Includes pull up MOS.	
Data Registers Input pins				
49	RCLK	DI	Data input clock input pin. The status of RDATA pin is fetched to the shift register at the falling edge of RCLK.	
50	RDATA	DI	Data input pin for setting control registers. Inputs data for rewriting the various internal control registers in the IC.	
47	STROBE	DI	Write enable signal input pin.	
Data Registers Input pins				
61 60 59 58	OUT1 OUT2 OUT3 OUT4	DO	Output data written to the address (11000) control register. The impedance of these pins goes high when MRSTB is at "L".	
Reference Voltage Source pins				
30	VBIAS	AO	Bias voltage output pin.	
31	AGND	AO	Reference analog ground output pin.	
26	RAGND	AO	Demodulator reference analog ground output pin.	

Pin#	Pin Name	I/O	Function	Remark
Power Supply / Ground pins				
29	TAVDD	PWR	Power supply pin for the modulator analog circuits.	
32	TAVSS	GND	Ground pin for the modulator analog circuits.	
25	RAVDD	PWR	Power supply pin for the demodulator analog circuits	
20	RAVSS	GND	Ground pin for the demodulator analog circuits.	
55	TDVDD	PWR	Power supply pin for the modulator digital circuits.	
45	TDVDD	GND	Ground pin for the modulator digital circuits.	
56	RDVDD	PWR	Power supply pins for the demodulator digital circuits.	
8	RDVSS	GND	Ground pins for the demodulator digital circuits.	
6	CVDD	PWR	Power supply pin for the 19.2 MHz clock output.	
Power Down / Reset / N.C pins				
37	PD1B	DI	Modulator power down control input pin. When at the "L", the modulator is powered down.	
12	PD2B	DI	Demodulator power down control input pin. The demodulator is powered down when this pin is at the "L".	
36	MRSTB	DI	Reset signal input pin. Initial setting of the control register is accomplished by inputting the "L" level. Reset once after turning on the power and before operation starts.	
(Note)	N.C	N.C	No connection	

Note: N.C pins # are 2, 5, 35, 41, 42, 43, 44, 48, 53 and 57.

Absolute Maximum Ratings

Parameter	Symbol	min	max	unit	Remarks
Power Supply Voltage (VDD)	TDVDD, RDVDD TAVDD, RAVDD, CVDD	-0.3	7.0	V	TAVDD ≧ other VDD
Ground Level (VSS)	TDVSS, RDVSS TAVSS, RAVSS	0	0	V	Voltage Reference Level
Input Voltage	V_{IN}	-0.3	VDD+0.3	V	
Input Current	I_{IN}	-10	+10	mA	
Storage Temperature	T_{stg}	-30	105	℃	

Note) Voltages are all given with the ground pin as reference :
TAVSS, RAVSS, TDVSS, RDVSS = 0V

Caution: If this device is used under conditions which exceed these values, the device may be destroyed. Also, normal operation cannot be guaranteed.

Recommended Operation Conditions

Parameter	Symbol	min	typ	max	unit
Power Supply Voltage	VDD	2.7		5.5	V
Operation Temperature	Ta	-10		60	℃

Note) Voltages are all given with the ground pin as reference :
TAVSS, RAVSS, TDVSS, RDVSS = 0V

Electrical Characteristics

1) DC Characteristics

Parameter	Symbol	Pin	Condition	min	typ	max	unit
Current Consumption	I_{PD12}		When in PD12 mode		50	200	μA
	I_{PD14}		When in PD14 mode		4.5	12	mA
	I_{PD32}		When in PD32 mode		3	9	mA
	I_{PD34}		When in PD34 mode		4.5	12	mA
	I_{DMOD}		When in MOD mode		10	22	mA
	I_{DDEM}		When in DEM mode		9	22	mA
High Level Output Voltage	V_{OH}	DO	I_{OH}=-1 mA	VDD-1.0			V
Low Level Output Voltage	V_{OL}	DO	I_{OL}= 1 mA			0.5	V
High Level Input Voltage	V_{IH}	DI		0.7VDD		VDD	V
Low Level Input Voltage	V_{IL}	DI		0		0.3VDD	V
Input Leak Current	I_I	DI				±10	μA

Note 1:Current consumption condition modes are defined as follows.
The power supply voltage when the max current consumption is measured is VDD = 5.5 V.
The power supply voltage when the typ current consumption is measured is VDD = 3.0 V.

Mode	Pin				Remarks
	PDIB	MEB	PD2B	DEB	
PD12 mode	0	×	0	×	Full off state.
PD14 mode	0	×	1	1	Demodulator in standby state.
PD32 mode	1	1	0	×	Modulator in standby state.
PD34 mode	1	1	1	1	Modulator and demodulator in standby state.
MOD mode	1	0	1	1	During modulator operation.
DEM mode	1	1	1	0	During demodulator operation.

Note 2: Current consumption doesn't include output drive current.
Note 3: Input leak current is defined except the current at AFC_CONTB and MONB.

2) Switching Characteristics

① Modulator

Parameter	Symbol	Pin	min	typ	max	unit	Remarks
Clock Frequency	f_{mclk}	EXCLKIN		19.2		MHz	
Pulse Duty	t_{mdut}	EXCLKIN	40		60	%	
Clock Input Amplifier		EXCLKIN	0.7			Vpp	
Clock Frequency	f_{clk}	ST		384		kHz	fig. 1
Pulse Duty	f_{dut}	ST		50		%	fig. 1
Set Up Time	t_s	ST → SD	0.65			μ sec	fig. 1
Hold Time	t_h	ST → SD	0.65			μ sec	fig. 1
Pulse Width	t_{lpw}	MEB	160			nsec	fig. 1
Delay Time	t_{dst}	MEB → ST	8.23 μ -26n	8.23 μ	8.23 μ +26n	sec	Note 1 fig. 1
	t_{diq}	MEB → I•Q	34.7	35.1	35.5	μ sec	Note 2 fig. 1
	t_{dbou}	ST → BSTO		4.75		symbol	Note 3 fig. 1
	t_{dbod}	ST → BSTO		6.75		symbol	Note 4 fig. 1

Note 1: The delay from the fall of MEB to the rise of the first ST clock output.
Note 2: The delay from cancellation of transmitter power down to start of transmission (analog circuit stabilization).
Note 3: The delay from rise of the first ST clock to rise of the BSTO output.
Note 4: The delay from rise of the 225th ST clock to fall of the BSTO output.

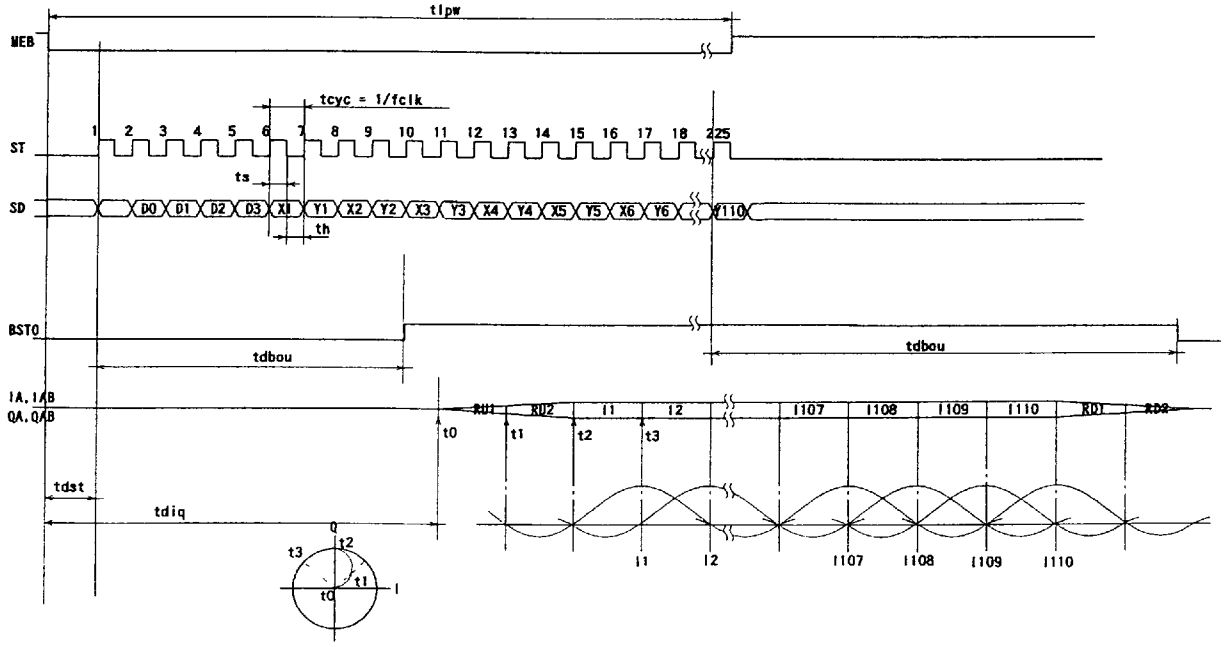


fig. 1

② Demodulator

Parameter	Symbol	Pin	min	typ	max	unit	Remarks
Clock Frequency	f_{clk}	RT		384		kHz	
Pulse Duty	f_{dut}	RT		52		%	
Pulse Width	t_{ipw}	DEB	10			μ sec	
Delay Time	t_{dif}	DEB → IFIN	7.0		7.5	symbol	Note 1 fig. 2
	t_{dplu}	DEB → DPLL ENABLE	9.0		9.5	symbol	Note 2 fig. 2
	t_{drd}	IFIN → RD		2.25		symbol	Note 3 fig. 2
	t_{dple}	DPLL ENABLE		110		symbol	Note 4 fig. 2
	t_{dpd}		122.5		123	symbol	Note 5 fig. 2

Note 1: The delay from cancellation of receiver power down to start of reception (analog circuit stabilization).
Note 2: The delay from the fall of DEB to the start of DPLL operation.
Note 3: The delay from IFIN input to RD output.
Note 4: The DPLL operation enable interval.
Note 5: The delay from the fall of DEB to receiver power down.

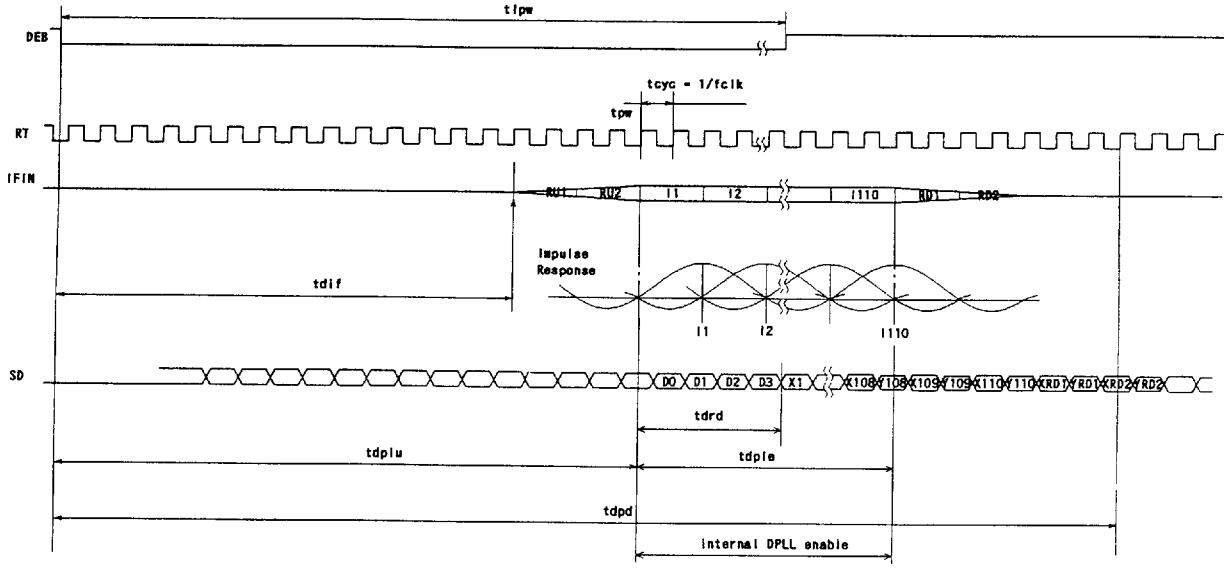


fig. 2. 1 (BURSTB = "L")

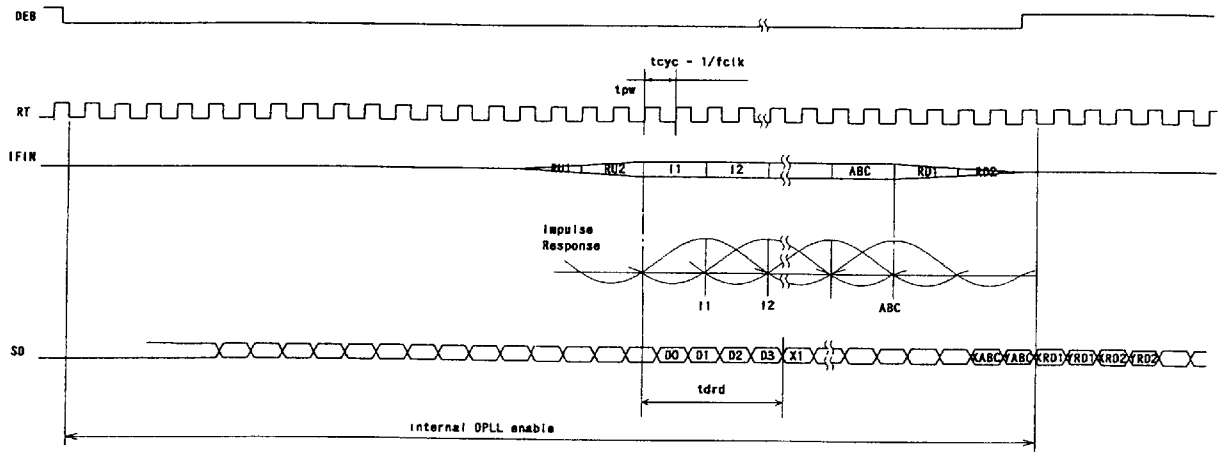


fig. 2. 2 (BURSTB = "h")

③ Data Registers

Parameter	Symbol	Pin	min	typ	max	unit	Remarks
Clock Frequency	f_{clk}	RCLK			5	MHz	fig. 3
Pulse Width	t_{pw}	STROBE	50			nsec	fig. 3
Set Up Time	t_{rs}	RCLK → RDATA	50			nsec	fig. 3
	t_{su}	RCLK → STROBE	50			nsec	fig. 3
Hold Time	t_{rh}	RCLK → RDATA	50			nsec	fig. 3
	t_{ht}	RCLK → STROBE	50			nsec	fig. 3

Note 1: Set data at times other than during operation of the MODEM.

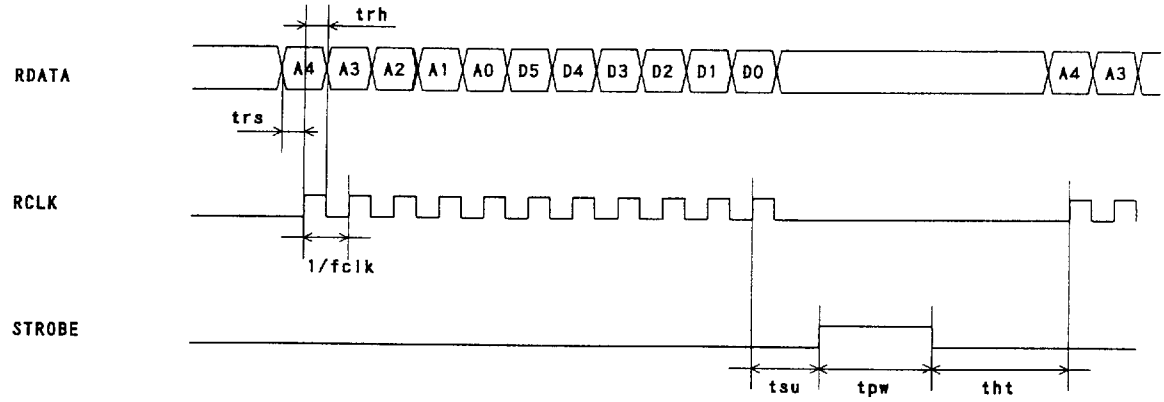


fig. 3

5) Analog Characteristics

① Modulator

Parameter	Pin	Symbol	min	typ	max	unit	Remarks
DC Output Level	IA, IAB QA, QAB	$\frac{IA+IAB}{2}$ $\frac{QA+QAB}{2}$	0.5VDD -0.2	0.5VDD	0.5VDD +0.2	V	
Output Amplitude Level	IA, IAB QA, QAB	R_L=5KΩ to analog ground level	0.45	0.5	0.55	Vpp	Note 1
Output Amplitude Adjustment Range	IA, IAB QA, QAB				±20	%	Note 2
Power Leakage to Adjacent Band	IA, IAB QA, QAB	600kHz detuning ±96kHz band			-60	dB	Note 3
		900kHz detuning ±96kHz band			-65	dB	Note 3
Spurious Transmission	IA, IAB QA, QAB	Above 1MHz up to 2MHz			-60	dB	Note 3
Modulation Accuracy	IA, IAB QA, QAB				3	%rms	Value after adjustment
Output Amplitude Drift	IA, IAB QA, QAB				±200	ppm /℃	Portion exceeding value in above item Note 4
DC Offset	IA, IAB QA, QAB	IA-IAB QA-QAB			±30	mV	
DC offset Adjustment Range	IA, IAB QA, QAB	IA-IAB QA-QAB			±40	mV	Note 5

Note 1: Value when input data are all "0."

Note 2: Absolute value with respect to B when the gain adjustment is 0 dB. (4 bits, 16 steps)

Note 3: Value with respect to double power between 0 an 96 kHz.

Note 4: Design target value.

Note 5: Absolute value when the offset adjustment is 0 mV. (6 bits, 84 steps)

② Demodulator

Parameter	Pin	Symbol	Min	typ	max	unit	Remarks
Input Signal Frequency	IFIN			1.2		MHz	
Input Amplitude	IFIN			1.5		Vpp	Note 1

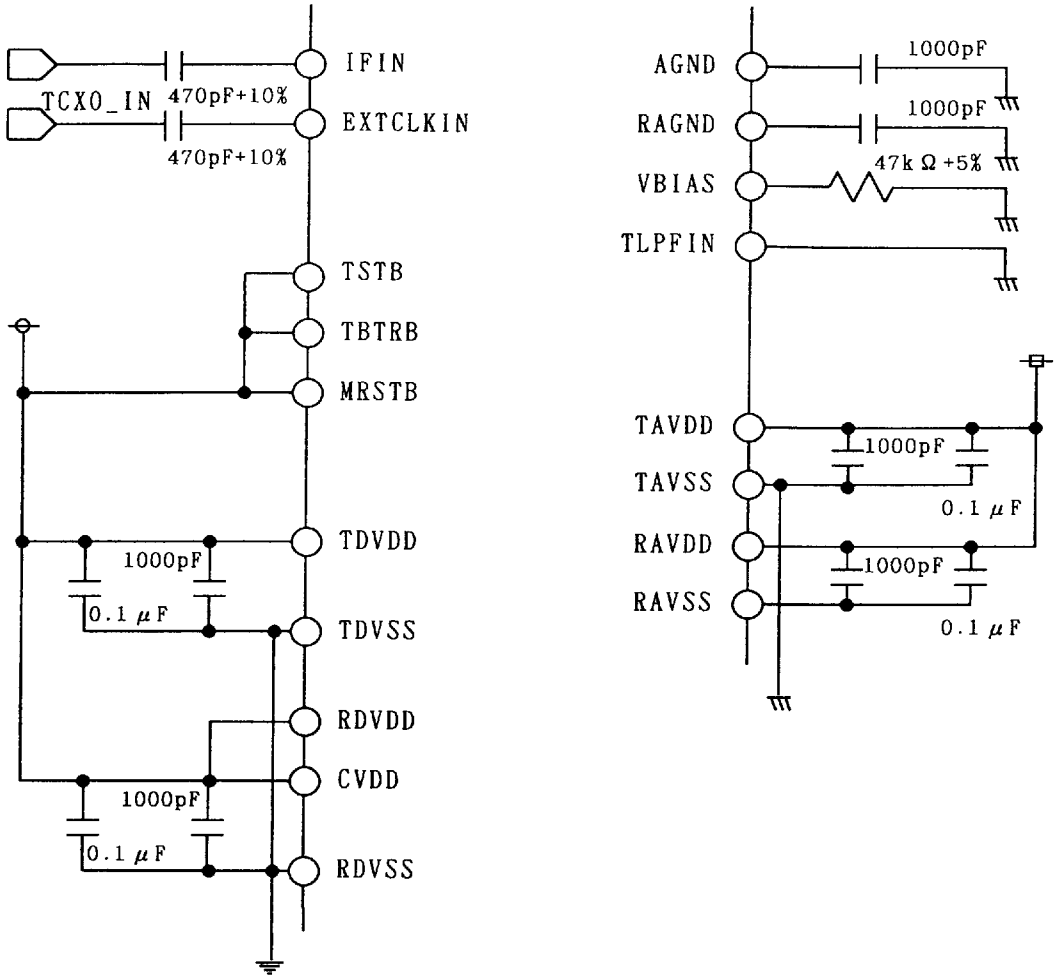
Note 1: Cut the DC and input.

③ Reference Voltage Block

Parameter	Pin	Symbol	min	typ	max	unit	Remarks
Analog GND Level	AGND		0.48VDD		0.52VDD	V	Note 1
Output Level	VBIAS	R_L=47KΩ	1.06	1.18	1.30	V	

Note 1 : VDD=TAVDD

Application Circuit



Package

□64Pin VQFP

■Marking

(1) Pin 1 Indication (Pin 1 is the pin at the chamfered corner.)
(2) Date Code: XXXXX (5 digits) Top 3 digits: Week Code
Bottom 2 digits: In-house Control Code
(3) Marketing Code: AK2392
(4) Country of Manufacture Indication: JAPAN
(5) Asahi Kasei Logo

■Package size