

V6355D

(LCDC)

■ OUTLINE

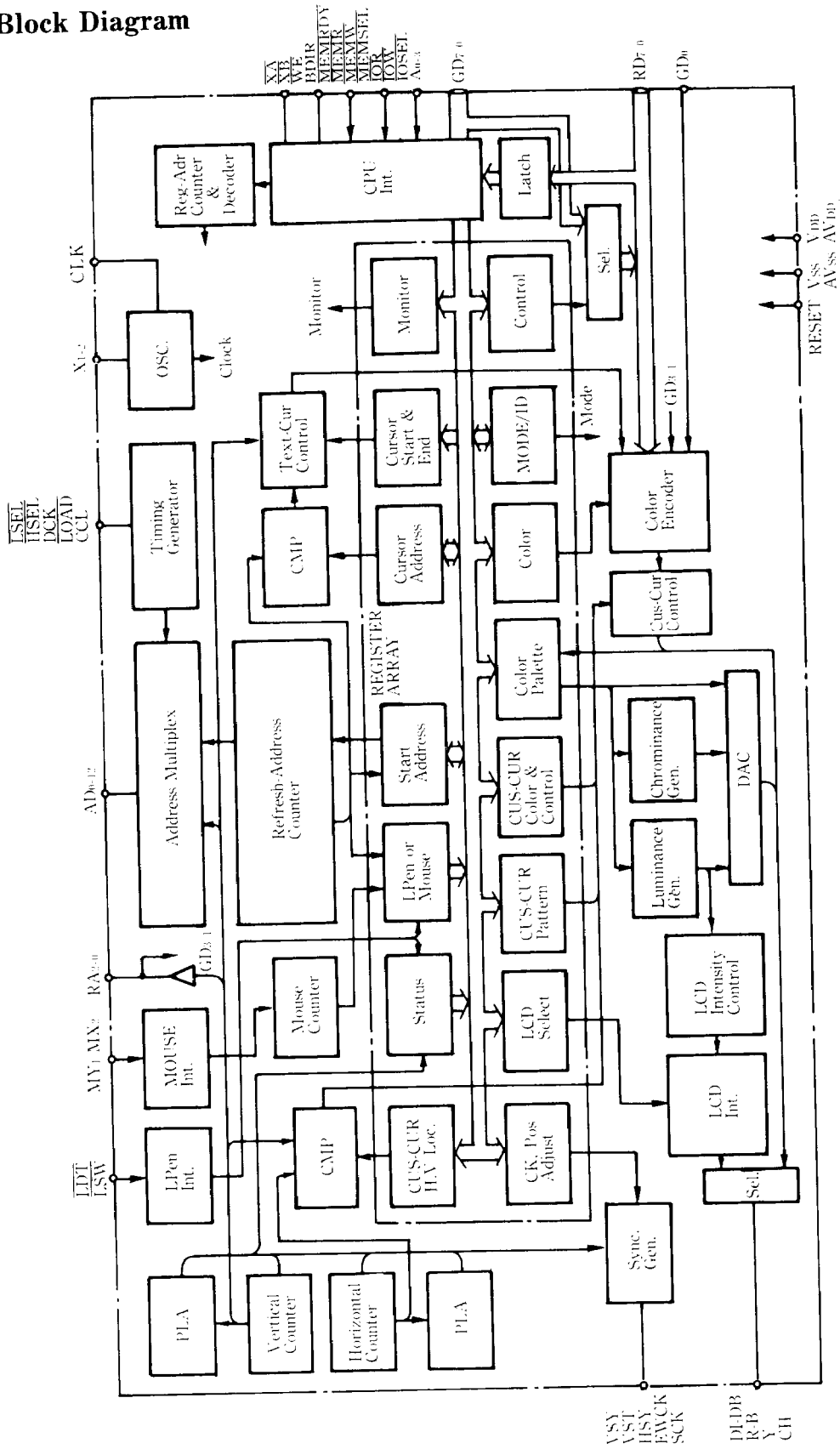
V6355D (LCDC) is a silicon gate CMOS device. This controller can be connected to both LCD and CRT displays. It is software compatible with IBM-PC and has a function to expand it.

V6355-DF is a 100 pin plastic flat package (QFP) type and V6355-DJ is a 84 pin plastic chip carrier type.

■ FEATURES

- Capable of controlling both LCD and CRT displays.
- Includes 6845 restricted mode and CRT peripheral circuits for IBM-PC.
- Both SRAM and DRAM are usable as VRAM.
- Includes MOUSE and LIGHT PEN interface.
- Cursor position can be specified by any 16×16 dot patterns in the bit unit (AND and EXOR screens).
- Includes color palette (16/512 colors).
- LCD intensity controllable (16 or 8 gradation steps)
- Screen modes are available in combinations of the following.
 - Horizontal dot number: 640, 320, 512, 256
 - Vertical dot number: 192, 200, 204, 64 (64 only with LCD)
 - Raster adjustment: 0, 2, 4 or 6 specifiable
- Capable of displaying 16 colors in 640×204 by using external circuits.
- CRT monitor selectable from among IBM Color, Monochrome, NTSC system and PAL system.
- Can be interfaced with 3 types of LCD driver.
- Usable with 16 bit bus CPU.

LCDC Block Diagram

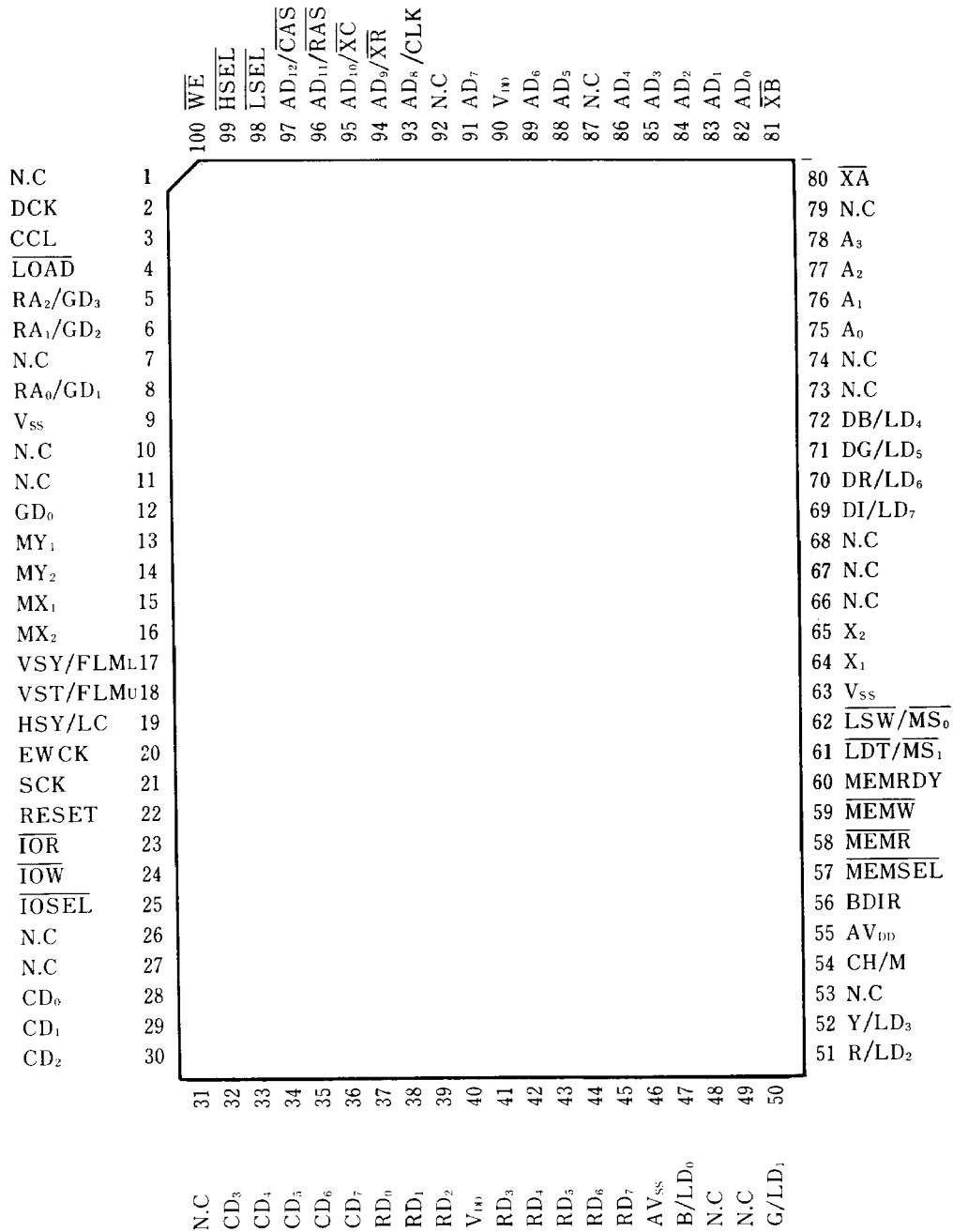


■ Pin Functions

Signature	I/O	Description	
$\overline{\text{IOR}}$	I	Read enable for I/O register, Active at low level	
$\overline{\text{IOW}}$	I	Write enable for I/O register, Active at low level	
$\overline{\text{IOSEL}}$	I	High-order bit decode signal of I/O register address signal, selected at low level	
A ₀ A ₁ A ₂ A ₃	I I I I	I/O register address signal	
$\overline{\text{MEMSEL}}$	I	High-order bit decode signal of memory address signal, selected at low level	
$\overline{\text{MEMR}}$	I	Read enable for memory, Active at low level	
$\overline{\text{MEMW}}$	I	Write enable for memory, Active at low level	
$\overline{\text{MEMRDY}}$	O	Memory (VRAM) access ready signal, Busy (wait) at low level (High impedance state when memory non-selected ($\overline{\text{MEMSEL}}$ = high level))	
$\overline{\text{WE}}$	O	Write enable for memory	
$\overline{\text{BDIR}}$	O	Direction control of bi-directional buffer (for CPU data bus)	
$\overline{\text{RESET}}$	I	Reset signal	
CD ₀ ⋮ CD ₇	I/O I/O I/O	Data bus with CPU	
RD ₀ ⋮ RD ₇	I/O I/O I/O	Data bus with VRAM	
AD ₀ ⋮ AD ₇	O O O	VRAM address	
AD ₈ / $\overline{\text{CLK}}$ AD ₉ / $\overline{\text{XR}}$ AD ₁₀ / $\overline{\text{XC}}$ AD ₁₁ / $\overline{\text{RAS}}$ AD ₁₂ / $\overline{\text{CAS}}$ $\overline{\text{XB}}$ $\overline{\text{XA}}$	O O O O O O	At SRAM	At DRAM
		VRAM address	Outputs external clock dividing signal of 14.31818MHz. Usable for CPU clock by dividing. CPU row Address enable CPU column Address enable
		do.	$\overline{\text{RAS}}$
		do.	$\overline{\text{CAS}}$
		do.	—
		do.	—
Data enable when memory read/write	—		
Memory read/write timing (CPU address enable at SRAM)	—		
$\overline{\text{LSEL}}$ $\overline{\text{HSEL}}$	O O	At SRAM (8bit CPU)	16bit CPU
		1st 8K byte selected 2nd 8K byte selected	Low byte selected High byte selected

Signature	I/O	Description	
		A/N Mode	640 × 200 Color mode
RA ₂ /GD ₃ RA ₁ /GD ₂ RA ₀ /GD ₁ GD ₀	I/O I/O I/O I	Raster address (Output) Dot data for character display	Graphic data (Input)
		CRT	LCD
VS _Y /FLM _L VS _T /FLM _U HS _Y /LC EWCK SCK	O O O O O	Vertical synchronizing signal Vertical retrace line period Horizontal synchronizing signal Display valid period	Lower block FLM Upper block FLM Latch clock Driver enable signal or tone graduation intensifying signal Shift clock
CH/M Y/LD ₃ R/LD ₂ G/LD ₁ B/LD ₀ DI/LD ₇ DR/LD ₆ DG/LD ₅ DB/LD ₄	O O O O O O O O O	Chrominance signal Brightness (black/white composite) signal Output for linear RGB Output for IBM monitor	Signal to change into AC Data output for upper block Data output for lower block
DCK CCL LOAD	O O O	Dot shift clock (for P/S) VRAM data latch clock Load signal for P/S	
MY ₁ MY ₂ MX ₁ MX ₂ LDT/MS ₁ LSW/MS ₀	I I I I I I	Counter pulse for MOUSE Y direction Counter pulse for MOUSE X direction Light pen detect signal or mouse switch signal Switch signal of light pen or mouse	
X ₁ X ₂ AVSS AVDD VSS VSS VDD VDD	I O I I I I I I	For X'tal oscillation, Input to X ₁ when inputting external clock 0V +5V 0V 0V +5V +5V Analog (for DAC) power supply Digital power supply	

Pin Assignment



■ Electrical Characteristics

① Absolute maximum ratings

Parameter	Signature	Min.	Max.	Unit
Supply voltage	V _{DD}	-0.5	+7.0	V
Input voltage	V _I	-0.5	V _{DD} +0.5	V
Output voltage	V _O	-0.5	V _{DD} +0.5	V
Operating temperature	T _{OP}	0	+70	°C
Storage temperature	T _{STG}	-50	+125	°C

(V_{SS}, AV_{SS}=0.0V as standard)

② Recommended conditions for use

Parameter	Signature	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}	4.75	5.0	5.25	V
Operating temperature	T _{OP}	0	25	70	°C

Used with V_{DD} and AV_{DD} at the same voltage and V_{SS}, AV_{SS}=0.0V.

③ DC characteristics

Parameter	Signature	Conditions	Min.	Max.	Unit
High-level output voltage (TTL)	V _{OH}	I _{OH} =-0.4mA	2.7		V
Low-level output voltage (TTL)	V _{OL}	I _{OL} =0.8mA		0.4	V
High-level output voltage (CMOS)	V _{OH}	I _{OH} <1μA	V _{DD} -0.4		V
Low-level output voltage (CMOS)	V _{OL}	I _{OL} <1μA		0.4	V
High-level input voltage	V _{IH}		2.2		V
Low-level input voltage	V _{IL}			0.8	V
High-level output current	I _{OH}	V _{OH} =2.7V	-0.4		mA
Low-level output current	I _{OL}	V _{OL} =0.4V	0.8		mA
Input leak current	I _L		-10	10	μA
Output leak current (tri-state)	I _{LZ}		-10	10	μA
Supply current (at normal operation)	I _{DD}	R _L =5.6KΩ		70	mA
Supply current (at standby)	I _{DD}	R _L =5.6KΩ		50	mA
High-level clock input voltage	V _{CH}		3.6		V
Low-level clock input voltage	V _{CL}			0.6	V

• V_{DD}, AV_{DD}=5.0V ± 5%, T_{OP}=0~70°C

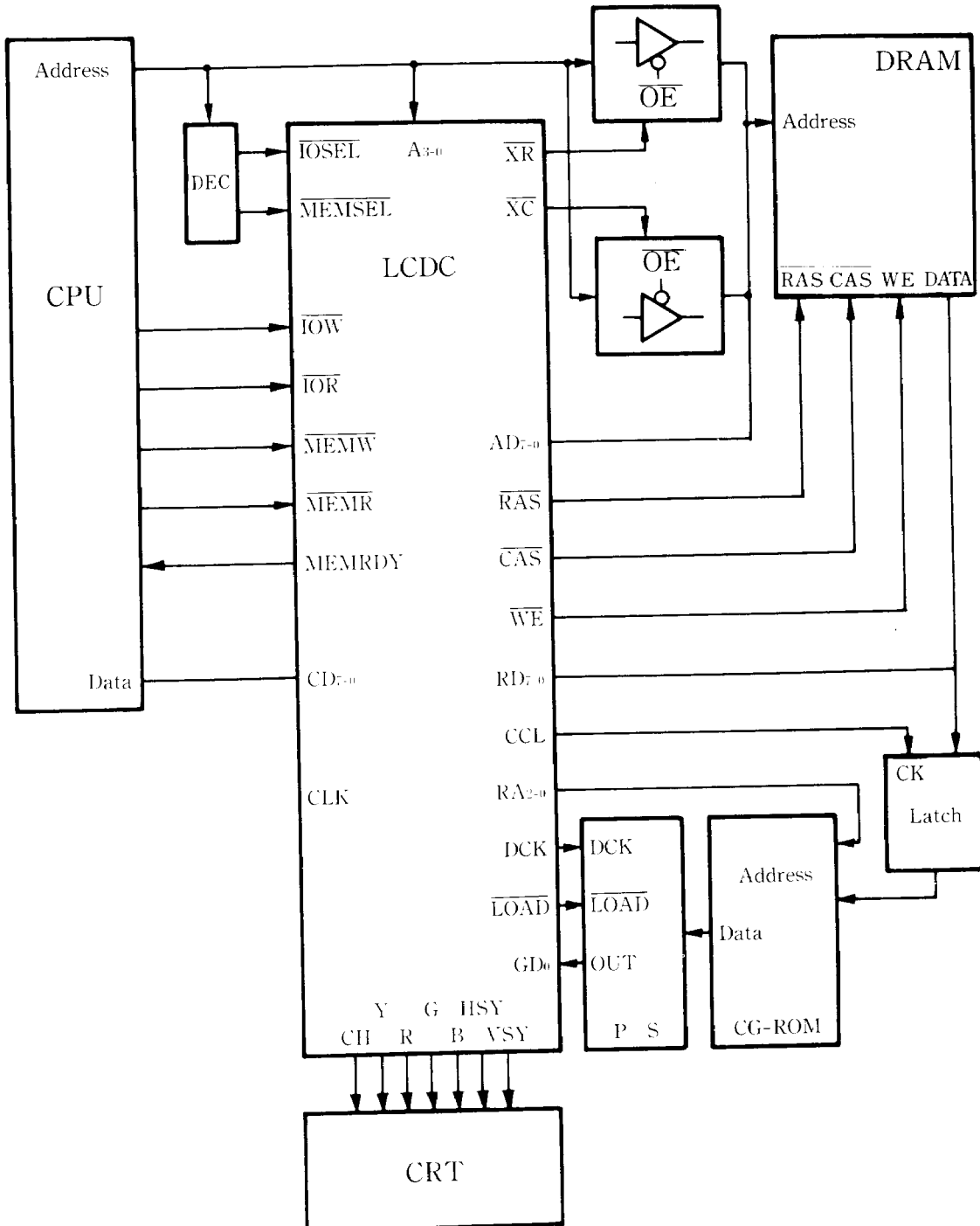
Supply voltage is obtained by adding mean current at V_{DD} and AV_{DD} terminals.

• R_L: Terminal resistance between Y, R, G, B, CH terminals and GND.

Output leak current (tri-state) is for when CD₀₋₇, RD₀₋₇ and RA₂/GD₃~RA₀/D₁ are in the input mode and when AD₀~AD₁₂ $\overline{\text{CAS}}$, $\overline{\text{LSEL}}$, $\overline{\text{HSEL}}$ and MEMRDY are in the high impedance mode.

■ System Configuration (Examples)

① When using CRT display (DRAM used)



② When using LCD display (SRAM used)

