NEC

MOS INTEGRATED CIRCUIT

μPD42S4400L, 424400L

3.3 V OPERATION 4 M-BIT DYNAMIC RAM 1 M-WORD BY 4-BIT, FAST PAGE MODE

DESCRIPTION ★

The μPD42S4400L, 424400L are 1 048 576 words by 4 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

Besides, the μPD42S4400L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packed in 26-pin plastic TSOP and 26-pin plastic SOJ.

FEATURES ★

- 1 048 576 words by 4 bits organization
- Single +3.3 V±0.3 V power supply
- Fast page mode
- The μPD42S4400L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S4400L	1 024 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.36 mW (CMOS level input)
μPD424400L	1 024 cycles/16 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1 8 mW (CMOS level input)

- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN)
μPD42S4400L-A60, 424400L-A60	288 mW	60 ns	120 ns	40 ns
μPD42S4400L-A70, 424400L-A70	252 mW	70 ns	130 ns	45 ns
μPD42S4400L-A80, 424400L-A80	216 mW	80 ns	150 ns	50 ns
μPD42S4400L-A10, 424400L-A10	180 mW	100 ns	180 ns	60 ns

- Mutiplexed address inputs……Row address:A0-A9, Column address:A0-A9

The information in this document is subject to change without notice.

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The mark ★ shows revised points.

★ ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μPD42S4400LGS-A60-9JD	60 ns	26-pin Plastic TSOP (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S4400LGS-A70-9JD	70 ns		
μPD42S4400LGS-A80-9JD	80 ns		
μPD42S4400LGS-A10-9JD	100 ns		
μPD42S4400LGS-A60-9KD	60 ns	26-pin Plastic TSOP Reverse bent (300 mil)	
μPD42S4400LGS-A70-9KD	70 ns		
μPD42S4400LGS-A80-9KD	80 ns		
μPD42S4400LGS-A10-9KD	100 ns		
μPD42S4400LLA-A60	60 ns	26-pin Plastic SOJ (300 mil)	
μPD42S4400LLA-A70	70 ns		
μPD42S4400LLA-A80	80 ns		
μPD42S4400LLA-A10	100 ns		
μPD424400LGS-A60-9JD	60 ns	26-pin Plastic TSOP (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD424400LGS-A70-9JD	70 ns		
μPD424400LGS-A80-9JD	80 ns		
μPD424400LGS-A10-9JD	100 ns		
μPD424400LGS-A60-9KD	60 ns	26-pin Plastic TSOP Reverse bent (300 mil)	
μPD424400LGS-A70-9KD	70 ns		
μPD424400LGS-A80-9KD	80 ns		
μPD424400LGS-A10-9KD	100 ns		
μPD424400LLA-A60	60 ns	26-pin Plastic SOJ (300 mil)	
μPD424400LLA-A70	70 ns		
μPD424400LLA-A80	80 ns		
μPD424400LLA-A10	100 ns		

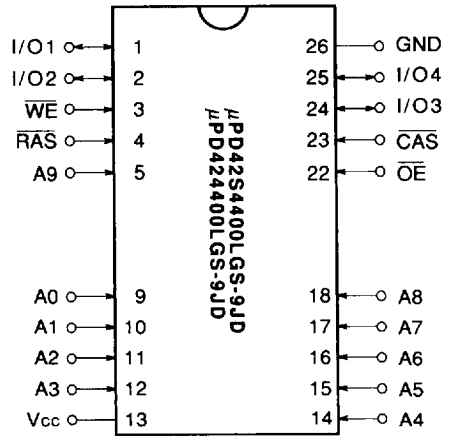
QUALITY GRADE

STANDARD

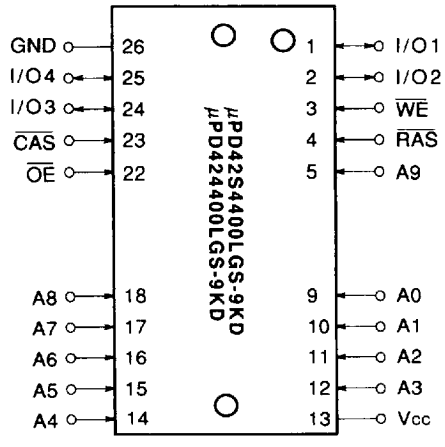
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS (Marking Side) ★

26-pin Plastic TSOP (300 mil)

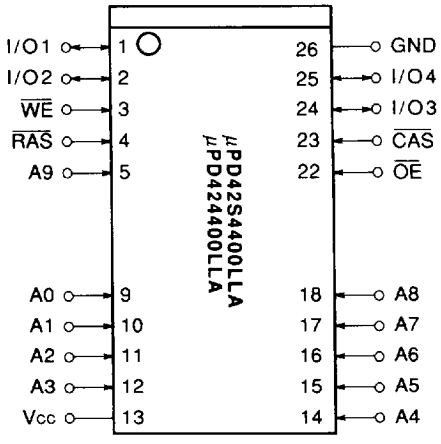


Reverse bent

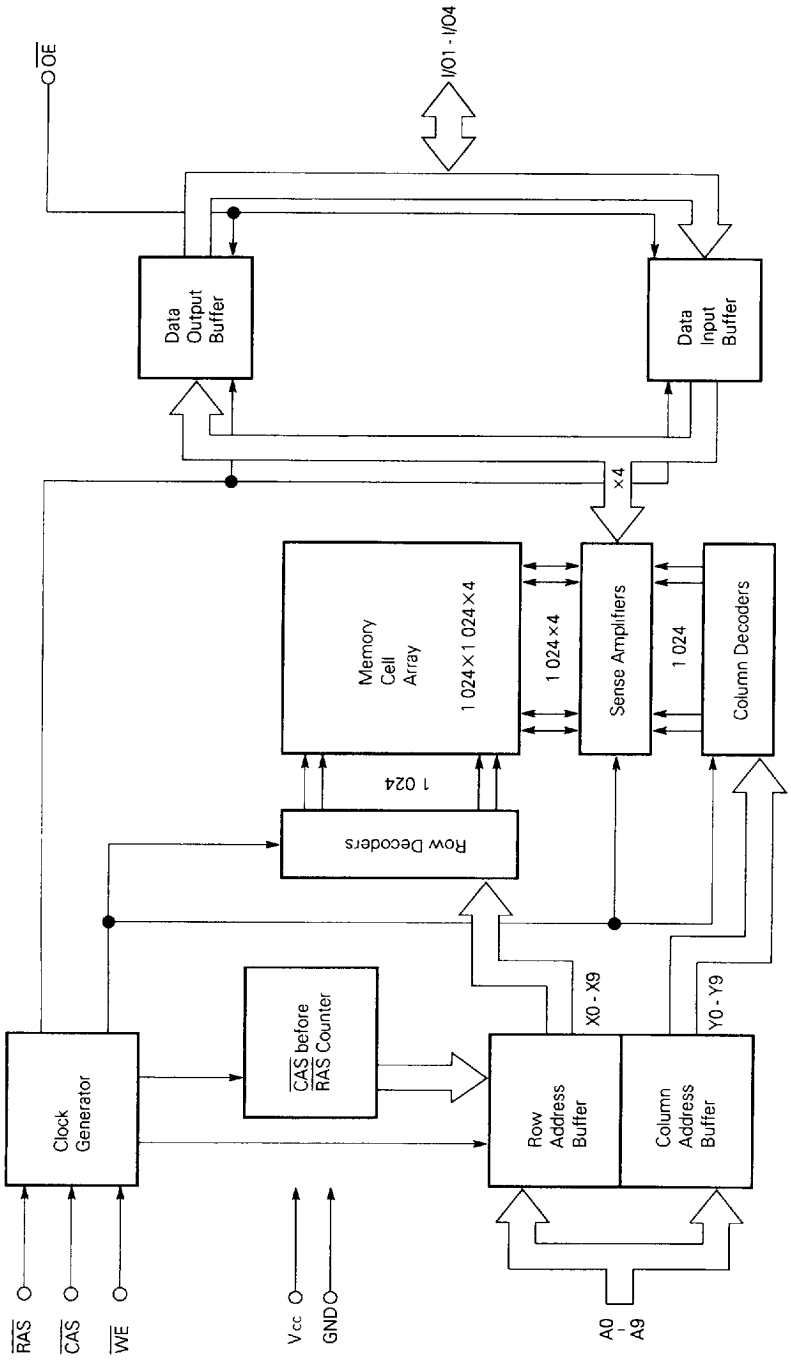


A0 to A9	: Address Inputs
I/O1 to I/O4	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{CAS}$	: Column Address Strobe
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Supply Voltage
GND	: Ground

26-pin Plastic TSOP (300 mil)



★ **BLOCK DIAGRAM**



INPUT/OUTPUT PIN FUNCTIONS ★

The μPD42S4400L, 424400L have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A9 and input/output pins I/O1 to I/O4.

Pin name	Input/ output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh.
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address input)		Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data input/output)	Input/ Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

ELECTRICAL SPECIFICATIONS Notes 1, 2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Ambient temperature	T_a		0		70	°C

CAPACITANCE (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A9			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output capacitance	C_D	I/O1 to I/O4			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted) ★

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Note
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN)}$ I_O = 0 mA	t_{RAC} = 60 ns		80	mA	3,4
				t_{RAC} = 70 ns		70		
				t_{RAC} = 80 ns		60		
				t_{RAC} = 100 ns		50		
Standby current	μPD42S4400L	I_{CC2}	$V_{IH(MIN)} \leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.5	mA	
			V_{CC}−0.2 V $\leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.1		
	μPD424400L		$V_{IH(MIN)} \leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		2		
			V_{CC}−0.2 V $\leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling $V_{IH(MIN)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN)}$ I_O = 0 mA	t_{RAC} = 60 ns		80	mA	3,4
				t_{RAC} = 70 ns		70		
				t_{RAC} = 80 ns		60		
				t_{RAC} = 100 ns		50		
Operating current (Fast page mode)		I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS} \leqq V_{IL(MAX)}$ $t_{PC} = t_{PC(MIN)}$ I_O = 0 mA	t_{RAC} = 60 ns		70	mA	3,4
				t_{RAC} = 70 ns		60		
				t_{RAC} = 80 ns		50		
				t_{RAC} = 100 ns		40		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN)}$ I_O = 0 mA	t_{RAC} = 60 ns		80	mA	3,4
				t_{RAC} = 70 ns		70		
				t_{RAC} = 80 ns		60		
				t_{RAC} = 100 ns		50		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1 024 cycles/128 ms, only for μPD42S4400L)		I_{CC6}	Standby : V_{CC}−0.2 V $\leqq \overline{RAS}$ $\overline{CAS} \leqq$ 0.2 V or V_{CC}−0.2 V $\leqq \overline{CAS}$ $\overline{CAS}$ before $\overline{RAS}$ Refresh : 1 024 cycles/128 ms $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}−0.2 V $\leqq V_{IH} \leqq V_{IH(MAX)}$ $\overline{WE}$, $\overline{OE}$: V_{IH} Address input : V_{IH} or V_{IL} Output : Don't care	$t_{RAS} \leqq$ 200 ns		100	μA	3,4
				$t_{RAS} \leqq$ 1 μs		150		
Self refresh current (CAS before RAS self refresh, only for μPD42S4400L)		I_{CC7}	I_O = 0 mA $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}−0.2 V $\leqq V_{IH} \leqq V_{IH(MAX)}$			100	μA	
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V all other pins except for testing pin = 0 V		−5	+5	μA	
Output leakage current		$I_{O(L)}$	Outputs are disabled (Hi-Z) V_O = 0 to 3.6 V		−5	+5	μA	
High level output voltage		V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

★ AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted) Notes 5, 6

(1/2)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	120		130		150		180		ns	7
Read Modify Write Cycle Time	t_{RWC}	165		175		200		240		ns	7
Fast Page Mode Cycle Time (Read or Write)	t_{PC}	40		45		50		60		ns	7
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		100		120		ns	7
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	8, 9
Access Time from $\overline{CAS}$ (Falling Edge)	t_{CAC}		20		20		20		25	ns	8, 9
Access Time from Column Address	t_{AA}		30		35		40		50	ns	8, 9
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45		55	ns	9
Access Time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	17	50	ns	8
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		0		ns	9
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	t_{OFF}	0	15	0	15	0	20	0	25	ns	10
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		25		ns	
Output Buffer Turn-off Delay Time ($\overline{OE}$)	t_{OEZ}	0	15	0	15	0	20	0	25	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time	t_{OES}	0		0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50		50		60		70		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)	t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		20		20		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	25	70	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		10		ns	11
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		15		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	12

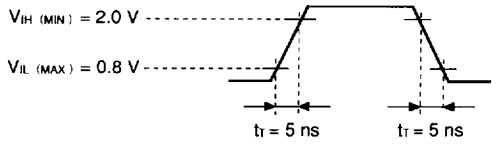
(2/2)

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Command Hold Time Referenced to $\overline{CAS}$		t_{WCH}	15		15		15		20		ns	13
Write Command Pulse Width		t_{WP}	15		15		15		20		ns	13
Data-in Setup Time		t_{DS}	0		0		0		0		ns	14
Data-in Hold Time		t_{DH}	15		15		15		20		ns	14
$\overline{WE}$ Command Setup Time		t_{WCS}	0		0		0		0		ns	15
$\overline{CAS}$ to $\overline{WE}$ Delay Time		t_{CWD}	40		40		45		55		ns	15
$\overline{RAS}$ to $\overline{WE}$ Delay Time		t_{RWD}	80		90		105		130		ns	15
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)		t_{CPWD}	55		60		70		85		ns	15
Column Address Delay Time Referenced to $\overline{WE}$		t_{AWD}	50		55		65		80		ns	15
Write Command Lead Time Referenced to $\overline{RAS}$		t_{RWL}	20		20		20		25		ns	
Write Command Lead Time Referenced to $\overline{CAS}$		t_{CWL}	15		15		15		20		ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh		t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh		t_{CHR}	15		15		15		20		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)		t_{RASS}	100		100		100		100		μs	16
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)		t_{RPS}	130		130		150		180		ns	16
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)		t_{CHS}	−50		−50		−50		−50		ns	16
$\overline{WE}$ Setup Time		t_{WSR}	10		10		10		10		ns	
$\overline{WE}$ Hold Time		t_{WHR}	15		15		15		20		ns	
Refresh Time	μPD42S4400L	t_{REF}		128		128		128		128	ms	16
	μPD424400L			16		16		16		16		

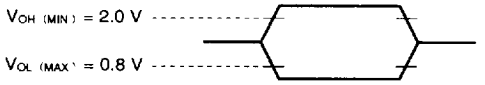
Notes

1. All voltages are referenced to GND.
2. An initial pause of 100 μs is required after power up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on t_{RC} and t_{PC} Specified values are obtained with outputs open.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
5. AC measurements assume t_T = 5 ns.
6. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



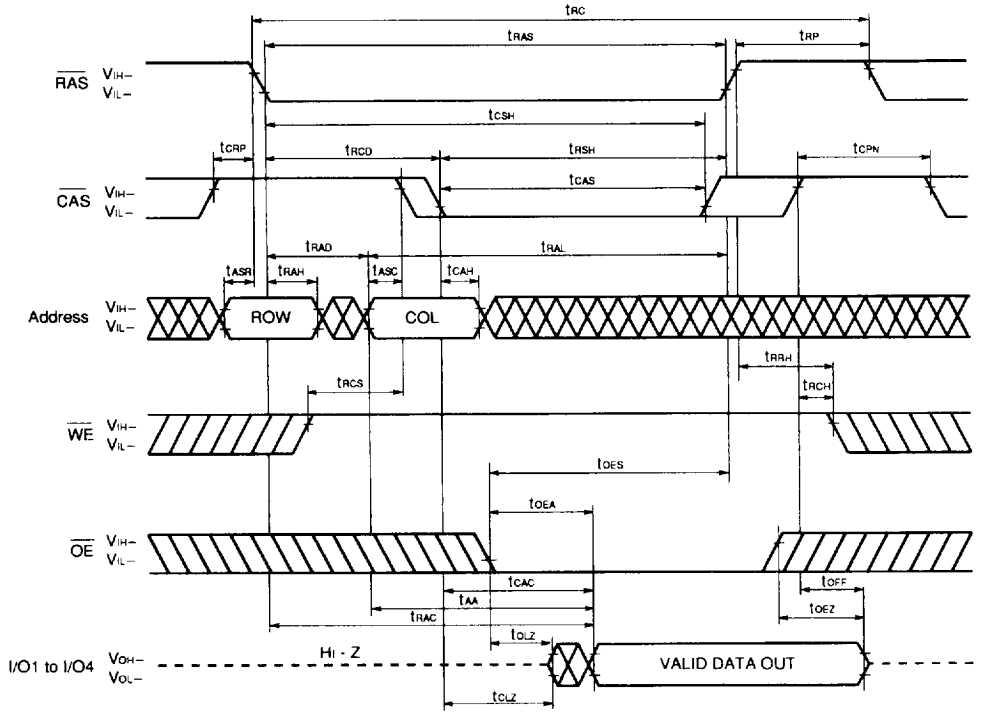
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70 °C) is assured.
8. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

CONDITION	ACCESS TIME
$t_{RAD} \leqq t_{RAD\,(MAX)}$ and $t_{RCD} \leqq t_{RCD\,(MAX)}$	$t_{RAC\,(MAX)}$
$t_{RAD\,(MAX)} \leqq t_{RAD}$ and $t_{RCD} \leqq t_{RCD\,(MAX)}$	$t_{AA\,(MAX)}$
$t_{RCD\,(MAX.)} \leqq t_{RCD}$	$t_{CAC\,(MAX)}$

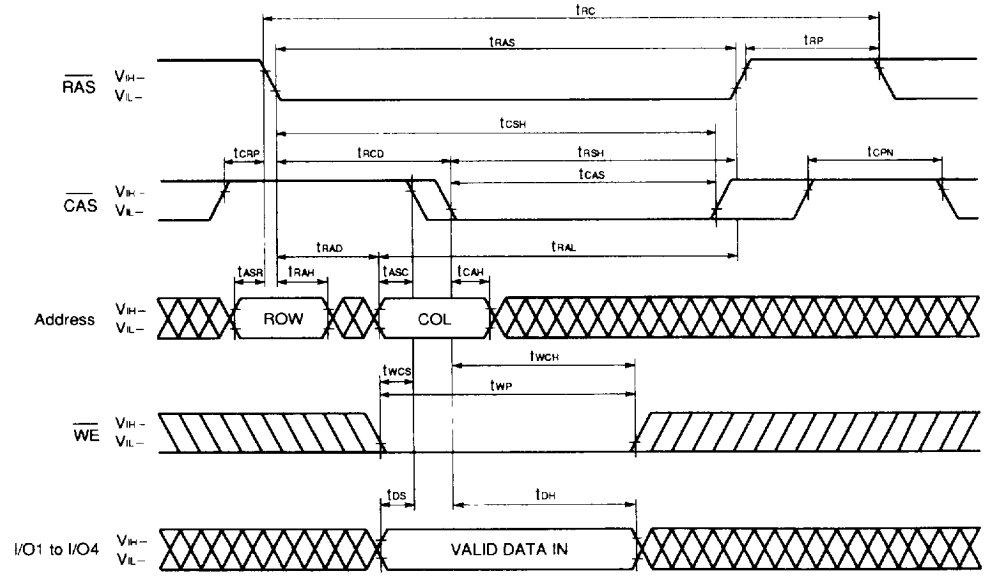
$t_{RAD\,(MAX)}$ and $t_{RCD\,(MAX)}$ indicate the points which the access time changes and are not the limits of operation.

9. Loading conditions are 1 TTL and 100 pF.
10. $t_{OFF\,(MAX)}$ and $t_{OEZ\,(MAX)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
11. $t_{CRP\,(MIN)}$ requirement should be applicable for $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycles.
12. Either $t_{RCH\,(MIN)}$ or $t_{RRH\,(MIN)}$ must be satisfied for a read cycle.
13. $t_{WP\,(MIN)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH\,(MIN.)}$ should be satisfied.
14. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD} t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS\,(MIN)} \leqq t_{WCS}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle. If $t_{RWD\,(MIN)} \leqq t_{RWD}$, $t_{CWD\,(MIN.)} \leqq t_{CWD}$, $t_{AWD\,(MIN)} \leqq t_{AWD}$ and $t_{CPWD\,(MIN)} \leqq t_{CPWD}$, the cycle is a read modify write cycle and condition of the data out (at access time) is indeterminate.
16. This specification is applicable only for μPD42S4400L.

READ CYCLE

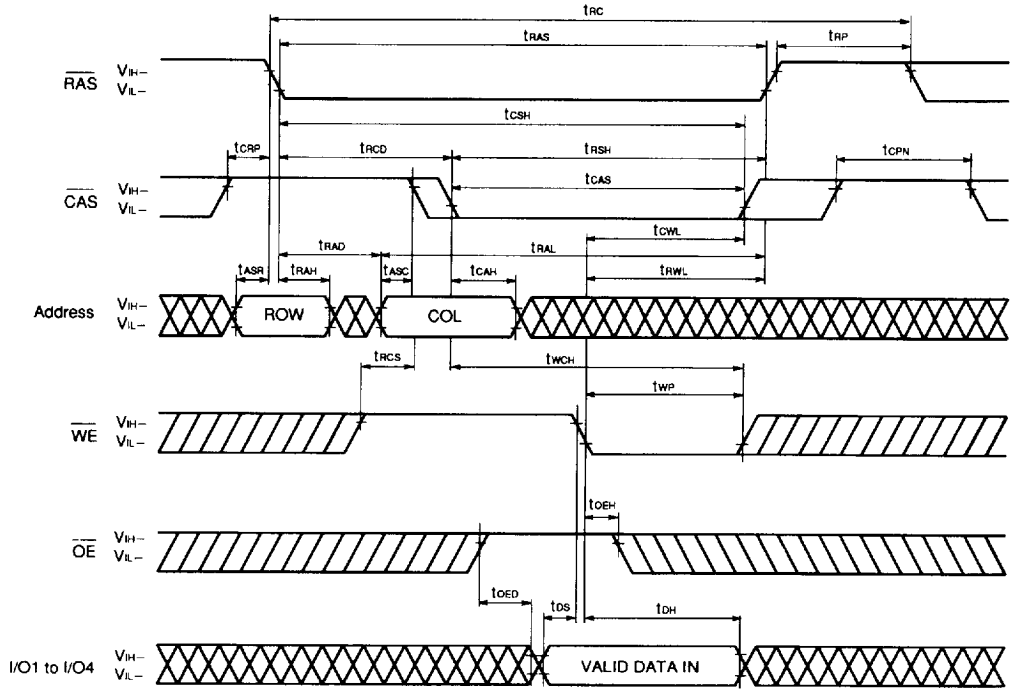


EARLY WRITE CYCLE

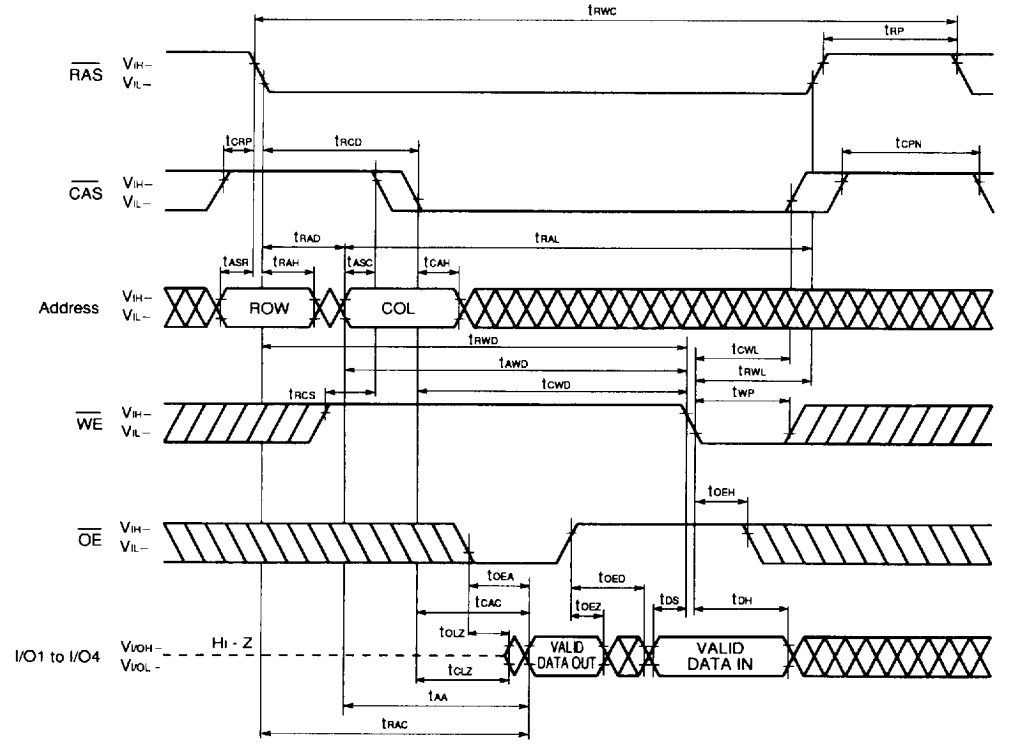


Remark $\overline{OE}$ = Don't Care

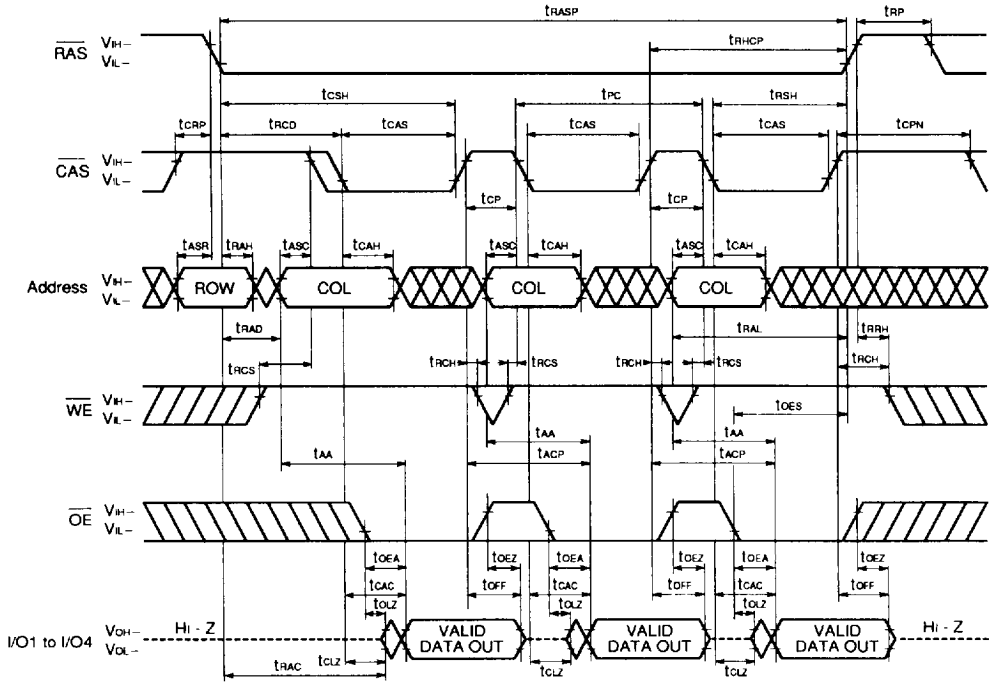
LATE WRITE CYCLE



READ MODIFY WRITE CYCLE

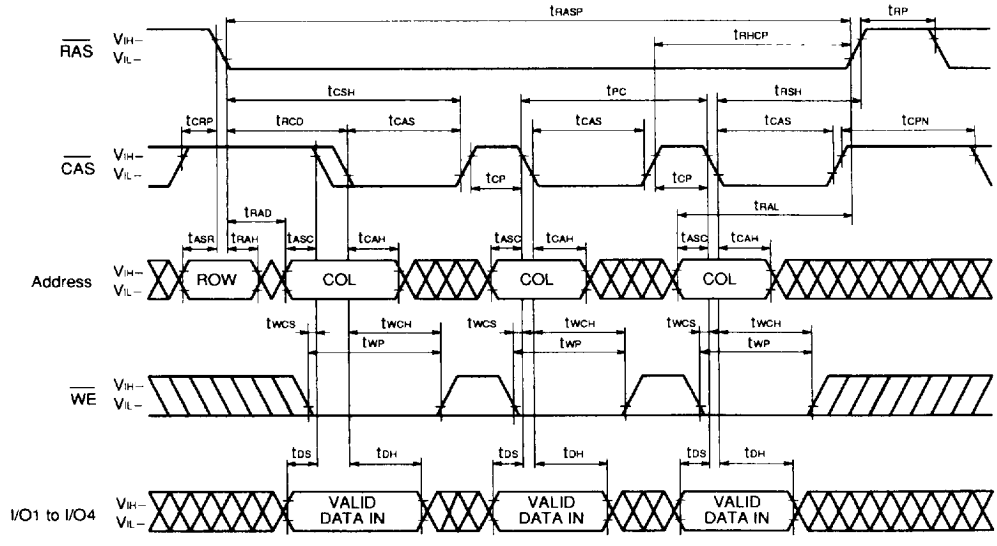


FAST PAGE MODE READ CYCLE



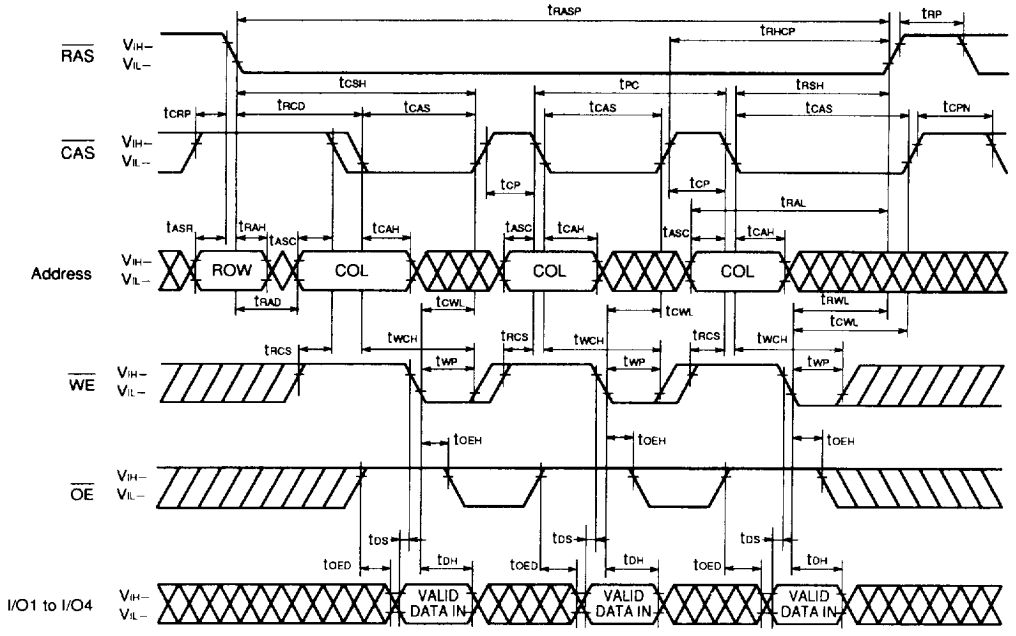
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle

FAST PAGE MODE EARLY WRITE CYCLE



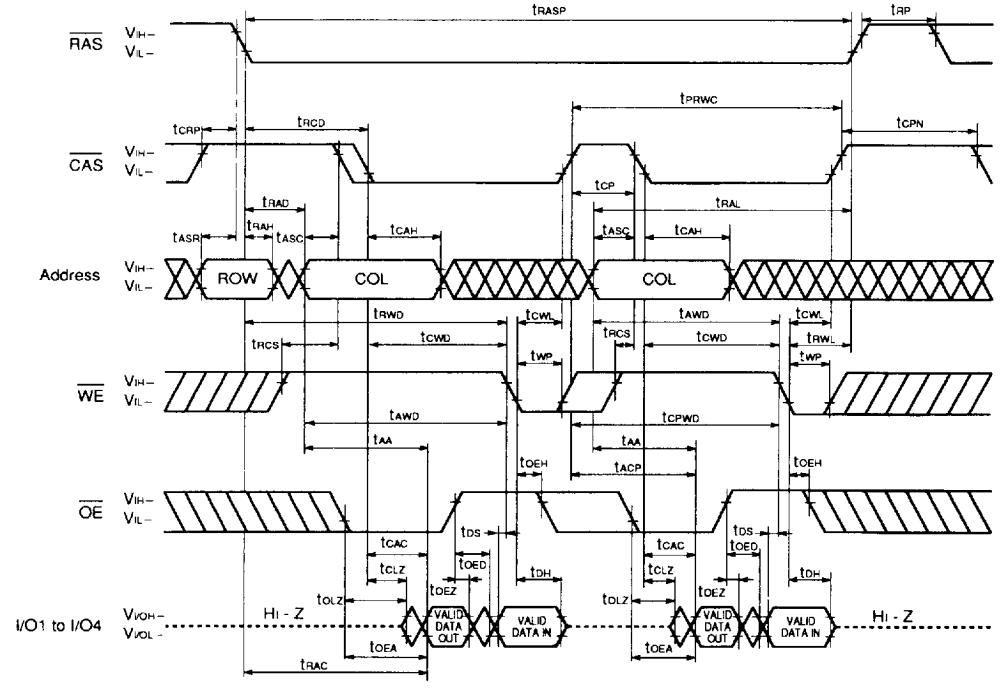
Remark $\overline{OE}$ = Don't Care
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle

FAST PAGE MODE LATE WRITE CYCLE



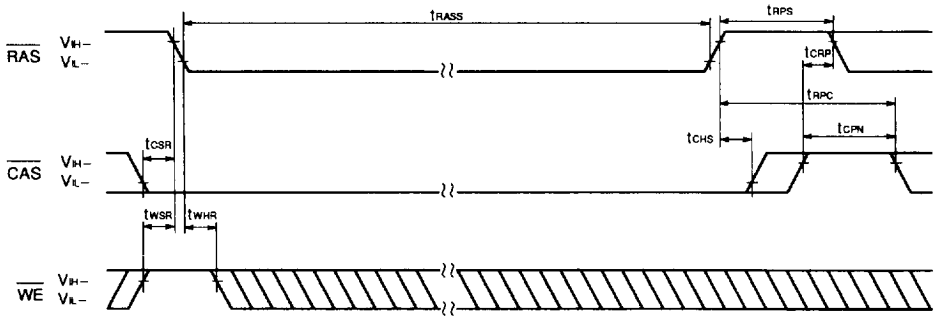
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle

FAST PAGE MODE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle

$\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE (Only for μPD42S4400L) ★



Remark Address, $\overline{OE}$ = Don't care I/O1 to I/O4 = Hi - Z

How to use $\overline{CAS}$ before $\overline{RAS}$ self refresh mode.

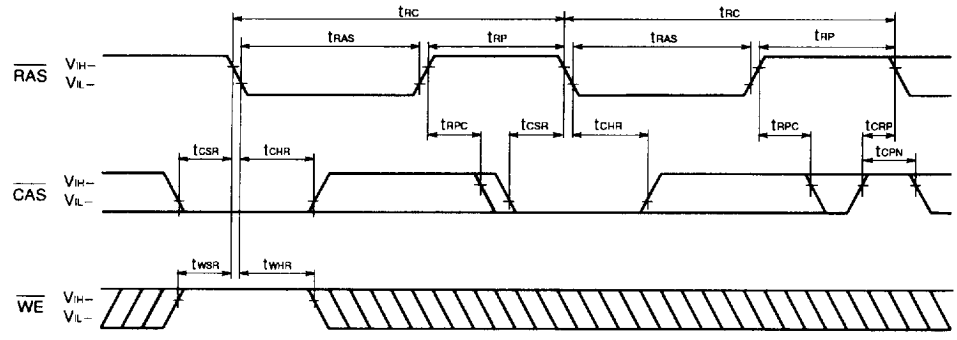
$\overline{CAS}$ before $\overline{RAS}$ self refresh mode can't be used by itself. It must be used with perfoming one of 3 refreshes below.

- **When using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh**
  Refresh 1 024 times during 128 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

- **When using burst $\overline{CAS}$ before $\overline{RAS}$ refresh**
  Refresh 1 024 times during 16 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

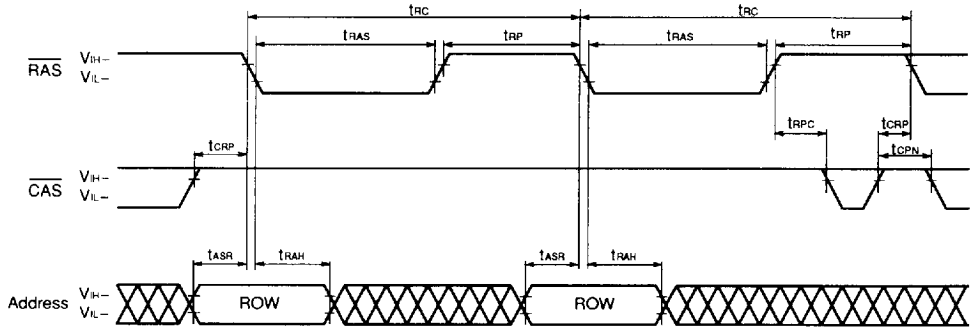
- **When using $\overline{RAS}$ only refresh**
  Refresh against all refresh addresses during 16 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

★ $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



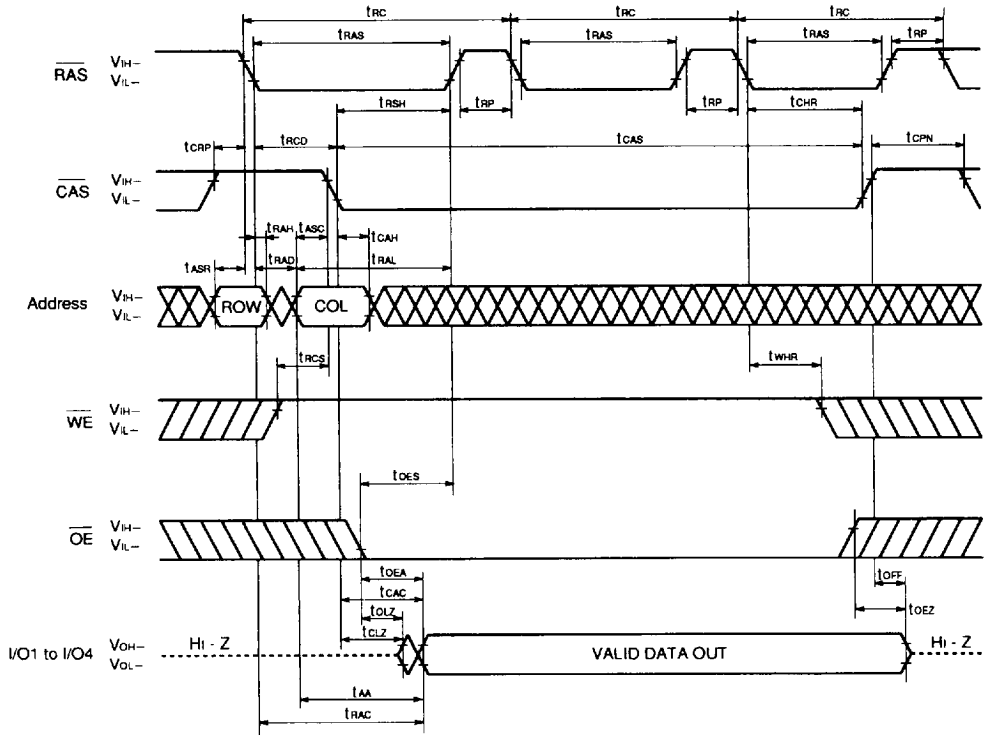
Remark Address, $\overline{OE}$ = Don't care I/O1 to I/O4 = HI - Z

★ $\overline{RAS}$ ONLY REFRESH CYCLE

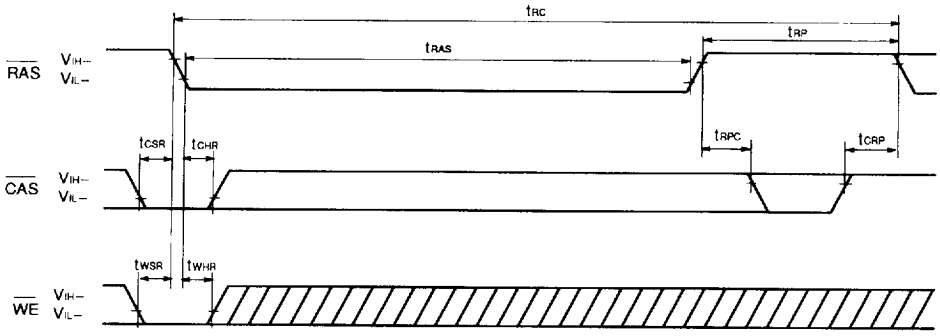


Remark $\overline{WE}$, $\overline{OE}$ = Don't care I/O1 to I/O4 = HI - Z

HIDDEN REFRESH CYCLE



TEST MODE SET CYCLE ($\overline{WE}$ AND $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE)



Remark Address, $\overline{OE}$ = Don't care I/O1 to I/O4 = Hi - Z

TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/2. In this TEST MODE, internal organization is 512 K words by 8 bits apparentry. Don't care about the input levels of the $\overline{CAS}$ input A0.

1. How to enter TEST MODE

Through TEST MODE SET CYCLE ($\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle), the device enters TEST MODE.

2. Write / Read in TEST MODE

Write data of "1" or "0" through I/O1 to I/O4 by controlling address except for above-mentioned address. Each input data through each I/O write 2 bits at once. And read through I/O1 to I/O4 to check written data. If each 2 bits are written rightly, each I/O data is "1". But wrong, the data is "0".

3. Refresh in TEST MODE

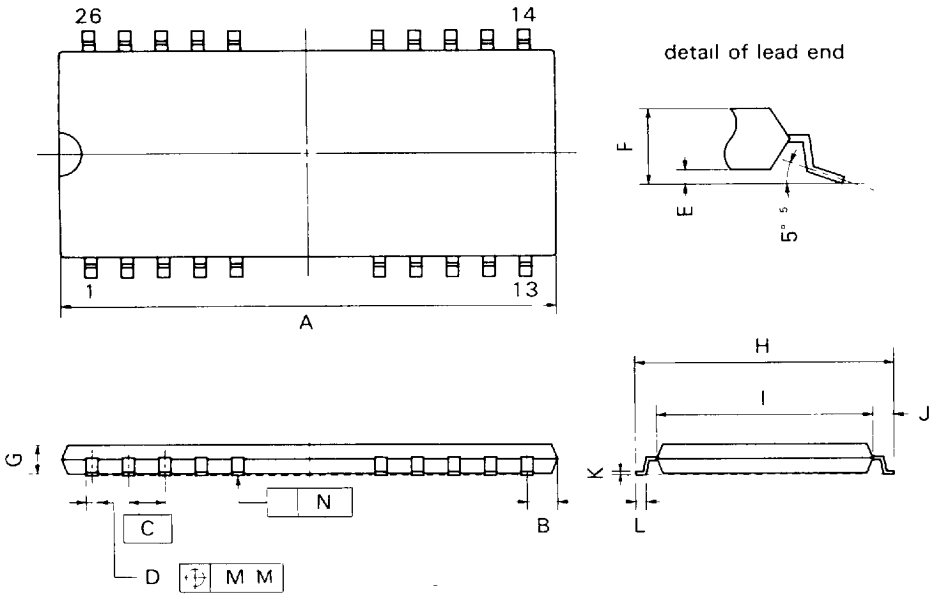
Use normal read cycle or $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

4. How to exit from TEST MODE

Through $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, the device exits from TEST MODE.

PACKAGE DRAWINGS

26 PIN PLASTIC TSOP (300mil)



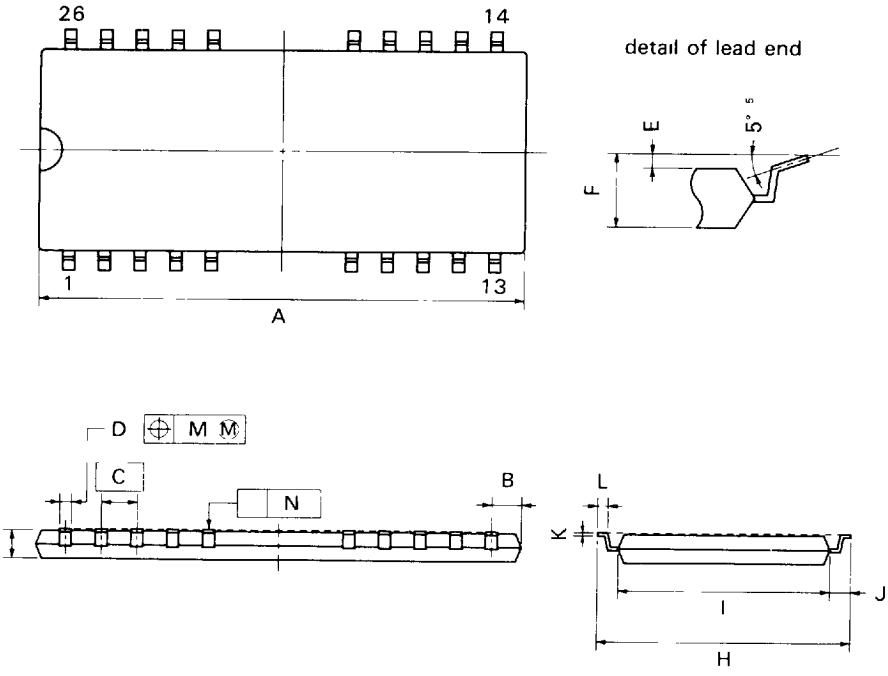
S26GS 50 9JD 1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition

ITEM	MILLIMETERS	INCHES
A	17.54 MAX	0.691 MAX
B	1.18 MAX	0.047 MAX
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}$	$0.016^{+0.004}_{-0.005}$
E	$0.05^{\pm0.05}$	$0.002^{\pm0.002}$
F	1.13 MAX	0.045 MAX
G	1.0	0.039
H	$9.22^{\pm0.2}$	$0.363^{\pm0.008}$
I	$7.62^{\pm0.1}$	$0.300^{\pm0.004}$
J	$0.8^{\pm0.2}$	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	$0.5^{\pm0.1}$	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC TSOP (300mil)



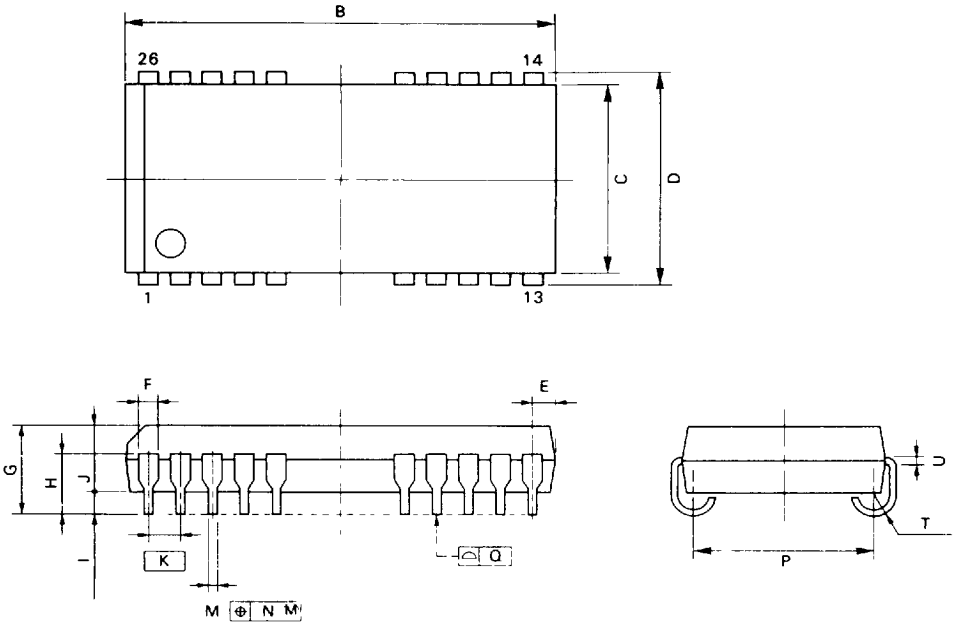
S26GS 50 9KD 1

NOTE

Each lead centerline is located within 0 21 mm (0 009 inch) of its true position (T P) at maximum material condition

ITEM	MILLIMETERS	INCHES
A	17 54 MAX	0 691 MAX
B	1 18 MAX	0 047 MAX
C	1 27 (T P)	0 050 (T P)
D	$0\ 40^{+0\ 10}$	$0\ 016^{+0\ 004}_{-0\ 005}$
E	$0\ 05^{\ 0\ 05}$	$0\ 002^{+0\ 002}$
F	1 13 MAX	0 045 MAX
G	1 0	0 039
H	$9\ 22^{+0\ 2}$	$0\ 363^{+0\ 008}$
I	$7\ 62^{+0\ 1}$	$0\ 300^{-0\ 004}$
J	$0\ 8^{+0\ 2}$	$0\ 031^{-0\ 008}_{0\ 008}$
K	$0\ 125^{-0\ 10}_{0\ 05}$	$0\ 005^{+0\ 004}_{0\ 002}$
L	$0\ 5^{+0\ 1}$	$0\ 020^{+0\ 004}_{0\ 005}$
M	0 21	0 009
N	0 10	0 004

26PIN PLASTIC SOJ (300 mil)



P26LA 50A 1

NOTE
Each lead centerline is located within 0 12 mm (0 005 inch) of its true position (T P) at maximum material condition

ITEM	MILLIMETERS	INCHES
B	17 4 $^{+0.2}_{-0.35}$	0 685 $^{+0.008}_{-0.013}$
C	7 57	0 298
D	8 47 $^{\pm 0.2}$	0 333 $^{+0.009}_{-0.008}$
E	1 08 $^{\pm 0.15}$	0 043 $^{+0.006}_{-0.007}$
F	0 6	0 024
G	3 5 $^{\pm 0.2}$	0 138 $^{\pm 0.008}$
H	2 4 $^{\pm 0.2}$	0 094 $^{+0.009}_{-0.008}$
I	0 8 MIN	0 031 MIN
J	2 6	0 102
K	1 27(T P)	0 050(T P)
M	0 40 $^{\pm 0.10}$	0 016 $^{+0.004}_{-0.005}$
N	0 12	0 005
P	6 73 $^{\pm 0.20}$	0 265 $^{\pm 0.008}$
Q	0 15	0 006
T	R 0 85	R 0 033
U	0 20 $^{+0.10}_{-0.05}$	0 008 $^{+0.004}_{-0.002}$

★ RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μPD42S4400L, 424400L.

TYPE OF SURFACE MOUNT DEVICE

μPD42S4400LGS, 424400LGS : 26-pin Plastic TSOP (300 mil)
μPD42S4400LLA, 424400LLA : 26-pin Plastic SOJ (300 mil)