

# 2 Megabit ROM + 1 Megabit SRAM ROM/RAM Combo

## SST30VR021



Data Sheet

### FEATURES:

- **Organized as 256K x8 ROM + 128K x8 SRAM**
- **ROM/RAM combo on a monolithic chip**
- **Equivalent ComboMemory (Flash + SRAM): SST31LF021E for code development and pre-production**
- **Wide Operating Voltage Range: 2.7-3.3V**
- **Chip Access Time**
  - 2.7V Operation: 500 ns (Max.)
- **Low Power Dissipation:**
  - Standby  
3.0V Operation: 3  $\mu$ W (Typical)
  - Operating  
3.0V Operation: 10 mW (Typical)
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Outputs**
- **Packages Available**
  - 32-Pin TSOP (8mm x 13.4mm)
  - 32-Pin TSOP (8mm x 14mm)

### PRODUCT DESCRIPTION

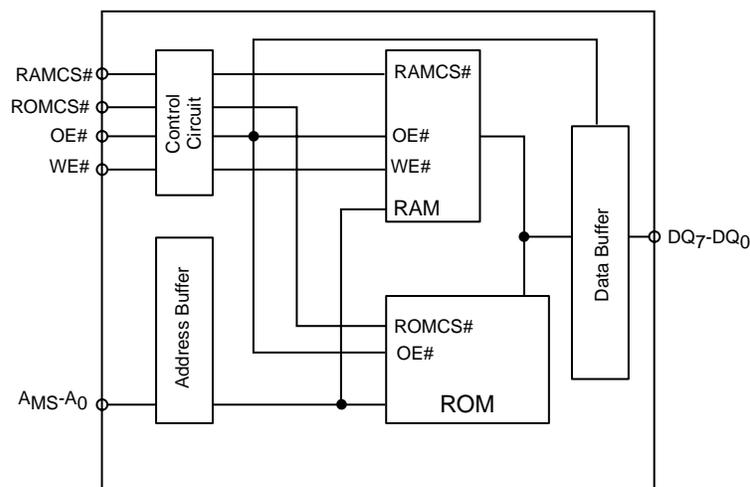
The SST30VR021 is a ROM/RAM combo chip consisting of 2 Mbit Read Only Memory organized as 256 KBytes and a 1 Mbit Static Random Access Memory organized as 128 KBytes.

The device is fabricated using SST's advanced CMOS low power processing technology.

The SST30VR021 has an output enable input for precise control of the data outputs. It also has two separate chip enable inputs for selection of either ROM or RAM and for minimizing current drain during power-down mode.

The SST30VR021 is particularly well suited for use with low voltage supplies (2.7-3.3V) such as pagers, organizers and other handheld applications.

### FUNCTIONAL BLOCK DIAGRAM OF SST30VR021 ROM/RAM COMBO





# 2 Megabit ROM + 1 Megabit SRAM ROM/RAM Combo SST30VR021

Data Sheet

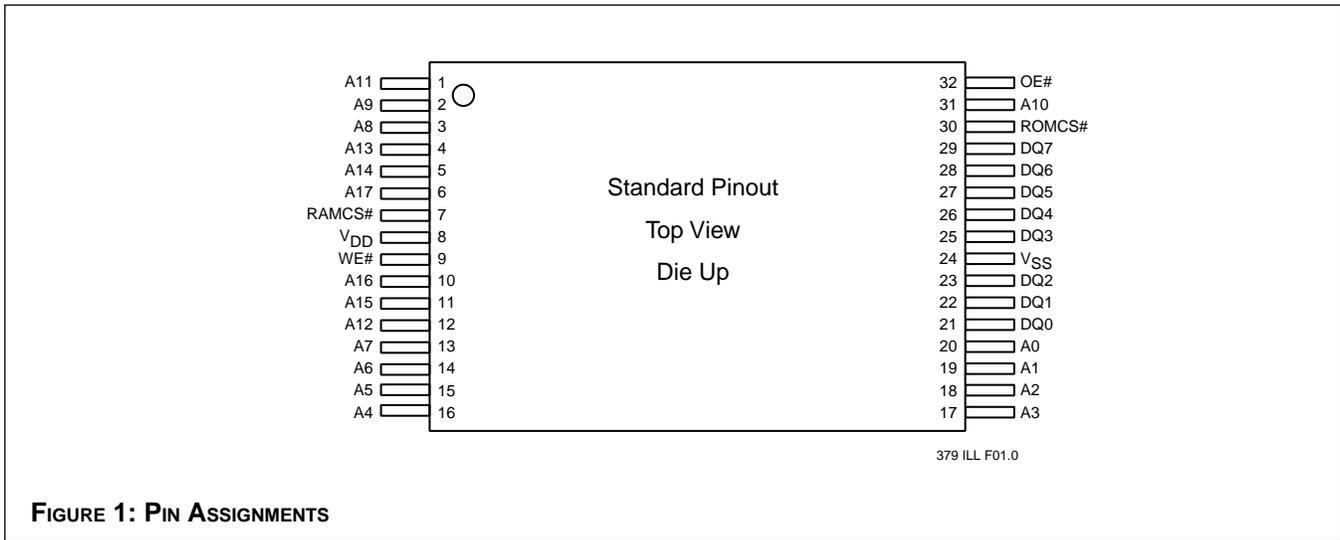


FIGURE 1: PIN ASSIGNMENTS

TABLE 1: PIN DESCRIPTION

Symbol	Pin Name
AMS-A <sub>0</sub>	Address Inputs, A <sub>MS</sub> = A <sub>17</sub> for ROM, A <sub>16</sub> for RAM
WE#	Write Enable Input
OE#	Output Enable
RAMCS#	RAM Enable Input
ROMCS#	ROM Enable Input
DQ <sub>7</sub> -DQ <sub>0</sub>	Data Inputs/Outputs
V <sub>DD</sub>	Power Supply
V <sub>SS</sub>	Ground

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**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Voltage on Any Pin Relative to V<sub>SS</sub> ..... -0.5V to V<sub>DD</sub>+ 0.5V  
 Voltage on V<sub>DD</sub> Supply Relative to V<sub>SS</sub> ..... -0.5 to 4.0V  
 Power Dissipation ..... 1.0W  
 Storage Temperature ..... -65°C to +150°C  
 Operating Temperature ..... -40°C to +85°C  
 Soldering Temperature (10 Seconds Lead Only) ..... 260°C

**OPERATING RANGE**

Range	Ambient Temp	V <sub>DD</sub>
Commercial	0 °C to +70 °C	2.7-3.3V
Extended	-20 °C to +70 °C	2.7-3.3V
Industrial	-40 °C to +85 °C	2.7-3.3V

**AC CONDITIONS OF TEST**

Input Pulse Level	0-V <sub>DD</sub>
Input & Output Timing Reference Levels	V <sub>DD</sub> /2
Input Rise/Fall Time	5 ns
Output Load	C <sub>L</sub> = 100 pF



# 2 Megabit ROM + 1 Megabit SRAM ROM/RAM Combo SST30VR021

Data Sheet

**TABLE 2: RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Units
$V_{DD}$	Supply Voltage	2.7	3.3	V
$V_{SS}$	Ground	0	0	V
$V_{IH}$	Input High Voltage	2.4	$V_{DD}+0.5$	V
$V_{IL}$	Input Low Voltage	-0.3	0.3	V

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**TABLE 3: DC OPERATING CHARACTERISTICS**

Symbol	Parameter	$V_{DD} = 3.0 \pm 0.3V$			Test Conditions
		Min	Max	Units	
$I_{LI}$	Input Leakage Current	-1	1	$\mu A$	$V_{IN} = V_{SS}$ to $V_{DD}$
$I_{LO}$	Output Leakage Current	-1	1	$\mu A$	ROMCS# = RAMCS# = $V_{IH}$ or OE# = $V_{IH}$ or WE# = $V_{IL}$ , $V_{I/O} = V_{SS}$ to $V_{DD}$
$I_{DD1}$	ROM Operating Supply Current		$4.0+1.1(f)$	mA	ROMCS# = $V_{IL}$ , RAMCS# = $V_{IH}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{I/O} =$ Opens
$I_{DD2}$	RAM Operating Supply Current		$2.5+1(f)$	mA	ROMCS# = $V_{IH}$ , RAMCS# = $V_{IL}$ , $I_{I/O} =$ Opens
$I_{SB}$	Standby $V_{DD}$ Current		10	$\mu A$	ROMCS# $\geq V_{DD}-0.2V$ , RAMCS# $\geq V_{DD}-0.2V$ $V_{IN} \geq V_{DD}-0.2V$ or $V_{IN} \leq 0.2V$
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 1.0$ mA
$V_{OH}$	Output High Voltage	2.2		V	$I_{OH} = -0.5$ mA

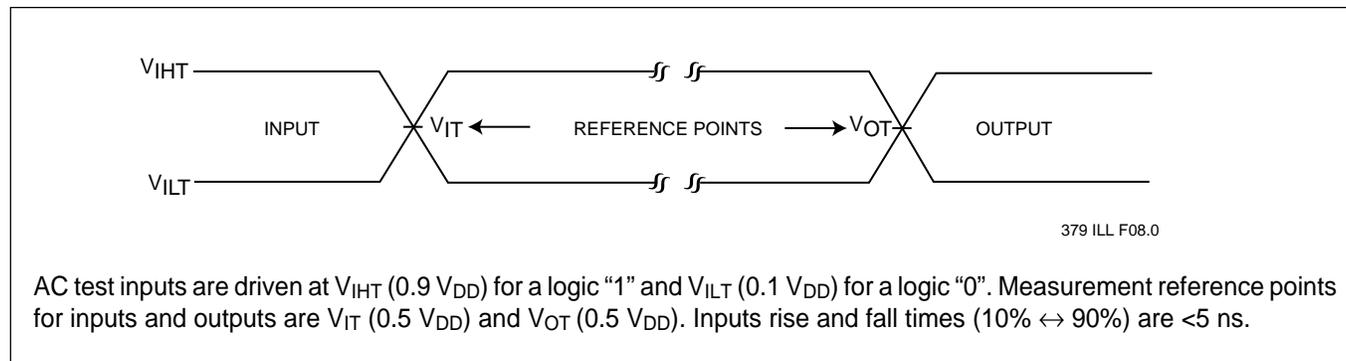
Note: f = frequency of operation (MHz) = 1/cycle time

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**TABLE 4: CAPACITANCE ( $T_a = 25^\circ C$ ,  $f=1$  Mhz)**

Parameter	Description	Test Condition	Maximum
$C_{I/O}$	I/O Capacitance	$V_{I/O} = 0V$	8 pF
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	6 pF

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**FIGURE 2: AC INPUT/OUTPUT REFERENCE WAVEFORMS**

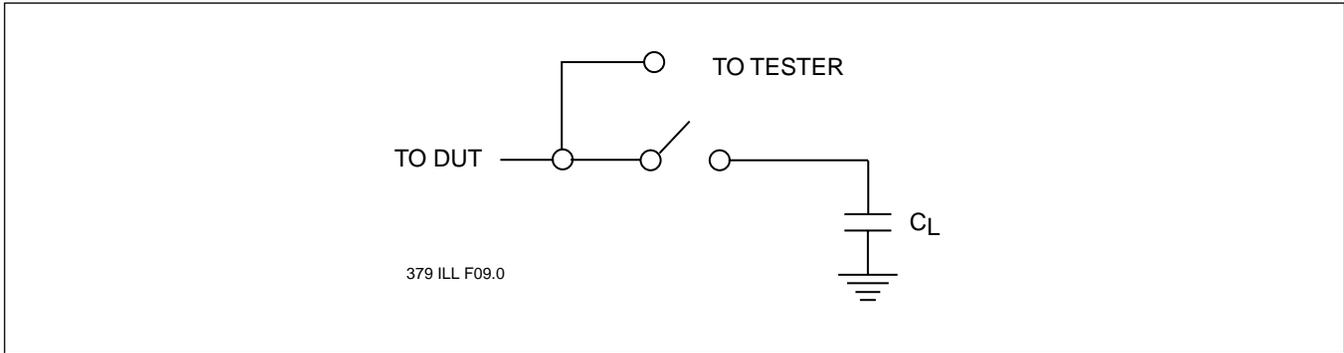


FIGURE 3: A TEST LOAD EXAMPLE

**AC CHARACTERISTICS**

**I. ROM Operation**

**TABLE 5: READ CYCLE TIMING PARAMETERS  $V_{DD} = 3.0 V \pm 0.3$**

Symbol	Parameter	Min	Max	Unit
$T_{RC}$	Read Cycle Time	500		ns
$T_{AA}$	Address Access Time		500	ns
$T_{CO}$	Chip Select to Output		500	ns
$T_{OE}$	Output Enable to Valid Output		250	ns
$T_{LZ}$	Chip Select to Low-Z Output	25		ns
$T_{OLZ}$	Output Enable to Low-Z Output	25		ns
$T_{HZ}$	Chip Disable to High-Z Output		30	ns
$T_{OHZ}$	Output Disable to High-Z Output		30	ns
$T_{OH}$	Output Hold from Address Change	15		ns

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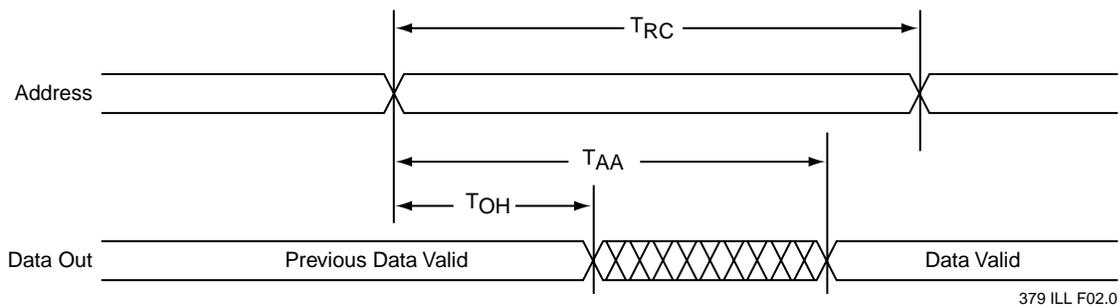
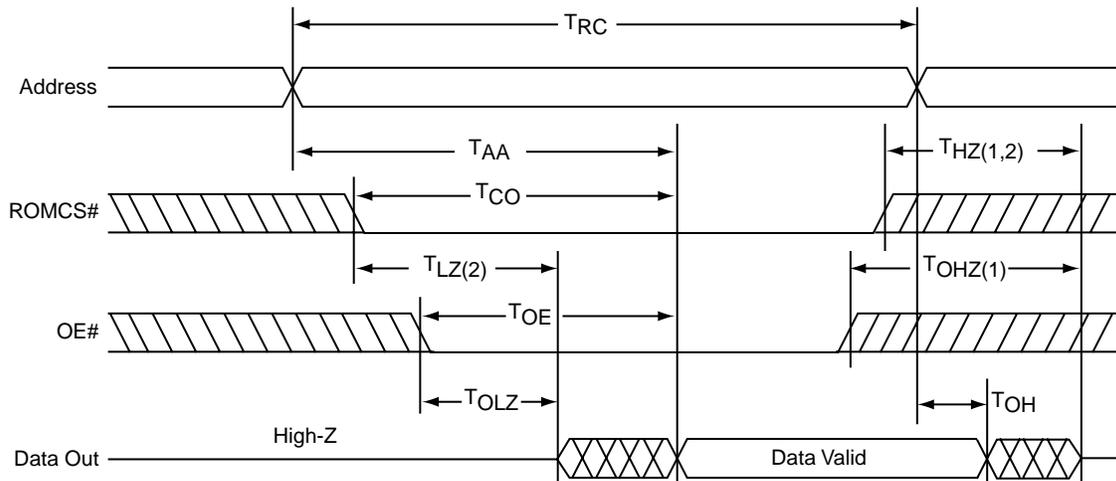


FIGURE 4: ROM READ CYCLE TIMING DIAGRAM (ADDRESS CONTROLLED) ( $ROMCS\# = OE\# = V_{IL}$ )



# 2 Megabit ROM + 1 Megabit SRAM ROM/RAM Combo SST30VR021

Data Sheet



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- Notes: 1.  $T_{HZ}$  and  $T_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are referenced to the  $V_{OH}$  or  $V_{OL}$ .  
2. At any given temperature and voltage condition  $T_{HZ}(\max)$  is less than  $T_{LZ}(\min)$  both for a given device and from device to device.

FIGURE 5: ROM READ CYCLE TIMING DIAGRAM (ROMCS# OR OE# CONTROLLED)

## II. SRAM Operation (ROMCS# = $V_{IH}$ )

TABLE 6: READ CYCLE TIMING PARAMETERS  $V_{DD}=3.0\text{ V} \pm 0.3$

Symbol	Parameter	Min	Max	Unit
$T_{RC}$	Read Cycle Time	500		ns
$T_{AA}$	Address Access Time		500	ns
$T_{CO}$	Chip Select to Output		500	ns
$T_{OE}$	Output Enable to Valid Output	25		ns
$T_{LZ}$	Chip Select to Low-Z Output	25		ns
$T_{HZ}$	Chip Disable to High-Z Output		30	ns
$T_{OHZ}$	Output Disable to High-Z Output		30	ns
$T_{OH}$	Output Hold from Address Change	15		ns

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TABLE 7: WRITE CYCLE TIMING PARAMETERS  $V_{DD}=3.0\text{ V} \pm 0.3$

Symbol	Parameter	Min	Max	Unit
$T_{WC}$	Write Cycle Time	500		ns
$T_{CW}$	Chip Select to End-of-Write	365		ns
$T_{AW}$	Address Valid to End-of-Write	375		ns
$T_{AS}$	Address Set-up Time	0		ns
$T_{WP}$	Write Pulse Width	375		ns
$T_{WR}$	Write Recovery Time	0		ns
$T_{WHZ}$	Write to Output High-Z		80	ns
$T_{DW}$	Data to Write Time Overlap	200		ns
$T_{DH}$	Data Hold from Write Time	0		ns
$T_{OW}$	End Write to Output Low-Z	15		ns

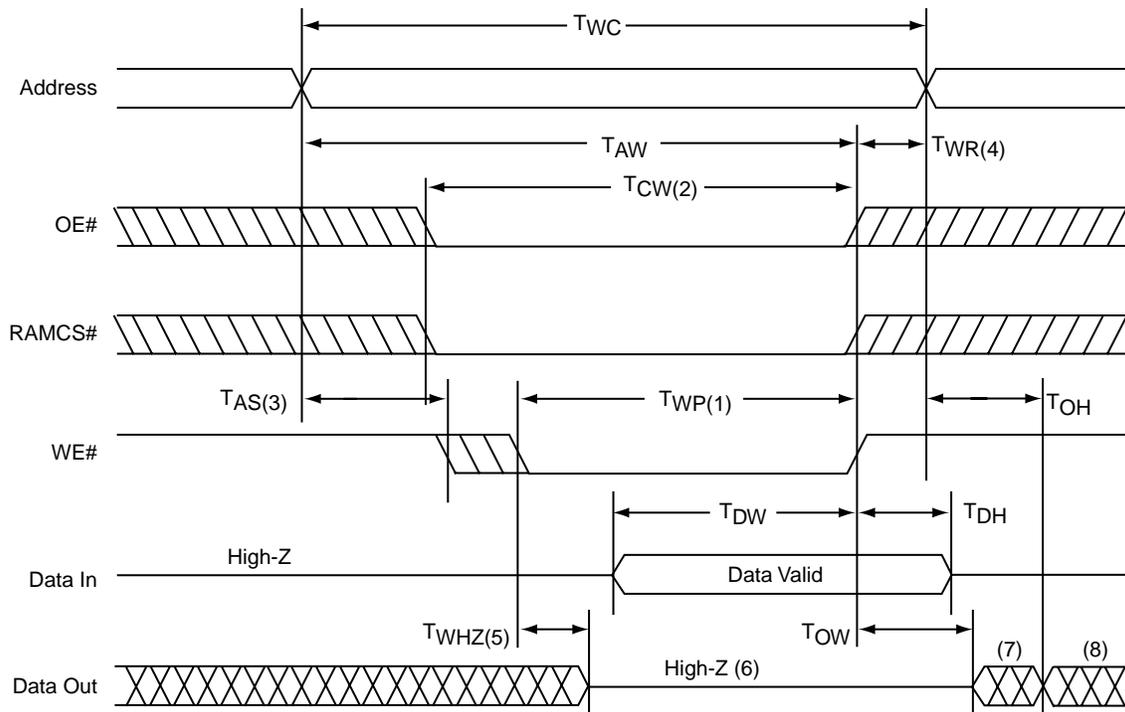
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# 2 Megabit ROM + 1 Megabit SRAM ROM/RAM Combo SST30VR021

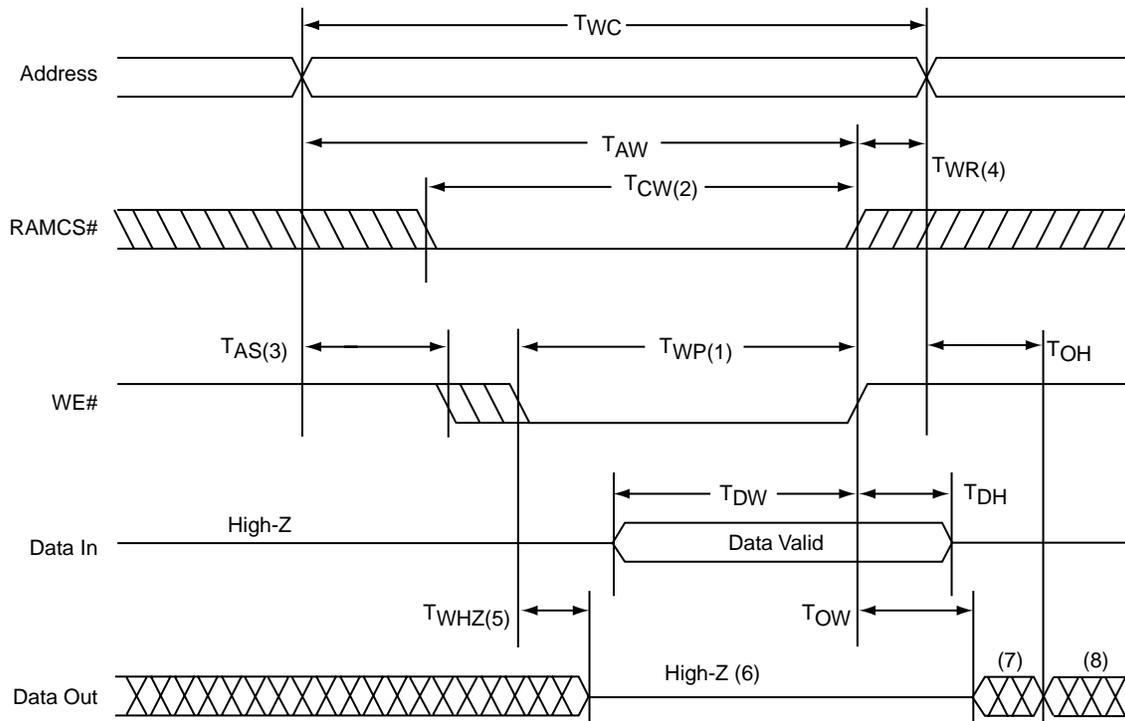
Data Sheet



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- Notes:
1. A write occurs during the overlap ( $T_{WP}$ ) of a low RAMCS# and low WE#. A write begins at the latest transition among RAMCS# going low and WE# going low. A write ends at the earliest transition among RAMCS# going high and WE# going high.  $T_{WP}$  is measured from the beginning of write to the end of write.
  2.  $T_{CW}$  is measured from the later of RAMCS# going low to the end of write.
  3.  $T_{AS}$  is measured from the address valid to the beginning of write.
  4.  $T_{WR}$  is measured from the end of write to the address change.
  5. If RAMCS#, WE# are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
  6. If RAMCS# goes low simultaneously with WE# going low or after WE# going low, the outputs remain high impedance state.
  7.  $D_{OUT}$  is the same phase of the latest written data in this write cycle.
  8.  $D_{OUT}$  is the read data of new address
  9. ROMCS# =  $V_{IH}$

**FIGURE 8: SRAM WRITE CYCLE TIMING DIAGRAM (OE# CLOCK)**



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- Notes:
1. A write occurs during the overlap ( $T_{WP}$ ) of a low RAMCS# and low WE#. A write begins at the latest transition among RAMCS# going low and WE# going low. A write ends at the earliest transition among RAMCS# going high and WE# going high.  $T_{WP}$  is measured from the beginning of write to the end of write.
  2.  $T_{CW}$  is measured from the later of RAMCS# going low to the end of write.
  3.  $T_{AS}$  is measured from the address valid to the beginning of write.
  4.  $T_{WR}$  is measured from the end of write to the address change.
  5. If RAMCS#, WE# are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
  6. If RAMCS# goes low simultaneously with WE# going low or after WE# going low, the outputs remain high impedance state.
  7.  $D_{OUT}$  is the same phase of the latest written data in this write cycle.
  8.  $D_{OUT}$  is the read data of new address
  9. ROMCS# =  $V_{IH}$

FIGURE 9: SRAM WRITE CYCLE TIMING DIAGRAM (OE# FIXED)



## 2 Megabit ROM + 1 Megabit SRAM ROM/RAM Combo SST30VR021

Data Sheet

TABLE 8: FUNCTIONAL DESCRIPTION/TRUTH TABLE

Address Inputs	ROMCS#	RAMCS#	WE#	OE#	DQ7-DQ0	
X	H	H	X	X	Z	Standby
A17-A0	L	H	X	H	Z	Output Floating
A17-A0	L	H	X	L	Dout	ROM Read
Only A16-A0 are valid *	H	L	H	H	Z	Output Floating
Only A16-A0 are valid *	H	L	H	L	Dout	RAM Read
Only A16-A0 are valid *	H	L	L	H	Din	RAM Write

\* A17 must be fixed to "L" or "H"

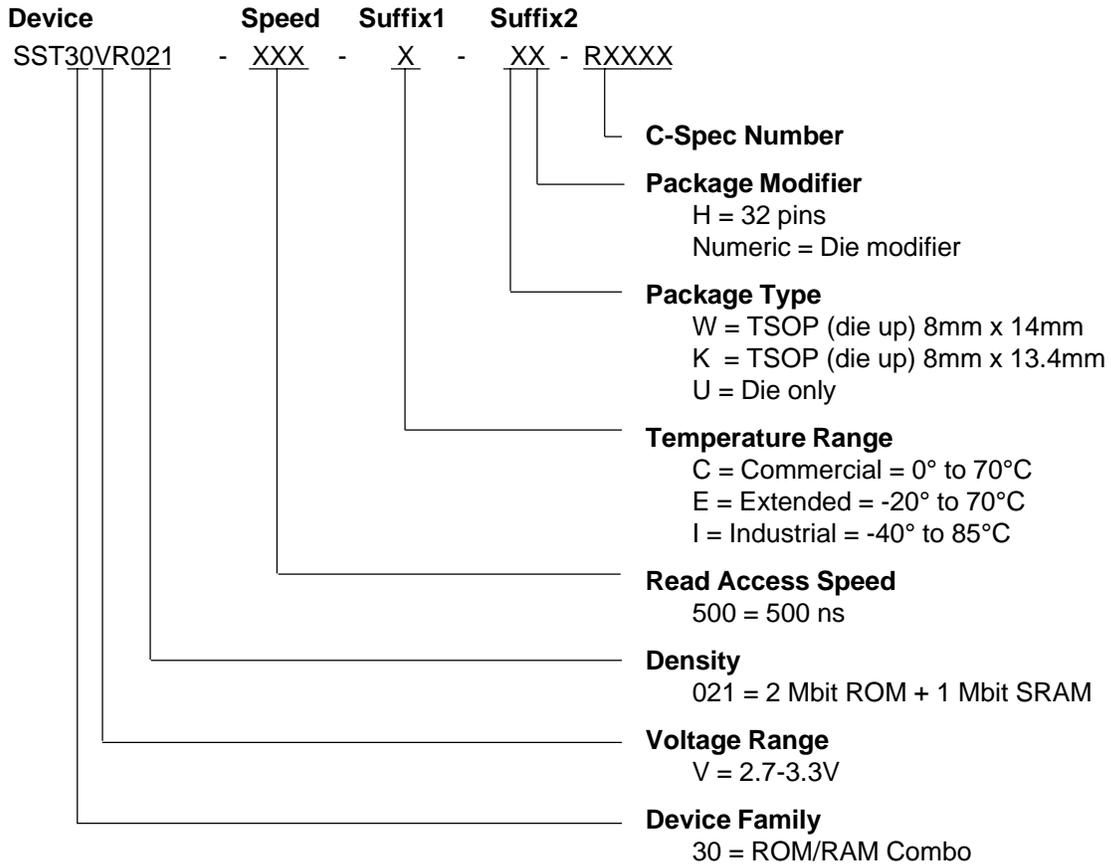
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Note: (1) It is forbidden that ROMCS# pin and RAMCS# pin will be "0" at the same time.  
(2) X means Don't Care.



## 2 Megabit ROM + 1 Megabit SRAM ROM/RAM Combo SST30VR021

Data Sheet



**SST30VR021 Valid combinations**

SST30VR021-500-C-WH	SST30VR021-500-C-KH	SST30VR021-500-C-U1
SST30VR021-500-E-WH	SST30VR021-500-E-KH	
SST30VR021-500-I-WH	SST30VR021-500-I-KH	

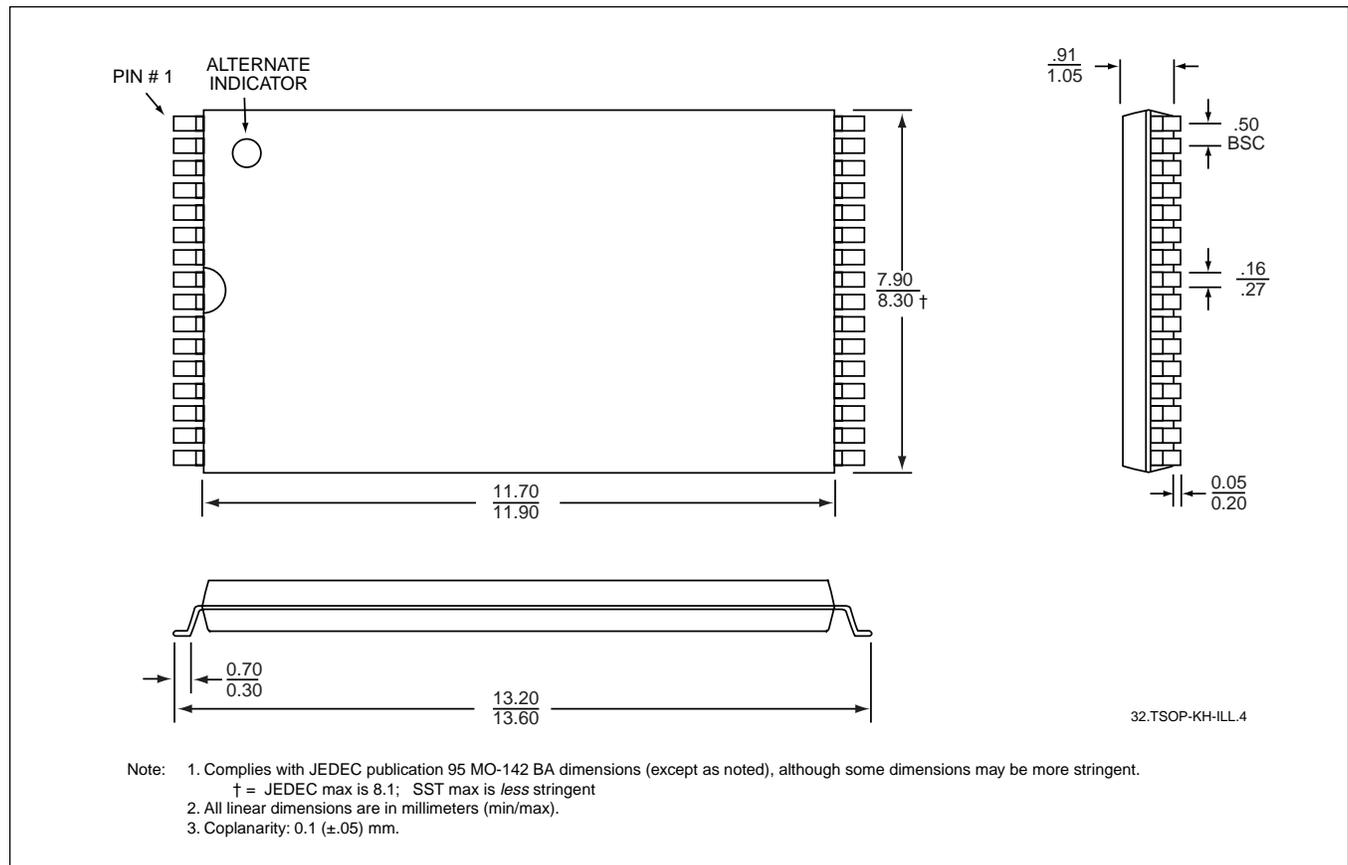
**Example:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



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Data Sheet

## PACKAGING DIAGRAMS



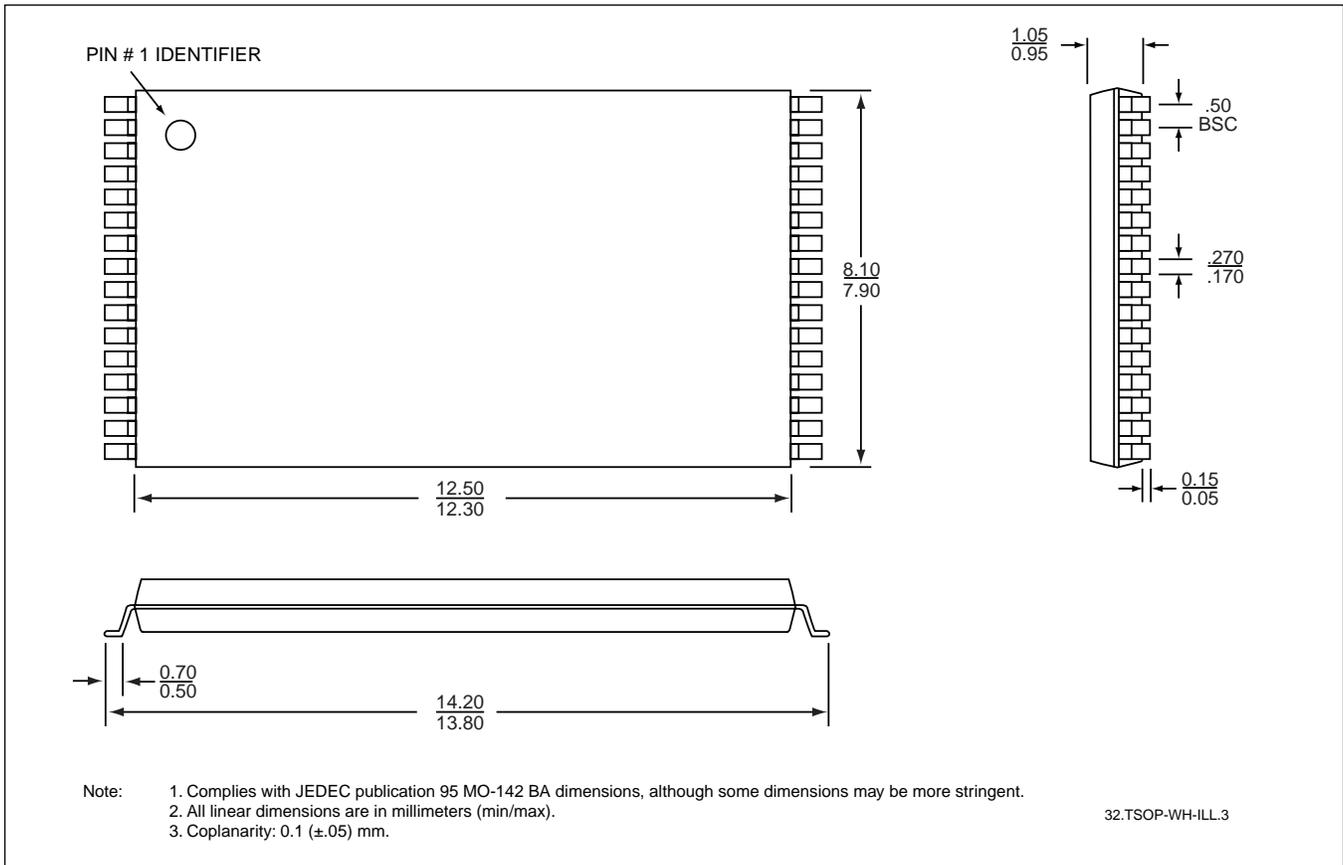
**32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 13.4MM**

**SST PACKAGE CODE: KH**



# 2 Megabit ROM + 1 Megabit SRAM ROM/RAM Combo SST30VR021

Data Sheet



## 32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM

SST PACKAGE CODE: WH