PM8610

SBS

SBI Bus Serializer

Data Sheet

Proprietary and Confidential

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Revision History

Issue No.	Issue Date	Details of Change
5	June, 2002	Created Issue 5 of the data sheet. General pre-production review and update. Updated SBI336 and SBI structure tables and cleaned up framing format tables. Added AMODE requirement in TelecomBus mode. Added a note pertaining to analog power filtering requirements, and corrected these requirements. Removed OPA section and replaced it with a reference to the application notes. Documented RX_INV bit in registers 0C0 and 0C8. Updated power requirements. Added more information on device latency. Added timing relationship between IC1FP and RC1FP for the DS0 loopbacks in register 02B and 04B. Updated thermal information based on new simulation data. Updated Microprocessor Timing diagram to reflect correct data bus width. Added 4xOC-3/4xSTM-1 Voice Processing Card diagram.
4	February, 2002	Created Issue 4 of the data sheet to reflect the following changes: Updated block diagram to reflect the new order of blocks. ISTT is now located in between the ISTA and the ICASE and OSTT is now located between the OCASM and OSTA Explained the differences between the HPT, MST and the LPT modes. Pin description of OACTIVE changed to indicate it should be ignored in 77MHz mode. Pin description of ODETECT changed to indicate that it must be held low in Telecom bus mode. Updated pin description for RSTB to indicate that is must be held low for a minimum of 1ms to reset the CSU. Updated pin description for RES and RESK. Separated CSU_AVDL pins from AVDL pins. Added analog filtering requirements. CSU description updated to state that it must be reset for a minimum of 1ms. Updated ARESET bit description in register 000h. Changed SBI_19M to SBI_19MB in register 001h to reflect the actual polarity of the bit. Changed the meaning of SPE_TYP bits in register 005h and 006h. Added C1 interrupts to register 011h and added interrupt enables to register 012h. Fixed bit description in register 016h. Added SPE_TYP registers 018h, 019h, 01Ah and 01Bh. Added restriction to registerS 03Ah and 042h stating that they must not be set in parallel mode. Added OMUS overwrite function to register 04Bh. Fixed description of ERR_CNT in register 071h and 081h (IADDR=4h). Updated description of MONx_SYNCV in register 07Bh and 08Bh. Updated description of DLCV in register 0B0H and 0B8H. Updated description of RX_XFER_SYNC in register 09Bh and 0ABh. Updated description of DLCV in register 0B0H and 0B8H. Added REFDLL and SYSDLL reset registers 0E2h and 0EAh. Updated JTAG ID. Updated Transmit and Receive LVDS timing diagrams. Updated Operation section, Absolute Maximum Ratings and D.C. Characteristics. Added Serial Interface Timing, RSTB Timing and SYSCLK / SREFCLK

Issue No.	Issue Date	Details of Change
		skew numbers.
3	May, 2001	Issue 3 of the data sheet created.
2	June, 2000	Issue 2 of the data sheet created.
1	February, 2000	Document creation.

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1 Features

- OC-12/STM-4 DS0, NxDS0, T1, E1, VT/TU/DS-3/E3/STS-1/AU-3 cross-connect and SBI/TelecomBus serializer.
- Quad byte wide 19.44MHz SBI bus to 777.6MHz serial SBI336S converter.
- Byte wide 77.76MHz SBI336 bus to 777.6MHz serial SBI336S converter.
- DS0, NxDS0, T1, E1, Transparent VT1.5 (TVT1.5), Transparent VT2 (TVT2), DS3 and E3 granular quad SBI to serial SBI336S switch. Supports subrate link switching with the restriction that subrate links must be symmetric in both the transmit and receive directions.
- DS0, NxDS0, T1, E1, Transparent VT1.5 (TVT1.5), Transparent VT2 (TVT2), DS3 and E3 granular SBI336 to serial SBI336S switch. Supports subrate link switching with the restriction that subrate links must be symmetric in both the transmit and receive directions.
- A byte wide 77.76MHz SBI336 bus interface can be used instead of the serial SBI336S interface. All converter and switch capabilities can be used with the byte wide SBI interface.
- VT/TU channelized telecom bus to telecom bus converter and TDM switch.TelecomBus
- Quad byte wide 19.44MHz telecom bus to serial 777.6MHz telecom bus converter.
- Byte wide 77.76MHz telecom bus to serial 777.6MHz telecom bus converter.
- VT/TU, STS/AU quad 19.44MHz telecom bus to serial telecom bus switch.
- VT/TU, STS/AU 77.76MHz telecom bus to serial telecom bus switch.
- A byte wide 77.76MHz telecom bus interface can be used instead of the serial telecom bus interface. All converter and switch capabilities can be used with the byte wide telecom bus interface.
- With the Narrowband Switch Element, NSE, the SBS can be used to implement a DS0 granularity SBI Memory:Space:Memory switch scaleable to 20Gb/s. In telecom bus mode a 20Gb/s VT/TU granularity Memory:Space:Memory switch can be implemented.
- Integrates two independent DS0 granularity Memory Switches. One switch is placed between the incoming 77.76MHz byte wide SBI336 bus (or quad multiplexed 19.44MHz SBI buses) and the transmit working and protect Serial SBI336S link (or the 77.76MHz byte wide transmit SBI336 bus). The transmit working and protect links transmit the same data. The other switch is placed between the receive working or protect Serial SBI336S link (or the 77.76MHz byte wide receive SBI336 bus) and the outgoing 77.76MHz byte wide SBI336 bus (or quad multiplexed 19.44MHz SBI buses).
- Nominal latency through the SBS in DS0 mode is 125uS. Channel Associated Signaling (CAS) latency through the SBS in DS0 mode is two T1 multi-frame (6mS) or two E1 multi-frame (4mS).
- In telecom bus mode or SBI mode without DS0 level switching nominal latency through the SBS is <15uS.
- The Memory Switch permits any receive or incoming byte from an input port to be mapped to any outgoing or transmit byte, respectively, on the associated output port

- Supports redundant working and protect serial SBI336S links in support of a redundant Memory:Space:Memory switch with the NSE.
- Encodes and decodes byte wide SBI and SBI336 bus control signals for all SBI supported link types and clock modes for transport over the serial SBI336S interface.
- Encodes data from the Incoming SBI bus or TelecomBus stream to a working and protect 777.6Mbps LVDS serial links with 8B/10B-based encoding.
- Decodes data from a working and protect 777.6MHz LVDS serial links with 8B/10B-based encoding to the Outgoing SBI bus or telecom bus stream.
- In SBI mode switches Channel Associated Signaling bits, CAS, with all DS0 data.
- Uses 8B/10B-based line coding protocol on the serial links to provide transition density guarantee and DC balance and to offer a greater control character vocabulary than the standard 8B/10B protocol.
- Provides optional PRBS generation for each outgoing LVDS serial data link for off-line link verification. PRBS can be inserted with STS/AU granularity.
- Provides PRBS detection for each incoming LVDS serial link for off-line link verification. PRBS is verified with STS/AU granularity.
- Provides pins to coordinate updating of the connection map of the time-slot interchange blocks in the local device, peer SBS devices and companion NSE switch device.
- Can communicate with the NSE switch device over an in-band communications channel in the LVDS links. This channel includes mechanisms for central control and configuration.
- Derives all internal timing from a single 77.76MHz system clock.
- Implemented in 1.8V/3.3V 0.18µm CMOS and packaged in a 352 ball 27mmx27mm UBGA.
- Low power consumption of 1.0W (typical, 77.76MHz Incoming/Outgoing interface with Serial LVDS Tx/Rx interface).

2 Applications

- T1/E1 SONET/SDH Cross-connects
- T1/E1 SONET/SDH Add-Drop Multiplexers
- OC-48 Multiservice Access Multiplexers
- Channelized OC-12/OC-48 Any Service Any Port Switches
- Serial backplane board interconnect
- Shelf to Shelf cabled serial interconnect
- Voice Gateways
- Multiservice Switches (MSS)
- Multiservice Provisioning Platforms (MSPP)

3 References

1. IEEE 802.3, “Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications”, Section 36.2, 1998.

2. PMC-Sierra, Inc. Saturn Compatible Scaleable Bandwidth Interconnect (SBI) Specification, PMC-1980577, Issue 4.

3. A.X. Widmer and P.A. Franaszek, “A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code,” IBM Journal of Research and Development, Vol. 27, No 5, September 1983, pp 440-451.

4. U.S. Patent No. 4,486,739, P.A. Franaszek and A.X. Widmer, “Byte Oriented DC Balanced (0,4) 8B/10B Partitioned Block Transmission Code,” December 4, 1984.

5. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, Revision 2, January 1999.

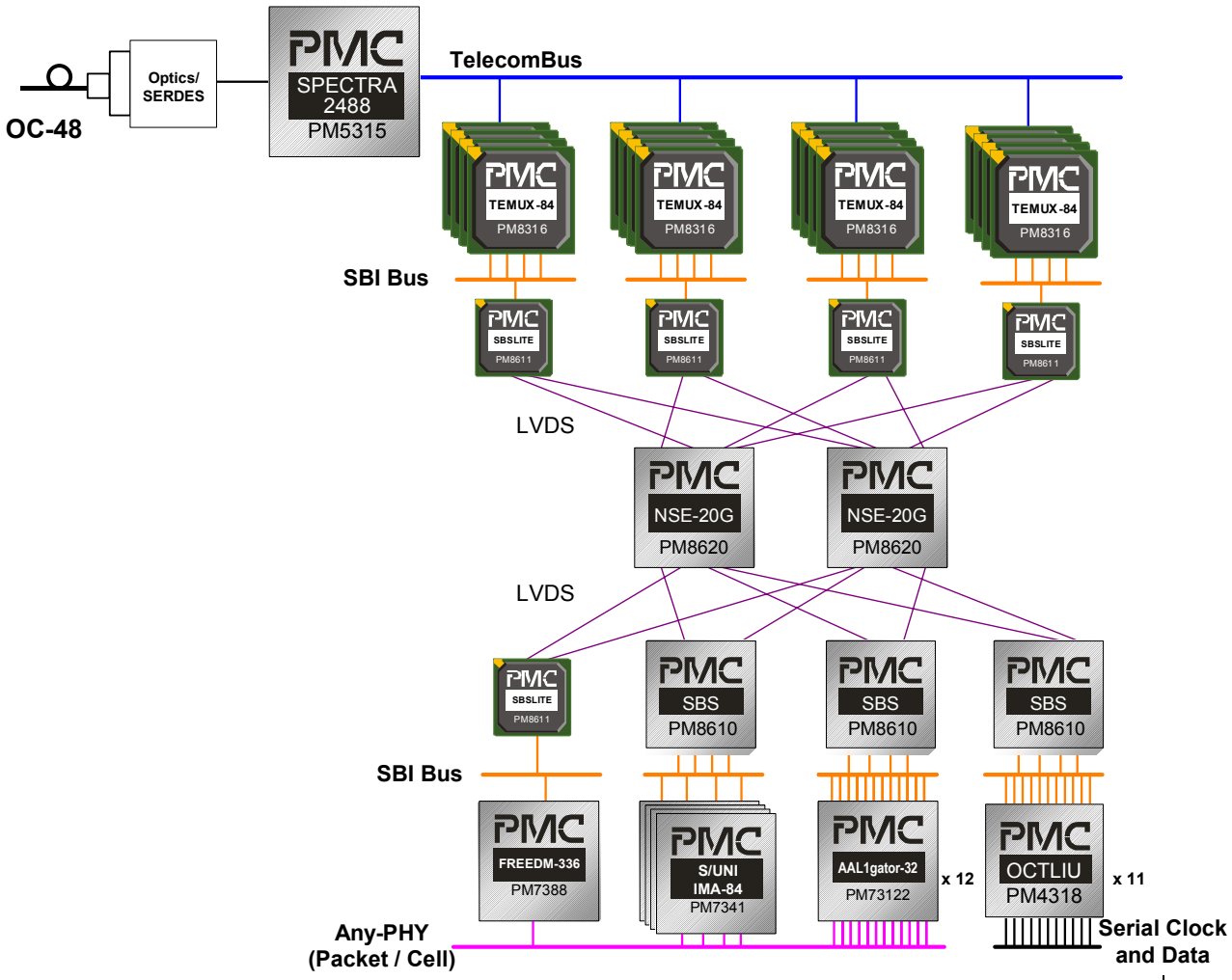
6. ITU, Recommendation G.707 - "Digital Transmission Systems – Terminal equipments - General", March 1996.

7. ITU, Rec Recommendation O.151 – “Error Performance Measuring Equipment Operating at the Primary Rate and Above", October 1992.

4 Application Examples

Figure 1 illustrates a DS0/T1/E1/VT/TU/STS-1-capable OC-48/STM-12 Any-Service-Any-Port (ASAP) architecture. The high-granularity optical signals are channelized down to the DS0 level and groomed to a variety of the service cards.

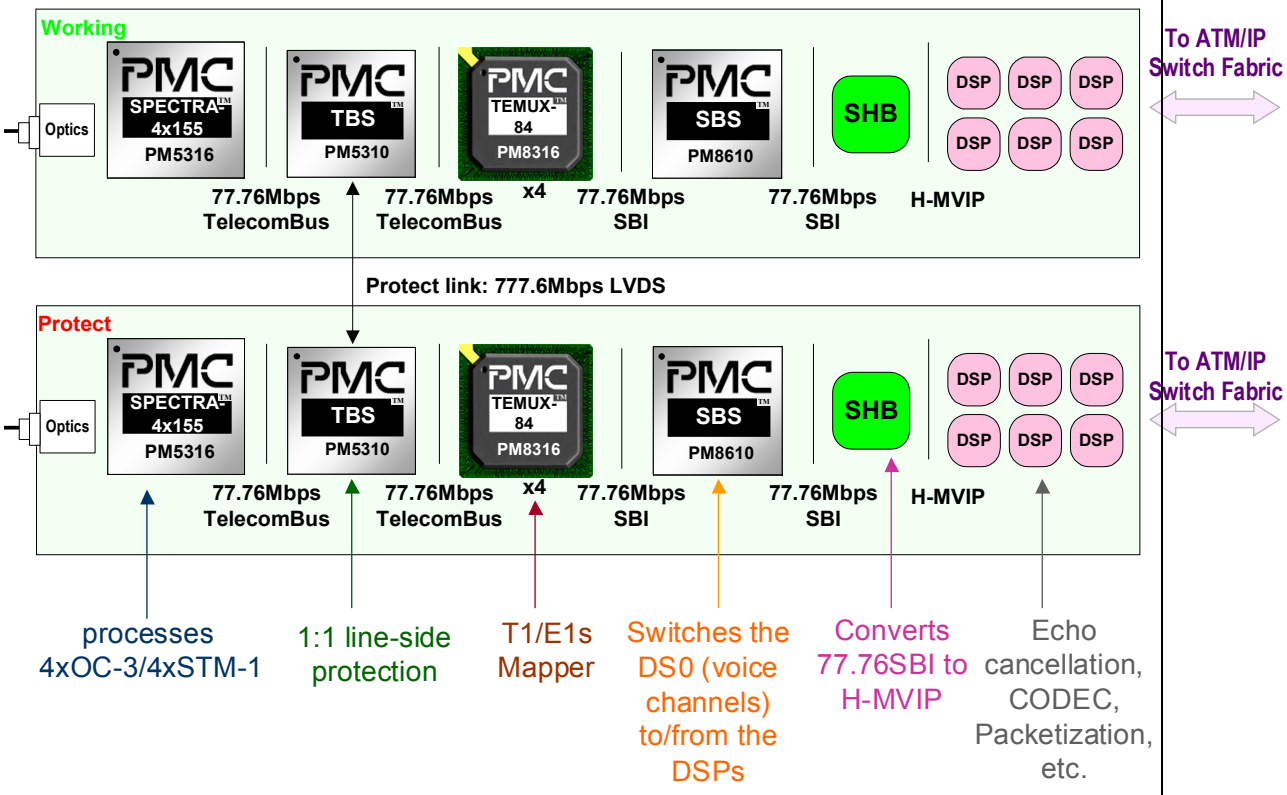
Figure 1 OC-48/STM-12 Any-Service-Any-Port (ASAP) DS0 TDM Switch Fabric Solution



In some architectures, it is necessary to perform the voice processing functions and move the TDM traffic into the packet/cell domain directly on the TDM interface cards. This approach is widely adopted by vendors using circuit emulation services (CES) to switch the traffic in the system. An example of a fully protected line card with voice processing functions is illustrated in Figure 2. The TBS is used for protection switching with high-speed serial streams running in between the cards. The same protection switching function can be performed by the SBSLITE, which is smaller, cost-effective and low on power.

The SBS is used to groom voice channels in between the TEMUX-84 devices and the DSPs. The traffic is processed and packetized in the DSPs and sent to the packet/cell switch for cross connecting to the appropriate packet/cell interfaces.

Figure 2 4xOC-3/4xSTM-1 Voice Processing sCard with 1+1 Protection



5 Block Diagram

Figure 3 Quad 19Mhz SBI Bus/TelecomBus SBS Block Diagram

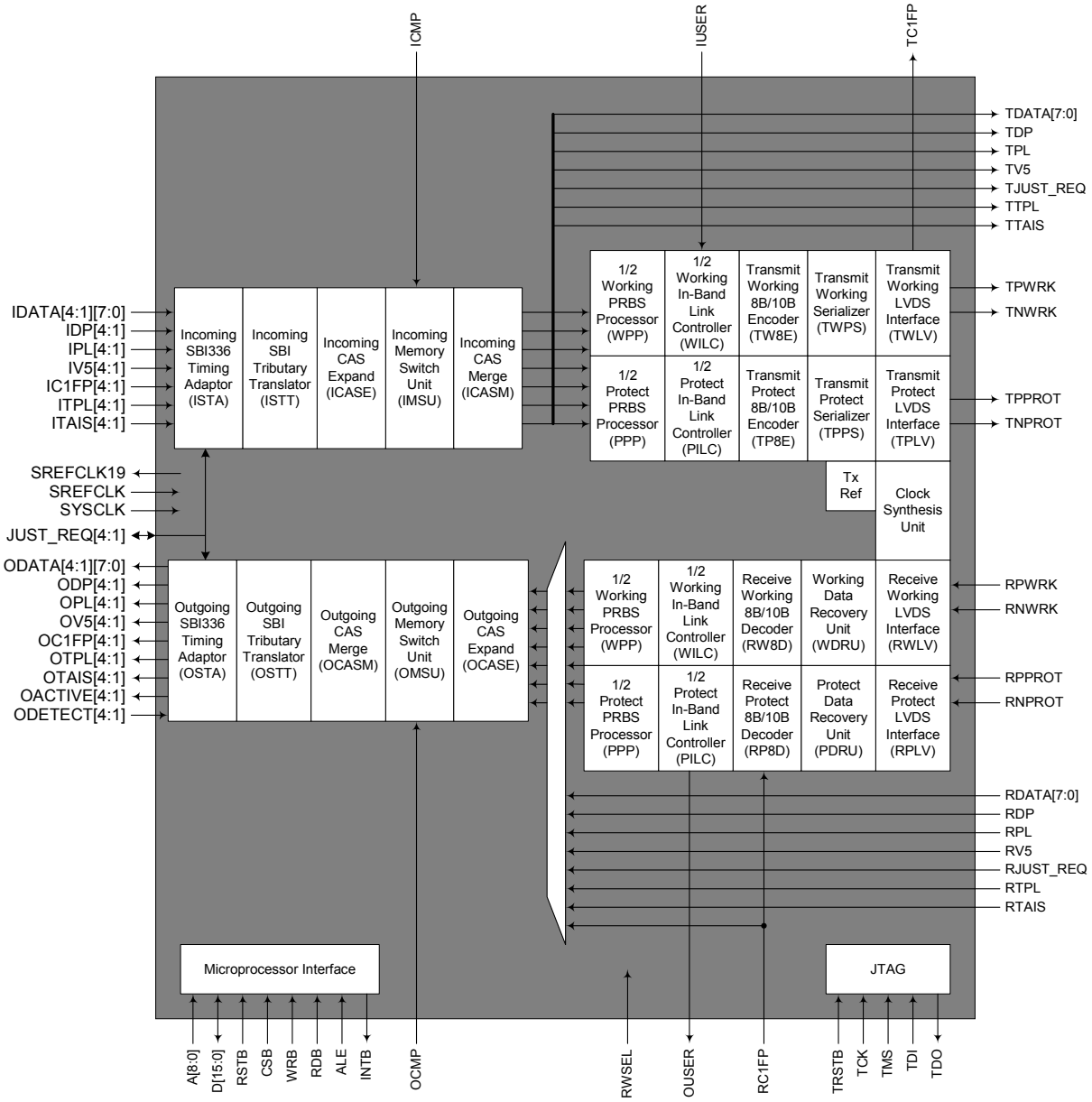
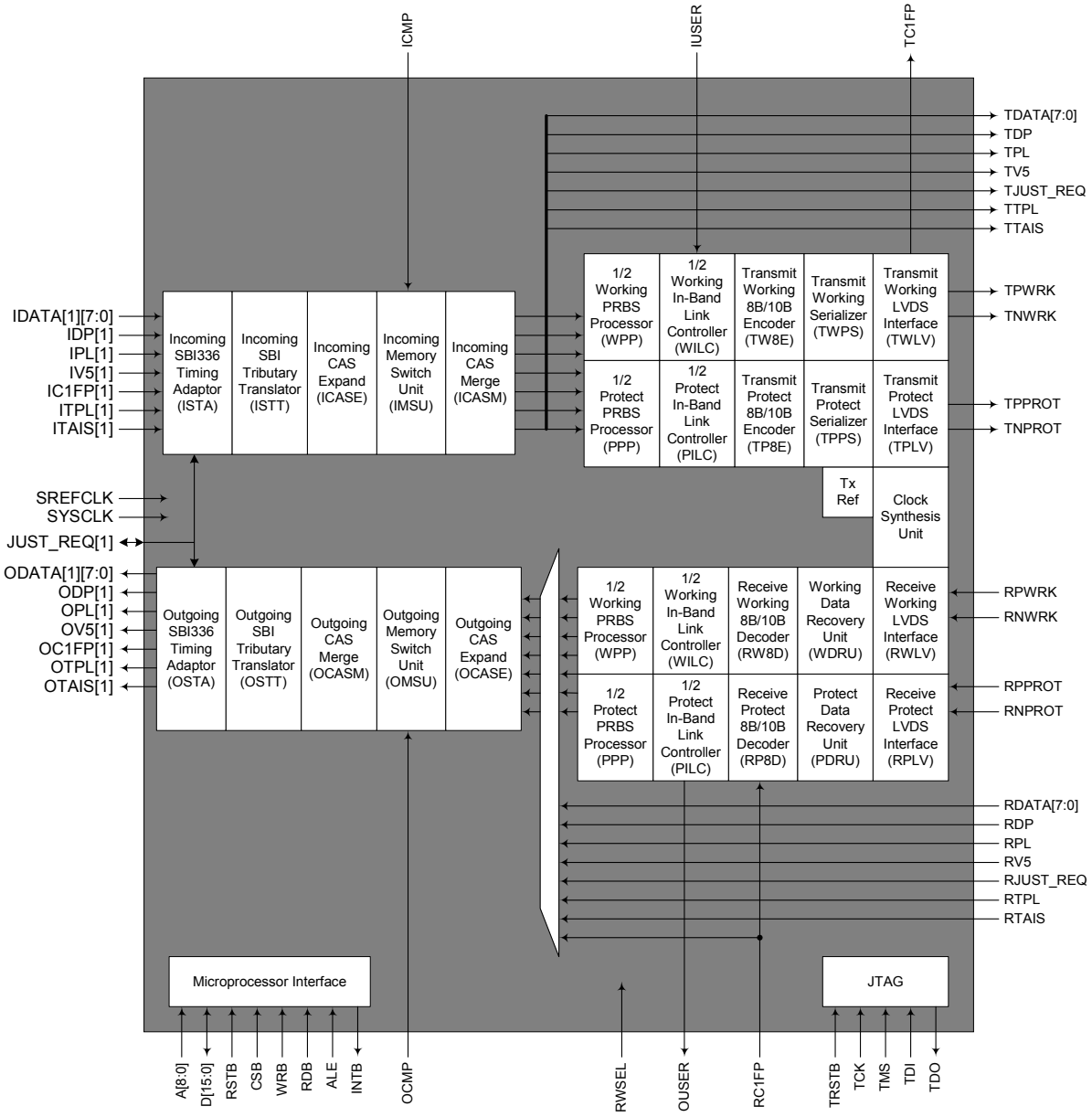
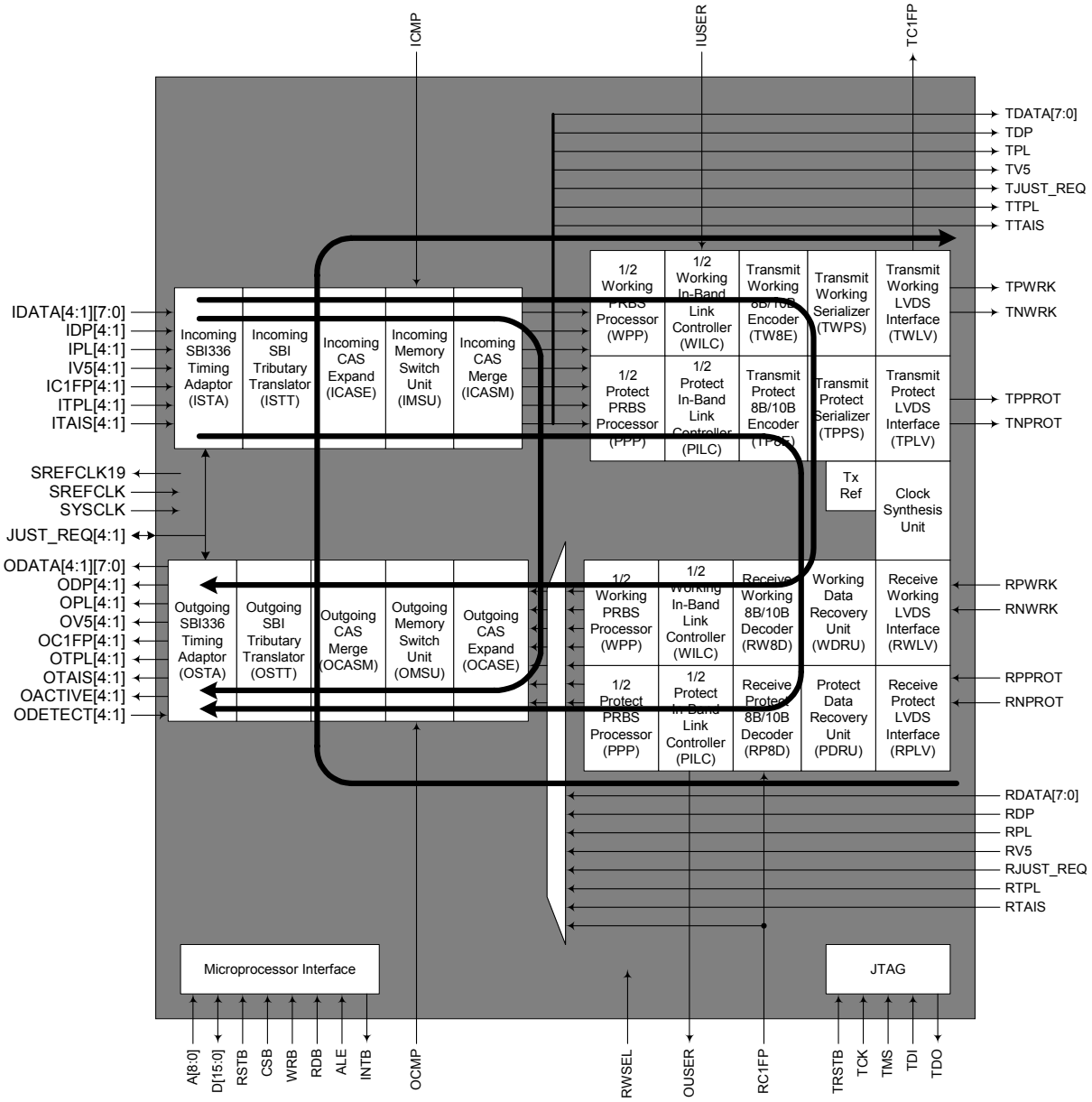


Figure 4 77MHz SBI Bus/TelecomBus SBS Block Diagram



6 Loop back Configurations

Figure 5 Loop back Block Diagram



7 Description

The PM8610 SBI336 Bus Serializer, SBS, is a monolithic integrated circuit that implements conversion between byte-serial 19.44Mhz SBI bus or 77.76MHz SBI336 bus and redundant 777.6Mbps bit-serial 8B/10B-base SBI336S bus. In telecom bus mode the SBS implements conversion between any 19.44MHz Telecom bus or 77.76MHz Telecom bus format and redundant 777.6Mbps bit-serial 8B/10B-base serial telecom bus format. In line with the bus conversion is a DS0 granular switch allowing any input DS0 to be output on any output DS0. The redundant 777.6 Mbps serial interfaces can be disabled and a byte-wide SBI336 bus can be enabled in its place with all the DS0 level switching capabilities.

The SBS can be used to connect and switch high-density T1/E1 framer devices supporting an SBI bus with link layer devices supporting an SBI bus over a serial backplane. Putting the Narrowband Switch Element, NSE, between the framer and link layer devices allows construction of up to 20Gb/s NxDS0 switches.

In the ingress direction, the SBS connects an incoming SBI stream to a pair of redundant serial SBI336S LVDS links through a DS0 memory switch. The incoming SBI bus can be either a single 77.76MHz SBI bus (SBI336) or four 19.44MHz SBI buses (SBI). In telecom bus mode an incoming 77.76MHz telecom bus or four 19.44MHz telecom buses that have the J1 path fixed and all high order pointer justifications converted to tributary pointer justifications can be switched through a VT/TU granular switch to a pair of redundant serial LVDS telecom bus format links. The incoming data is encoded into an extended set of 8B/10B characters and transferred onto two redundant 777.6 Mbps serial LVDS links. SBI or telecom bus frame boundaries, pointer justification events and master timing controls are marked by 8B/10B control characters. Incoming SPEs may be optionally overwritten with the locally generated $X^{23} + X^{18} + 1$ PRBS pattern for diagnosis of downstream equipment. The PRBS processor is configurable to handle any combination of SPEs and can be inserted independently into either of the redundant LVDS links. A DS0 memory switch provides arbitrary mapping of streams on the incoming SBI bus stream(s) to the working and protect LVDS links at DS0 granularity. In telecom bus mode a VT/TU memory switch provides arbitrary mapping of tributaries on the incoming telecom bus stream(s) to the working and protect LVDS links. Multi-cast is supported.

In the egress direction, the SBS connects two independent 777.6 Mbps serial LVDS links to an outgoing SBI Bus. Each link contains a constituent SBI336S stream. Bytes on the links are carried as 8B/10B characters. The SBS decodes the characters into data and control signals for a single 77.76MHz SBI336 bus or four 19.44MHz SBI buses. Alternatively the SBS decodes two independent 777.6 Mbps telecom bus formatted serial LVDS links characters into a single 77.76MHz or quad 19.44MHz telecom buses. A pseudo-random bit sequence (PRBS) processor is provided to monitor the decoded payload for the $X^{23} + X^{18} + 1$ pattern in each SPE. The PRBS processor is configurable to handle any combination of SPEs in the serial LVDS link. Data on the outgoing SBI bus stream(s) may be sourced from either of the LVDS links.

An In-band signaling link over the serial LVDS links allows this device to be controlled by a companion-switching device, the Narrowband Switching Element, NSE20G. This link can be used as communication link between a central processor and the local microprocessor.

Three loop backs are provided on the SBS. The outgoing to incoming loop back allows data entering the SBS on the receive interface to be looped back from the output of the OCASM to the input of the ICASE and then returned to the transmit interface. The transmit 8b/10b to receive 8b/10b loop back allows data entering on the incoming bus to be looped back from the output of the TW8E and TP8E to the input of the RW8D and RP8D, respectively. Only the data looped back on the active link (working or protection) will make it back to the outgoing bus. The transmit to receive loop back allows data entering on the incoming bus to be looped back from the output of the ICASM to the input of the OCASE and then returned to the outgoing bus.

8 Pin Diagram

The SBS is packaged in a 352-pin UBGA package having a body size of 27mm by 27mm and a ball pitch of 1mm.

Figure 6 Pin Diagram

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	TC1FP	NC	NC	TDATA[7]	ODATA[1][1]	TTPL	TTAIS	ODATA[1][3]	ODATA[1][5]	ODATA[1][7]	VSS	VSS	OPL[1]	RJUST_REQ	RDATA[2]	NC	RDP	RTAIS	NC	DVDDI	JUST_REQ[2]	NC	VSS	VSS	A
B	VSS	DVDDO	VSS	TDATA[0]	TDATA[2]	TDATA[4]	ODP[1]	ODATA[1][2]	NC	ODETECT[1]	NC	NC	OTAIS[1]	OTPL[1]	NC	RDATA[1]	RDATA[4]	RDATA[7]	RTPL	OTAIS[2]	OCMP	OACTIVE[2]	SREFCLK19	VSS	DVDDO	VSS	B
C	VSS	VSS	DVDDO	NC	NC	NC	TDATA[5]	ODATA[1][0]	TDP	TV5	DVDDI	ODATA[1][6]	NC	OV5[1]	OC1FP[1]	RDATA[3]	RDATA[6]	RV5	OTPL[2]	ICMP	ODETECT[2]	SREFCLK	NC	DVDDO	VSS	IDATA[1][0]	C
D	VSS	VSS	AVDH	DVDDO	TJUST_REQ	TDATA[1]	TDATA[3]	TDATA[6]	DVDDO	TPL	OACTIVE[1]	ODATA[1][4]	NC	DVDDO	RDATA[0]	RDATA[5]	RPL	NC	DVDDO	NC	SYSCLK	NC	DVDDO	NC	IDATA[1][1]	NC	D
E	VSS	NC	AVDH	NC																			NC	IDATA[1][2]	IDATA[1][4]	IDATA[1][7]	E
F	RESK	RES	NC	NC																			IDATA[1][3]	IDATA[1][5]	NC	ITPL[1]	F
G	VSS	NC	NC	NC																			IDATA[1][6]	IDP[1]	IV5[1]	IPL[1]	G
H	TNPROT	TPPROT	NC	NC																			DVDDO	IC1FP[1]	ITAIS[1]	ODATA[2][0]	H
J	VSS	NC	NC	AVDH																			NC	DVDDI	ODATA[2][1]	ODATA[2][3]	J
K	TPWRK	TNWRK	NC	NC																			NC	ODATA[2][2]	ODATA[2][5]	ODATA[2][7]	K
L	VSS	NC	NC	NC																			ODATA[2][4]	ODATA[2][6]	ODP[2]	OV5[2]	L
M	RPWRK	RNWRK	ATB0	ATB1																			OPL[2]	OC1FP[2]	TDO	NC	M
N	RPPROT	RNPROT	NC	AVDL																			DVDDO	INTB	NC	VSS	N
P	CSU_AVDL	CSU_AVDL	NC	CSU_AVDH																			TRSTB	TMS	TCK	VSS	P
R	ITPL[4]	ITAIS[4]	CSU_AVDL	IV5[4]																			ODATA[3][2]	ODATA[3][0]	ODETECT[3]	TDI	R
T	VSS	IPL[4]	IC1FP[4]	AVDH																			ODATA[3][7]	ODATA[3][5]	ODATA[3][3]	ODATA[3][1]	T
U	IDATA[4][6]	IDATA[4][7]	DVDDI	IDP[4]																			NC	ODP[3]	ODATA[3][6]	ODATA[3][4]	U
V	VSS	IDATA[4][3]	IDATA[4][4]	IDATA[4][5]																			DVDDO	OTPL[3]	OPL[3]	OACTIVE[3]	V
W	ITAIS[2]	IDATA[4][0]	IDATA[4][2]	IDATA[4][1]																			NC	OC1FP[3]	OV5[3]	NC	W
Y	VSS	IC1FP[2]	ITPL[2]	AVDH																			IDATA[3][1]	A[0]	JUST_REQ[1]	OTAIS[3]	Y
AA	WRB	RDB	DVDDI	ALE																			A[2]	A[1]	JUST_REQ[3]	OUSER2	AA
AB	VSS	CSB	AVDH	DVDDO																			NC	A[3]	NC	IDATA[3][0]	AB
AC	VSS	VSS	AVDH	DVDDO	RSTB	JUST_REQ[4]	OTPL[4]	DVDDO	NC	ODATA[4][6]	ODATA[4][2]	IUSER2	DVDDO	NC	IDATA[2][4]	D[8]	ITAIS[3]	DVDDO	D[5]	IDATA[3][4]	D[2]	A[7]	DVDDO	NC	A[4]	DVDDI	AC
AD	VSS	VSS	DVDDO	RWSEL	ODETECT[4]	OV5[4]	NC	D[14]	ODATA[4][7]	NC	ODATA[4][0]	D[12]	D[9]	IPL[2]	IDATA[2][6]	IDATA[2][1]	D[7]	ITPL[3]	IDP[3]	D[4]	IDATA[3][3]	D[1]	A[6]	DVDDO	VSS	A[5]	AD
AE	VSS	DVDDO	VSS	OACTIVE[4]	OTAIS[4]	ODP[4]	D[15]	NC	ODATA[4][4]	ODATA[4][1]	NC	D[11]	NC	IV5[2]	IDATA[2][7]	IDATA[2][3]	IDATA[2][0]	DVDDI	IC1FP[3]	IDATA[3][7]	IDATA[3][6]	IDATA[3][2]	D[0]	VSS	DVDDO	VSS	AE
AF	VSS	VSS	RC1FP	OC1FP[4]	OPL[4]	NC	DVDDI	ODATA[4][5]	ODATA[4][3]	NC	D[13]	D[10]	VSS	VSS	IDP[2]	IDATA[2][5]	IDATA[2][2]	NC	IV5[3]	IPL[3]	D[6]	IDATA[3][5]	D[3]	A[8]	VSS	VSS	AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

352 UBGA

BOTTOM VIEW

9 Pin Description

Pin Name	Type	Pin No.	Function
Receive Serial Data Interface (5 Signals)			
RPWRK RNWRK	Analog LVDS Input	M26 M25	**Receive Working Serial Data.** In SBI336 mode, the differential receive working serial data link (RPWRK/RNWRK) carries the receive 77.76MHz SBI336 data from an upstream working source, in bit serial format, SBI336S. In Telecom bus mode, RPWRK/RNWRK carries the receive 77.76MHz Telecom bus from an upstream working source, in bit serial format. Data on RPWRK/RNWRK is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is expected first and the bit 'j' is expected last. RPWRK/RNWRK are nominally 777.6 Mbps data streams. If this serial link is unused, the LVDS inputs RPWRK/RNWRK may be left floating or the inputs may be grounded. In either case the analog blocks (RWLV and WDRU) can be disabled to reduce power consumption. Tying one pin high and the other pin low will apply voltage across the internal termination resistor, which will increase system power consumption.
RPPROT RNPROT	Analog LVDS Input	N26 N25	**Receive Protect Serial Data.** In SBI336 mode, the differential receive protect serial data link (RPPROT/RNPROT) carries the receive 77.76MHz SBI336 data from an upstream protect source, in bit serial format, SBI336S. In Telecom bus mode, RPPROT/RNPROT carries the receive 77.76MHz Telecom bus from an upstream protection source, in bit serial format. Data on RPPROT/RNPROT is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is expected first and the bit 'j' is expected last. RPPROT/RNPROT are nominally 777.6 Mbps data streams. If this serial link is unused, the LVDS inputs RPPROT/RNPROT may be left floating or the inputs may be grounded. In either case the analog blocks (RPLV and PDRU) can be disabled to reduce power consumption. Tying one pin high and the other pin low will apply voltage across the internal termination resistor, which will increase system power consumption.
RC1FP	Input	AF24	**Receive Serial Frame Pulse.** The receive serial SBI336S frame pulse signal (RC1FP) provides system timing of the receive serial interface. When using the receive parallel interface, this signal pulses high for one SYSCLK cycle to indicate the first C1 byte on the bus. Using the Receive Serial Interface:

Pin Name	Type	Pin No.	Function
			When using the receive serial interface, RC1FP is set high for one SYSCLK cycle once every multi-frame (4 frames for SBI without CAS, 48 frames for SBI with CAS, and 4 frames for Telecom Bus), or multiple thereof. The RC1FP_DLY[13:0] bits (register 007H) are used to align the C1 frame boundary 8B/10B character on the receive serial interface (RPWRK/RNWRK and RPPROT/RNPROT) with RC1FP. <u>Using the Receive Parallel Interface:</u> In SBI mode, this signal also indicates multi-frame alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multi-frame signal. The frame pulse does not need to be repeated every 2KHz as the SBS will flywheel in its absence. When using the SBI bus in synchronous mode the RC1FP signal can be used to indicate T1 and E1 multi-frame alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data. In Telecom bus mode, this signal may also be pulsed to indicate the J1 byte position and the byte following J1. For locked STS/AUs, the J1 byte position must be locked to an offset of either 0 or 522. The byte following J1 is used to indicate multi-frame alignment and should only pulse once every 4 frames marking the frame with the V1s. RC1FP is sampled on the rising edge of SYSCLK.
Receive SBI336 Interface (14 Signals)			
RDATA[7] RDATA[6] RDATA[5] RDATA[4] RDATA[3] RDATA[2] RDATA[1] RDATA[0]	Input	B9 C10 D11 B10 C11 A10 B11 D12	**Receive Data (RDATA[7:0]).** This is the receive SBI336 data bus when configured for SBI336 byte wide interface instead of the Serial SBI336S interface. When in telecom bus mode this is the data bus for 77.76MHz telecom bus. The receive data bus is a time division multiplexed bus which transports tributaries by assigning them to fixed octets within the SBI or Telecom Bus structure. In SBI336 mode, multiple devices can drive this bus at uniquely assigned tributary columns within the SBI336 bus structure. RDATA[7:0] is sampled on the rising edge of SYSCLK. RDATA[7:0] have integral pull-up resistors.
RDP	Input	A8	**Receive Data Parity (RDP).** This is the receive data bus parity when configured for the Receive byte wide interface. This signal carries the even or odd parity for the receive bus signals. In SBI336 mode, the parity calculation encompasses the RDATA[7:0], RPL and RV5 signals. In Telecom Bus mode, the parity calculation encompasses the RDATA[7:0] and optionally the RC1FP and RPL signals. Multiple devices can drive this signal at uniquely assigned tributary columns within the fixed structure.

Pin Name	Type	Pin No.	Function
			This parity signal is intended to detect multiple sources in the column assignment. RDP is sampled on the rising edge of SYSCLK. RDP has an integral pull-up resistor.
RPL	Input	D10	**Receive Payload (RPL).** This is the receive SBI336 data bus payload signal indicates valid tributary payload data when configured for the receive SBI336 byte wide interface. In telecom bus mode this signal indicates valid path payload. In SBI336 mode: This active high signal indicates valid data within the SBI336 structure. This signal is high during all octets making up a tributary which includes all octets shaded gray in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI336 bus structure. This signal goes low during the octet following the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI336 bus structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high. Multiple SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI336 bus structure. In Telecom Bus mode: This signal distinguishes between transport overhead bytes and synchronous payload bytes. RPL is set high to mark each payload byte on RDATA[7:0] and is set low to mark each transport overhead byte on RDATA[7:0]. RPL is sampled on the rising edge of SYSCLK. RPL has an integral pull-up resistor.
RV5	Input	C9	**Receive Payload Indicator (RV5).** This is the receive payload indicator which locates the floating payload on the SBI336 or Telecom bus when configured for the receive byte wide interface. In SBI336 mode: This active high signal locates the position of the floating payloads for each tributary within the SBI336 structure. Timing differences between the port timing and the SBI336 bus timing are indicated by adjustments of this payload indicator relative to the fixed SBI336 structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the RPL signal. Multiple devices can drive this signal at uniquely assigned tributary columns within the SBI336 structure. In Telecom Bus mode: This signal identifies tributary payload frame boundaries

Pin Name	Type	Pin No.	Function
			on the receive parallel data bus. RV5 is set high to mark the V5 bytes on the bus. RV5 is sampled on the rising edge of SYSCLK. RV5 has an integral pull-up resistor.
RTPL	Input	B8	**Receive Tributary Payload (RTPL).** This signal indicates valid tributary payload data when configured for the receive byte wide Telecom bus interface. RTPL is set high during valid VC11 and VC12 bytes. RTPL is set low for all transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1,V2,V3,V4). RTPL is ignored when configured for SBI336 mode. RTPL is sampled on the rising edge of SYSCLK. RTPL has an integral pull-up resistor.
RTAIS	Input	A7	**Receive Tributary AIS Indicator (RTAIS).** This signal indicates tributaries in low order path AIS state when configured for the receive byte wide Telecom bus interface. RTAIS is set high when the tributary on the receive bus is in AIS state and is set low when the tributary is out of AIS state. RTAIS is ignored when configured for SBI336 mode. RTAIS is sampled on the rising edge of SYSCLK. RTAIS has an integral pull-up resistor.
RJUST_REQ	Input	A11	**Receive Justification Request (RJUST_REQ).** This is the receive side justification request when configured for SBI336 byte wide interface instead of the Serial SBI336S interface and when connecting to a PHY device. This signal is not used when connecting to a SBI336 link layer device nor when in telecom bus mode. The SBI336 Bus Justification Request signal, RJUST_REQ, is used to speed up, slow down or maintain the minimal rate of a slave timed SBI device. This active high signal indicates negative timing adjustments on the SBI336 bus when asserted high during the V3 or H3 octet, depending on the tributary type. In response to this the slave timed SBI336 device should send an extra byte in the V3 or H3 octet of the next frame along with a valid payload signal indicating a negative justification. This signal indicates positive timing adjustments on the SBI336 bus when asserted high during the octet following the V3 or H3 octet, depending on the tributary type. The slave timed SBI336 device should respond to this by not sending an octet during the V3 or H3 octet of the next frame along with a valid payload signal indicating a positive justification. For fractional rate links this signal is asserted high during any available information byte to indicate to the

Pin Name	Type	Pin No.	Function
			slave timed SBI336 device that the timing master device is able to accept another byte of data. For every byte that this signal is asserted high the slave device is expected to send a valid byte of data. All timing adjustments from the slave timed device in response to the justification request must still set the payload and payload indicators appropriately for timing adjustments. RJUST_REQ is sampled on the rising edge of SYSCLK. RJUST_REQ has an integral pull-up resistor.
Outgoing SBI Bus (68 Signals)			
OC1FP[4] OC1FP[3] OC1FP[2] OC1FP[1]	Output	AF23 W3 M3 C12	**Outgoing C1 Frame Pulse (OC1FP[4:1]).** This signal indicates the first C1 octet on the outgoing SBI or Telecom bus. <u>In SBI/SBI336 mode:</u> This signal also indicates multi-frame alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multi-frame signal. When using the SBI bus in synchronous mode the OC1FP signal indicates T1 and E1 signaling multi-frame alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data. For both 19.44Mhz SBI and 77.76MHz SBI336 buses, only OC1FP[1] will indicate the C1 byte position and OC1FP[4:2] are held low. <u>In Telecom Bus mode:</u> This signal may also be pulsed to indicate the J1 byte position and the byte following J1. For locked STS/AUs, the J1 byte position is locked to an offset of either 0 or 522. The byte following J1 is used to indicate multi-frame alignment and is only pulsed once every 4 frames marking the frame with the V1s. For a 77.76MHz Telecom bus, only OC1FP[1] is used and OC1FP[4:2] are held low. For a 19.44MHz Telecom bus, OC1FP[4:1] are all generated with the same C1 frame alignment. OC1FP[4:1] is updated on the rising edge of SREFCLK.
ODATA[4][7] ODATA[4][6] ODATA[4][5] ODATA[4][4] ODATA[4][3] ODATA[4][2] ODATA[4][1] ODATA[4][0] ODATA[3][7] ODATA[3][6] ODATA[3][5]	Tristate Output	AD18 AC17 AF19 AE18 AF18 AC16 AE17 AD16 T4 U2 T3	**Outgoing Data (ODATA[4:1][7:0]).** The Outgoing Data buses, ODATA[4:1][7:0], are separate time division multiplexed buses which transport tributaries by assigning them to fixed octets within the SBI or Telecom Bus structure. In 19.44MHz SBI mode, the SBS can drive this bus at uniquely assigned tributary columns within the SBI bus structure. ODATA[1][7:0] can be either a 19.44MHz SBI or Telecom Bus when combined with ODATA[4:2][7:0] or can be used as a standalone 77.76MHz SBI336 or

Pin Name	Type	Pin No.	Function
ODATA[3][5] ODATA[3][4] ODATA[3][3] ODATA[3][2] ODATA[3][1] ODATA[3][0] ODATA[2][7] ODATA[2][6] ODATA[2][5] ODATA[2][4] ODATA[2][3] ODATA[2][2] ODATA[2][1] ODATA[2][0] ODATA[1][7] ODATA[1][6] ODATA[1][5] ODATA[1][4] ODATA[1][3] ODATA[1][2] ODATA[1][1] ODATA[1][0]		T3 U1 T2 R4 T1 R3 K1 L3 K2 L4 J1 K3 J2 H1 A15 C15 A16 D15 A17 B19 A20 C19	Telecom Bus. ODATA[4:2][7:0] are held tri-state when configured for 77.76MHz operation. When the SBS is held reset, ODATA[4:1][7:0] is driven low. ODATA[4:1][7:0] are updated on the rising edge of SREFCLK.
ODP[4] ODP[3] ODP[2] ODP[1]	Tristate Output	AE21 U3 L2 B20	**Outgoing Bus Data Parity (ODP[4:1]).** The outgoing data parity signals carry the even or odd parity for the corresponding outgoing buses. In SBI/SBI336 modes, the parity calculation for ODP[x] encompasses the ODATA[x][7:0], OPL[x] and OV5[x] signals. In Telecom Bus mode, the parity calculation encompasses the ODATA[x][7:0] and optionally the OC1FP[x] and OPL[x] signals. In 19.44MHz SBI mode, The SBS can drive this bus at uniquely assigned tributary columns within the SBI bus structure. This parity signal is intended to detect conflicts in the tributary assignment. ODP[1] can be part of either a 19.44MHz SBI or Telecom Bus when combined with ODP[4:2] or can be used as part of a standalone 77.76MHz SBI336 or Telecom Bus. ODP[4:2] are held tri-state when configured for 77.76MHz operation. When the SBS is held reset, ODP[4:1] is driven low. ODP[4:1] is updated on the rising edge of SREFCLK.

Pin Name	Type	Pin No.	Function
OPL[4] OPL[3] OPL[2] OPL[1]	Tristate Output	AF22 V2 M4 A12	**Outgoing Bus Payload (OPL[4:1]).** The outgoing payload signal, OPL[x], indicates valid tributary data within each of the corresponding SBI buses. In Telecom bus mode, this signal indicates valid path payload. In SBI/SBI336 mode: This active high signal is asserted during all octets making up a tributary which includes all octets shaded gray in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI bus structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high. In 19.44MHz SBI mode, the SBS can drive this signal at uniquely assigned tributary columns within the SBI bus structure. In locked TVT mode, this signal must be driven in the same manner as for floating TVTs. In Telecom Bus mode: This signal distinguishes between transport overhead bytes and synchronous payload bytes. OPL[x] is set high to mark each payload byte on ODATA[x][7:0] and is set low to mark each transport overhead byte. OPL[1] can be part of either a 19.44MHz SBI or Telecom Bus when combined with OPL[4:2] or can be used as part of a standalone 77.76MHz SBI336 or Telecom Bus. OPL[4:2] are held tri-state when configured for 77.76MHz operation. When the SBS is held reset, OPL[4:1] is driven low. OPL[4:1] is updated on the rising edge of SREFCLK.
OV5[4] OV5[3] OV5[2] OV5[1]	Tristate Output	AD21 W2 L1 C13	**Outgoing Bus Payload Indicator (OV5[4:1]).** The active high signal, OV5[x], locates the position of the floating payload for each tributary within each of the corresponding outgoing SBI/SBI336 or Telecom buses. In SBI/SBI336 mode: This active high signal locates the position of the floating payloads for each tributary within the SBS/SBI336 structure. Timing differences between the port timing and the bus timing are indicated by adjustments of this payload indicator relative to the fixed bus structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the OPL[x] signal. In 19.44MHz SBI mode, the SBS can drive this signal at uniquely assigned tributary columns within the SBI bus

Pin Name	Type	Pin No.	Function
			structure. In locked TVT mode or fractional rate link mode this signal may be driven but must be ignored by the receiving device. In Telecom Bus mode: This signal identifies tributary payload frame boundaries on the corresponding outgoing data bus. OV5[x] is set high to mark the V5 bytes on the bus. OV5[1] can be part of either a 19.44MHz SBI or Telecom Bus when combined with OV5[4:2] or can be used as part of a standalone 77.76MHz SBI336 or Telecom Bus. OV5[4:2] are held tri-state when configured for 77.76MHz operation. When the SBS is held reset, OV5[4:1] is driven low. OV5[4:1] is updated on the rising edge of SREFCLK.
JUST_REQ[4] JUST_REQ[3] JUST_REQ[2] JUST_REQ[1]	Bidir	AC21 AA2 A4 Y2	**Shared Bus Justification Request (JUST_REQ[4:1]).** The SBI Bus Justification Request signal, JUST_REQ[x], is used to speed up, slow down or maintain the minimal rate of a slave timed SBI device. When the SBS is configured to be connected to a physical layer device, JUST_REQ[4:1] is an input. In SBI mode, JUST_REQ[4:1] is aligned to OC1FP[1] and the Outgoing bus. In SBI336 mode, JUST_REQ[1] is aligned to the IC1FP[1] and Incoming Bus. When the SBS is configured to be connected to a link layer device, JUST_REQ[4:1] is an output. In SBI mode, JUST_REQ[4:1] is aligned to IC1FP[1] and the Incoming bus. In SBI336 mode, JUST_REQ[1] is aligned to OC1FP[1] and the Outgoing bus. This active high signal, JUST_REQ[x], indicates negative timing adjustments on the corresponding SBI bus when asserted high during the V3 or H3 octet, depending on the tributary type. In response to this the slave timed SBI device should send an extra byte in the V3 or H3 octet of the next frame along with a valid payload signal indicating a negative justification. This signal indicates positive timing adjustments on the corresponding SBI bus when asserted high during the octet following the V3 or H3 octet, depending on the tributary type. The slave timed SBI device should respond to this by not sending an octet during the V3 or H3 octet of the next frame along with a valid payload signal indicating a positive justification. For fractional rate links this signal is asserted high during any available information byte to indicate to the slave timed SBI device that the timing master device is able to accept another byte of data. For every byte that this signal is asserted high the slave device is expected to send a valid byte of data. All timing adjustments from the slave timed device in response to the justification request must still set the

Pin Name	Type	Pin No.	Function
			payload and payload indicators appropriately for timing adjustments. JUST_REQ[1] can be part of either a 19.44MHz SBI bus when combined with JUST_REQ[4:2] or can be used as part of a standalone 77.76MHz SBI336 bus. JUST_REQ[4:1] is configured as an input in Telecom Bus mode and is ignored. JUST_REQ[4:1] is asserted and sampled on the rising edge of SREFCLK. JUST_REQ[4:2] have integral pull-up resistors.
OACTIVE[4] OACTIVE[3] OACTIVE[2] OACTIVE[1]	Output	AE23 V1 B5 D16	**Outgoing Bus Active Indicator (OACTIVE[4:1]).** The active high Outgoing SBI Bus Active Indicator signal, OACTIVE[x], is asserted high during all octets when driving data and control signals, ODATA[x][7:0], ODP[x], OPL[x] and OV5[x], onto the bus. All other SBI devices driving the bus listen to this signal to detect multiple sources driving the bus which can occur due to configuration problems. OACTIVE[4:1] should only be used when the SBS is configured for a 19.44MHz SBI bus. In all other modes, OACTIVE[4:1] should be ignored. When the SBS is held reset, OACTIVE[4:1] is driven low. OACTIVE[4:1] is updated on the rising edge of SREFCLK.
ODETECT[4] ODETECT[3] ODETECT[2] ODETECT[1]	Input	AD22 R2 C6 B17	**Outgoing Bus Active Detector (ODETECT[4:1]).** This input listens to the OR of all other SBI device ACTIVE signals. When another device is driving OACTIVE[x] high and this device detects ODETECT[x] is high from that other device it signals a collision and tristates the bus to minimize or eliminate contention. Tristating is only done with the 19.44MHz SBI buses. The AND of OACTIVE[x] and ODETECT[x] is sampled on the rising edge of SREFCLK to indicate that a collision occurred and can be used to indicate contention to management procedures. ODETECT[4:1] is only valid when the SBS is configured for a 19.44MHz SBI bus. ODETECT[4:1] must be held low when configured for 19.44MHz Telecom bus. In all other modes, ODETECT[4:1] is ignored. ODETECT[4:1] have integral pull-up resistors.
OTPL[4] OTPL[3] OTPL[2] OTPL[1]	Tristate Output	AC20 V3 C8 B13	**Outgoing Tributary Payload (OTPL[4:1]).** This signal is used to indicate tributary payload when configured for Telecom Bus and is held low when configured for SBI or SBI336 buses. OTPL[x] is set high during valid VC11 and VC12 bytes of the corresponding Outgoing bus. OTPL[x] is set low for all transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary

Pin Name	Type	Pin No.	Function
			transport overhead bytes (V1,V2,V3,V4). OTPL[1] can be part of either a 19.44MHz Telecom Bus when combined with OTPL[4:2] or can be used as part of a standalone 77.76MHz Telecom Bus. OTPL[4:2] are held tri-state when configured for 77.76MHz operation. When the SBS is held reset, OTPL[4:1] is driven low. OTPL[4:1] is updated on the rising edge of SREFCLK.
OTAIS[4] OTAIS[3] OTAIS[2] OTAIS[1]	Tristate Output	AE22 Y1 B7 B14	**Outgoing Tributary Alarm Indication Signal (OTAIS[4:1]).** This signal indicates tributaries in low order path AIS state for the corresponding Outgoing Telecom Bus and is held low when configured for SBI or SBI336 buses. OTAIS[x] is set high when the tributary on the corresponding Outgoing bus is in AIS state and is set low when the tributary is out of AIS state. OTAIS[1] can be part of either a 19.44MHz telecom bus when combined with OTAIS[4:2] or can be used as part of a standalone 77.76MHz telecom bus. OTAIS[4:2] are held tri-state when configured for 77.76MHz operation. When the SBS is held reset, OTAIS[4:1] is driven low. OTAIS[4:1] is updated on the rising edge of SREFCLK.
Incoming SBI Bus (56 Signals)			
IC1FP[4] IC1FP[3] IC1FP[2] IC1FP[1]	Input	T24 AE8 Y25 H3	**Incoming C1 Frame Pulse (IC1FP[4:1]).** This signal pulses high for one SREFCLK cycle to indicate the first C1 octet on the incoming SBI or Telecom Bus. <u>In SBI/SBI336 mode:</u> This signal also indicates multi-frame alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multi-frame signal. The frame pulse does not need to be repeated every 2KHz as the SBS will flywheel in its absence. When using the SBI bus in synchronous mode the IC1FP signal can be used to indicate T1 and E1 multi-frame alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data. For both 19.44MHz SBI and 77.76MHz SBI336 buses, only IC1FP[1] is used and IC1FP[4:2] are ignored. <u>In Telecom bus mode:</u> This signal may also be pulsed to indicate the J1 byte position and the byte following J1. For locked STS/AUs, the J1 byte position must be locked to an offset of either 0 or 522. The byte following J1 is used to indicate multi-frame alignment and should only pulse once every 4 frames marking the frame with the V1s. IC1FP[1] can be part of either a 19.44MHz Telecom bus when combined with IC1FP[4:2] or can be used as part of a standalone 77.76MHz Telecom bus. When using

Pin Name	Type	Pin No.	Function
			a 19.44MHz Telecom bus, all 4 C1 positions must be aligned and the four signals, IC1FP[4:1], are logically ORed together internally. IC1FP[4:1] is sampled on the rising edge of SREFCLK. IC1FP[4:2] have integral pull-up resistors.
IDATA[4][7] IDATA[4][6] IDATA[4][5] IDATA[4][4] IDATA[4][3] IDATA[4][2] IDATA[4][1] IDATA[4][0] IDATA[3][7] IDATA[3][6] IDATA[3][5] IDATA[3][4] IDATA[3][3] IDATA[3][2] IDATA[3][1] IDATA[3][0] IDATA[2][7] IDATA[2][6] IDATA[2][5] IDATA[2][4] IDATA[2][3] IDATA[2][2] IDATA[2][1] IDATA[2][0] IDATA[1][7] IDATA[1][6] IDATA[1][5] IDATA[1][4] IDATA[1][3] IDATA[1][2] IDATA[1][1] IDATA[1][0]	Input	U25 U26 V23 V24 V25 W24 W23 W25 AE7 AE6 AF5 AC7 AD6 AE5 Y4 AB1 AE12 AD12 AF11 AC12 AE11 AF10 AD11 AE10 E1 G4 F3 E2 F4 E3 D2 C1	**Incoming Bus Data (IDATA[4:1][7:0]).** The Incoming data buses, IDATA[4:1][7:0], are separate time division multiplexed buses which transports tributaries by assigning them to fixed octets within the SBI or Telecom Bus structure. Multiple SBI/SBI336 devices can drive this bus at uniquely assigned tributary columns within the SBI/SBI336 bus structure. IDATA[1][7:0] can be either a 19.44MHz SBI or Telecom bus when combined with IDATA[4:2][7:0] or can be used as a standalone 77.76MHz SBI336 or Telecom bus. IDATA[4:1][7:0] is sampled on the rising edge of SREFCLK. IDATA[4:2][7:0] have integral pull-up resistors.
IDP[4] IDP[3] IDP[2] IDP[1]	Input	U23 AD8 AF12 G3	**Incoming Bus Data Parity (IDP[4:1]).** The Incoming data parity signals carry the even or odd parity for the corresponding Incoming buses. In SBI/SBI336 modes, the parity calculation encompasses the IDATA[x][7:0], IPL[x] and IV5[x] signals. In Telecom bus mode, the parity calculation encompasses the IDATA[x][7:0] and optionally the IC1FP[x] and IPL[x] signals. Multiple SBI/SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI/SBI336 bus structure. This parity signal is intended to detect multiple sources in the column assignment. IDP[1] can be part of either a 19.44MHz SBI or Telecom Bus when combined with IDP[4:2] or can be used as part of a standalone 77.76MHz SBI336 or Telecom Bus.

Pin Name	Type	Pin No.	Function
			IDP[x] is sampled on the rising edge of SREFCLK. IDP[4:2] have integral pull-up resistors.
IPL[4] IPL[3] IPL[2] IPL[1]	Input	T25 AF7 AD13 G1	**Incoming Bus Payload (IPL[4:1]).** The Incoming Payload signal, IPL[4:1], indicates valid tributary data within each of the corresponding SBI buses. In Telecom Bus mode, this signal indicates valid path payload. In SBI/SBI336 mode: This active high signal is asserted during all octets making up a tributary which includes all octets shaded gray in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI/SBI336 structure. This signal goes low during the octet following the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI/SBI336 structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high. Multiple SBI/SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI/SBI336 structure. For locked TVTs, this signal must be driven in the same manner as for floating TVTs. In telecom bus mode: This signal distinguishes between transport overhead bytes and the synchronous payload bytes. IPL[x] is set high to mark each payload byte on IDATA[x][7:0] and is set low to mark each transport overhead byte.. IPL[1] can be part of either a 19.44MHz SBI or Telecom Bus when combined with IPL[4:2] or can be used as part of a standalone 77.76MHz SBI336 or Telecom Bus. IPL[x] is sampled on the rising edge of SREFCLK. IPL[4:2] have integral pull-up resistors.
IV5[4] IV5[3] IV5[2] IV5[1]	Input	R23 AF8 AE13 G2	**Incoming Bus Payload Indicator (IV5[4:1]).** This signal locates the position of the floating payload for each tributary within each of the incoming SBI/SBI336 or Telecom buses. In SBI/SBI336 mode: This active high signal locates the position of the floating payloads for each tributary within the SBI/SBI336 structure. Timing differences between the port timing and the bus timing are indicated by adjustments of this payload indicator relative to the fixed bus structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the IPL[x] signal. Multiple SBI/SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI/SBI336 structure.

Pin Name	Type	Pin No.	Function
			For locked TVTs, this signal must either be driven in the same manner as for floating TVTs or held low. In Telecom Bus mode: This signal identifies tributary payload frame boundaries on the corresponding incoming data bus. IV5[x] is set high to mark the V5 bytes on the bus. IV5[1] can be part of either a 19.44MHz SBI or Telecom Bus when combined with IV5[4:2] or can be used as part of a standalone 77.76MHz SBI336 or Telecom Bus. IV5[x] is sampled on the rising edge of SREFCLK. IV5[4:2] have integral pull-up resistors.
ITPL[4] ITPL[3] ITPL[2] ITPL[1]	Input	R26 AD9 Y24 F1	**Incoming Tributary Payload (ITPL[4:1]).** This signal is used to indicate tributary payload when configured for Telecom Bus and is unused when configured for SBI or SBI336 buses. ITPL[x] is set high during valid VC11 and VC12 bytes of the corresponding Incoming bus. ITPL[x] is set low for all transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1,V2,V3,V4). ITPL[1] can be part of either a 19.44MHz Telecom Bus when combined with ITPL[4:2] or can be used as part of a standalone 77.76MHz Telecom Bus. ITPL[x] is sampled on the rising edge of SREFCLK. ITPL[4:2] have integral pull-up resistors.
ITAIS[4] ITAIS[3] ITAIS[2] ITAIS[1]	Input	R25 AC10 W26 H2	**Incoming Tributary Alarm Indication Signal (ITAIS[4:1]).** This signal indicates tributaries in low order path AIS state for the corresponding Incoming Telecom Bus and is unused when configured for SBI or SBI336 buses. ITAIS[x] is set high when the tributary on the corresponding Incoming bus is in AIS state and is set low when the tributary is out of AIS state. ITAIS[1] can be part of either a 19.44MHz Telecom Bus when combined with ITAIS[4:2] or can be used as part of a standalone 77.76MHz Telecom Bus. ITAIS[x] is sampled on the rising edge of SREFCLK. ITAIS[4:2] have integral pull-up resistors.
Transmit Serial Data Interface (4 Signals)			
TPWRK TNWRK	Analog LVDS Output	K26 K25	**Transmit Working Serial Data.** In SBI336 mode, the differential transmit working serial data link (TPWRK/TNWRK) carries a transmit 77.76Mhz SBI336 data stream to a downstream working sink, in bit serial format, SBI336S. In Telecom bus mode, TPWRK/TNWRK carries the transmit 77.76MHz Telecom bus data stream to a downstream working sink, in bit serial format. Data on TPWRK/TNWRK is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B

Pin Name	Type	Pin No.	Function
			character bit 'a' is transmitted first and the bit 'j' is transmitted last. TPWRK/TNWRK are nominally 777.6 Mbps data streams.
TPPROT TNPROT	Analog LVDS Output	H25 H26	**Transmit Protect Serial Data.** In SBI336 mode, the differential transmit protect serial data link (TPPROT/TNPROT) carries a transmit 77.76Mhz SBI336 data stream to a downstream protect sink, in bit serial format, SBI336S. In Telecom bus mode, TPPROT/TNPROT carries the transmit 77.76MHz Telecom bus data stream to a downstream protection sink, in bit serial format. Data on TPPROT/TNPROT is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. TPPROT/TNPROT are nominally 777.6 Mbps data streams.
Transmit SBI336 Interface (15 Signals)			
TC1FP	Output	A24	**Transmit Serial SBI Frame Pulse.** The transmit serial SBI frame pulse signal (TC1FP) provides system timing of the transmit serial interface. When using the transmit parallel interface, this signal indicated the first C1 octet on the transmit SBI336 or Telecom bus. <u>Using the Transmit Serial Interface:</u> TC1FP is set high to indicate that the C1 frame boundary 8B/10B character has been serialized out on the transmit working serial data link (TPWRK/TNWRK) and the transmit protection serial data link (TPPROT/ TNPROT). TC1FP is output every 4 frame for SBI mode without CAS and for Telecom bus mode. TC1FP is output every 48 frames for SBI mode with CAS. <u>Using the Transmit Parallel Interface:</u> In SBI/SBI336 mode, this signal also indicates multi-frame alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multi-frame signal. When using the SBI bus in synchronous mode the TC1FP signal indicates T1 and E1 signaling multi-frame alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data. In Telecom bus mode, this signal may also be pulsed to indicate the J1 byte position and the byte following J1. For locked STS/AUs, the J1 byte position is locked to an offset of either 0 or 522. The byte following J1 is used to indicate multi-frame alignment and is only pulsed once every 4 frames marking the frame with the V1s. TC1FP is updated on the rising edge of SYSCLK.
TDATA[7]	Output	A21	**Transmit Data (TDATA[7:0]).** This is the transmit data

Pin Name	Type	Pin No.	Function
TDATA[6] TDATA[5] TDATA[4] TDATA[3] TDATA[2] TDATA[1] TDATA[0]		D19 C20 B21 D20 B22 D21 B23	bus when configured for the Transmit byte wide interface. The transmit data bus is a time division multiplexed bus which transports tributaries by assigning them to fixed octets within the 77.76MHz SBI336 or Telecom Bus structure. TDATA[7:0] is updated on the rising edge of SYSCLK.
TDP	Output	C18	**Transmit Data Parity (TDP).** This is the transmit data bus parity when configured for the Transmit byte wide interface. This signal carries the even or odd parity for the transmit bus signals. In SBI336 mode, the parity calculation encompasses the TDATA[7:0], TPL and TV5 signals. In Telecom Bus mode, the parity calculation encompasses the TDATA[7:0] and optionally the TC1FP and TPL signals. TDP is updated on the rising edge of SYSCLK.
TPL	Output	D17	**Transmit Payload (TPL).** The transmit SBI336 data bus payload signal indicates valid tributary payload data when configured for the transmit SBI336 byte wide interface. In telecom bus mode this signal indicates valid path payload. In SBI336 mode: This active high signal indicates valid data within the SBI336 structure. This signal is high during all octets making up a tributary which includes all octets shaded gray in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI336 structure. This signal goes low during the octet following the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI336 structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high. In Telecom Bus mode: This signal distinguishes between transport overhead bytes and synchronous payload bytes. TPL is set high to mark each payload byte on TDATA[7:0] and is set low to mark each transport overhead byte on TDATA[7:0]. TPL is updated on the rising edge of SYSCLK.
TV5	Output	C17	**Transmit Payload Indicator (TV5).** The transmit payload indicator (TV5) locates the floating payload on the SBI336 or Telecom bus when configured for the transmit byte wide interface. In SBI336 mode: This active high signal locates the position of the floating payloads for each tributary within the SBI336 structure. Timing differences between the port timing and the SBI336 bus timing are indicated by adjustments of this payload indicator relative to the fixed SBI336 structure. All movements indicated by this signal must

Pin Name	Type	Pin No.	Function
			be accompanied by appropriate adjustments in the TPL signal. In Telecom Bus mode: This signal identifies tributary payload frame boundaries on the transmit parallel data bus. TV5 is set high to mark the V5 bytes on the bus. TV5 is updated on the rising edge of SYSCLK.
TTPL	Output	A19	**Transmit Tributary Payload (TTPL).** This signal indicates valid tributary payload data when configured for transmit byte wide telecom bus interface. TTPL is set high during valid VC11 and VC12 bytes. TTPL is set low for all transport overhead bytes, high order path overhead bytes, fixes stuff column bytes and tributary transport overhead bytes (V1,V2,V3,V4). TTPL is held low in SBI336 mode. TTPL is updated on the rising edge of SYSCLK.
TTAIS	Output	A18	**Transmit Tributary AIS Indicator (TAIS).** This signal indicates tributaries in low order path AIS state when configured for the transmit byte wide Telecom Bus interface. TTAIS is set high when the tributary on the transmit bus is in AIS state and is set low when the tributary is out of AIS state. TTAIS is held low in SBI336 mode TTAIS is updated on the rising edge of SYSCLK.
TJUST_REQ	Output	D22	**Transmit Justification Request (TJUST_REQ).** This is the transmit side justification request when configured for SBI336 byte wide interface instead of the Serial SBI336S interface and when connecting to a link layer device. This signal is held low when connecting to a SBI336 physical layer device or when in telecom bus mode. The SBI336 Bus Justification Request signal, TJUST_REQ, is used to speed up, slow down or maintain the minimal rate of a slave timed SBI336 device. This active high signal indicates negative timing adjustments on the SBI336 bus when asserted high during the V3 or H3 octet, depending on the tributary type. In response to this the slave timed SBI336 device should send an extra byte in the V3 or H3 octet of the next receive frame along with a valid payload signal indicating a negative justification. This signal indicates positive timing adjustments on the SBI336 bus when asserted high during the octet following the V3 or H3 octet, depending on the tributary type. The slave timed SBI336 device should respond to this by not sending an octet during the V3 or H3 octet of the next receive frame along with a valid payload signal indicating a positive justification. For fractional rate links this signal is asserted high

Pin Name	Type	Pin No.	Function
			during any available information byte to indicate to the slave timed SBI336 device that the timing master device is able to accept another byte of data. For every byte that this signal is asserted high the slave device is expected to send a valid byte of data. All timing adjustments from the slave timed device in response to the justification request must still set the payload and payload indicators appropriately for timing adjustments. TJUST_REQ is updated on the rising edge of SYSCLK.
Microprocessor Interface (30 Signals)			
CSB	Input	AB25	**Chip Select Bar.** The active low chip select signal (CSB) controls microprocessor access to registers in the SBS device. CSB is set low during SBS Microprocessor Interface Port register accesses. CSB is set high to disable microprocessor accesses. If CSB is not required (i.e. register accesses controlled using RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.
RDB	Input	AA25	**Read Enable Bar.** The active low read enable bar signal (RDB) controls microprocessor read accesses to registers in the SBS device. RDB is set low and CSB is also set low during SBS Microprocessor Interface Port register read accesses. The SBS drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	AA26	**Write Enable Bar.** The active low write enable bar signal (WRB) controls microprocessor write accesses to registers in the SBS device. WRB is set low and CSB is also set low during SBS Microprocessor Interface Port register write accesses. The contents of D[15:0] are clocked into the addressed register on the rising edge of WRB while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	AE20 AD19 AF16 AD15 AE15 AF15 AD14 AC11 AD10 AF6 AC8 AD7 AF4 AC6 AD5 AE4	**Microprocessor Data Bus.** The bi-directional data bus, D[15:0] is used during SBS Microprocessor Interface Port register reads and write accesses. D[15] is the most significant bit of the data words and D[0] is the least significant bit.
A[8]/TRS A[7] A[6] A[5]	Input	AF3 AC5 AD4 AD1	**Microprocessor Address Bus.** The microprocessor address bus (A[8:0]) selects specific Microprocessor Interface Port registers during SBS register accesses. A[8] is also the Test Register Select (TRS) address pin

Pin Name	Type	Pin No.	Function
A[4] A[3] A[2] A[1] A[0]		AC2 AB3 AA4 AA3 Y3	and selects between normal and test mode register accesses. TRS is set high during test mode register accesses, and is set low during normal mode register accesses.
ALE	Input	AA23	**Address Latch Enable.** The address latch enable signal (ALE) is active high and latches the address bus (A[11:0]) when it is set low. The internal address latches are transparent when ALE is set high. ALE allows the SBS to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
INTB	Open Drain Output	N3	**Interrupt Request Bar**. The active low interrupt enable signal (INTB) output goes low when an SBS interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
General Function (9 Signals)			
SYSCLK	Input	D6	**SBI System Clock.** The 77MHz SBI reference clock signal, SYSCLK, is the master clock for the SBS device. SYSCLK is a 77.76 MHz clock, with a nominal 50% duty cycle. RC1FP, RDATA[7:0], RDP, RPL, RV5, RTPL, RTAIS and RJUST_REQ are sampled on the rising edge of SYSCLK. TC1FP, TDATA[7:0], TDP, TPL, TV5, TTPL, TAIS and TJUST_REQ are updated on the rising edge of SYSCLK.
SREFCLK19	Output	B4	**19.44MHz SBI Reference Clock.** The19.44MHz SBI reference clock signal, SREFCLK19, is a reference for 19.44MHz SBI bus and telecom bus interfaces. SREFCLK19 is a 19.44MHz clock, with a nominal 50% duty cycle and is generated from the 77.76MHz SYSCLK. When the incoming and outgoing buses are running at 19.44MHz, this signal should be tied to SREFCLK.
SREFCLK	Input	C5	**SBI Reference Clock.** The SBI reference clock, SREFCLK, is a reference for the incoming and outgoing SBI bus and telecom bus interfaces. SREFCLK is either a 77.76MHz clock with a nominal 50% duty cycle or a 19.44MHz clock with a nominal 50% duty cycle. IC1FP, IDATA[4:1][7:0], IDP[4:1], IPL[4:1], IV5[4:1], ITPL[4:1], ITAIS[4:1] and JUST_REQ[4:1] are sampled on the rising edge of SREFCLK. OC1FP, ODATA[4:1][7:0], ODP[4:1], OPL[4:1], OV5[4:1], OTPL[4:1], OTAIS[4:1] and JUST_REQ[4:1] are updated on the rising edge of SREFCLK. When the incoming and outgoing buses are running at 77.76MHz, this signal should be tied to SYSCLK. When the incoming and outgoing buses are running at 19.44MHz, this signal should be tied to SREFCLK19.
ICMP	Input	C7	**Incoming Connection Memory Page.** The incoming connection memory page select signal, ICMP, controls the selection of the connection memory page in the Incoming Memory Switch Unit, IMSU. When ICMP is

Pin Name	Type	Pin No.	Function
			set high, connection memory page 1 is selected. When ICMP is set low, connection memory page 0 is selected. The byte location during which ICMP is sampled is dependant on the mode of operation. 4-Frame SBI/SBI336 mode: ICMP is sampled at the C1 byte position of the incoming bus on the first frame of the 4-frame multi-frame (marked by IC1FP[1]). Changes to the connection memory page selection is synchronized to the frame boundary (A1 byte position) of the next four-frame multi-frame. 48-Frame SBI/SBI336 mode: ICMP is sampled at the C1 byte position of the incoming bus on the first frame of the 48-frame multi-frame (marked by IC1FP[1]). Changes to the connection memory page selection is synchronized to the frame boundary (A1 byte position) of the next 48-frame multi-frame. Telecom Bus mode: ICMP is sampled at the C1 byte position of every frame on the incoming bus (marked by IC1FP[4:1]). Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the next frame. ICMP is sampled on the rising edge of SREFCLK.
OCMP	Input	B6	**Outgoing Connection Memory Page.** The outgoing connection memory page select signal, OCMP, controls the selection of the connection memory page in the Outgoing Memory Switch Unit, OMSU. When OCMP is set high, connection memory page 1 is selected. When OCMP is set low, connection memory page 0 is selected. The byte location during which OCMP is sampled is dependant on the mode of operation. 4-Frame SBI/SBI336 mode: OCMP is sampled at the C1 byte position of the receive bus on the first frame of the 4-frame multi-frame (marked by RC1FP). Changes to the connection memory page selection is synchronized to the frame boundary (A1 byte position) of the next four-frame multi-frame. 48-Frame SBI/SBI336 mode: OCMP is sampled at the C1 byte position of the receive bus on the first frame of the 48-frame multi-frame (marked by RC1FP). Changes to the connection memory page selection is synchronized to the frame boundary (A1 byte position) of the next 48-frame multi-frame. Telecom Bus mode: OCMP is sampled at the C1 byte position of every frame on the receive bus (marked by RC1FP).

Pin Name	Type	Pin No.	Function
			Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the next frame. OCMP is sampled on the rising edge of SYSCLK.
RWSEL	Input	AD23	**Receive Working Serial Data Select.** The receive working serial data select signal, RWSEL, selects between sourcing outgoing data, ODATA[4:1][7:0], from the receive working serial data link, RPWRK/RNWRK, or the receive protect serial data link, RPPROT/RNPROT. When RWSEL is set high, the working serial bus is selected. When RWSEL is set low, the protect serial bus is selected. RWSEL is sampled at the C1 byte location as defined by the receive serial interface frame pulse signal, RC1FP. Changes to the selection of the working and protect serial streams are synchronized to the SBI frame boundary of the next frame. RWSEL is sampled on the rising edge of SYSCLK.
IUSER2	Input	AC15	**Input In-band Link User Signal.** The input in-band link user signal, IUSER2, provides external control over one of the bits in the in-band link. The USER[2] bit in the header of the in-band signaling channel of both the working and protection serial links will reflect the state of this input. IUSER2 an asynchronous signal and is internally synchronized to SYSCLK.
OUSER2	Output	AA1	**Output In-Band Link User Signal.** The output in-band link user signal, OUSER2, reflects the state of the USER[2] bit in the header of the in-band signaling channel of either the working or the protection serial link, whichever is active. OUSER2 is an asynchronous output.
RSTB	Input	AC22	**Reset Enable Bar.** The active low reset signal, RSTB, provides an asynchronous SBS reset. RSTB is a Schmitt triggered input with an integral pull-up resistor. When performing a reset of the SBS, this pin should be held low for a minimum of 1ms to properly reset the CSU. Alternatively, the ARESET bit in register 000H must be set for a minimum of 1ms after the SBS is reset by RSTB.
JTAG Interface (5 Signals)			
TCK	Input	P2	**Test Clock.** The JTAG test clock signal, TCK, provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	P3	**Test Mode Select.** The JTAG test mode select signal, TMS, controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	R1	**Test Data Input.** The JTAG test data input signal, TDI, carries test data into the SBS via the IEEE P1149.1 test

Pin Name	Type	Pin No.	Function
			access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tristate	M2	**Test Data Output.** The JTAG test data output signal, TDO, carries test data out of the SBS via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	P4	**Test Reset Bar.** The active low JTAG test reset signal, TRSTB, provides an asynchronous SBS test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when TRSTB is not being used, it must be connected to the RSTB input.
Analog Reference Resistors (2 Signals)			
RES	Analog	F25	**Reference Resistor Connection (RES).** An off-chip 3.16kΩ ±1% resistor is connected between this positive resistor reference pin, RES, and a Kelvin ground pin, RESK. An on-chip negative feedback path will force the 0.8V VREF voltage onto RES, therefore forcing 252uA of current to flow through the resistor.
RESK	Analog	F26	**Reference Resistor Connection (RESK).** An off-chip 3.16kΩ ±1% resistor is connected between the positive resistor reference pin, RES, and this Kelvin ground pin, RESK. An on-chip negative feedback path will force the 0.8V VREF voltage onto RES, therefore forcing 252uA of current to flow through the resistor.
Analog Test Bus (2 Signals)			
ATB0	Analog	M24	**Analog test pin (ATB0).** This pin is used for PMC validation and testing. This pin must be grounded.
ATB1	Analog	M23	**Analog test pin (ATB1).** This pin is used for PMC validation and testing. This pin must be grounded.
Analog High Voltage Power (8 Signals)			
CSU_AVDH	Power	P23	**CSU Analog Power (CSU_AVDH).** This pin should be connected to a well-decoupled +3.3V ± 5% DC supply.
AVDH[6] AVDH[5] AVDH[4] AVDH[3] AVDH[2] AVDH[1] AVDH[0]	Power	Y23 T23 J23 D24 E24 AB24 AC24	**Analog Power (AVDH[6:0]).** These pins should be connected to a well-decoupled +3.3V ± 5% DC supply.
Analog Low Voltage Power (4 Signals)			

Pin Name	Type	Pin No.	Function
CSU_AVDL[2] CSU_AVDL[1] CSU_AVDL[0]	Power	P25 P26 R24	**CSU Analog Power (CSU_AVDL[3:0]).** This pin should be connected to a well-decoupled +1.8V ± 5% DC supply. Each CSU_AVDL pin requires individual filtering.
AVDL	Power	N23	**Analog Power (AVDL).** This pin should be connected to a well-decoupled +1.8V ± 5% DC supply.
Digital Core Power (8 Signals)			
DVDDI[7] DVDDI[6] DVDDI[5] DVDDI[4] DVDDI[3] DVDDI[2] DVDDI[1] DVDDI[0]	Power	U24 AA24 AF20 AE9 AC1 J3 A5 C16	**Digital Core Power (DVDDI[7:0]).** The digital core power pins should be connected to a well-decoupled +1.8V ± 5% DC supply.
Digital I/O Power (22 Signals)			
DVDDO[21] DVDDO[20] DVDDO[19] DVDDO[18] DVDDO[17] DVDDO[16] DVDDO[15] DVDDO[14] DVDDO[13] DVDDO[12] DVDDO[11] DVDDO[10] DVDDO[9] DVDDO[8] DVDDO[7] DVDDO[6] DVDDO[5] DVDDO[4] DVDDO[3] DVDDO[2] DVDDO[1] DVDDO[0]	Power	AB23 D23 C24 B25 D18 D13 D8 D4 C3 B2 H4 N4 V4 AC4 AD3 AE2 AC9 AC14 AC19 AC23 AD24 AE25	**Digital I/O Power (DVDDO[21:0]).** The digital I/O power pins should be connected to a well-decoupled +3.3V ± 5% DC supply.
Ground (40 Signals)			
VSS[39] VSS[38] VSS[37] VSS[36] VSS[35] VSS[34] VSS[33] VSS[32] VSS[31] VSS[30] VSS[29] VSS[28] VSS[27] VSS[26] VSS[25]	Ground	A26 B26 C25 A25 B24 A14 A13 B3 A2 A1 B1 C2 N1 P1 AD2	**Ground (VSS[39:0]).** The ground pins, VSS[39:0], should be connected to GND.

Pin Name	Type	Pin No.	Function
VSS[24] VSS[23] VSS[22] VSS[21] VSS[20] VSS[19] VSS[18] VSS[17] VSS[16] VSS[15] VSS[14] VSS[13] VSS[12] VSS[11] VSS[10] VSS[9] VSS[8] VSS[7] VSS[6] VSS[5] VSS[4] VSS[3] VSS[2] VSS[1] VSS[0]		AE1 AF1 AF2 AE3 AF13 AF14 AE24 AF25 AF26 AE26 AD25 AD26 AC25 AC26 AB26 Y26 V26 T26 L26 J26 G26 E26 D26 D25 C26	
No Connect (60 signals)			
NC[59:0]	No Connect	A23 A22 A9 A6 A3 B18 B16 B15 B12 C23 C22 C21 C14 C4 D14 D9 D7 D5 D3 D1 E25 E23 E4 F24 F23 F2 G25 G24 G23 H24	The No Connect pins must be left floating.

Pin Name	Type	Pin No.	Function
		H23 J25 J24 J4 K24 K23 K4 L25 L24 L23 M1 N24 N2 P24 U4 W4 W1 AB4 AB2 AC18 AC13 AC3 AD20 AD17 AE19 AE16 AE14 AF21 AF17 AF9	

Notes on Pin Description:

1. All SBS inputs and bi-directionals except the LVDS links present minimum capacitive loading and operate at TTL (Vdd reference) logic levels.
2. Inputs RSTB, ALE, TMS, TDI, TRSTB, RDATA[7:0], RDP, RPL, RV5, RTPL, RTAIS, RJUST_REQ, JUST_REQ[4:2], ODETECT[4:1], IC1FP[4:2], IDATA[4:2][7:0], IDP[4:2], IPL[4:2], IV5[4:2], ITPL[4:2] and ITAIS[4:2] have internal pull-up resistors.
3. All SBS outputs have 20 mA drive capability except for JUST_REQ[4:1], D[15:0], TDO and INTB which have 12mA drive capability.
4. The DVDDI and AVDL and CSU_AVDL power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the SBS.
5. The AVDH, CSU_AVDH and DVDDO power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the SBS.
6. The DVDDI, DVDDO, AVDH, CSU_AVDH, AVDL and CSU_AVDL power pins all share a common ground.
7. See section 16.2 for information on power sequencing.
8. See section 16.3 for information on analog power filtering recommendations.

10 Functional Description

10.1 SBI Bus Data Formats

The 19.44MHz SBI bus is a multi-point to multi-point bus. Since each SBS SBI interface handles the full SBI bus capacity it will be more common for a single SBS to talk to multiple devices over the SBI bus, but there is nothing in the SBS that would prevent the SBS from sharing an SBI bus with other SBI devices.

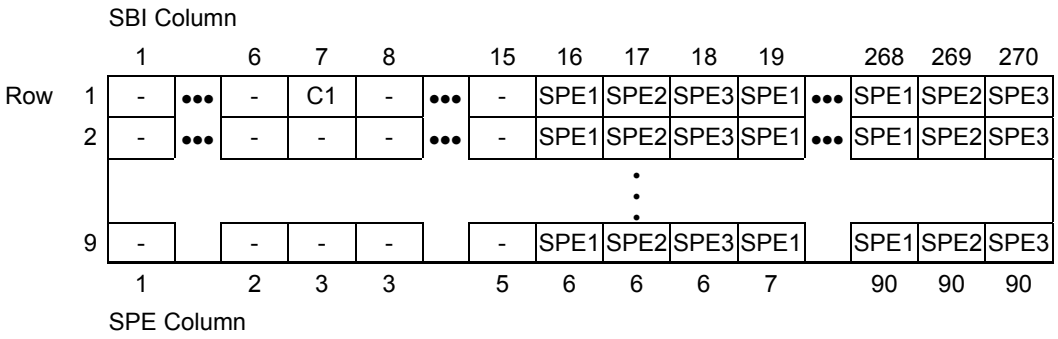
10.1.1 SBI Multiplexing Structure

The SBI structure uses a locked SONET/SDH structure fixing the position of the TU-3 relative to the STS-3/STM-1. The SBI is also of fixed frequency and alignment as determined by the reference clock (SREFCLK19) and frame indicator signal (IC1FP). Frequency deviations are compensated by adjusting the location of the T1/E1/DS3/E3/TVT1.5/TVT2 channels using floating tributaries as determined by the V5 indicator and payload signals (IV5[x] and IPL[x]). TVTs also allow for synchronous operation where SONET/SDH tributary pointers are carried within the SBI structure in place of the V5 indicator and payload signals (IV5[x] and IPL[x]). Fractional links use as many bytes as required within a given synchronous payload envelope (SPE) using the payload signals to indicate bytes carrying valid data.

Table 1 shows the bus structure for carrying T1, E1, TVT1.5, TVT2, DS3, E3 and Fractional tributaries in a SDH STM-1 like format. Up to 84 T1s, 63 E1s, 84 TVT1.5s, 63 TVT2s, 3 DS3s, 3 E3s or 3 Fractional rate links are carried within the octets labeled SPE1, SPE2 and SPE3 in columns 16-270. All other octets are unused and are of fixed position. The frame signal (IC1FP) occurs during the octet labeled C1 in Row 1 column 7.

The multiplexed links are separated into three Synchronous Payload Envelopes called SPE1, SPE2 and SPE3. Each envelope carries up to 28 T1s, 21 E1, 28 TVT1.5s, 21 TVT2s, a DS3, an E3 or a Fractional link. SPE1 carries the T1s numbered 1,1 through 1,28, E1s numbered 1,1 through 1,21, DS3 number 1,1, E3 number 1,1 or Fractional link 1,1. SPE2 carries T1s numbered 2,1 through 2,28, E1s numbered 2,1 through 2,21, DS3 number 2,1, E3 number 2,1 or Fractional link 2,1. SPE3 carries T1s numbered 3,1 through 3,28, E1s numbered 3,1 through 3,21, DS3 number 3,1, E3 number 3,1 or Fractional link 3,1. TVT1.5s are numbered the same as T1 tributaries and TVT2s are numbered the same as E1 tributaries.

Table 1 Structure for Carrying Multiplexed Links



The mappings for each link type are rigidly defined, however the mix of links transported across the bus at any one time is flexible. Each synchronous payload envelope, comprising 85 columns numbered 6 through 90, operates independently allowing a mix of T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s or Fractional links. For example, SPE1 could transport a single DS3, SPE2 could transport a single E3 and SPE3 could transport either 28 T1s or 21 E1s. Each SPE is restricted to carrying a single tributary type. SBI columns 16-18 are unused for T1, E1, TVT1.5 and TVT2 tributaries.

Tributary Numbering

Tributary numbering for T1 and E1 uses the SPE number, followed by the Tributary number within that SPE and are numbered sequentially. Table 2 and Table 3 show the T1 and E1 column numbering and relates the tributary number to the SPE column numbers and overall SBI column structure. Numbering for DS3 or E3 follows the same naming convention even though there is only one DS3 or E3 per SPE. TVT1.5s and TVT2s follow the same numbering conventions as T1 and E1 tributaries respectively. SBI columns 16-18 are unused for T1, E1, TVT1.5 and TVT2 tributaries.

Table 2 T1/TVT1.5 Tributary Column Numbering

T1#	SPE1 Column	SPE2 Column	SPE3 Column	SBI Column
1,1	7,35,63			19,103,187
2,1		7,35,63		20,104,188
3,1			7,35,63	21,105,189
1,2	8,36,64			22,106,190
2,2		8,36,64		23,107,191
•••				
1,28	34,62,90			100,184,268
2,28		34,62,90		101,185,269
3,28			34,62,90	102,186,270

Table 3 E1/TVT2 Tributary Column Numbering

E1#	SPE1 Column	SPE2 Column	SPE3 Column	SBI Column
1,1	7,28,49,70			19,82,145,208
2,1		7,28,49,70		20,83,146,209
3,1			7,28,49,70	21,84,147,210
1,2	8,29,50,71			22,85,148,211
2,2		8,29,50,71		23,86,149,212
•••				
1,21	27,48,69,90			79,142,205,268
2,21		27,48,69,90		80,143,206,269
3,21			27,48,69,90	81,144,207,270

10.1.2 SBI Timing Master Modes

The Scaleable Bandwidth Interconnect is a synchronous bus which is timed to a reference 19.44MHz clock and a 2KHz frame pulse (8KHz is easily derived from the 2KHz and 19.44MHz clock). All sources and sinks of data on this bus are timed to the reference clock and frame pulse.

The data format on the data bus allows for compensating between clock differences on the PHY, SBI and Link Layer devices. This is achieved by floating data structures within the SBI format.

Timing is communicated across the SBI bus by floating data structures within the bus. Payload indicator signals in the SBI control the position of the floating data structure and therefore the timing. When sources are running faster than the SBI the floating payload structure is advanced by an octet be passing an extra octet in the V3 octet locations (H3 octet for DS3 and E3 mappings). When the source is slower than the SBI the floating payload is retarded by leaving the octet after the V3 or H3 octet unused. Both these rate adjustments are indicated by the SBI control signals.

On the DROP BUS all timing is sourced from the PHY and is passed onto the Link Layer device by the arrival rate of data over the SBI.

On the ADD BUS timing can be controlled by either the PHY or the Link Layer device by controlling the payload and by making justification requests. When the Link Layer device is the timing master the PHY device gets its transmit timing information from the arrival rate of data across the SBI. When the PHY device is the timing master it signals the Link Layer device to speed up or slow down with justification request signals. The PHY timing master indicates a speedup request to the Link Layer by asserting the justification request signal high during the V3 or H3 octet. When this is detected by the Link Layer it will advance the channel by inserting data in the next V3 or H3 octet as described above. The PHY timing master indicates a slowdown request to the Link Layer by asserting the justification request signal high during the octet after the V3 or H3 octet. When detected by the Link Layer it will retard the channel by leaving the octet following the next V3 or H3 octet unused. Both advance and retard rate adjustments take place in the frame or multi-frame following the justification request.

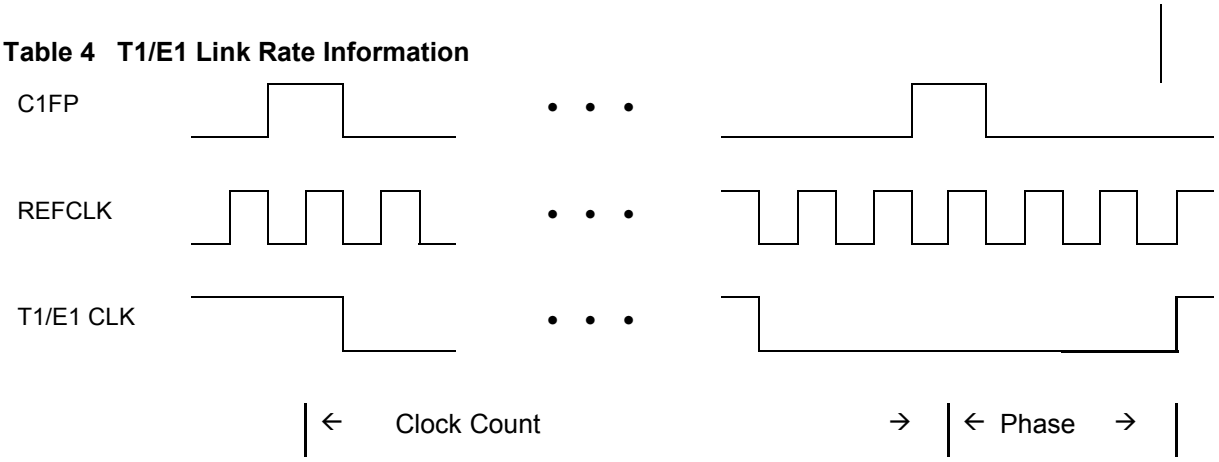
The SBI bus supports a synchronous SBI mode for T1 and E1 links. In this mode the DS0s or timeslots within the T1 or E1 tributaries are fixed to the locations shown in the T1 and E1 mappings. Effectively synchronous mode locks the V5 in the octet following the V1 octet and does not allow the tributaries to float relative to SREFCLK19.

10.1.3 SBI Link Rate Information

The SBI bus provides a method for carrying link rate information. This is optional on a per channel basis. Two methods are specified, one for T1 and E1 channels and the second for DS3 and E3 channels. Link rate information is not available for TVTs. These methods use the reference 19.44MHz SBI clock and the IC1FP frame synchronization signal to measure channel clock ticks and clock phase for transport across the bus.

The T1 and E1 method allows for a count of the number of T1 or E1 rising clock edges between two IC1FP frame pulses. This count is encoded in ClkRate[1:0] to indicate that the nominal number of clocks, one more than nominal or one less than nominal should be generated during the IC1FP period. This method also counts the number of 19.44MHz clock rising edges after sampling IC1FP high to the next rising edge of the T1 or E1 clock, giving the ability to control the phase of the generated clock. The link rate information passed across the SBI bus via the V4 octet and is shown in Table 4. Table 5 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

Table 4 T1/E1 Link Rate Information



Link Rate Octet	Bit #	7	6	5:4	3:0
T1/E1 Format		ALM	0	ClkRate[1:0]	Phase[3:0]

Table 5 T1/E1 Clock Rate Encoding

ClkRate[1:0]	T1 Clocks / 2KHz	E1 Clocks / 2 KHz
“00” – Nominal	772	1024
“01” – Fast	773	1025
“1x” – Slow	771	1023

The DS3 and E3 method for transferring link rate information across the SBI passes the encoded count of DS3/E3 clocks between C1FP pulses in the same method used for T1/E1 tributaries, but does not pass any phase information. The other difference from T1/E1link rate is that ClkRate[1:0] indicates whether the nominal number of clocks are generated or if four fewer or four extra clocks are generated during the C1FP period. The format of the DS3/E3 link rate octet is shown in Table 6. This is passed across the SBI via the Linkrate octet which follows the H3 octet in the column, see Table 12 and Table 15. Table 7 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

Table 6 DS3/E3 Link Rate Information

Link Rate Octet	Bit #	7	6	5:4	3:0
DS3/E3 Format		ALM	0	ClkRate[1:0]	Unused

Table 7 DS3/E3 Clock Rate Encoding

ClkRate[1:0]	DS3 Clocks / 2KHz	E3 Clocks / 2 KHz
“00” – Nominal	22368	17184
“01” – Fast	22372	17188
“1x” – Slow	22364	17180

10.1.4 Alarms

This specification provides a method for transferring alarm conditions across the SBI bus. This is optional on a per tributary basis and is valid for T1, E1, DS3, and E3 tributaries but not valid for transparent VTs nor Fractional links.

Table 4 and Table 6 show the alarm indication bit, ALM, as bit 7 of the Link Rate Octet. Devices which do not support alarm indications should set this bit to 0. When not enabled the value of this bit must be ignored by the receiving device.

The presence of an alarm condition is indicated by the ALM bit set high in the Link Rate Octet. The absence of an alarm condition is indicated by the ALM bit set low in the Link Rate Octet. The ALM bit is transparent to the SBS.

10.1.5 T1 Tributary Mapping

Table 8 shows the format for mapping 84 T1s within the SPE octets. The DS0s and framing bits within each T1 are easily located within this mapping for channelized T1 applications. It is acceptable for the framing bit to not carry a valid framing bit on the Add Bus since the physical layer device will provide this information. Unframed T1s use the exact same format for mapping 84 T1s into the SBI except that the T1 tributaries need not align with the frame bit and DS0 locations. The V1,V2 and V4 octets are not used to carry T1 data and are either reserved or used for control across the interface. When enabled, the V4 octet is the Link Rate octet of Tables 1 and 3. It carries alarm and clock phase information across the SBI bus. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries a T1 data octet but only during rate adjustments as indicated by the V5 indicator signals, IV5 and OV5, and payload signals, IPL and OPL. The PPSSSSFR octets carry channel associated signaling (CAS) bits and the T1 framing overhead. The DS0 octets are the 24 DS0 channels making up the T1 link.

The V1,V2,V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for T1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2KHz multi-frame. The position of the floating T1 is identified via the V5 Indicator signals, IV5 and OV5, which locate the V5 octet. When the T1 tributary rate is faster than the SBI nominal T1 tributary rate, the T1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the T1 tributary rate is slower than the nominal SBI tributary rate the T1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

Table 8 T1 Framing Format

	COL #	**T1#1,1**	T1#2,1-3,28	**T1#1,1**	T1#2,1-3,28	**T1#1,1**	T1#2,1-3,28
ROW #	1-18	19	20-102	103	104-186	187	188-270
1	Unused	V1	V1	V5	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V2	V2	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-

	COL #	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V3	V3	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V4	V4	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-

The $P_1P_0S_1S_2S_3S_4$FR octet carries T1 framing in the F bit and channel associated signaling in the $P_1P_0$and $S_1S_2S_3S_4$bits. Channel associated signaling is optional. The R bit is reserved and is set to 0. The P_1P_0bits are used to indicate the phase of the channel associated signaling and the $S_1S_2S_3S_4$ bits are the channel associated signaling bits for the 24 DS0 channels in the T1. Table 9 shows the channel associated signaling bit mapping and how the phase bits locate the sixteen state CAS mapping as well as T1 frame alignment for super frame and extended superframe formats. When using four state CAS then the signaling bits are A1-A24, B1-B24, A1-B24, B1-B24 in place of are A1-A24, B1-B24, C1-C24, D1-D24. When using 2 state CAS there are only A1-A24 signaling bits.

Table 9 T1 Channel Associated Signaling Bits

				SF	ESF	
S_1	**S_2**	**S_3**	**S_4**	**F**	**F**	**P_1 P_0**
A1	A2	A3	A4	F1	M1	00
A5	A6	A7	A8	S1	C1	00
A9	A10	A11	A12	F2	M2	00
A13	A14	A15	A16	S2	F1	00
A17	A18	A19	A20	F3	M3	00

				SF	ESF	
S_1	S_2	S_3	S_4	F	F	P_1 P_0
A21	A22	A23	A24	S3	C2	00
B1	B2	B3	B4	F4	M4	01
B5	B6	B7	B8	S4	F2	01
B9	B10	B11	B12	F5	M5	01
B13	B14	B15	B16	S5	C3	01
B17	B18	B19	B20	F6	M6	01
B21	B22	B23	B24	S6	F3	01
C1	C2	C3	C4	F1	M7	10
C5	C6	C7	C8	S1	C4	10
C9	C10	C11	C12	F2	M8	10
C13	C14	C15	C16	S2	F4	10
C17	C18	C19	C20	F3	M9	10
C21	C22	C23	C24	S3	C5	10
D1	D2	D3	D4	F4	M10	11
D5	D6	D7	D8	S4	F5	11
D9	D10	D11	D12	F5	M11	11
D13	D14	D15	D16	S5	C6	11
D17	D18	D19	D20	F6	M12	11
D21	D22	D23	D24	S6	F6	11

T1 tributary asynchronous timing is compensated via the V3 octet as described in section 10.1.2. T1 tributary link rate adjustments are optionally passed across the SBI via the V4 octet as described in section 10.1.3. T1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location as described in section 10.1.3 and 10.1.4.

The SBI bus allows for a synchronous T1 mode of operation. In this mode the T1 tributary mapping is fixed to that shown in Table 8 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.

10.1.6 E1 Tributary Mapping

Table 10 shows the format for mapping 63 E1s within the SPE octets. The timeslots and framing bits within each E1 are easily located within this mapping for channelized E1 applications. It is acceptable for the framing bits to not carry valid framing information on the Add Bus since the physical layer device will provide this information. Unframed E1s use the exact same format for mapping 63 E1s into the SBI except that the E1 tributaries need not align with the timeslot locations associated with channelized E1 applications. The V1, V2 and V4 octets are not used to carry E1 data and are either reserved used for control information across the interface. When enabled, the V4 octet carries clock phase information across the SBI. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries an E1 data octet but only during rate adjustments as indicated by the V5 indicator signals, IV5 and OV5, and payload signals, IPL and OPL. The PP octets carry channel associated signaling phase information and E1 frame alignment. TS#0 through TS#31 make up the E1 channel.

The V1, V2, V3, and V4 octets are fixed to the locations shown. All the other octets, shown shaded for E1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2KHz multi-frame. The position of the floating E1 is identified via the V5 Indicator signals, IV5 and OV5, which locate the V5 octet. When the E1 tributary rate is faster than the E1 tributary nominal rate, the E1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the E1 tributary rate is slower than the nominal rate the E1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

Table 10 E1 Framing Format

	COL #	**E1#1,1**	#2,1-3,21	**E1#1,1**	#2,1-3,21	**E1#1,1**	#2,1-3,21	**E1#1,1**	#2,1-3,21
ROW #	1-18	19	20-81	82	83-144	145	146-207	208	209-270
1	Unused	V1	V1	V5	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V2	V2	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V3	V3	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-

	COL #	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21
ROW #	1-18	19	20-81	82	83-144	145	146-207	208	209-270
1	Unused	V4	V4	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-

When using channel associated signaling (CAS) TS#16 carries the ABCD signaling bits and the timeslots 17 through 31 are renumbered 16 through 30. The PP octet is 0h for all frames except for the frame which carries the CAS for timeslots 15/30 at which time the PP octet is C0h. The first octet of the CAS multi-frame, RRRRRRRR, is reserved and should be ignored by the receiver when CAS signaling is enabled. Table 11 shows the format of timeslot 16 when carrying channel associated signaling.

Table 11 E1 Channel Associated Signaling bits

TS#16[7:4]	TS#16[3:0]	PP
RRRR	RRRR	00
ABCD1	ABCD16	00
ABCD2	ABCD17	00
ABCD3	ABCD18	00
ABCD4	ABCD19	00
ABCD5	ABCD20	00
ABCD6	ABCD21	00
ABCD7	ABCD22	00
ABCD8	ABCD23	00
ABCD9	ABCD24	00
ABCD10	ABCD25	00
ABCD11	ABCD26	00
ABCD12	ABCD27	00
ABCD13	ABCD28	00
ABCD14	ABCD29	00
ABCD15	ABCD30	C0

E1 tributary asynchronous timing is compensated via the V3 octet as described in section 10.1.2. E1 tributary link rate adjustments are optionally passed across the SBI via the V4 octet as described in section 10.1.3. E1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location as described in section 10.1.3 and 10.1.4.

The SBI bus allows for a synchronous E1 mode of operation. In this mode the E1 tributary mapping is fixed to that shown in Table 10 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.

10.1.7 DS3 Tributary Mapping

Table 12 shows a DS3 tributary mapped within the first synchronous payload envelope SPE1. The V5 indicator pulse identifies the V5 octet. The DS3 framing format does not follow an 8KHz frame period so the floating DS3 multi-frame located by the V5 indicator, shown in heavy border gray region in Table 12, will jump around relative to the H1 frame on every pass. In fact the V5 indicator will often be asserted twice per H1 frame, as is shown by the second V5 octet in Table 12. The V5 indicator and payload signals indicate negative and positive rate adjustments which are carried out by either putting a data byte in the H3 octet or leaving empty the octet after the H3 octet.

Table 12 DS3 Framing Format

	SPE **COL #**		DS3 **1**	DS3 **2-56**	DS3 **57**	DS3 **58-84**	DS3 **Col 85**
ROW	**SBI COL# 1,4,7,10**	**13**	**16**	**•••**	**184**	**•••**	**268**
1	Unused	**H1**	V5	DS3	DS3	DS3	DS3
2	Unused	**H2**	DS3	DS3	DS3	DS3	DS3
3	Unused	**H3**	DS3	DS3	DS3	DS3	DS3
4	Unused	**Linkrate**	DS3	DS3	DS3	DS3	DS3
5	Unused	Unused	DS3	DS3	DS3	DS3	DS3
6	Unused	Unused	DS3	DS3	DS3	DS3	DS3
7	Unused	Unused	DS3	DS3	DS3	DS3	DS3
8	Unused	Unused	DS3	DS3	V5	DS3	DS3
9	Unused	Unused	DS3	DS3	DS3	DS3	DS3

Because the DS3 tributary rate is less than the rate of the gray region, padding octets are interleaved with the DS3 tributary to make up the difference in rate. Interleaved with every DS3 multi-frame are 35 stuff octets, one of which is the V5 octet. These 35 stuff octets are spread evenly across seven DS3 subframes. Each DS3 subframe is eight blocks of 85 bits. The 85 bits making up a DS3 block are padded out to be 11 octets. Table 13 shows the DS3 block 11 octet format where R indicates a stuff bit, F indicates a DS3 framing bit and I indicates DS3 information bits. Table 14 shows the DS3 multi-frame format that is packed into the gray region of Table 12. In this table V5 indicates the V5 octet which is also a stuff octet, R indicates a stuff octet and B indicates the 11 octet DS3 block. Each row in Table 14 is a DS3 multi-frame. The DS3 multi-frame stuffing format is identical for 5 multi-frames and then an extra stuff octet after the V5 octet is added every sixth frame.

Table 13 DS3 Block Format

Octet #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Data	RRRFIIII	8*I	8*I	8*I	8*I	8*I	8*I	8*I	8*I	8*I	8*I

Table 14 DS3 Multi-frame Stuffing Format

V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B

DS3 asynchronous timing is compensated via the H3 octet as described in section 10.1.2. DS3 link rate adjustments are optionally passed across the SBI via the Linkrate octet as described in section 10.1.3. DS3 alarm conditions are optionally passed across the SBI bus via the Linkrate octet as described in section 10.1.3 and 10.1.4.

10.1.8 E3 Tributary Mapping

Table 15 shows a E3 tributary mapped within the first synchronous payload envelope SPE1. The V5 indicator pulse identifies the V5 octet. The E3 framing format does not follow an 8KHz frame period so the floating frame located by the V5 indicator and shown in gray in Table 15, will jump around relative to the H1 frame on every pass. In fact the V5 indicator will be asserted two or three times per H1 frame, as is shown by the second and third V5 octet in Table 15. The V5 indicator and payload signals indicate negative and positive rate adjustments which are carried out by either putting a data byte in the H3 octet or leaving empty the octet after the H3 octet.

Table 15 E3 Framing Format

	SPE **COL #**		E3 **1**	E3 **2-18**	E3 **19**	E3 **20-38**	E3 **39**	E3 **40-84**	E3 **85**
ROW	**SBI COL# 1,4,7,10**	**13**	**16**	**•••**	**70**	**•••**	**130**	**•••**	**268**
1	Unused	**H1**	V5	E3	E3	E3	E3	E3	E3
2	Unused	**H2**	E3	E3	E3	E3	E3	E3	E3
3	Unused	**H3**	E3	E3	E3	E3	E3	E3	E3
4	Unused	**Linkrate**	E3	E3	V5	E3	E3	E3	E3
5	Unused	Unused	E3	E3	E3	E3	E3	E3	E3
6	Unused	Unused	E3	E3	E3	E3	E3	E3	E3
7	Unused	Unused	E3	E3	E3	E3	V5	E3	E3
8	Unused	Unused	E3	E3	E3	E3	E3	E3	E3
9	Unused	Unused	E3	E3	E3	E3	E3	E3	E3

Because the E3 tributary rate is less than the rate of the gray region, padding octets are interleaved with the E3 tributary to make up the difference in rate. Interleaved with every E3 frame is an alternating pattern of 81 and 82 stuff octets, one of which is the V5 octet. These 81 or 82 stuff octets are spread evenly across the E3 frame. Each E3 subframe is 48 octet which is further broken into 4 equal blocks of 12 octets each. Table 16 shows the alternating E3 frame stuffing format that is packed into the gray region of Table 15. Note that there are 6 stuff octets after the V5 octet in one frame and 5 stuff octets after the V5 octet in the next frame. In this table V5 indicates the V5 octet which is also a stuff octet, R indicates a stuff octet, D indicates an E3 data octet, FAS indicates the first byte of the 10 bit E3 Frame Alignment Signal.

Table 16 E3 Frame Stuffing Format

V5	6*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	12*D		5*R	12*D	5*R	12*D	5*R	12*D
	5*R	12*D		5*R	12*D	5*R	12*D	5*R	12*D
	5*R	12*D		5*R	12*D	5*R	12*D	5*R	12*D
V5	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	12*D		5*R	12*D	5*R	12*D	5*R	12*D
	5*R	12*D		5*R	12*D	5*R	12*D	5*R	12*D
	5*R	12*D		5*R	12*D	5*R	12*D	5*R	12*D

E3 asynchronous timing is compensated via the H3 octet as described in section 10.1.2. E3 link rate adjustments are optionally passed across the SBI via the Linkrate octet as described in section 10.1.3. E3 alarm conditions are optionally passed across the SBI bus via the Linkrate octet as described in section 10.1.3 and 10.1.4.

10.1.9 Transparent VT1.5/TU11 Mapping

VT1.5 and TU11 virtual tributaries, TVT1.5s, are transported across the SBI bus in a similar manner to the T1 tributary mapping. Table 17 shows the transparent structure where "I" is used to indicate information bytes. There are two options when carrying virtual tributaries on the SBI bus, the primary difference being how the floating V5 payload is located.

The first option is locked TVT mode which carries the entire VT1.5/TU11 virtual tributary indicated by the shaded region in Table 17. Locked is used to indicate that the location of the V1,V2 pointer is locked. The virtual tributary must have a valid V1,V2 pointer to locate the V5 payload. In this mode the V5 indicator and payload signals, IV5, OV5, IPL and OPL, may be generated but must be ignored by the receiving device. In locked mode timing is always sourced by the transmitting side, therefore justification requests are not used and the JUST_REQ signal is ignored. Other than the V1 and V2 octets which must carry valid pointers, all octets can carry data in any format. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 17.

The second option is floating TVT mode which carries the payload comprised of the V5 and I octets within the shaded region of Table 17. In this mode the V1,V2 pointers are still in a fixed location and may be valid but are ignored by the receiving device. The V5 indicator and payload signals, IV5, OV5, IPL and OPL, must be valid and are used to locate the floating payload. The justification request signal can be used to control the timing on the add bus. The V3 octets are used to accommodate justification requests. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 17.

Table 17 Transparent VT1.5/TU11 Format

	COL #	VT1.5#1,1	**#2,1-3,28**	VT1.5#1,1	**#2,1-3,28**	VT1.5#1,1	**#2,1-3,28**
ROW #	**1-18**	**19**	**20-102**	**103**	**104-186**	**187**	**188-270**
1	Unused	V1	V1	V5	-	I	-

	COL #	VT1.5#1,1	**#2,1-3,28**	VT1.5#1,1	**#2,1-3,28**	VT1.5#1,1	**#2,1-3,28**
ROW #	**1-18**	**19**	**20-102**	**103**	**104-186**	**187**	**188-270**
2	Unused	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-
7	Unused	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-
1	Unused	V2	V2	I	-	I	-
2	Unused	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-
7	Unused	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-
1	Unused	V3	V3	I	-	I	-
2	Unused	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-
7	Unused	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-
1	Unused	V4	V4	I	-	I	-
2	Unused	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-
7	Unused	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-

10.1.10 Transparent VT2/TU12 Mapping

VT2 and TU12 virtual tributaries, TVT2s, are transported across the SBI bus in a similar manner to the E1 tributary mapping. Table 18 shows the transparent structure where "I" is used to indicate information bytes. There are two options when carrying virtual tributaries on the SBI bus, the primary difference being how the floating V5 payload is located.

The first option is locked TVT mode which carries the entire VT2/TU12 virtual tributary indicated by the shaded region in Table 18. Locked is used to indicate that the location of the V1,V2 pointer is locked. The virtual tributary must have a valid V1,V2 pointer to locate the V5 payload. In this mode the V5 indicator and payload signals, IV5, OV5, IPL and OPL, are optionally generated but must be ignored by the receiving device. In locked mode timing is always sourced by the transmitting side, therefore justification requests are not used and the JUST_REQ signal is ignored. Other than the V1 and V2 octets which are carrying valid pointers, all octets can carry data in any format. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 18.

The second option is floating TVT mode which carries the payload comprised of the V5 and I octets within the shaded region of Table 18. In this mode the V1,V2 pointers are still in a fixed location and may be valid but are ignored by the receiving device. The V5 indicator and payload signals, IV5, OV5, IPL and OPL, must be valid and are used to locate the floating payload. The justification request signal can be used to control the timing on the add bus. The V3 octet is used to accommodate justification requests. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 18.

Table 18 Transparent VT2/TU12 Format

	COL #	E1#1,1	**#2,1-3,21**	E1#1,1	**#2,1-3,21**	E1#1,1	**#2,1-3,21**	E1#1,1	**#2,1-**
ROW #	**1-18**	**19**	**20-81**	**82**	**83-144**	**145**	**146-207**	**208**	**209-270**
1	Unused	V1	V1	V5	-	I	-	I	-
2	Unused	I	-	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-	I	-
7	Unused	I	-	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-	I	-
1	Unused	V2	V2	I	-	I	-	I	-
2	Unused	I	-	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-	I	-

	COL #	E1#1,1	**#2,1-3,21**	E1#1,1	**#2,1-3,21**	E1#1,1	**#2,1-3,21**	E1#1,1	**#2,1-**
ROW #	**1-18**	**19**	**20-81**	**82**	**83-144**	**145**	**146-207**	**208**	**209-270**
7	Unused	I	-	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-	I	-
1	Unused	V3	V3	I	-	I	-	I	-
2	Unused	I	-	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-	I	-
7	Unused	I	-	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-	I	-
1	Unused	V4	V4	I	-	I	-	I	-
2	Unused	I	-	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-	I	-
7	Unused	I	-	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-	I	-

10.1.11 Fractional Rate Tributary Mapping

The Fractional Rate SBI mapping is intended for support of data services over fractional DS3 or similar links. A fractional rate link is mapped into any SPE octet as defined in Table 1. Table 19 shows all the available information (I) octets useable for carrying a Fractional rate link mapped to a single SPE. There are no V1 to V5 bytes nor frame alignment signals in a fractional rate link. The Add bus and Drop bus payload signals, IPL and OPL, indicate when a fractional rate information byte contains valid data or is empty. The fractional rate link Add bus can have the timing master be either the PHY or the Link Layer device. When the PHY is the timing master the JUST_REQ signal from the PHY communicates the transmit rate to the Link Layer device. The JUST_REQ signal is asserted during any of the available fractional rate link octets to indicate that the PHY can accept another byte of data. For every byte that is marked with the JUST_REQ signal the Link Layer device should respond with a valid byte to the PHY within a short time. The PHY accepts data from the Link Layer device whenever it sees valid data as indicated by the IPL or OPL signal, whether it is timing master or slave.

Table 19 Fractional Rate Format

	SPE **COL #**	Fractional **1**	Fractional **2-84**	Fractional **Col 85**
ROW	**SBI COL# 1,4,7,10,13**	**16**	**•••**	**268**
1	Unused	I	I	I
2	Unused	I	I	I
3	Unused	I	I	I
4	Unused	I	I	I
5	Unused	I	I	I
6	Unused	I	I	I
7	Unused	I	I	I
8	Unused	I	I	I
9	Unused	I	I	I

10.1.12 SBI336 Bus Format

The 77.76MHz SBI336 bus is exactly four interleaved 19.44MHz SBI buses. There are some slight differences between the two formats to accommodate the increased clock rate. The differences are:

The JUST_REQ signal is referenced to the Drop bus C1FP alignment rather than the common Add/Drop C1FP alignment of the SBI bus. This aids 77.76MHz bus timing by allowing buffering and retiming logic to be put between SBI336 devices. This change also aids construction of larger SBI cross connect systems using smaller buffers between devices by controlling the C1 frame alignment independently in each direction.

10.1.13 SBI336 Multiplexing Structure

Table 20 Structure for Carrying Multiplexed Links in SBI336

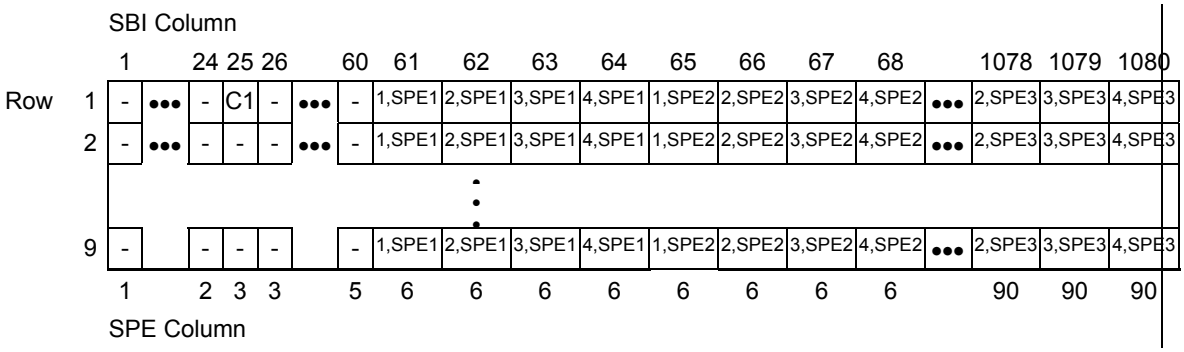


Table 20 shows how 12 SPEs are multiplexed into a 77.76MHz SBI336 bus. The structure is exactly the same as byte interleaving four 19.44MHz SBI buses. 1,SPE1 identifies SPE1 from the first SBI equivalent bus, 2,SPE1 identifies SPE1 from the second SBI equivalent bus, and so on. All tributary mapping formats are exactly the same as for the 19.44MHz SBI bus with the only difference that there are four times the number of tributaries. Tributary numbering appends the equivalent SBI number to the original SBI numbering. For example, the first T1 in a SBI bus would be numbered T1 #1,1 whereas the first T1 in a SBI336 bus would be numbered T1 #1,1,1. Likewise the second T1 in a SBI bus would be T1 #2,1 whereas the second T1 in a SBI336 bus would be T1 #2,1,1.

10.2 Incoming SBI336 Timing Adapter

The Incoming SBI336 Timing Adapter, ISTA, provides a multiplexing function of four incoming 19.44MHz SBI or Telecom buses into a 77.76MHz SBI336 or Telecom bus. This involves simple column muxing of the four incoming SBI or Telecom buses. The timing adapter block also provides a transparent mode when the incoming interface is already in SBI336 or 77.76MHz Telecom bus format.

When the SBS is connected to an 19.44MHz SBI physical layer device, the justification request signal, JUST_REQ, is an input to the SBS and is aligned to the outgoing bus. This block re-aligns the justification request signal from the outgoing frame alignment, marked by OC1FP, to the internal incoming SBI336 frame alignment. When the SBS is connected to a 19.44MHz SBI link layer device or any 77.76MHz SBI336 device, no re-alignment of the justification request is required by this block.

10.3 CAS Expanders

The Channel Associated Signaling Expander blocks, ICASE and OCASE, pull the CAS information from the SBI336 formatted bus on a tributary basis so that it can be switched through the memory switch with the DS0 data. For tributaries enabled for DS0 switching the Channel Associated Signaling bits (CAS bits) are double buffered on a signaling multi-frame boundary and repeated along side the tributary data for the duration of the multi-frame. This block can be used for T1 and E1 tributaries simultaneously across different SBI SPEs. This block adds one T1 multi-frame (24 frames) or one E1 multi-frame (16 frames) of latency to the CAS bits.

10.4 Memory Switch Units

The Memory Switch Unit blocks, IMSU and OMSU, provide DS0 or column switching of the SBI336 or 77.76MHz Telecom bus. Any input byte (or column) can be switched to any output byte (or column). Four bits of Channel Associated Signaling (CAS) and three or four bits of control information are switched along with the data byte. In SBI336 mode, the control signals are PL, V5 and JUST_REQ. In Telecom bus mode, the control signals are PL, TPL, V5 and TAIS.

In DS0 switch mode, the data entering the MSU is stored in two alternating pages of memory. Each page contains one complete frame (9720 bytes) of data. One of these alternating pages is currently filling while the other is currently full. Data exiting the MSU is extracted from the currently full page. As a consequence, the MSU imposes a nominal switching latency of 1 frame (125us). The selection of bytes to fill each output port requires a switching connection memory. Control is required for each of the 9720 bytes in the output SBI336 frame. Complete specification of an output byte requires 14 bits to specify which of the 9720 input bytes to use. Dual copies of this control memory are required to provide hitless frame boundary switchover.

In column switch mode, the same switching principle described above is used, but less memory is required. Data entering the MSU is stored in two alternating pages of memory. Each page contains one row (1080 bytes) of data. In this mode, the nominal latency is 1 row if a frame (<15 us). The switching connection memory for the output port requires control for each of the 1080 columns in the frame. Complete specification of an output column requires 11 bits to specify which of the 1080 input columns to use. Dual copies of this control memory are required to provide hitless frame boundary switchover.

Each MSU can be independently bypassed for reduced latency or debugging purposes.

10.4.1 Data Buffer

The Data Buffer block contains a double buffer structure for each frame consisting of a data byte, 4-bits of Channel Associated Signaling information and 4 bits of control information necessary for identifying valid data and timing.

10.4.2 Connection Memory

The Connection Memory sub-block contains two pages of mapping configuration, page 0 and page 1. One page is designated the active page and the other the stand-by page. Selection between which page is to be active and which is to be stand-by is controlled by the ICMP signal (for the IMSU) and OCMP signal (for the OMSU). The Connection Memory sub-block samples the value on the ICMP signal at the C1 byte position as defined by the incoming frame pulse signal, IC1FP. The Connection Memory sub-block samples the value on the OCMP signal at the C1 byte position as defined by the receive serial interface frame pulse signal, RC1FP. Swaps between the active/standby status of the two pages are synchronized to the first A1 byte of the next frame or multi-frame. This arrangement allows all devices in a cross-connect system to be updated in a coordinated fashion. Consequently, DS0 streams or tributaries not being assigned new positions are unaffected by page swaps.

The CMP input signals can be overridden by register configuration or by the SBI336S in-band link channel.

10.5 CAS Merging

The Channel Associated Signaling Merge blocks, ICASM and OCASM, insert the CAS signaling information into the SBI bus on a tributary basis. CAS signaling channels within the SBI bus are constructed out of the available CAS bits for T1 and E1 SBI tributaries that are enabled for CAS signaling. The resulting CAS signaling channel replaces the octets of the SBI bus where the new CAS signaling is to be inserted. This function is enabled on a per-tributary basis and can be used for T1 and E1 tributaries simultaneously across different SBI SPEs. This block adds one T1 multi-frame (24 frames) or one E1 multi-frame (16 frames) of latency to the CAS bits.

10.6 Incoming SBI336 Tributary Translator

The Incoming SBI336 Tributary Translator block, ISTT, translates all SBI336 timing and Channel Associated Signaling information for all tributaries into SBI336S format. The output from this block is a 77.76MHz SBI336 stream with all tributaries and control signals encoded into an internal format that closely resembles the serial SBI336S format.

This block translates all tributary types into a form that is easy for the 8B/10B encoder to handle in a more generic form. A control RAM keeps the current configuration for each of the incoming SBI bus tributaries so that it can perform the translation function.

Common to all tributaries is identification of the first C1 byte. There are unique mappings of the 8B/10B codes for the supported SBI and SBI336 bus link types: Asynchronous T1/E1, Synchronous (locked) T1/E1, Transparent VT1.5/VT2, DS3/E3 and Fractional rate links. Much of the identification and mapping of a link into serial SBI format is based on the C1 frame pulse and a tributaries location relative to that C1 pulse. In addition to the C1FP identification this block identifies multi-frame alignment, valid payload, pointer movements for floating tributaries and timing control for encoding into the 8B/10B serial SBI format.

This block is transparent in Telecom bus mode.

10.7 PRBS Processors

The Working and Protection PRBS Processor blocks, WPP and PPP, provides in-service and off-line PRBS generation and detection for diagnostics of the equipment downstream of the two LVDS links. Each PRBS Processor has the capacity to source and monitor PRBS data for the associated Working or Protection Serial SBI336S stream with a granularity of unchannelized SBI SPEs of telecom bus STS/AUs.

10.7.1 PRBS Generator

The PRBS generator sub-block optionally overwrites the data originating from the incoming data streams, IDATA[4:1][7:0]. When enabled, the PRBS generator sub-block inserts synchronous payload envelope, SPE bytes into the serial transmit links. The inserted data is derived from an internal linear feedback shift register (LFSR) with a polynomial of $X^{23} + X^{18} + 1$.

10.7.2 PRBS Detector

The PRBS detector sub-block monitors the synchronous payload envelope, SPE, bytes in the incoming data stream. The incoming data is compared against the expected value derived from an internal linear feedback shift register (LFSR) with a polynomial of $X^{23} + X^{18} + 1$. If the incoming data fails to match the expected value for three consecutive bytes, the PRBS detector sub-block will enter out-of-synchronization (OOS) state. The LFSR will be re-initialized using the incoming data bytes. The new LFSR seed is confirmed by comparison with subsequent incoming data bytes. The PRBS detector sub-block will exit the OOS state when the incoming data matches the LFSR output for three consecutive bytes. The PRBS detector sub-block will remain in the OOS state and re-load the LFSR if confirmation failed. The PRBS sub-block counts PRBS byte errors and optionally generates interrupts when it enters and exits the OOS state.

10.8 Transmit 8B/10B Encoders

The Transmit 8B/10B Encoder blocks, TW8E and TP8E, construct an 8B/10B character stream from an incoming translated SBI336 bus or Telecom bus carrying an STS-12/STM-4 equivalent stream.

In SBI mode, these blocks encode the SBI336S stream as shown in Table 21. When configured for Synchronous mode for DS0 switching, the 8B/10B encoder transmits CAS signaling multi-frame alignment across the SBI336S interface by generating a C1FP character every 48 frame times. When not configured for DS0 switching the C1FP character is sent every 4 frames.

10.8.1 SBI336S 8B/10B Character Encoding

Table 21 shows the mapping of SBI336S bus control bytes and signals into 8B/10B control characters. The linkrate octet in location V4, V1 and V2, the in-band programming channel, the V3 octet when it contains data are all carried as data. Justification requests for master timing are carried in the V5 character so there are three V5 characters used, nominal, negative timing adjustment request, and positive timing adjustment request.

Table 21 SBI336S Character Encoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Common to All Link Types			
K28.5	001111 1010	110000 0101	IC1FP='b1 C1FP frame and multi-frame alignment
K23.7-	111010 1000	-	Overhead Bytes (columns 1-60 or 1-72 except for C1 and in-band programming channel), V3 or H3 byte except during negative justification, byte after V3 or H3 byte during positive justification, unused bytes in fraction rate links
Asynchronous T1/E1 Links			
K27.7-	110110 1000	-	V5 byte, no justification request
K28.7-	001111 1000	-	V5 byte, negative justification request

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
K29.7-	101110 1000	-	V5 byte, positive justification request
Synchronous T1/E1 Links			
K27.7-	110110 1000	-	V5 byte
Asynchronous DS3/E3 Links			
K27.7-	110110 1000	-	V5 byte, no justification request
K28.7-	001111 1000	-	V5 byte, negative justification request*
K29.7-	101110 1000	-	V5 byte, positive justification request*
Fractional Rate Links			
K28.7-	001111 1000	-	V5 byte, send one extra byte request**
K29.7-	101110 1000	-	V5 byte, send one less byte request**
Floating Transparent Virtual Tributaries			
K27.7-	110110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = ‘b00, IDATA[5] = REI = ‘b0
K27.7+	-	001001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = ‘b00, IDATA[5] = REI = ‘b1
K28.7-	001111 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = ‘b01, IDATA[5] = REI = ‘b0
K28.7+	-	110000 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = ‘b01, IDATA[5] = REI = ‘b1
K29.7-	101110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = ‘b10, IDATA[5] = REI = ‘b0
K29.7+	-	010001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = ‘b10, IDATA[5] = REI = ‘b1
K30.7-	011110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = ‘b11, IDATA[5] = REI = ‘b0
K30.7+	-	100001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = ‘b11, IDATA[5] = REI = ‘b1

* Note there can be multiple V5s per SBI frame when in DS3 or E3 mode but only one justification can occur per SBI frame. Positive and negative justification request through V5 required by the SBI336S interface should be limited to one per frame.

** Note fractional rate links are symmetric in the transmit and receive direction over SBI336S. When using clock slave mode with a fractional rate link the clock master makes single byte adjustments to the slave's rate once per frame.

10.8.2 Serial Telecom Bus 8B/10B Character Encoding

Table 22 shows the mapping of Telecom bus control bytes and signals into 8B/10B control characters. When the Telecom bus control signals conflict each other, the 8B/10B control characters are generated according to the sequence of the table, with the characters at the top of the table taking precedence over those lower in the table.

Table 22 Serial Telecom Bus Character Encoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 1010	110000 0101	IC1FP='b1 IPL='b0 C1FP frame and multi-frame alignment
High Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	IPL='b0 High-order path H3 byte position, no negative justification event.
K28.0+	-	110000 1011	IPL='b0 High-order path PSO byte position, positive justification event.
K28.6	001111 0110	110000 1001	IC1FP='b1, IPL='b1 High-order path frame alignment (J1).
Low Order Path Termination (LPT) Mode			
K28.4+	-	110000 1101	ITAIS='b1 Low-order path AIS.
K27.7-	110110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K27.7+	-	001001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K28.7-	001111 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K28.7+	-	110000 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5]

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
			= REI = ‘b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K29.7-	101110 1000	-	IV5=’b1, IDATA[0,4] = ERDI[1:0] = ‘b10, IDATA[5] = REI = ‘b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K29.7+	-	010001 0111	IV5=’b1, IDATA[0,4] = ERDI[1:0] = ‘b10, IDATA[5] = REI = ‘b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K30.7-	011110 1000	-	IV5=’b1, IDATA[0,4] = ERDI[1:0] = ‘b11, IDATA[5] = REI = ‘b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K30.7+	-	100001 0111	IV5=’b1, IDATA[0,4] = ERDI[1:0] = ‘b11, IDATA[5] = REI = ‘b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K23.7-	111010 1000	000101 0111	ITPL=’b0 Non low-order path payload bytes.

10.9 Transmit Serializer

The Transmit Serializer blocks, TWPS and TPPS, convert 8B/10B characters to bit-serial format. The Transmit Working Serializer, TWPS, generates a serial stream for the working transmit LVDS link, TPWRK/TNWRK. The Transmit Protect Serializer, TPPS, generates a serial stream for the protect transmit LVDS link, TPPROT/TNPROT.

10.10 LVDS Transmitters

The LVDS Transmitters, TWLV and TPLV, convert 8B/10B encoded digital bit-serial streams to LVDS signaling levels. The Transmit Working LVDS Interface, TWLV, drives the working transmit LVDS links, TPWRK/TNWRK. The Transmit Protect LVDS Interface block, TPLV, drives the protect transmit LVDS link, TPPROT/TNPROT.

10.11 Clock Synthesis Unit

The Clock Synthesis Unit, CSU, block generates the 777.6 MHz clock for the transmit and receive LVDS links. To ensure proper operation of the CSU, it must be reset for a minimum of 1ms. This can be accomplished by either holding RSTB low for 1ms or by setting the ARESET bit in register 000H for 1ms.

10.12 Transmit Reference Generator

The Transmit Voltage Reference Generator block generates bias voltages and currents for the LVDS Transmitters.

10.13 LVDS Receivers

The LVDS Receivers, RWLV and RPLV, convert LVDS signaling levels to 8B/10B encoded digital bit-serial. The Receive Working LVDS Interface block, RWLV, connects to the working receive LVDS links, RPWRK/RNWRK. The Receive Protect LVDS Interface block, RPLV, connects to the protect receive LVDS link RPPROT/RNPROT.

10.14 Data Recovery Units

The Data Recovery Units, WDRU and PDRU, monitor the receive LVDS link for transitions to determine the extent of bit cycles on the link. It then adjusts its internal timing to sample the link in the middle of the data "eye". WDRU retrieves data from the working receive LVDS link, RPWRK/RNWRK. PDRU processes the protect receive LVDS link, RPPROT/RNPROT.

The DRU block also converts the serial stream into 10-bit words. The words are constructed from ten consecutive received bits without regard to 8B/10B character boundaries.

10.15 Receive 8B/10B Decoders

The Receive 8B/10B serial SBI336S Bus decoders, RW8D and RP8D, frame to the receive stream to find 8B/10B character boundaries. It also contains a FIFO to bridge between the timing domain of the receive LVDS links and the system clock timing domain. The RW8D block performs framing and elastic store functions on data retrieved from the working receive LVDS link, RPWRK/RNWRK. The RP8D block processes data on the protect receive LVDS link, RPPROT/RNPROT.

10.15.1 FIFO Buffer

The FIFO buffer sub-block provides isolation between the timing domain of the associated receive LVDS link and that of the system clock, SYSCLK. The FIFO also provides a retiming function to allow individual links in a multi-SBS system to have varying interconnect delay. This eases timing distribution and synchronization in large systems. Data with arbitrary alignment to 8B/10B characters are written into a 10-bit by 24-word deep FIFO at the link clock rate. Data is read from the FIFO at every SYSCLK cycle.

10.15.2 Serial SBI336S and Telecom Bus Alignment

The alignment functionality preformed by each receiver can be broken down into two parts, character alignment and frame alignment. Character alignment finds the 8B/10B character boundary in the arbitrarily aligned incoming data. Frame alignment finds SBI336S or Telecom bus frame and multi-frame boundaries within the Serial link.

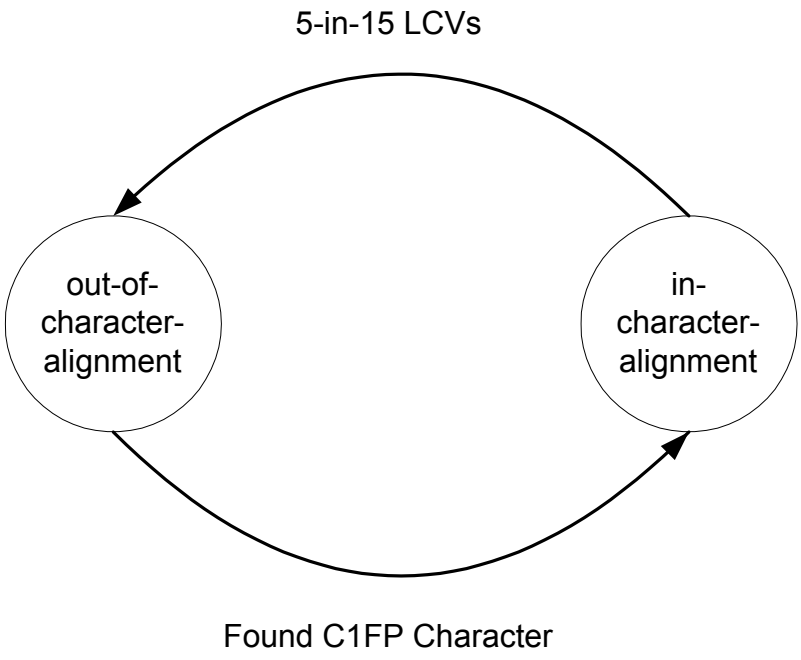
The character and frame alignment are expected to be robust enough for operation over a cabled interconnect.

10.15.3 Character Alignment Block

Character alignment locates character boundaries in the incoming 8B/10B data stream. The character alignment algorithm may be in one of two states, in-character-alignment state and out-of-character-alignment state. The two states of the character alignment algorithm is shown in Figure 7.

When the character alignment state machine is in the out-of-character-alignment state, it maintains the current alignment, while searching for a C1FP character. If it finds the C1FP character it will re-align to the C1FP character and move to the in-character-alignment state. The C1FP character is found by searching for the 8B/10B C1FP character, K28.5+ or K28.5-, simultaneously in ten possible bit locations. While in the in-character-alignment state, the state machine monitors LCVs. If 5 or more LCVs are detected within a 15 character window the character alignment state machine transitions to out-of-character-alignment state. The special characters listed in Table 21 and Table 22 are ignored for LCV purposes. Upon return to in-character-alignment state the LCV count is cleared.

Figure 7 Character Alignment State Machine



10.15.4 Frame Alignment

Frame alignment locates SBI or Telecom bus frame and multi-frame boundaries in the incoming 8B/10B data stream. The frame alignment state machine may be in one of two states, in-frame-alignment state and out-of-frame-alignment state. Each SBI336S frame is 125uS in duration.

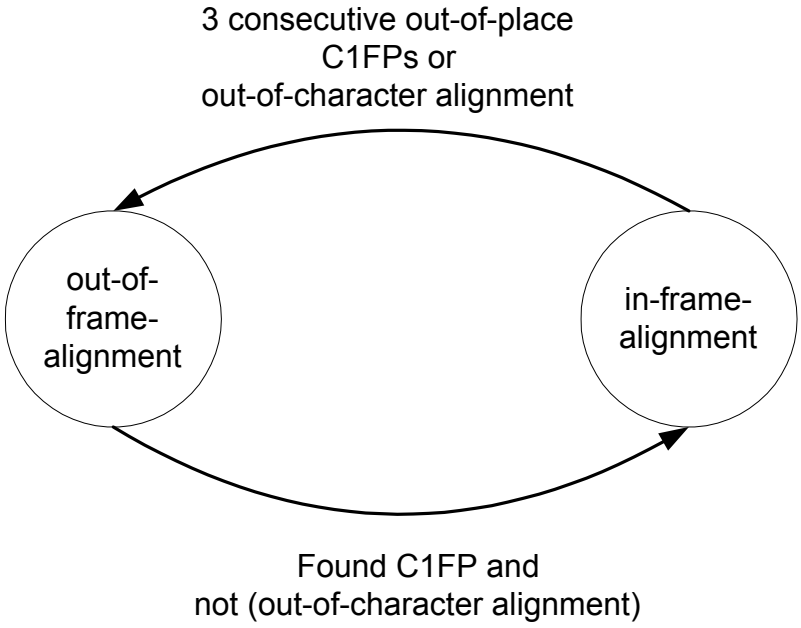
In SBI mode: Encoded over the SBI336S frame alignment is SBI336S multi-frame alignment which is every four SBI336S frames or 500uS. When carrying DS0 traffic in synchronous mode, signaling multi-frame alignment is also necessary and is also encoded over SBI336S alignment. Signaling multi-frame alignment is every 24 frames for T1 links and every 16 frames for E1 links, therefore signaling multi-frame alignment covering both T1 and E1 multi-frame alignment is every 48 SBI336S frames or 6ms. Therefore C1FP characters are sent every four or every 48 frames.

In Telecom Bus mode: Encoded over the serial link is the tributary multi-frame alignment which is every 4 frames or 500uS. Multi-frame alignment is required so that a downstream device can extract the T1 or E1 data from the tributary. The multi-frame information is preserved by only sending out C1FP characters every four frames.

The frame alignment state machine establishes frame alignment over the link and is based on the frame and not the multi-frame alignments. When the frame alignment state machine is in the out-of-frame-alignment state, it maintains the current alignment, while searching for a C1FP character. When it finds the C1FP character the state machine transitions to the in-frame-alignment state. While in the in-frame-alignment state the state machine monitors out-of-place C1FP characters. Out-of-place C1FP characters are identified by maintaining a frame counter based on the C1FP character. The counter is initialized by the C1FP character when in the out-of-character-alignment state, and is unaffected in the in-character-alignment state. If 3 consecutive C1FPs have been found that do not agree with the expected location as defined by the frame counter, the state will change to out-of-frame-alignment state.

The frame alignment state machine is also sensitive to character alignment. When the character alignment state machine is in the out-of-character-alignment state, the frame alignment state machine is forced out-of-alignment, and is held in that state until the character alignment state machine transitions to the in-character alignment state.

Figure 8 Frame Alignment State Machine



10.15.5 SBI336S Multi-frame Alignment

SBI336S multi-frame alignment is communicated across the link by controlling the frequency of the C1FP character. The most frequent transmission of the C1FP character is every four SBI336S frame times. This is the SBI336S multi-frame and is used when there are no synchronous tributaries requiring signaling multi-frame alignment on the SBI336S bus. When there are synchronous tributaries on the SBI336S bus the C1FP character is transmitted every 48 frame times. This is the CAS signaling multi-frame and is the lowest common multiple of the 24 frame T1 multi-frame and the 16 frame E1 multi-frame.

The SBI336S multi-frame and signaling multi-frame alignment is based a free running multi-frame counter that is reset with each C1FP character received. Under normal operating conditions each received C1FP character will coincide with the free running multi-frame counter. SBI336S multi-frame alignment is always required, SBI336S signaling multi-frame alignment is optional and only required when synchronous tributaries are supported with DS0 level switching.

10.16 Outgoing SBI336S Tributary Translator

The Outgoing SBI Tributary Translator block, OSTT, processes all timing information and Channel Associated Signaling information for the tributaries on the outgoing SBI Bus or buses. Input to this block is a 77MHz SBI stream with all tributaries encoded in an internal format that closely resembles the serial SBI format.

This block is transparent in Telecom bus mode.

10.16.1 Outgoing SBI336S Translation

This block translates the generic internal SBI format to the external SBI format. A control RAM keeps the current configuration of the outgoing SBI bus(es) and the tributaries carried so that it can perform the translation function.

Common to all tributaries is identification of the first C1 byte. There are unique mappings of the 8B/10B codes for the supported SBI bus link types: Asynchronous T1/E1, Synchronous (locked) T1/E1, Transparent VT1.5/VT2, DS3/E3 and Fractional rate links. Much of the identification and mapping of a link from serial SBI format is based on the OC1FP frame pulse and a tributaries location relative to that C1 reference. In addition to the OC1FP identification this block identifies multi-frame alignment, valid payload, pointer movements for floating tributaries and timing control for decoding from the 8B/10B serial SBI format.

10.17 Outgoing SBI336 Timing Adapter

The Outgoing SBI336 Timing Adapter, OSTA, provides a demultiplexing from a 77.76MHz SBI336 or Telecom bus to four outgoing 19.44MHz SBI or Telecom buses. The outgoing timing adapter block also provides a transparent mode when the outgoing interface is already in 77.76MHz SBI336 or Telecom bus format.

When the SBS is connected to a 19.44MHz SBI link layer device the justification request signal, JUST_REQ, is an output from the SBS and is aligned to the incoming bus. This block re-aligns the internal justification request signal from the internal outgoing SBI336 frame alignment to the incoming SBI frame alignment, marked by IC1FP. When the SBS is connected to a 19.44Mhz SBI physical layer device or any 77.76MHz SBI336 device, no re-alignment of the justification request is required by this block.

10.18 In-band Link Controller

In order to permit centralized control of distributed NSE/SBS fabrics from the NSE microprocessor interface (for applications in which NSEs are located on fabric cards, and SBSs are located on multiple line cards), an in-band signaling channel is provided between the NSE and the SBS over the Serial interface. Each NSE can control up to 32 SBSs which are attached by the LVDS links. The NSE-SBS in-band channel is full duplex, but the NSE has active control of the link.

The SBS contains two independent In-Band Link Controllers. One ILC is connected to the Working Transmit Serial LVDS Link and the other is connected to the Protection Transmit Serial LVDS Link.

The in-band channel is carried in the first 36 columns of four rows of the SBI or Telecom bus structure, rows 3, 6, 7 and 8. The overall in-band channel capacity is thus 36*4*64kb/s = 9.216Mb/s. Each 36 bytes per row allocated to the in-band signaling channel is its own in-band message between the end points. Four bytes of each 36 byte in-band message are reserved for end-to-end control information and error protection, leaving 8.192Mb/s available for user data transfer between the end points.

The data transferred between the end points has no fixed format, effectively providing a clear channel for packet transfer between the attached microprocessors at each of the LVDS link terminating devices. Using the microprocessor interface, the user is able to send and receive any packet up to 32 bytes in length. The first two bytes of each 36-byte message contains a header and the last two bytes of the message is a CRC-16 which detects errors in the message.

This in-band channel is expected to be used almost entirely to carry out switching control changes in the SBSs. To configure a DS0 in an SBS device most often requires a local microprocessor to write to one memory location consisting of a 16-bit address and a 16-bit data. Using this as a baseline and assuming an efficient use of the in-band channel bandwidth we can set a maximum of (32bytes/row * 4 rows/frame * 8000 frames/sec / 4 bytes/write) 256,000 DS0 configurations per second.

Considering that configuring a T1 when switching DS0s requires 27 DS0 writes indicates that the in-band signaling channel bandwidth sets maximum limit of over 9000 T1 configurations per second. In real life these limits will not be achieved but this shows that the in-band link should not be the bottleneck. In telecom bus mode this same configuration will require only 3 writes per T1 link.

In N+1 protected architectures it is likely that full configuration of a port card will be necessary during the switchover. This would require the entire connection memory be reconfigured. Assuming connections for overhead bytes are also reconfigured, the fastest that a complete reconfiguration can take place is 9720 register writes which equates to (9720 writes * 4 bytes/write / (32 bytes/row * 4 rows/frame * 8000 frames/second)) 38 milliseconds. It is also possible that the spare card could hold all the connection configurations for all the port cards it is protecting locally, for even faster switch over.

10.18.1 In-Band Signaling Channel Fixed Overhead

The In-Band Link Controller block generates and terminates two bytes of fixed header and a CRC-16 per every 36-byte in-band message. The two-byte header provides control and status between devices at the ends of the LVDS link. The CRC-16 is calculated over the entire 34-byte in-band message and provides the terminating end the ability to detect errors in the in-band message. The format of the in-band message and header bytes is shown in Figure 9 and Figure 10.

Figure 9 In-Band Signaling Channel Message Format

1 byte	1 byte	32 bytes	2 bytes
Header1	Header2	Free Format Information	CRC-16

Figure 10 In-Band Signaling Channel Header Format

Header1							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0
Valid	Link[1:0]		Page[1:0]		User[2:0]		

Header2							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0

Aux[7:0]

Table 23 In-band Message Header Fields

Field Name	Received by SBS	Transmitted by SBS
Valid	Message slot contains a valid message(1) or is empty(0). If empty this message will not be put into Rx Message FIFO (other header information processed as usual)	Message slot contains a valid message(1) or is empty(0). The header and CRC bytes are transmitted regardless of the state of this bit.
Link[1:0]#	Each bit indicates which Link to use, working(0) or Protect(1). Other algorithms are possible in indicate Working or Protect over these 2 bits.	Each bit shows current Link in use, working(0) or Protect(1). Other algorithms are possible in indicate Working or Protect over these 2 bits. These bits are transmitted immediately.
Page[1:0]#	Each bit indicates which configuration page to use, page (1) or page (0) for the corresponding MSU. Page[1] controls the IMSU configuration page and Page[0] controls the OMSU configuration page.	Each bit shows current control page in use, page (1) or page (0) for the corresponding MSU. Page[1] indicates the IMSU configuration page and Page[0] indicates the OMSU configuration page Only transmitted from the beginning of the first message of the frame
User[2:0]#	User defined bits which may be read through the microprocessor interface. User[2] is also output from the SBS on the OUSER2 pin.	User defined bits. User[2] is sourced from the IUSER2 input to the SBS. User[1:0] are sourced from an internal register. Transmitted immediately.
Aux[7:0]#	User defined auxiliary register indication.	User defined auxiliary register indication. Transmitted immediately.

#Change in these bits(received side) will not be processed if the received message CRC-16 indicates an error.

Interrupts can be generated when CRC errors are detected or the USER or LINK bits change state. There is no inherent flow control provided by the In-Band Link Controller. The attached microprocessor is able to provide flow control via interrupts when the in-band message FIFO overflows and via the USER bits in the header.

As each message arrives, the CRC-16 and valid bit is checked; if the valid bit is not set the message is discarded, if it fails the CRC check it is flagged as being in error and an interrupt is generated if enabled. If the CRC-16 is OK, regardless of the valid bit, the Page Link, User and Aux bits are passed on immediately. If the FIFO erroneously overflows, an interrupt is generated.

10.19 Microprocessor Interface

The Microprocessor Interface block provides normal and test mode registers, and logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance testability of the SBS.

Address	Register
000H	SBS Master Reset
001H	SBS Master Configuration
002H	SBS Revision/Part Number
003H	SBS Part Number/Manufacturer ID
004H	SBS Master Bypass
005H	SBS Incoming SPE Control #1
006H	SBS Incoming SPE Control #2
007H	SBS Receive Synchronization Delay
008H	SBS In-Band Link User Bits
009H	SBS Receive Configuration
00AH	SBS Transmit Configuration
00BH	SBS Transmit J1 Configuration
00CH	SBS Transmit V1 Configuration
00DH	SBS Transmit H1-H2 Pointer Value
00EH	SBS Transmit Alternate H1-H2 Pointer Value
00FH	SBS Transmit H1-H2 Pointer Selection
010H	SBS Master Interrupt Source
011H	SBS Interrupt Register
012H	SBS Interrupt Enable Register
013H	SBS Loop back Configuration
014H	SBS Master Clock Monitor #1, Accumulation Trigger
015H	SBS Master Clock Monitor #2
016H	SBS Master Interrupt Enable Register
017H	SBS Free User Register
018H	SBS Outgoing SPE Control #1
019H	SBS Outgoing SPE Control #2
01AH	SBS Transmit SPE Control
01BH	SBS Receive SPE Control
01CH – 01FH	Reserved
020H	ISTA Incoming Parity Configuration
021H	ISTA Incoming Parity Status
022H	ISTA Telecom Bus Configuration
023H	ISTA Reserved
024H – 027H	Reserved
028H	IMSU Configuration
029H	IMSU Interrupt Status and Memory Page Update

Address	Register
02AH	IMSU Indirect Time Switch Address
02BH	IMSU Indirect Time Switch Data
02CH – 02FH	Reserved
030H	ICASM CAS Enable Indirect Address
031H	ICASM CAS Enable Indirect Control
032H	ICASM CAS Enable Indirect Data
033H	ICASM Reserved
034H – 037H	Reserved
038H	ISTT Control RAM Indirect Access Address Register
039H	ISTT Control RAM Indirect Access Control Register
03AH	ISTT Control RAM Indirect Access Data Register
03BH	ISTT Reserved
03CH – 03FH	Reserved
040H	OSTT Control RAM Indirect Access Address Register
041H	OSTT Control RAM Indirect Access Control Register
042H	OSTT Control RAM Indirect Access Data Register
043H	OSTT Reserved
044H – 047H	Reserved
048H	OMSU Configuration
049H	OMSU Interrupt Status and Memory Page Update
04AH	OMSU Indirect Time Switch Address
04BH	OMSU Indirect Time Switch Data
04CH – 04FH	Reserved
050H	OCASM Indirect Address
051H	OCASM Indirect Control
052H	OCASM Indirect Data
053H	OCASM Reserved
054H – 05FH	Reserved
060H	OSTA Outgoing Configuration and Parity
061H	OSTA Outgoing J1 Configuration
062H	OSTA Outgoing V1 Configuration
063H	OSTA H1-H2 Pointer Value
064H	OSTA Alternate H1-H2 Pointer Value
065H	OSTA H1-H2 Pointer Selection
066H	OSTA Output Enable Indirect Access Address
067H	OSTA Output Enable Indirect Access Control
068H	OSTA Output Enable Indirect Access Data
069H – 06FH	OSTA Reserved
070H	WPP Indirect Address
071H	WPP Indirect Data

Address	Register
072H	WPP Generator Payload Configuration
073H	WPP Monitor Payload Configuration
074H	WPP Monitor Byte Error Interrupt Status
075H	WPP Monitor Byte Error Interrupt Enable
076H – 078H	WPP Reserved
079H	WPP Monitor Synchronization Interrupt Status
07AH	WPP Monitor Synchronization Interrupt Enable
07BH	WPP Monitor Synchronization State
07CH	WPP Performance Counters Transfer Trigger
07DH – 07FH	WPP Reserved
080H	PPP Indirect Address
081H	PPP Indirect Data
082H	PPP Generator Payload Configuration
083H	PPP Monitor Payload Configuration
084H	PPP Monitor Byte Error Interrupt Status
085H	PPP Monitor Byte Error Interrupt Enable
086H – 088H	PPP Reserved
089H	PPP Monitor Synchronization Interrupt Status
08AH	PPP Monitor Synchronization Interrupt Enable
08BH	PPP Monitor Synchronization State
08CH	PPP Performance Counters Transfer Trigger
08DH – 08FH	PPP Reserved
090H	WILC Transmit Message FIFO Data High
091H	WILC Transmit Message FIFO Data Low
092H	WILC Reserved
093H	WILC Transmit Control
094H	WILC Reserved
095H	WILC Transmit Status and FIFO Synch
096H	WILC Receive Message FIFO Data High
097H	WILC Receive Message FIFO Data Low
098H	WILC Reserved
099H	WILC Receive Control
09AH	WILC Receive Auxiliary
09BH	WILC Receive Status and FIFO Synch
09CH	WILC Reserved
09DH	WILC Interrupt Enable and Control
09EH	WILC Reserved
09FH	WILC Interrupt Reason
0A0H	PILC Transmit Message FIFO Data High
0A1H	PILC Transmit Message FIFO Data Low

Address	Register
0A2H	PILC Reserved
0A3H	PILC Transmit Control
0A4H	PILC Reserved
0A5H	PILC Transmit Status and FIFO Synch
0A6H	PILC Receive Message FIFO Data High
0A7H	PILC Receive Message FIFO Data Low
0A8H	PILC Reserved
0A9H	PILC Receive Control
0AAH	PILC Receive Auxiliary
0ABH	PILC Receive Status and FIFO Synch
0ACH	PILC Reserved
0ADH	PILC Interrupt Enable and Control
0AEH	PILC Reserved
0AFH	PILC Interrupt Reason
0B0H	TW8E Control and Status
0B1H	TW8E Interrupt Status
0B2H	TW8E Time-slot Configuration #1
0B3H	TW8E Time-slot Configuration #2
0B4H	TW8E Test Pattern
0B5H	TW8E Analog Control
0B6H – 0B7H	TW8E Reserved
0B8H	TP8E Control and Status
0B9H	TP8E Interrupt Status
0BAH	TP8E Time-slot Configuration #1
0BBH	TP8E Time-slot Configuration #2
0BCH	TP8E Test Pattern
0BDH	TP8E Analog Control
0BEH – 0BFH	TP8E Reserved
0C0H	RW8D Control and Status
0C1H	RW8D Interrupt Status
0C2H	RW8D Line Code Violation Count
0C3H	RW8D Analog Control #1
0C4H – 0C7H	RW8D Reserved
0C8H	RP8D Control and Status
0C9H	RP8D Interrupt Status
0CAH	RP8D Line Code Violation Count
0CBH	RP8D Analog Control
0CCH – 0CFH	RP8D Reserved
0D0H	CSTR Control
0D1H	CSTR Interrupt Enable and Status

Address	Register
0D2H	CSTR Interrupt Indication
0D3H	CSTR Reserved
0D4H – 0DFH	Reserved
0E0H	REFDLL Configuration
0E1H	REFDLL Reserved
0E2H	REFDLL Reset
0E3H	REFDLL Control Status
0E4H – 0E7H	Reserved
0E8H	SYSDLL Configuration
0E9H	SYSDLL Reserved
0EAH	SYSDLL Reset
0EBH	SYSDLL Control Status
0ECH – 0FFH	Reserved
100H	SBS Master Test
101H – 1FFH	Reserved for Test

For all register accesses, CSB must be set low.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the SBS. Normal mode registers (as opposed to test mode registers) are selected when A[8] is set low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TSB to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect SBS operation unless otherwise noted.

Register 000H: SBS Master Reset

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ARESET	0
Bit 0	R/W	DRESET	0

Reserved

These bits must be set low for proper operation of the SBS.

ARESET

The analogue reset bit (ARESET) allows the analogue circuitry in the SBS to be reset and disabled under software control. When the ARESET bit is set high, all SBS analogue circuitry is held in reset and disabled. This bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset and enable it. Holding SBS in analogue reset state places it into a low power, disabled mode. A hardware reset clears the ARESET bit, thus negating the analogue software reset.

This bit must be set for a minimum of 1ms after a hardware reset to properly reset the CSU. Alternatively, the hardware reset, RSTB, must be held low for a minimum of 1ms.

DRESET

The digital reset bit (DRESET) allows the digital circuitry in the SBS to be reset under software control. When the DRESET bit is set high, all SBS digital circuitry is held in reset with the exception of this register. This bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. Holding SBS in digital reset state places it into a low power, digital stand-by mode. A hardware reset clears the DRESET bit, thus negating the digital software reset.

Register 001H: SBS Master Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14	R/W	ICMP_SRC[1]	0
Bit 13	R/W	ICMP_SRC[0]	0
Bit 12	R/W	ICMP_VAL	0
Bit 11		Unused	0
Bit 10	R/W	OCMP_SRC[1]	0
Bit 9	R/W	OCMP_SRC[0]	0
Bit 8	R/W	OCMP_VAL	0
Bit 7	R/W	RWSEL_SRC	0
Bit 6	R/W	RWSEL_VAL	1
Bit 5	R/W	PARALLEL_MODE	0
Bit 4	R/W	COLUMN_MODE	0
Bit 3	R/W	PHY_SBI	1
Bit 2	R/W	MF_48	0
Bit 1	R/W	TELECOM_BUS	0
Bit 0	R/W	19M_BUSB	0

ICMP_SRC[1:0]

The ICMP_SRC[1:0] bits select the source for the incoming connection memory page information.

ICMP_SRC[1:0]	Source
00	ICMP_VAL register bit
01	ICMP input pin
10	PAGE bit from the active ILC (as determined by the RWSEL_VAL bit or RWSEL input)
11	Reserved

ICMP_VAL

The ICMP_VAL bit controls the selection of the connection memory page in each Incoming Memory Switch Unit, IMSU. When ICMP_VAL is a logic 1, connection memory page 1 is selected. When ICMP_VAL is a logic 0, connection memory page 0 is selected. ICMP_VAL is sampled at the C1 byte position as defined by the incoming frame pulse signal (IC1FP). Changes to the connection memory page selection are synchronized to the frame boundary of the next frame (in Telecom bus mode), 4 frame multi-frame (in SBI mode without CAS), or 48 frame multi-frame (in SBI mode with CAS). This bit is only used when ICMP_SRC[1:0] = ‘b00.

OCMP_SRC[1:0]

The OCMP_SRC[1:0] bits select the source for the outgoing connection memory page information.

OCMP_SRC[1:0]	Source
00	OCMP_VAL register bit
01	OCMP input pin
10	PAGE bit from the active ILC (as determined by the RWSEL_VAL bit or RWSEL input)
11	Reserved

OCMP_VAL

The OCMP_VAL bit controls the selection of the connection memory page in each Outgoing Memory Switch Unit, OMSU. When OCMP_VAL is a logic 1, connection memory page 1 is selected. When OCMP_VAL is a logic 0, connection memory page 0 is selected. OCMP_VAL is sampled at the C1 byte position as defined by the receive frame pulse signal (RC1FP). Changes to the connection memory page selection are synchronized to the frame boundary of the next frame (in Telecom bus mode), 4 frame multi-frame (in SBI mode without CAS), or 48 frame multi-frame (in SBI mode with CAS). This bit is only used when OCMP_SRC[1:0] = ‘b00.

RWSEL_SRC

The RWSEL_SRC bit selects the source for the selection of which link, the working or the protect, is active. When RWSEL_SRC is a logic 0, the RWSEL_VAL register bit is used as the source for selecting the active link. When RWSEL_SRC is a logic 1, the RWSEL input is used as the source for selecting the active link.

RWSEL_VAL

The RWSEL_VAL bit selects between the receive working and protect links when the RWSEL_SRC is a logic 0. When RWSEL_VAL is a logic 1, the working link is selected and the SBS listens to the data from the RPWRK and RNWRK inputs. When RWSEL_VAL is a logic 0, the protect link is selected and the SBS listens to the data from the RPPROT and RNPROT inputs. This bit has no effect when the RWSEL_SRC bit is a logic 1 or when the parallel interface is used (PARALLEL_MODE = ‘b1).

PARALLEL_MODE

The PARALLEL_MODE bit selects between the parallel bus or the serial LVDS links on the transmit and receive interfaces. When PARALLEL_MODE is set to a logic 1, parallel mode is enabled. When PARALLEL_MODE is set to a logic 0, the serial LVDS mode is enabled.

COLUMN_MODE

The COLUMN_MODE bit selects between column switching and DS0 switching. When COLUMN_MODE is set to a logic 1, column switching is enabled and the SBS is configured to switch columns within the SBI336 or Telecom bus. When COLUMN_MODE is set to a logic 0, DS0 switching is enabled and the SBS is configured to switch DS0's within the SBI336 bus. DS0 switching is not permitted in Telecom Bus mode.

PHY_SBI

The PHY_SBI bit configures the direction of the JUST_REQ[4:1] input/output signals on the incoming and outgoing buses. When PHY_SBI is set to a logic 1, the SBS is configured to be connected to a PHY device and the JUST_REQ[4:1] signal is an input. When PHY_SBI is set to a logic 0, the SBS is configured to be connected to a Link layer device and the JUST_REQ[4:1] signal is an output.

MF_48

The MF_48 bit selects between 4 frame multi-frame mode or 48 frame multi-frame mode on the SBI336 bus. When MF_48 is a logic 1, 48 frame mode is selected. IC1FP is expected once every 48 frames and OC1FP is output every 48 frames, indicating CAS signaling multi-frame alignment. When MF_48 is a logic 0, 4 frame mode is selected. IC1FP is expected once every 4 frames and OC1FP is output every 4 frames. This bit has no effect when in Telecom bus mode (TELECOM_BUS = 'b1) or when in column switching mode (COLUMN_MODE = 'b1).

TELECOM_BUS

The TELECOM_BUS bit selects between Telecom bus and SBI bus modes on the incoming and outgoing buses. When TELECOM_BUS is set to a logic 1, Telecom bus mode is selected and all frame pulses must mark C1J1V1 positions. When TELECOM_BUS is set to a logic 0, SBI bus mode is selected and the all frame pulses only mark the C1 position.

19M_BUSB

The 19M_BUSB bit selects between 19MHz and 77MHz mode on the incoming and outgoing buses. When 19M_BUSB is set to a logic 0, 19MHz mode is selected and 4 separate 19MHz buses are used. When 19M_BUSB is set to a logic 1, 77MHz mode is selected and a single 77MHz bus is used.

Note: Whenever this bit is changed from a logic 0 to a logic 1, the REFDLL must be reset by writing to register 0E2H.

Register 002H: SBS Version/Part Number

Bit	Type	Function	Default
Bit 15	R	VERSION[3]	0
Bit 14	R	VERSION[2]	0
Bit 13	R	VERSION[1]	0
Bit 12	R	VERSION[0]	1
Bit 11	R	PART_NUMBER[15]	1
Bit 10	R	PART_NUMBER[14]	0
Bit 9	R	PART_NUMBER[13]	0
Bit 8	R	PART_NUMBER[12]	0
Bit 7	R	PART_NUMBER[11]	0
Bit 6	R	PART_NUMBER[10]	1
Bit 5	R	PART_NUMBER[9]	1
Bit 4	R	PART_NUMBER[8]	0
Bit 3	R	PART_NUMBER[7]	0
Bit 2	R	PART_NUMBER[6]	0
Bit 1	R	PART_NUMBER[5]	0
Bit 0	R	PART_NUMBER[4]	1

VERSION[3:0]

The VERSION[3:0] bits report the binary revision number of the SBS silicon. VERSION[3:0] = ‘b0001 for revision B of the SBS.

PART_NUMBER[15:4]

The PART NUMBER[15:4] bits represent the 12 most significant bits of the part number of the SBS device.

Register 003H: SBS Part Number/Manufacturer ID

Bit	Type	Function	Default
Bit 15	R	PART_NUMBER[3]	0
Bit 14	R	PART_NUMBER[2]	0
Bit 13	R	PART_NUMBER[1]	0
Bit 12	R	PART_NUMBER[0]	0
Bit 11	R	MANUFACTURER_ID[10]	0
Bit 10	R	MANUFACTURER_ID[9]	0
Bit 9	R	MANUFACTURER_ID[8]	0
Bit 8	R	MANUFACTURER_ID[7]	0
Bit 7	R	MANUFACTURER_ID[6]	1
Bit 6	R	MANUFACTURER_ID[5]	1
Bit 5	R	MANUFACTURER_ID[4]	0
Bit 4	R	MANUFACTURER_ID[3]	0
Bit 3	R	MANUFACTURER_ID[2]	1
Bit 2	R	MANUFACTURER_ID[1]	1
Bit 1	R	MANUFACTURER_ID[0]	0
Bit 0	R	JID	1

PART_NUMBER[3:0]

The PART NUMBER[3:0] bits represent the 4 least significant bits of the part number of the SBS device.

MANUFACTURER_ID[10:0]

The MANUFACTURER ID[10:0] bits represent the 11 bit manufacturer's code assigned to PMC-Sierra, Inc. for inclusion in the JTAG Boundary Scan Identification Code. For more information on JTAG Boundary Scan, refer to Section 12.

JID

The JID bit is bit 0 in the JTAG identification code.

Register 004H: SBS Master Bypass Register

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5	R/W	IMSU_BYPASS	0
Bit 4	R/W	ICASE_BYPASS	0
Bit 3	R/W	ICASM_BYPASS	0
Bit 2	R/W	OMSU_BYPASS	0
Bit 1	R/W	OCASE_BYPASS	0
Bit 0	R/W	OCASM_BYPASS	0

IMSU_BYPASS

The IMSU_BYPASS bit is used to bypass the functionality of the IMSU block. When IMSU_BYPASS is a logic 1, the incoming memory switch is bypassed and the incoming data bus is passed to the transmit data bus unmodified. This eliminates the one frame delay through the IMSU and places the IMSU in a low power mode. When IMSU_BYPASS is a logic 0, the IMSU is not bypassed and must be configured.

ICASE_BYPASS

The ICASE_BYPASS bit is used to bypass the functionality of the ICASE block. When ICASE_BYPASS is a logic 1, the incoming CAS extractor is bypassed and the CAS bits are not extracted from the SBI336 bus. This places the ICASE block in a low power mode. When ICASE_BYPASS is a logic 0, the ICASE is not bypassed and the CAS bits are extracted from the SBI336 bus.

ICASM_BYPASS

The ICASM_BYPASS bit is used to bypass the functionality of the ICASM block. When ICASM_BYPASS is a logic 1, the incoming CAS merge block is bypassed and the CAS bits are not inserted into the SBI336 bus. This places the ICASM block in a low power mode. When ICASM_BYPASS is a logic 0, the ICASM is not bypassed and the CAS bits are inserted into the SBI336 bus.

OMSU_BYPASS

The OMSU_BYPASS bit is used to bypass the functionality of the OMSU block. When OMUS_BYPASS is a logic 1, the outgoing memory switch is bypassed and the receive data bus is passed to the outgoing data bus unmodified. This eliminates the one frame delay through the OMSU and places the OMSU in a low power mode. When OMSU_BYPASS is a logic 0, the OMSU is not bypassed and must be configured.

OCASE_BYPASS

The OCASE_BYPASS bit is used to bypass the functionality of the OCASE block. When OCASE_BYPASS is a logic 1, the transmit CAS extractor is bypassed and the CAS bits are not extracted from the SBI336 bus. This places the OCASE block in a low power mode. When OCASE_BYPASS is a logic 0, the OCASE is not bypassed and the CAS bits are extracted from the SBI336 bus.

OCASM_BYPASS

The OCASM_BYPASS bit is used to bypass the functionality of the OCASM block. When OCASM_BYPASS is a logic 1, the transmit CAS merge block is bypassed and the CAS bits are not inserted into the SBI336 bus. This places the OCASM block in a low power mode. When OCASM_BYPASS is a logic 0, the OCASM is not bypassed and the CAS bits are inserted into the SBI336 bus.

Register 005H: SBS Incoming SPE Control #1

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7	R/W	ISBI4_SPE3_TYP[1] / ISTS1_TYP[12]	0
Bit 6	R/W	ISBI4_SPE3_TYP[0]	0
Bit 5	R/W	ISBI3_SPE3_TYP[1] / ISTS1_TYP[11]	0
Bit 4	R/W	ISBI3_SPE3_TYP[0]	0
Bit 3	R/W	ISBI2_SPE3_TYP[1] / ISTS1_TYP[10]	0
Bit 2	R/W	ISBI2_SPE3_TYP[0]	0
Bit 1	R/W	ISBI1_SPE3_TYP[1] / ISTS1_TYP[9]	0
Bit 0	R/W	ISBI1_SPE3_TYP[0]	0

Register 006H: SBS Incoming SPE Control #2

Bit	Type	Function	Default
Bit 15	R/W	ISBI4_SPE2_TYP[1] / ISTS1_TYP[8]	0
Bit 14	R/W	ISBI4_SPE2_TYP[0]	0
Bit 13	R/W	ISBI3_SPE2_TYP[1] / ISTS1_TYP[7]	0
Bit 12	R/W	ISBI3_SPE2_TYP[0]	0
Bit 11	R/W	ISBI2_SPE2_TYP[1] / ISTS1_TYP[6]	0
Bit 10	R/W	ISBI2_SPE2_TYP[0]	0
Bit 9	R/W	ISBI1_SPE2_TYP[1] / ISTS1_TYP[5]	0
Bit 8	R/W	ISBI1_SPE2_TYP[0]	0
Bit 7	R/W	ISBI4_SPE1_TYP[1] / ISTS1_TYP[4]	0
Bit 6	R/W	ISBI4_SPE1_TYP[0]	0
Bit 5	R/W	ISBI3_SPE1_TYP[1] / ISTS1_TYP[3]	0
Bit 4	R/W	ISBI3_SPE1_TYP[0]	0
Bit 3	R/W	ISBI2_SPE1_TYP[1] / ISTS1_TYP[2]	0
Bit 2	R/W	ISBI2_SPE1_TYP[0]	0
Bit 1	R/W	ISBI1_SPE1_TYP[1] / ISTS1_TYP[1]	0
Bit 0	R/W	ISBI1_SPE1_TYP[0]	0

ISBIx_SPEy_TYP[1:0] (SBI mode only)

In SBI mode (TELECOM_BUS = ‘b0), the ISBIx_SPEy_TYP[1:0] bits select the SPE type for the specified SPE within the specified Incoming SBI bus. The types for each SPE are independently configured with possible types being T1, E1, DS3/E3 and fractional rate links. In Telecom bus mode (TELECOM_BUS = ‘b1), the ISBIxSPEy_TYP[0] bits are unused.

The setting for ISBIx_SPEy_TYP[1:0] are:

ISBIx_SPEy_TYP[1:0]	Payload Type
00	T1
01	E1
10	DS3/E3
11	Fractional Rate

ISTS1_TYP[12:1] (Telecom bus mode only)

In Telecom bus mode (TELECOM_BUS = ‘b1), the ISTS1_TYP[12:1] bits select between floating and fixed STS/AUs on the Incoming bus. When ISTS1_TYP[x] is a logic 1, the associated STS/AU is floating and may have high order pointer movements. When ISTS1_TYP[x] is a logic 0, the associated STS/AU is fixed and cannot have high order pointer movements.

Register 007H: SBS Receive Synchronization Delay

Bit	Type	Function	Default
Bit 15	R	TIP	0
Bit 14		Unused	0
Bit 13	R/W	RC1FPDLY[13]	0
Bit 12	R/W	RC1FPDLY[12]	0
Bit 11	R/W	RC1FPDLY[11]	0
Bit 10	R/W	RC1FPDLY[10]	0
Bit 9	R/W	RC1FPDLY[9]	0
Bit 8	R/W	RC1FPDLY[8]	0
Bit 7	R/W	RC1FPDLY[7]	0
Bit 6	R/W	RC1FPDLY[6]	0
Bit 5	R/W	RC1FPDLY[5]	0
Bit 4	R/W	RC1FPDLY[4]	0
Bit 3	R/W	RC1FPDLY[3]	0
Bit 2	R/W	RC1FPDLY[2]	0
Bit 1	R/W	RC1FPDLY[1]	0
Bit 0	R/W	RC1FPDLY[0]	0

TIP

The transfer in progress bit (TIP) reports the status of latching performance monitor counting into holding registers. TIP is set high when a transfer is initiated by a write access to the SBS Master Signal Monitor #1, Accumulation Trigger Register (014H). It is set low when all the counters in the SBS have transferred their values to holding registers. The updated counts are now available for reading at the designated registers. These registers are the WPP Monitor Error Count (Register 071H with IADDR = 4H), the PPP Monitor Error Count (Register 081H with IADDR = 4H), the RW8D LCV Count (Register 0C2H), and the RP8D LCV Count (Register 0CAH).

RC1FPDLY[13:0]

The receive transport frame delay bits (RC1FPDLY[13:0]) controls the delay, in SYSCLK cycles, inserted by the SBS before processing the C1 characters delivered by the receive serial data links. RC1FPDLY should be set such that after the specified delay the active receive link should have delivered the C1 character. The relationships between RC1FP, RC1FPDLY and the receive serial links is described in the Functional Timing section.

Register 008H: SBS In-Band Link User Bits

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3	R/W	TXWUSER[1]	0
Bit 2	R/W	TXWUSER[0]	0
Bit 1	R/W	TXPUSER[1]	0
Bit 0	R/W	TXPUSER[0]	0

TXWUSER[1:0]

The Transmit Working USER bits (TXWUSER[1:0]) contain the values to be inserted in the USER[1:0] bits in the header of the working in-band signaling channel.

TXPUSER[1:0]

The Transmit Protection USER bits (TXWUSER[1:0]) contain the values to be inserted in the USER[1:0] bits in the header of the protection in-band signaling channel.

Register 009H: SBS Receive Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8	R/W	RLOCK0	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2	R/W	INCLRC1	0
Bit 1	R/W	INCLRPL	0
Bit 0	R/W	ROP	0

RLOCK0

The RLOCK0 bit controls the expected position of the J1 byte in the Incoming TelecomBus for locked STS/AUs. The selection of locked or floating STS/AUs is controlled by the RSTS1_TYP[x] bits in register 01BH. When RLOCK0 is a logic 1, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When RLOCK0 is a logic 0, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to sample RC1FP in order to find the byte following J1 which will indicate multi-frame alignment. This bit only has an effect when in Telecom Bus mode (TELECOM_BUS = ‘b1 in the SBS Master Configuration Register).

INCLRPL

The INCLRPL bit controls whether the RPL input signal participates in the receive parity calculations. When INCLRPL is set to a logic 1, the parity calculation includes the RPL input. When INCLRPL is set to a logic 0, parity is calculated without regard to the state of RPL. This bit only takes effect when in Telecom bus mode.

INCLRC1

The INCLRC1 bit controls whether the RC1FP input signal participates in the receive parity calculations. When INCLRC1 is set to a logic 1, the parity calculation includes the RC1FP input. When INCLRC1 is set to a logic 0, parity is calculated without regard to the state of RC1FP. This bit only takes effect when in Telecom bus mode.

ROP

The receive odd parity bit (ROP) controls the expected parity on the receive bus. When ROP is set to a logic 1, the expected parity on the RDP input is odd. When ROP is set to a logic 0, the parity is even. In SBI bus mode, the parity calculation encompasses the RDATA[7:0], RPL and RV5 signals. In Telecom bus mode, the parity calculation encompasses the RDATA[7:0] and optionally RPL and RC1FP as determined by the INCLRPL and INCLRC1 bits.

Register 00AH: SBS Transmit Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8	R/W	TLOCK0	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2	R/W	INCLTC1	0
Bit 1	R/W	INCLTPL	0
Bit 0	R/W	TOP	0

TLOCK0

The TLOCK0 bit controls the position of the J1 byte in the Transmit Telecom Bus. When TLOCK0 is a logic 1, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When TLOCK0 is a logic 0, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to pulse the TC1FP output when any part of STS1_TJ1EN[12:1] or STS1_TV1EN[12:1] are set. This bit only has an effect when in Telecom Bus mode (TELECOM_BUS = ‘b1 in the SBS Master Configuration Register).

INCLTC1

The INCLTC1 bit controls whether the TC1FP output signal participates in the transmit parity calculations. When INCLTC1 is set to a logic 1, the parity calculation includes the TC1FP output. When INCLTC1 is set to a logic 0, parity is calculated without regard to the state of TC1FP. This bit only take effect when in Telecom bus mode.

INCLTPL

The INCLTPL bit controls whether the TPL output signal participates in the transmit parity calculations. When INCLTPL is set to a logic 1, the parity calculation includes the TPL output. When INCLTPL is set to a logic 0, parity is calculated without regard to the state of TPL. This bit only takes effect when in Telecom bus mode.

TOP

The transmit odd parity bit (TOP) controls the parity generated on the transmit bus. When TOP is set to a logic 1, the parity on the TDP output is odd. When TOP is set to a logic 0, the parity is even. In SBI bus mode, the parity calculation encompasses the TDATA[7:0], TPL and TV5 signals. In Telecom bus mode, the parity calculation encompasses the TDATA[7:0] and optionally TPL and TC1FP as determined by the INCLTPL and INCLTC1 bits.

Register 00BH: SBS Transmit J1 Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_TJ1EN[12]	0
Bit 10	R/W	STS1_TJ1EN[11]	0
Bit 9	R/W	STS1_TJ1EN[10]	0
Bit 8	R/W	STS1_TJ1EN[9]	0
Bit 7	R/W	STS1_TJ1EN[8]	0
Bit 6	R/W	STS1_TJ1EN[7]	0
Bit 5	R/W	STS1_TJ1EN[6]	0
Bit 4	R/W	STS1_TJ1EN[5]	0
Bit 3	R/W	STS1_TJ1EN[4]	0
Bit 2	R/W	STS1_TJ1EN[3]	0
Bit 1	R/W	STS1_TJ1EN[2]	0
Bit 0	R/W	STS1_TJ1EN[1]	0

STS1_TJ1EN[12:1]

The STS1_TJ1EN[12:1] bit may be used to control the inclusion of the J1 byte identification on the TC1FP output for each of the 12 STS/AUs. When STS1_TJ1EN[x] is a logic 1, the TC1FP output will pulse high during the J1 byte position of the associated STS/AU along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the TLOCK0 bit. When STS1_TJ1EN[x] is a logic 0, the TC1FP will not pulse high during the J1 byte position of the associated STS/AU. This bit only has an effect when in Telecom Bus mode (TELECOM_BUS = ‘b1 in the SBS Master Configuration Register). These register bits should not be set if the IC1FP[4:1] inputs contain J1 indications.

Register 00CH: SBS Transmit V1 Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_TV1EN[12]	0
Bit 10	R/W	STS1_TV1EN[11]	0
Bit 9	R/W	STS1_TV1EN[10]	0
Bit 8	R/W	STS1_TV1EN[9]	0
Bit 7	R/W	STS1_TV1EN[8]	0
Bit 6	R/W	STS1_TV1EN[7]	0
Bit 5	R/W	STS1_TV1EN[6]	0
Bit 4	R/W	STS1_TV1EN[5]	0
Bit 3	R/W	STS1_TV1EN[4]	0
Bit 2	R/W	STS1_TV1EN[3]	0
Bit 1	R/W	STS1_TV1EN[2]	0
Bit 0	R/W	STS1_TV1EN[1]	0

STS1_TV1EN[12:1]

The STS1_TV1EN[12:1] bit controls the inclusion of the byte following J1 identification on the TC1FP output for each of the 12 STS/AUs. When STS1_TV1EN[x] is a logic 1, the TC1FP output will pulse high during the byte following the J1 position of the associated STS/AU along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the TLOCK0 bit. When STS1_TV1EN is a logic 0, the TC1FP will not pulse high during the byte following the J1 position of the associated STS/AU. This bit only has an effect when in Telecom Bus mode (TELECOM_BUS = ‘b1 in the SBS Master Configuration Register). These bits should only be set when the associated STS/AU does not contain any high order pointer movements and the J1 bytes are in a fixed position relative to the C1 byte.

Register 00DH: SBS Transmit H1-H2 Pointer Value

Bit	Type	Function	Default
Bit 15	R/W	H1[7]	0
Bit 14	R/W	H1[6]	0
Bit 13	R/W	H1[5]	0
Bit 12	R/W	H1[4]	0
Bit 11	R/W	H1[3]	0
Bit 10	R/W	H1[2]	0
Bit 9	R/W	H1[1]	0
Bit 8	R/W	H1[0]	0
Bit 7	R/W	H2[7]	0
Bit 6	R/W	H2[6]	0
Bit 5	R/W	H2[5]	0
Bit 4	R/W	H2[4]	0
Bit 3	R/W	H2[3]	0
Bit 2	R/W	H2[2]	0
Bit 1	R/W	H2[1]	0
Bit 0	R/W	H2[0]	0

H1[7:0]

The H1[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Transmit Telecom bus when the STS1_PTR_SEL[x] bit is a logic 0 and the H1H2EN bit is set high. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

H2[7:0]

The H2[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Transmit Telecom bus when the STS1_PTR_SEL[x] bit is a logic 0 and the H1H2EN bit is set high. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

Register 00EH: SBS Transmit Alternate H1-H2 Pointer Value

Bit	Type	Function	Default
Bit 15	R/W	H1_ALT[7]	0
Bit 14	R/W	H1_ALT[6]	0
Bit 13	R/W	H1_ALT[5]	0
Bit 12	R/W	H1_ ALT[4]	0
Bit 11	R/W	H1_ ALT[3]	0
Bit 10	R/W	H1_ ALT[2]	0
Bit 9	R/W	H1_ ALT[1]	0
Bit 8	R/W	H1_ ALT[0]	0
Bit 7	R/W	H2_ ALT[7]	0
Bit 6	R/W	H2_ ALT[6]	0
Bit 5	R/W	H2_ ALT[5]	0
Bit 4	R/W	H2_ ALT[4]	0
Bit 3	R/W	H2_ ALT[3]	0
Bit 2	R/W	H2_ ALT[2]	0
Bit 1	R/W	H2_ ALT[1]	0
Bit 0	R/W	H2_ ALT[0]	0

H1_ALT[7:0]

The H1_ALT[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Transmit Telecom bus when the STS1_PTR_SEL[x] bit is a logic 1 and the H1H2EN bit is set high. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

H2_ALT[7:0]

The H2_ALT[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Transmit Telecom bus when the STS1_PTR_SEL[x] bit is a logic 1 and the H1H2EN bit is set high. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

Register 00FH: SBS Transmit H1-H2 Pointer Selection

Bit	Type	Function	Default
Bit 15	R/W	H1H2EN	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_PTR_SEL[12]	0
Bit 10	R/W	STS1_PTR_SEL[11]	0
Bit 9	R/W	STS1_PTR_SEL[10]	0
Bit 8	R/W	STS1_PTR_SEL[9]	0
Bit 7	R/W	STS1_PTR_SEL[8]	0
Bit 6	R/W	STS1_PTR_SEL[7]	0
Bit 5	R/W	STS1_PTR_SEL[6]	0
Bit 4	R/W	STS1_PTR_SEL[5]	0
Bit 3	R/W	STS1_PTR_SEL[4]	0
Bit 2	R/W	STS1_PTR_SEL[3]	0
Bit 1	R/W	STS1_PTR_SEL[2]	0
Bit 0	R/W	STS1_PTR_SEL[1]	0

H1H2EN

The H1H2EN bit enables the insertion of the H1 and H2 bytes in the transport overhead. When H1H2EN is a logic 1, the values in the internal registers is inserted into the H1 and H2 bytes of the Transmit Telecom bus according to the STS1_PTR_SEL[12:1] bits. When H1H2EN is a logic 0, the values from the internal registers is not inserted into the H1 and H2 bytes. This bit has no effect when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register). This bit should not be set if any of the STS/AUs are floating.

STS1_PTR_SEL[12:1]

The STS1_PTR_SEL[12:1] bits select which of the two H1-H2 Pointer registers is used for each of the 12 STS/AUs output on the Transmit Telecom bus when the H1H2EN bit is set. When STS1_PTR_SEL[x] is a logic 0, the SBS Transmit H1-H2 Pointer Value register is used for the associated STS/AU on the Transmit bus. When STS1_PTR_SEL[x] is a logic 1, the SBS Transmit Alternate H1-H2 Pointer Value register is used for the associated STS/AU on the Transmit bus. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

Register 010H: SBS Master Interrupt Source

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14	R	SBS_INT	X
Bit 13	R	IMSU_INT	X
Bit 12	R	OMSU_INT	X
Bit 11	R	REFDLL_INT	X
Bit 10	R	SYSDLL_INT	X
Bit 9	R	CSTR_INT	X
Bit 8	R	TW8E_INT	X
Bit 7	R	TP8E_INT	X
Bit 6	R	RW8D_INT	X
Bit 5	R	RP8D_INT	X
Bit 4	R	WPP_INT	X
Bit 3	R	PPP_INT	X
Bit 2	R	WILC_INT	X
Bit 1	R	PILC_INT	X
Bit 0	R	ISTA_INT	X

SBS_INT

If the SBS_INT bit is a logic 1, an interrupt has been generated by the top level circuitry. The SBS Interrupt register must be read to clear this interrupt.

IMSU_INT

If the IMSU_INT bit is a logic 1, an interrupt has been generated by the IMSU block. The IMSU Interrupt register must be read to clear this interrupt.

OMSU_INT

If the OMSU_INT bit is a logic 1, an interrupt has been generated by the OMSU block. The OMSU Interrupt register must be read to clear this interrupt.

REFDLL_INT

If the REFDLL_INT bit is a logic 1, an interrupt has been generated by the REFDLL block. The REFDLL Interrupt register must be read to clear this interrupt.

SYSDLL_INT

If the SYSDLL_INT bit is a logic 1, an interrupt has been generated by the SYSDLL block. The SYSDLL Interrupt register must be read to clear this interrupt.

CSTR_INT

If the CSTR_INT bit is a logic 1, an interrupt has been generated by the CSTR block. The CSTR Interrupt register must be read to clear this interrupt.

TW8E_INT

If the TW8E_INT bit is a logic 1, an interrupt has been generated by the TW8E block. The TW8E Interrupt register must be read to clear this interrupt.

TPPP_INT

If the TP8E_INT bit is a logic 1, an interrupt has been generated by the TP8E block. The TP8E Interrupt register must be read to clear this interrupt.

RW8D_INT

If the RW8D_INT bit is a logic 1, an interrupt has been generated by the RW8D block. The RW8D Interrupt register must be read to clear this interrupt.

RP8D_INT

If the RP8D_INT bit is a logic 1, an interrupt has been generated by the RP8D block. The RP8D Interrupt register must be read to clear this interrupt.

WPP_INT

If the WPP_INT bit is a logic 1, an interrupt has been generated by the WPP block. The WPP Interrupt register must be read to clear this interrupt.

PPP_INT

If the PPP_INT bit is a logic 1, an interrupt has been generated by the PPP block. The PPP Interrupt register must be read to clear this interrupt.

WILC_INT

If the WILC_INT bit is a logic 1, an interrupt has been generated by the WILC block. The WILC Interrupt register must be read to clear this interrupt.

PILC_INT

If the PILC_INT bit is a logic 1, an interrupt has been generated by the PILC block. The PILC Interrupt register must be read to clear this interrupt.

ISTA_INT

If the ISTA_INT bit is a logic 1, an interrupt has been generated by the ISTA block. The ISTA Interrupt register must be read to clear this interrupt.

Register 011H: SBS Interrupt Register

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12	R	WRC1_EXP_INT	X
Bit 11	R	WRC1_EXTRA_INT	X
Bit 10	R	WRC1_MISS_INT	X
Bit 9	R	PRC1_EXP_INT	X
Bit 8	R	PRC1_EXTRA_INT	X
Bit 7	R	PRC1_MISS_INT	X
Bit 6	R	ICMP_INT	X
Bit 5	R	OCMP_INT	X
Bit 4	R	OCOL_INT[4]	X
Bit 3	R	OCOL_INT[3]	X
Bit 2	R	OCOL_INT[2]	X
Bit 1	R	OCOL_INT[1]	X
Bit 0	R	RP_INT	X

WRC1_EXP_INT

The WRC1_EXP_INT bit is set to a logic 1 when a C1 character is received on the receive working serial link in its expected position with respect to the RC1FP input. This interrupt is enabled with the WRC1_EXPE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

WRC1_EXTRA_INT

The WRC1_EXTRA_INT bit is set to a logic 1 when a C1 character is received on the receive working serial link in an unexpected position with respect to the RC1FP input. This interrupt is enabled with the WRC1_EXTRAE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

WRC1_MISS_INT

The WRC1_MISS_INT bit is set to a logic 1 when a C1 character is not received on the receive working serial link in its expected position with respect to the RC1FP input. This interrupt is enabled with the WRC1_MISSE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

PRC1_EXP_INT

The PRC1_EXP_INT bit is set to a logic 1 when a C1 character is received on the receive protection serial link in its expected position with respect to the RC1FP input. This interrupt is enabled with the PRC1_EXPE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

PRC1_EXTRA_INT

The PRC1_EXTRA_INT bit is set to a logic 1 when a C1 character is received on the receive protection serial link in an unexpected position with respect to the RC1FP input. This interrupt is enabled with the PRC1_EXTRAE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

PRC1_MISS_INT

The PRC1_MISS_INT bit is set to a logic 1 when a C1 character is not received on the receive protection serial link in its expected position with respect to the RC1FP input. This interrupt is enabled with the PRC1_MISSE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

ICMP_INT

The ICMP_INT bit is set to a logic 1 when the ICMP input is sampled by the SBS. In Telecom bus mode, ICMP is sampled during the first C1 position of every frame, as marked by IC1FP. In SBI mode, ICMP is sampled during the first C1 position of every 4 or 48 frame multi-frame, as marked by IC1FP. This interrupt may be helpful in scheduling configuration page changes in the IMSU. This interrupt is enabled with the ICMPE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

OCMP_INT

The OCMP_INT bit is set to a logic 1 when the OCMP input is sampled by the SBS. In Telecom bus mode, OCMP is sampled during the first C1 position of every frame, as marked by RC1FP. In SBI mode, OCMP is sampled during the first C1 position of every 4 or 48 frame multi-frame, as marked by RC1FP. This interrupt may be helpful in scheduling configuration page changes in the OMSU. This interrupt is enabled with the OCMPE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

OCOL_INT[4:1]

If the OCOL_INT[x] bit is a logic 1, an interrupt has been generated from a collision on the associated outgoing bus. A collision is detected when ODETECT[x] is sampled high during the same clock cycle that the OACTIVE[x] is set high. These interrupts are enabled with the OCOLE[4:1] bits in the SBS Interrupt Enable register. These interrupt bits will be cleared when read.

RP_INT

If the RP_INT is a logic 1, an interrupt has been generated from a parity error on the associated receive bus. This in an indication that there may be hardware or configuration problem on the receive bus. This interrupt is enabled with the RPE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

Register 012H: SBS Interrupt Enable Register

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12	R/W	WRC1_EXPE	0
Bit 11	R/W	WRC1_EXTRAE	0
Bit 10	R/W	WRC1_MISSE	0
Bit 9	R/W	PRC1_EXPE	0
Bit 8	R/W	PRC1_EXTRAE	0
Bit 7	R/W	PRC1_MISSE	0
Bit 6	R/W	ICMPE	0
Bit 5	R/W	OCMPE	0
Bit 4	R/W	OCOLE[4]	0
Bit 3	R/W	OCOLE[3]	0
Bit 2	R/W	OCOLE[2]	0
Bit 1	R/W	OCOLE[1]	0
Bit 0	R/W	RPE	0

WRC1_EXPE

The WRC1_EXPE interrupt enable bit is an active high interrupt enable. When WRC1_EXPE is set to a logic 1, an interrupt will be asserted on the INTB output when the WRC1_EXP_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When WRC1_EXPE is set to a logic 0, The WRC1_EXP_INT bit will not cause an interrupt.

WRC1_EXTRAE

The WRC1_EXTRAE interrupt enable bit is an active high interrupt enable. When WRC1_EXTRAE is set to a logic 1, an interrupt will be asserted on the INTB output when the WRC1_EXTRA_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When WRC1_EXTRAE is set to a logic 0, The WRC1_EXTRA_INT bit will not cause an interrupt.

WRC1_MISSE

The WRC1_MISSE interrupt enable bit is an active high interrupt enable. When WRC1_MISSE is set to a logic 1, an interrupt will be asserted on the INTB output when the WRC1_MISS_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When WRC1_MISSE is set to a logic 0, The WRC1_MISS_INT bit will not cause an interrupt.

PRC1_EXPE

The PRC1_EXPE interrupt enable bit is an active high interrupt enable. When PRC1_EXPE is set to a logic 1, an interrupt will be asserted on the INTB output when the PRC1_EXP_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When PRC1_EXPE is set to a logic 0, The PRC1_EXP_INT bit will not cause an interrupt.

PRC1_EXTRAE

The PRC1_EXTRAE interrupt enable bit is an active high interrupt enable. When PRC1_EXTRAE is set to a logic 1, an interrupt will be asserted on the INTB output when the PRC1_EXTRA_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When PRC1_EXTRAE is set to a logic 0, The PRC1_EXTRA_INT bit will not cause an interrupt.

PRC1_MISSE

The PRC1_MISSE interrupt enable bit is an active high interrupt enable. When PRC1_MISSE is set to a logic 1, an interrupt will be asserted on the INTB output when the PRC1_MISS_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When PRC1_MISSE is set to a logic 0, The PRC1_MISS_INT bit will not cause an interrupt.

ICMPE

The ICMPE interrupt enable bit is an active high interrupt enable. When ICMPE is set to a logic 1, an interrupt will be asserted on the INTB output when the ICMP_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When ICMPE is set to a logic 0, The ICMP_INT bit will not cause an interrupt.

OCMPE

The OCMPE interrupt enable bit is an active high interrupt enable. When OCMPE is set to a logic 1, an interrupt will be asserted on the INTB output when the OCMP_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When OCMPE is set to a logic 0, The OCMP_INT bit will not cause an interrupt.

OCOLE[4:1]

The outgoing collision detect interrupt enable bits (OCOLE[4:1] are active high interrupt enables. When OCOLE[x] is set to a logic 1 and the SBSE and INTE bits in register 016H are set high, the occurrence of a collision detection on the associated outgoing bus will cause an interrupt to be asserted on the INTB output. When OCOLE[x] is set to a logic 0, outgoing collision detection will not cause an interrupt.

RPE

The receive parity interrupt enable bit (RPE) is an active high interrupt enable. When RPE is set to a logic 1 and the SBSE and INTE bits in register 016H are set high, the occurrence of a parity error on the receive bus will cause an interrupt to be asserted on the INTB output. When RPE is set to a logic 0, receive parity errors will not cause an interrupt.

Register 013H: SBS Loop back Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2	R/W	O2ILOOP	0
Bit 1	R/W	T82R8LOOP	0
Bit 0	R/W	T2RLOOP	0

O2ILOOP

The O2ILOOP bit enables a diagnostic loop back from the outgoing interface to the incoming interface. When O2ILOOP is a logic 1, the entire SBI336 or Telecom bus is looped back from the output of the OCASM to the input of the ICASE. When O2ILOOP is a logic 0, no loop back is performed.

T82R8LOOP

The T82R8LOOP bit enables a diagnostic loop back from the transmit 8b/10b encoded bus to the receive 8b/10b encoded bus. When T82R8LOOP is a logic 1, the entire SBI336 or Telecom bus is looped back from the output of the TW8E and TP8E to the input of the RW8D and RP8D, respectively. When T82R8LOOP is a logic 0, no loop back is performed.

T2RLOOP

The T2RLOOP bit enables a diagnostic loop back from the transmit interface to the receive interface. When T2RLOOP is a logic 1, the entire SBI336 or Telecom bus is looped back from the output of the ICASM to the input of the OCASE. When T2RLOOP is a logic 0, no loop back is performed.

Register 014H: SBS Master Signal Monitor #1, Accumulation Trigger

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10	R	RTPLA	X
Bit 9	R	RV5A	X
Bit 8	R	RPLA	X
Bit 7	R	RDATAA	X
Bit 6	R	RC1FPA	X
Bit 5	R	SYSCLKA	X
Bit 4	R	SREFCLKA	X
Bit 3	R	IC1FPA[4]	X
Bit 2	R	IC1FPA[3]	X
Bit 1	R	IC1FPA[2]	X
Bit 0	R	IC1FPA[1]	X

This register provides activity monitoring on major SBS inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. Bits that depend on multiple inputs making a low to high transition must have each input make a low to high transition between subsequent reads before the activity bit will be set high. The corresponding register bit reading low indicates a lack of transitions. This register should be read periodically to detect for stuck at conditions.

Writing to this register delimits the accumulation intervals in the various performance monitor accumulation registers. These registers are the WPP Monitor Error Count (Register 071H with IADDR = 4H), the PPP Monitor Error Count (Register 081H with IADDR = 4H), the RW8D LCV Count (Register 0C2H), and the RP8D LCV Count (Register 0CAH). Counts accumulated in those registers are transferred to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent loss of data, accumulation intervals must be 1.0 second or shorter. The bits in this register are not affected by write accesses.

RTPLA

The RTPL active bits (RTPLA) detects low to high transitions on the RTPL input. RTPLA is set high when a rising edge has been observed on the RTPL input, and is set low when this register is read.

RV5A

The RV5 active bits (RV5A) detects low to high transitions on the RV5 input. RV5A is set high when a rising edge has been observed on the RV5 input, and is set low when this register is read.

RPLA

The RPL active bits (RPLA) detects low to high transitions on the RPL input. RPLA is set high when a rising edge has been observed on the RPL input, and is set low when this register is read.

RDATAA

The RDATA active bit (RDATAA) detects low to high transitions on the RDATA input bus. RDATAA is set high when rising edges have been observed on all the signals on the RDATA[7:0] bus, and is set low when this register is read.

RC1FPA

The RC1FP active bit (RC1FPA) detects low to high transitions on the RC1FP input. RC1FPA is set high on a rising edge of RC1FP, and is set low when this register is read.

SYSCLKA

The SYSCLK active bit (SYSCLKA) detects low to high transitions on the SYSCLK input. SYSCLKA is set high on a rising edge of SYSCLK, and is set low when this register is read.

SREFCLKA

The SREFCLK active bit (SREFCLKA) detects low to high transitions on the SREFCLK input. SREFCLKA is set high on a rising edge of SREFCLK, and is set low when this register is read.

IC1FPA[4:1]

The IC1FP[x] active bits (IC1FPA[x]) detects low to high transitions on the corresponding IC1FP[x] input. IC1FPA[x] is set high on a rising edge of IC1FP[x], and is set low when this register is read.

Register 015H: SBS Master Signal Monitor #2

Bit	Type	Function	Default
Bit 15	R	ITPLA[4]	X
Bit 14	R	ITPLA[3]	X
Bit 13	R	ITPLA[2]	X
Bit 12	R	ITPLA[1]	X
Bit 11	R	IV5A[4]	X
Bit 10	R	IV5A[3]	X
Bit 9	R	IV5A[2]	X
Bit 8	R	IV5A[1]	X
Bit 7	R	IPLA[4]	X
Bit 6	R	IPLA[3]	X
Bit 5	R	IPLA[2]	X
Bit 4	R	IPLA[1]	X
Bit 3	R	IDATAA[4]	X
Bit 2	R	IDATAA[3]	X
Bit 1	R	IDATAA[2]	X
Bit 0	R	IDATAA[1]	X

This register provides activity monitoring on major SBS inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. Bits that depend on multiple inputs making a low to high transition must have each input make a low to high transition between subsequent reads before the activity bit will be set high. The corresponding register bit reading low indicates a lack of transitions. This register should be read periodically to detect for stuck at conditions.

ITPLA[4:1]

The ITPL[4:1] active bits (ITPLA[4:1]) detects low to high transitions on the ITPL[4:1] inputs. ITPLA[x] is set high when a rising edge has been observed on the ITPL[x] input, and is set low when this register is read.

IV5A[4:1]

The IV5[4:1] active bits (IV5A[4:1]) detects low to high transitions on the IV5[4:1] inputs. IV5A[x] is set high when a rising edge has been observed on the IV5[x] input, and is set low when this register is read.

IPLA[4:1]

The IPL[4:1] active bits (IPLA[4:1]) detects low to high transitions on the IPL[4:1] inputs. IPLA[x] is set high when a rising edge has been observed on the IPL[x] input, and is set low when this register is read.

IDATAA[4:1]

The IDATA[4:1] active bits (IDATAA[4:1]) detects low to high transitions on the IDATA[4:1] input buses. IDATAA[x] is set high when rising edges have been observed on all the signals on the IDATA[x][7:0] bus, and is set low when this register is read.

Register 016H: SBS Master Interrupt Enable

Bit	Type	Function	Default
Bit 15	R/W	INTE	0
Bit 14	R/W	SBSE	0
Bit 13	R/W	IMSUE	0
Bit 12	R/W	OMSUE	0
Bit 11	R/W	REFDLLE	0
Bit 10	R/W	SYSDLLE	0
Bit 9	R/W	CSTRE	0
Bit 8	R/W	TW8EE	0
Bit 7	R/W	TP8EE	0
Bit 6	R/W	RW8DE	0
Bit 5	R/W	RP8DE	0
Bit 4	R/W	WPPE	0
Bit 3	R/W	PPPE	0
Bit 2	R/W	WILCE	0
Bit 1	R/W	PILCE	0
Bit 0	R/W	ISTAE	0

INTE

The INTE bit is a global interrupt enable bit. When INTE is set to a logic 1, interrupts will be indicated on the INTB output. When INTE is set to a logic 0, the INTB output will be held high impedance.

SBSE

The SBSE interrupt enable bit, when set to a logic 1, enables interrupts from the SBS Interrupt Register (register 011H) to be propagated to the INTB output.

IMSUE

The IMSUE interrupt enable, when set to a logic 1, enables interrupts from the IMSU block to be propagated to the INTB output.

OMSUE

The OMSUE interrupt enable, when set to a logic 1, enables interrupts from the OMSU block to be propagated to the INTB output.

REFDLLE

The REFDLLE interrupt enable, when set to a logic 1, enables interrupts from the REFDLL block to be propagated to the INTB output.

SYSDLLE

The SYSDLLE interrupt enable, when set to a logic 1, enables interrupts from the SYSDLL block to be propagated to the INTB output.

CSTRE

The CSTRE interrupt enable, when set to a logic 1, enables interrupts from the CSTR block to be propagated to the INTB output.

TW8EE

The TW8EE interrupt enable, when set to a logic 1, enables interrupts from the TW8E block to be propagated to the INTB output.

TP8EE

The TP8EE interrupt enable, when set to a logic 1, enables interrupts from the TP8E block to be propagated to the INTB output.

RW8DE

The RW8DE interrupt enable, when set to a logic 1, enables interrupts from the RW8D block to be propagated to the INTB output.

RP8DE

The RP8DE interrupt enable, when set to a logic 1, enables interrupts from the RP8D block to be propagated to the INTB output.

WPPE

The WPPE interrupt enable, when set to a logic 1, enables interrupts from the WPP block to be propagated to the INTB output.

PPPE

The PPPE interrupt enable, when set to a logic 1, enables interrupts from the PPP block to be propagated to the INTB output.

WILCE

The WILCE interrupt enable, when set to a logic 1, enables interrupts from the WILC block to be propagated to the INTB output.

PILCE

The PILCE interrupt enable, when set to a logic 1, enables interrupts from the PILC block to be propagated to the INTB output.

ISTAE

The ISTAE interrupt enable, when set to a logic 1, enables interrupts from the ISTA block to be propagated to the INTB output.

Register 017H: SBS Free User Register

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

FREE[7:0]

The software ID register (FREE) holds whatever value is written into it. Reset clears the contents of this register. This register has no impact on the operation of the SBS.

Register 018H: SBS Outgoing SPE Control #1

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7	R/W	OSBI4_SPE3_TYP[1]	0
Bit 6	R/W	OSBI4_SPE3_TYP[0]	0
Bit 5	R/W	OSBI3_SPE3_TYP[1]	0
Bit 4	R/W	OSBI3_SPE3_TYP[0]	0
Bit 3	R/W	OSBI2_SPE3_TYP[1]	0
Bit 2	R/W	OSBI2_SPE3_TYP[0]	0
Bit 1	R/W	OSBI1_SPE3_TYP[1]	0
Bit 0	R/W	OSBI1_SPE3_TYP[0]	0

Register 019H: SBS Outgoing SPE Control #2

Bit	Type	Function	Default
Bit 15	R/W	OSBI4_SPE2_TYP[1]	0
Bit 14	R/W	OSBI4_SPE2_TYP[0]	0
Bit 13	R/W	OSBI3_SPE2_TYP[1]	0
Bit 12	R/W	OSBI3_SPE2_TYP[0]	0
Bit 11	R/W	OSBI2_SPE2_TYP[1]	0
Bit 10	R/W	OSBI2_SPE2_TYP[0]	0
Bit 9	R/W	OSBI1_SPE2_TYP[1]	0
Bit 8	R/W	OSBI1_SPE2_TYP[0]	0
Bit 7	R/W	OSBI4_SPE1_TYP[1]	0
Bit 6	R/W	OSBI4_SPE1_TYP[0]	0
Bit 5	R/W	OSBI3_SPE1_TYP[1]	0
Bit 4	R/W	OSBI3_SPE1_TYP[0]	0
Bit 3	R/W	OSBI2_SPE1_TYP[1]	0
Bit 2	R/W	OSBI2_SPE1_TYP[0]	0
Bit 1	R/W	OSBI1_SPE1_TYP[1]	0
Bit 0	R/W	OSBI1_SPE1_TYP[0]	0

OSBIx_SPEy_TYP[1:0]

The OSBIx_SPEy_TYP[1:0] bits select the SPE type for the specified SPE within the specified Outgoing SBI bus. The types for each SPE are independently configured with possible types being T1, E1, DS3/E3 and fractional rate links. In Telecom bus mode (TELECOM_BUS = ‘b1), the OSBIxSPEy_TYP[1:0] bits are unused.

The setting for OSBIx_SPEy_TYP[1:0] are:

OSBIx_SPEy_TYP[1:0]	Payload Type
00	T1
01	E1
10	DS3/E3
11	Fractional Rate

Register 01AH: SBS Transmit SPE Control

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	TSBI4_SPE3_TYP	0
Bit 10	R/W	TSBI3_SPE3_TYP	0
Bit 9	R/W	TSBI2_SPE3_TYP	0
Bit 8	R/W	TSBI1_SPE3_TYP	0
Bit 7	R/W	TSBI4_SPE2_TYP	0
Bit 6	R/W	TSBI3_SPE2_TYP	0
Bit 5	R/W	TSBI2_SPE2_TYP	0
Bit 4	R/W	TSBI1_SPE2_TYP	0
Bit 3	R/W	TSBI4_SPE1_TYP	0
Bit 2	R/W	TSBI3_SPE1_TYP	0
Bit 1	R/W	TSBI2_SPE1_TYP	0
Bit 0	R/W	TSBI1_SPE1_TYP	0

TSBIx_SPEy_TYP

The TSBIx_SPEy_TYP bits select the SPE type for the specified SPE within the specified Transmit SBI bus for the purpose of CAS merging by the ICASM block. The types for each SPE are independently configured to be either T1 or E1. When TSBIx_SPEy_TYP is a logic 0, the associated SPE is configured for T1. When TSBIx_SPEy_TYP is a logic 1, the associated SPE is configured for E1. If the SPE contains something other than T1 or E1, the TSBIx_SPEy_TYP bit is unused. In Telecom bus mode (TELECOM_BUS = ‘b1), the TSBIxSPEy_TYP bits are unused.

Register 01BH: SBS Receive SPE Control

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	RSBI4_SPE3_TYP / RSTS1_TYP[12]	0
Bit 10	R/W	RSBI3_SPE3_TYP / RSTS1_TYP[11]	0
Bit 9	R/W	RSBI2_SPE3_TYP / RSTS1_TYP[10]	0
Bit 8	R/W	RSBI1_SPE3_TYP / RSTS1_TYP[9]	0
Bit 7	R/W	RSBI4_SPE2_TYP / RSTS1_TYP[8]	0
Bit 6	R/W	RSBI3_SPE2_TYP / RSTS1_TYP[7]	0
Bit 5	R/W	RSBI2_SPE2_TYP / RSTS1_TYP[6]	0
Bit 4	R/W	RSBI1_SPE2_TYP / RSTS1_TYP[5]	0
Bit 3	R/W	RSBI4_SPE1_TYP / RSTS1_TYP[4]	0
Bit 2	R/W	RSBI3_SPE1_TYP / RSTS1_TYP[3]	0
Bit 1	R/W	RSBI2_SPE1_TYP / RSTS1_TYP[2]	0
Bit 0	R/W	RSBI1_SPE1_TYP / RSTS1_TYP[1]	0

RSBIx_SPEy_TYP (SBI mode only)

In SBI mode (TELECOM_BUS = ‘b0), the RSBIx_SPEy_TYP bits select the SPE type for the specified SPE within the specified Receive SBI bus for the purpose of expanding the CAS by the OCASE block. The types for each SPE are independently configured to be either T1 or E1. When RSBIx_SPEy_TYP is a logic 0, the associated SPE is configured for T1. When RSBIx_SPEy_TYP is a logic 1, the associated SPE is configured for E1. If the SPE contains something other than T1 or E1, the RSBIx_SPEy_TYP bit is unused.

RSTS1_TYP[12:1] (Telecom bus mode only)

In Telecom bus mode (TELECOM_BUS = ‘b1), the RSTS1_TYP[12:1] bits select between floating and fixed STS/AUs on the Receive bus. When RSTS1_TYP[x] is a logic 1, the associated STS/AU is floating and may have high order pointer movements. When RSTS1_TYP[x] is a logic 0, the associated STS/AU is fixed and cannot have high order pointer movements. These bits only have an effect when configured for the parallel transmit and receive interface (PARALLEL_MODE = ‘b1).

Register 020H: ISTA Incoming Parity Configuration

Bit	Type	Function	Default
Bit 15	R/W	IPE[4]	0
Bit 14	R/W	IPE[3]	0
Bit 13	R/W	IPE[2]	0
Bit 12	R/W	IPE[1]	0
Bit 11	R/W	INCLIC1[4]	0
Bit 10	R/W	INCLIC1[3]	0
Bit 9	R/W	INCLIC1[2]	0
Bit 8	R/W	INCLIC1[1]	0
Bit 7	R/W	INCLIPL[4]	0
Bit 6	R/W	INCLIPL[3]	0
Bit 5	R/W	INCLIPL[2]	0
Bit 4	R/W	INCLIPL[1]	0
Bit 3	R/W	IOP[4]	0
Bit 2	R/W	IOP[3]	0
Bit 1	R/W	IOP[2]	0
Bit 0	R/W	IOP[1]	0

IPE[4:1]

The incoming parity interrupt enable bits (IPE[4:1]) are active high interrupt enables. When IPE[x] is set to a logic 1, the occurrence of a parity error on the incoming bus will cause an interrupt to be asserted on the INTB output. When IPE is set to a logic 0, incoming parity errors will not cause and interrupt. IPE[4:2] are only valid when in 19MHz mode.

INCLIPL[4:1]

The INCLIPL bits control whether the IPL[x] input signal participates in the incoming parity calculations. When INCLIPL[x] is set to a logic 1, the parity signal includes the IPL[x] input. When INCLIPL[x] is set to a logic 0, parity is calculated without regard to the state of IPL[x]. These bits only take effect when in Telecom bus mode. INCLIPL[4:2] are only valid when in 19MHz mode.

INCLIC1[4:1]

The INCLIC1 bits control whether the IC1FP input signal participates in the incoming parity calculations. When INCLIC1[x] is set to a logic 1, the parity signal includes the IC1FP input. When INCLIC1[x] is set to a logic 0, parity is calculated without regard to the state of IC1FP. These bits only take effect when in Telecom bus mode. INCLIC1[4:2] are only valid when in 19MHz mode.

IOP[4:1]

The incoming odd parity bits (IOP[4:1]) control the expected parity on the incoming bus. When IOP is set to a logic 1, the expected parity on the IDP[x] input is odd. When IOP is set to a logic 0, the parity is even. In SBI bus mode, the parity calculation encompasses the IDATA[x][7:0], IPL[x] and IV5[x] signals. In Telecom bus mode, the parity calculation encompasses the IDATA[x][7:0] and optionally IPL[x] and IC1FP as determined by the INCLIPL[x] and INCLIC1[x] bits. IOP[4:2] are only valid when in 19MHz mode.

Register 021H: ISTA Incoming Parity Status

Bit	Type	Function	Default
Bit 15	R	IPI[4]	X
Bit 14	R	IPI[3]	X
Bit 13	R	IPI[2]	X
Bit 12	R	IPI[1]	X
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2		Unused	0
Bit 1		Unused	0
Bit 0		Unused	0

IPI[4:1]

The incoming parity error indication bits (IPI[4:1]) are set high when a parity error has occurred on the associated Incoming bus. These bits are cleared when this register is read. IPI[4:2] are only valid when in 19MHz mode.

Register 022H: ISTA Telecom Bus Configuration

Bit	Type	Function	Default
Bit 15	R/W	ILOCK0	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2		Unused	0
Bit 1		Unused	0
Bit 0		Unused	0

ILOCK0

The ILOCK0 bit controls the expected position of the J1 byte in the Incoming TelecomBus for locked STS/AUs. The selection of locked or floating STS/AUs is controlled by the ISTS1_TYP[x] bits in register 005H and 006H. When ILOCK0 is a logic 1, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When ILOCK0 is a logic 0, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to sample the IC1FP[4:1] input in order to find the byte following J1 which will indicate multi-frame alignment. This bit only has an effect when in Telecom Bus mode (TELECOM_BUS = ‘b1 in the SBS Master Configuration Register).

Register 028H: IMSU Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4	R/W	AUTO_UPDATE	0
Bit 3	R/W	SWAP_PENDINGE	0
Bit 2	R/W	UPDATEE	0
Bit 1	R	SWAP_PENDINGV	0
Bit 0	R	UPDATEV	0

AUTO_UPDATE

The AUTO_UPDATE bit selects when an off-line page update is performed. When AUTO_UPDATE is a logic 1, the on-line page is automatically copied into the off-line page whenever there is a change to the connection memory page. When AUTO_UPDATE is a logic 0, the off-line page is not updated when there is a change to the connection memory page. A page update may still be performed by writing to the Interrupt Status and Memory Page Update Register.

SWAP_PENDINGE

A logic 1 on the SWAP_PENDINGE bit enables the generation of an interrupt on a change of state of SWAP_PENDINGV.

UPDATEE

A logic 1 on the UPDATEE bit enables the generation of an interrupt on a change of state from high to low of UPDATEV.

SWAP_PENDINGV

The SWAP_PENDINGV bit contains the current state of the page swap circuitry. This bit is a logic 1 when a switch to the connection memory page (CMP) has been recognized but the page swap has not yet happened. This bit is a logic 0 when there is not a page swap pending.

UPDATEV

The UPDATEV bit contains the current state of the time switch ram off-line page update circuitry. This bit is a logic 1 when the on-line page is being copied to the offline page. This bit is a logic 0 when the on-line page is not being copied.

Register 029H: IMSU Interrupt Status and Memory Page Update Register

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2		Unused	0
Bit 1	R	SWAP_PENDINGI	X
Bit 0	R	UPDATEI	X

Writing to this register initiates an update of the off-line page in the time switch ram. The contents of the on-line page are written to the off-line page. During this update, the time switch ram may not be accessed through the indirect registers.

SWAP_PENDINGI

The page swap pending interrupt status bit, SWAP_PENDINGI, reports and acknowledges a change of state of the SWAP_PENDINGV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the SWAP_PENDINGE bit, the INT output reflects the state of this bit.

UPDATEI

The off-line page update interrupt status bit, UPDATEI, reports and acknowledges a change of state from high to low of the UPDATEV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the UPDATEE bit, the INT output reflects the state of this bit.

Register 02AH: IMSU Indirect Time Switch Address

Bit	Type	Function	Default
Bit 15	R/W	RWB	0
Bit 14		Unused	0
Bit 13	R/W	OUT_BYTE[13]	0
Bit 12	R/W	OUT_BYTE[12]	0
Bit 11	R/W	OUT_BYTE[11]	0
Bit 10	R/W	OUT_BYTE[10]	0
Bit 9	R/W	OUT_BYTE[9]	0
Bit 8	R/W	OUT_BYTE[8]	0
Bit 7	R/W	OUT_BYTE[7]	0
Bit 6	R/W	OUT_BYTE[6]	0
Bit 5	R/W	OUT_BYTE[5]	0
Bit 4	R/W	OUT_BYTE[4]	0
Bit 3	R/W	OUT_BYTE[3]	0
Bit 2	R/W	OUT_BYTE[2]	0
Bit 1	R/W	OUT_BYTE[1]	0
Bit 0	R/W	OUT_BYTE[0]	0

This register provides the address and the read/write control for the time switch configuration ram. Writing to this register triggers a ram access. Note that when an indirect write access is to be performed, the Indirect Time Switch Data register must first be setup before writing to this register. There must be a minimum of 4 SYSCLK cycles between consecutive ram write accesses. For a ram read access, it will take a maximum of 8 SYSCLK cycles for the Indirect Time Switch Data Register to contain valid data.

RWB

The indirect access control bit (RWB) selects between a write or read access to the time switch configuration RAM. Writing a logic zero to RWB triggers and indirect write operation. Data to be written is taken from the Indirect Time Switch Data register. Writing a logic one to RWB triggers an indirect read operation. The read data can be found in the Indirect Time Switch Data Register.

OUT_BYTE[13:0]

The OUT_BYTE[13:0] bits indicate the ram address to be accessed. Each address in the ram corresponds to a location in the output data bus. The contents stored in each ram address points to the byte from the input data bus which is to be output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079). The byte numbers of the output frame are shown in the following table.

Row								
1	0	1	2	3	…	1077	1078	1079
2	1080	1081	1082	1083	…	2157	2158	2159
3								
4								
5								
6								
7								
8								
9	8640	8641	8642	8643	…	9717	9718	9719

Register 02BH: IMSU Indirect Time Switch Data

Bit	Type	Function	Default
Bit 15	R	VALID	0
Bit 14	R/W	T2R_DS0_LOOP	0
Bit 13	R/W	IN_BYTE[13]	0
Bit 12	R/W	IN_BYTE [12]	0
Bit 11	R/W	IN_BYTE [11]	0
Bit 10	R/W	IN_BYTE [10]	0
Bit 9	R/W	IN_BYTE [9]	0
Bit 8	R/W	IN_BYTE [8]	0
Bit 7	R/W	IN_BYTE [7]	0
Bit 6	R/W	IN_BYTE [6]	0
Bit 5	R/W	IN_BYTE [5]	0
Bit 4	R/W	IN_BYTE [4]	0
Bit 3	R/W	IN_BYTE [3]	0
Bit 2	R/W	IN_BYTE [2]	0
Bit 1	R/W	IN_BYTE [1]	0
Bit 0	R/W	IN_BYTE [0]	0

This register contains data read from the time switch RAM after an indirect read operation or data to be inserted into the time switch RAM during an indirect write operation. The value held in the ram indicates which byte of the input data bus is to be switched to the output.

VALID

The VALID bit reports the presence of valid data from an indirect read. VALID is set to logic 1 when indirect read access returns data from the off-line RAM and remains asserted until the next time Indirect Time Switch Data register is read.

T2R_DS0_LOOP

This bit, when set, enables DS0 or Column loop backs between the output of the IMSU and the input of the OMSU. When enabling these loop backs, the offset between IC1FP and RC1FP must be set such that the normal data and the loop back data arrive at the OMSU at the same time.

The following are the RC1FP to IC1FP offsets, in SYSCLK cycles, in various operating modes:

Mode	Offset
77MHz parallel Telecom Column switched	1092
77MHz parallel SBI Column switched	1088
77MHz parallel SBI DS0 switched	9728
19MHz parallel Telecom Column switched	1094*
19MHz parallel SBI Column switched	1090*
19MHz parallel SBI DS0 switched	9730*

* Measured from the SYSCLK cycle corresponding to the sampling REFCLK rising edge

IN_BYTE[13:0]

The IN_BYTE[13:0] bits indicate which byte in the input frame is to be switched to the output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079).

The MSU has the ability of overwrite the outputs when a value outside the range specified above is programmed. When IN_BYTE[13:12] = 'b11, the value output on TPL, TTPL, TV5, TC1FP, TTAIS and TDATA[7:0] is overwritten as shown in the following tables. Note that this overwrite function should only be used when configured for the transmit parallel interface.

In Column Mode (Telecom bus):

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	MODE[2]	MODE[1]	MODE[0]	TTAIS	TDATA[7:0]

Where

MODE[2:0]		**Setting of Outputs**				
		TPL	**TTPL**	**TC1FP (marking the J1 byte)**	**TV5**	**Special Setting**
000	Transport Overhead (TOH)	0	0	0	0	
001	J1 column	1	0	1 for 1st row, 0 for rows 2-9	0	TDATA is set to 111111CC at the H4 byte. CC indicates the frame number in the multi-frame.
010	Path level stuff columns	1	0	0	0	

MODE[2:0]		Setting of Outputs				
		TPL	TTPL	TC1FP (marking the J1 byte)	TV5	Special Setting
011	Tributary Vx columns (V1, V2, V3, V4)	1	0 for 1st row, 1 for rows 2-9	0	0	
100	Tributary data columns	1	1	0	0	
101	Tributary data columns with V5	1	1	0	1 for 1st row in multi-frame, 0 otherwise	
110 – 111	Reserved					

In Column Mode or DS0 mode (SBI bus):

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	TPL	Reserved	Reserved	Reserved	TDATA[7:0]

Note that the Reserved bits should be set to a logic 0.

Register 030H: ICASM CAS Enable Indirect Access Address Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 CAS enable register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.

Sequential SPE	SBI	SPE
1	1	1
2	2	1
3	3	1
4	4	1
5	1	2
6	2	2
7	3	2
8	4	2
9	1	3
10	2	3
11	3	3
12	4	3

Register 031H: ICASM CAS Enable Indirect Access Control Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the CAS Enable register. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the CAS Enable Indirect Access Data register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the CAS Enable Indirect Access Data register.

HST_ADDR_ERR

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the CAS Enable Indirect Access Control register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the CAS Enable Indirect Access Data register or to determine when a new indirect write operation may commence.

Register 032H: ICASM CAS Enable Indirect Access Data Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R	Unused	0
Bit 0	R/W	CAS_EN	0

CAS_EN

The CAS_EN bit is used to enable the insertion of CAS into the proper location in the associated tributary. When CAS_EN is a logic 1 and the associated tributary is a T1, the CAS bits and PP bits are inserted into the PPSSSSFR byte. When CAS_EN is a logic 1 and the associated tributary is an E1, the CAS bits are inserted into TS#16 and proper data is placed in the PP byte. When CAS_EN is a logic 0, both the CAS and PP bits are not inserted. This bit should only be set if operating in 48-frame mode.

When CAS insertion is enabled, the latency of the CAS bits through the SBS is two multi-frames. For T1 tributaries, this is 48 frames or 6ms. For E1 tributaries, this is 32 frames or 4 ms.

Register 038H: ISTT Tributary Translator Control RAM Indirect Access Address Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 tributary translator control register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b’00001’ through b‘11100’. Legal values for SPE[1:0] are b’01’ through b‘11’. Legal values for SBI[2:0] are b’o01’ through b‘100’.

Sequential SPE	SBI	SPE
1	1	1
2	2	1
3	3	1
4	4	1
5	1	2
6	2	2
7	3	2
8	4	2
9	1	3
10	2	3
11	3	3
12	4	3

Register 039H: ISTT Tributary Translator Control RAM Indirect Access Control Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary translator control RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Tributary Translator Control RAM Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Tributary Translator Control RAM Indirect Access Data.

HST_ADDR_ERR

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Tributary Translator Control RAM Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Translator Control RAM Indirect Access Data register or to determine when a new indirect write operation may commence.

Register 03AH: ISTT Tributary Translator Control RAM Indirect Access Data Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	TVT	0
Bit 0	R/W	JUST_REQ_EN	0

JUST_REQ_EN

The JUST_REQ_EN bit is used to enable T1, E1, DS3, E3 and Fractional rate justification request state machines to convert JUST_REQ to V5, V5+ and V5- characters to be carried over the serial SBI336S link. When this bit is set to 1 the justification request state machines will convert JUST_REQ signals to V5 characters. When this bit is set to 0 the state machines will not generate additional V5 characters for the specified link and will only pass existing V5 characters through as nominal rate V5 characters. This bit should be set to 1 when this device is being used in SBI mode and is connected to physical layer device which is clock master of the transmit tributary.

This bit should not be set if the TVT bit is set. This bit has no effect in Telecom bus mode.

This bit should not be set when configured for the transmit parallel interface (PARALLEL_MODE = ‘b1 in the SBS Master Configuration Register).

TVT

The TVT bit configures a T1 or E1 tributary as a transparent virtual tributary. When TVT is set to 1 the T1 or E1 tributary is configured as a TVT and the ERDI and REI bits in the V5 byte are transmitted across the serial link in one of the V5 characters. When TVT is set to 0 the T1 or E1 tributary is configured as a standard T1 or E1 link.

This bit should not be set if the JUST_REQ_EN bit is set. This bit has no effect in Telecom bus mode or if the SPE is configured to something other that T1 or E1 data.

This bit should not be set when configured for the transmit parallel interface (PARALLEL_MODE = ‘b1 in the SBS Master Configuration Register).

Register 040H: OSTT Tributary Translator Control RAM Indirect Access Address Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 tributary translator control register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.

Sequential SPE	SBI	SPE
1	1	1
2	2	1
3	3	1
4	4	1
5	1	2
6	2	2
7	3	2
8	4	2
9	1	3
10	2	3
11	3	3
12	4	3

Register 041H: OSTT Tributary Translator Control RAM Indirect Access Control Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary translator control RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Tributary Translator Control RAM Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Tributary Translator Control RAM Indirect Access Data.

HST_ADDR_ERR

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Tributary Translator Control RAM Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Translator Control RAM Indirect Access Data register or to determine when a new indirect write operation may commence.

Register 042H: OSTT Tributary Translator Control RAM Indirect Access Data Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	TVT	0
Bit 0	R/W	JUST_REQ_EN	0

JUST_REQ_EN

The JUST_REQ_EN bit is used to enable T1, E1, DS3, E3 and Fractional rate justification request state machines to convert V5, V5+ and V5- characters to JUST_REQs. When this bit is set to 1 the justification request state machines will convert V5 characters to the JUST_REQ signal. When this bit is set to 0 the state machines will not generate JUST_REQ. This bit should be set to 1 when this device is being used in SBI mode and is connected to link layer device which is clock slave to the transmit tributary.

This bit should not be set if the TVT bit is set. This bit has no effect in Telecom bus mode.

This bit should not be set when configured for the receive parallel interface (PARALLEL_MODE = ‘b1 in the SBS Master Configuration Register).

TVT

The TVT bit configures a T1 or E1 tributary as a transparent virtual tributary. When TVT is set to 1 the T1 or E1 tributary is configured as a TVT. Being a TVT, the ERDI and REI bits are received from the serial link in one of the V5 characters and are output on ODATA during the V5 byte. When TVT is set to 0 the T1 or E1 tributary is configured as a standard T1 or E1 link.

This bit should not be set if the JUST_REQ_EN bit is set. This bit has no effect in Telecom bus mode or if the SPE is configured to something other that T1 or E1 data.

This bit should not be set when configured for the receive parallel interface (PARALLEL_MODE = ‘b1 in the SBS Master Configuration Register).

Register 048H: OMSU Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4	R/W	AUTO_UPDATE	0
Bit 3	R/W	SWAP_PENDINGE	0
Bit 2	R/W	UPDATEE	0
Bit 1	R	SWAP_PENDINGV	0
Bit 0	R	UPDATEV	0

AUTO_UPDATE

The AUTO_UPDATE bit selects when an off-line page update is performed. When AUTO_UPDATE is a logic 1, the on-line page is automatically copied into the off-line page whenever there is a change to the connection memory page. When AUTO_UPDATE is a logic 0, the off-line page is not updated when there is a change to the connection memory page. A page update may still be performed by writing to the Interrupt Status and Memory Page Update Register.

SWAP_PENDINGE

A logic 1 on the SWAP_PENDINGE bit enables the generation of an interrupt on a change of state of SWAP_PENDINGV.

UPDATEE

A logic 1 on the UPDATEE bit enables the generation of an interrupt on a change of state from high to low of UPDATEV.

SWAP_PENDINGV

The SWAP_PENDINGV bit contains the current state of the page swap circuitry. This bit is a logic 1 when a switch to the connection memory page (CMP) has been recognized but the page swap has not yet happened. This bit is a logic 0 when there is not a page swap pending.

UPDATEV

The UPDATEV bit contains the current state of the time switch ram off-line page update circuitry. This bit is a logic 1 when the on-line page is being copied to the offline page. This bit is a logic 0 when the on-line page is not being copied.

Register 049H: OMSU Interrupt Status and Memory Page Update Register

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2		Unused	0
Bit 1	R	SWAP_PENDINGI	X
Bit 0	R	UPDATEI	X

Writing to this register initiates an update of the off-line page in the time switch ram. The contents of the on-line page are written to the off-line page. During this update, the time switch ram may not be accessed through the indirect registers.

SWAP_PENDINGI

The page swap pending interrupt status bit, SWAP_PENDINGI, reports and acknowledges a change of state of the SWAP_PENDINGV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the SWAP_PENDINGE bit, the INT output reflects the state of this bit.

UPDATEI

The off-line page update interrupt status bit, UPDATEI, reports and acknowledges a change of state from high to low of the UPDATEV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the UPDATEE bit, the INT output reflects the state of this bit.

Register 04AH: OMSU Indirect Time Switch Address

Bit	Type	Function	Default
Bit 15	R/W	RWB	0
Bit 14		Unused	0
Bit 13	R/W	OUT_BYTE[13]	0
Bit 12	R/W	OUT_BYTE[12]	0
Bit 11	R/W	OUT_BYTE[11]	0
Bit 10	R/W	OUT_BYTE[10]	0
Bit 9	R/W	OUT_BYTE[9]	0
Bit 8	R/W	OUT_BYTE[8]	0
Bit 7	R/W	OUT_BYTE[7]	0
Bit 6	R/W	OUT_BYTE[6]	0
Bit 5	R/W	OUT_BYTE[5]	0
Bit 4	R/W	OUT_BYTE[4]	0
Bit 3	R/W	OUT_BYTE[3]	0
Bit 2	R/W	OUT_BYTE[2]	0
Bit 1	R/W	OUT_BYTE[1]	0
Bit 0	R/W	OUT_BYTE[0]	0

This register provides the address and the read/write control for the time switch configuration ram. Writing to this register triggers a ram access. Note that when an indirect write access is to be performed, the Indirect Time Switch Data register must first be setup before writing to this register. There must be a minimum of 4 SYSCLK cycles between consecutive ram accesses. For a ram read access, it will take a maximum of 8 SYSCLK cycles for the Indirect Time Switch Data Register to contain valid data.

RWB

The indirect access control bit (RWB) selects between a write or read access to the time switch configuration RAM. Writing a logic zero to RWB triggers and indirect write operation. Data to be written is taken from the Indirect Time Switch Data register. Writing a logic one to RWB triggers an indirect read operation. The read data can be found in the Indirect Time Switch Data Register.

OUT_BYTE[13:0]

The OUT_BYTE[13:0] bits indicate the ram address to be accessed. Each address in the ram corresponds to a location in the output data bus. The contents stored in each ram address points to the byte from the input data bus which is to be output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079). The byte numbers of the output frame are shown in the following table.

Row								
1	0	1	2	3	…	1077	1078	1079
2	1080	1081	1082	1083	…	2157	2158	2159
3								
4								
5								
6								
7								
8								
9	8640	8641	8642	8643	…	9717	9718	9719

Register 04BH: OMSU Indirect Time Switch Data

Bit	Type	Function	Default
Bit 15	R	VALID	0
Bit 14	R/W	O2I_DS0_LOOP	0
Bit 13	R/W	IN_BYTE[13]	0
Bit 12	R/W	IN_BYTE [12]	0
Bit 11	R/W	IN_BYTE [11]	0
Bit 10	R/W	IN_BYTE [10]	0
Bit 9	R/W	IN_BYTE [9]	0
Bit 8	R/W	IN_BYTE [8]	0
Bit 7	R/W	IN_BYTE [7]	0
Bit 6	R/W	IN_BYTE [6]	0
Bit 5	R/W	IN_BYTE [5]	0
Bit 4	R/W	IN_BYTE [4]	0
Bit 3	R/W	IN_BYTE [3]	0
Bit 2	R/W	IN_BYTE [2]	0
Bit 1	R/W	IN_BYTE [1]	0
Bit 0	R/W	IN_BYTE [0]	0

This register contains data read from the time switch RAM after an indirect read operation or data to be inserted into the time switch RAM during an indirect write operation. The value held in the ram indicates which byte of the input data bus is to be switched to the output.

VALID

The VALID bit reports the presence of valid data from an indirect read. VALID is set to logic 1 when indirect read access returns data from the off-line RAM and remains asserted until the next time Indirect Time Switch Data register is read.

O2I_DS0_LOOP

This bit, when set, enables DS0 or Column loop backs between the output of the OMSU and the input of the IMSU. When enabling these loop backs, the offset between RC1FP and IC1FP must be set such that the normal data and the loop back data arrive at the IMSU at the same time.

The following are the IC1FP to RC1FP offsets, in SYSCLK cycles, in various operating modes:

Mode	Offset
77MHz parallel Telecom Column switched	1078
77MHz parallel SBI Column switched	1082
77MHz parallel SBI DS0 switched	9722
19MHz parallel Telecom Column switched	1076*
19MHz parallel SBI Column switched	1080*
19MHz parallel SBI DS0 switched	9720*

* Measured from the SYSCLK cycle corresponding to the sampling REFCLK rising edge

IN_BYTE[13:0]

The IN_BYTE[13:0] bits indicate which byte in the input frame is to be switched to the output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079).

The MSU has the ability of overwrite the outputs when a value outside the range specified above is programmed. When IN_BYTE[13:12] = 'b11, the value output on OPL, OTPL, OV5, OC1FP, OTAIS and ODATA[7:0] is overwritten as shown in the following tables.

In Column Mode (Telecom bus), using the receive serial or parallel interface:

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	MODE[2]	MODE[1]	MODE[0]	OTAIS	ODATA[7:0]

Where

MODE[2:0]		Setting of Outputs				
		OPL	OTPL	OC1FP (marking the J1 byte)	OV5	Special Setting
000	Transport Overhead (TOH)	0	0	0	0	
001	J1 column	1	0	1 for 1st row, 0 for rows 2-9	0	ODATA is set to 111111CC at the H4 byte. CC indicates the frame number in the multi-frame.
010	Path level stuff columns	1	0	0	0	
011	Tributary Vx columns (V1, V2, V3,	1	0 for 1st row, 1 for rows 2-9	0	0	

MODE[2:0]		Setting of Outputs				
		OPL	OTPL	OC1FP (marking the J1 byte)	OV5	Special Setting
	V4)					
100	Tributary data columns	1	1	0	0	
101	Tributary data columns with V5	1	1	0	1 for 1st row in multi-frame, 0 otherwise	
110 – 111	Reserved					

In Column Mode (SBI bus), using the receive serial interface:

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	MODE[2]	MODE[1]	MODE[0]	Reserved	ODATA[7:0]

Where

MODE[2:0]		Setting of Outputs		
		OPL	OV5	Special Instructions
000	Transport Overhead (TOH)	0	0	Should be set for columns 0 to 35.
001	Reserved			Do not use
010	Path level stuff columns	0	0	Should be set for stuff columns > 35
011	Tributary Vx columns (V1, V2, V3, V4)	0 for 1st row, 1 for rows 2-9	0	Use for T1 and E1 tributaries only
100	Tributary data columns	1	0	Use for any data type
101	Tributary data columns with V5	1	1 for 1st row in multi-frame, 0 otherwise.	Use for T1 and E1 tributaries only. Note that ODATA=00H for first row in multi-frame.
110 – 111	Reserved			Do not use

In Column Mode (SBI bus), using the receive parallel interface:

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	OPL	Reserved	Reserved	Reserved	ODATA[7:0]

In DS0 Mode (SBI bus), using the receive serial interface:

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	Reserved	OPL	Reserved	Reserved	ODATA[7:0]

In DS0 Mode (SBI bus), using the receive parallel interface:

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	OPL	Reserved	Reserved	Reserved	ODATA[7:0]

Note that for all modes, the Reserved bits should be set to a logic 0.

Register 050H: OCASM CAS Enable Indirect Access Address Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 CAS enable register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.

Sequential SPE	SBI	SPE
1	1	1
2	2	1
3	3	1
4	4	1
5	1	2
6	2	2
7	3	2
8	4	2
9	1	3
10	2	3
11	3	3
12	4	3

Register 051H: OCASM CAS Enable Indirect Access Control Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the CAS Enable register. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the CAS Enable Indirect Access Data register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the CAS Enable Indirect Access Data register.

HST_ADDR_ERR

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the CAS Enable Indirect Access Control register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the CAS Enable Indirect Access Data register or to determine when a new indirect write operation may commence.

Register 052H: OCASM CAS Enable Indirect Access Data Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R	Unused	0
Bit 0	R/W	CAS_EN	0

CAS_EN

The CAS_EN bit is used to enable the insertion of CAS into the proper location in the associated tributary. When CAS_EN is a logic 1 and the associated tributary is a T1, the CAS bits and PP bits are inserted into the PPSSSSFR byte. When CAS_EN is a logic 1 and the associated tributary is an E1, the CAS bits are inserted into TS#16 and proper data is placed in the PP byte. When CAS_EN is a logic 0, both the CAS and PP bits are not inserted. This bit should only be set if operating in 48-frame mode.

When CAS insertion is enabled, the latency of the CAS bits through the SBS is two multi-frames. For T1 tributaries, this is 48 frames or 6ms. For E1 tributaries, this is 32 frames or 4 ms.

Register 060H: OSTA Outgoing Configuration and Parity

Bit	Type	Function	Default
Bit 15	R/W	OUTGOING_OE	0
Bit 14	R/W	OLOCK0	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	INCLOC1FP[4]	0
Bit 10	R/W	INCLOC1FP[3]	0
Bit 9	R/W	INCLOC1FP[2]	0
Bit 8	R/W	INCLOC1FP[1]	0
Bit 7	R/W	INCLOPL[4]	0
Bit 6	R/W	INCLOPL[3]	0
Bit 5	R/W	INCLOPL[2]	0
Bit 4	R/W	INCLOPL[1]	0
Bit 3	R/W	OOP[4]	0
Bit 2	R/W	OOP[3]	0
Bit 1	R/W	OOP[2]	0
Bit 0	R/W	OOP[1]	0

OUTGOING_OE

The OUTGOING_OE bit controls the output enable on the outgoing bus. When OUTGOING_OE is a logic 1, the entire outgoing bus is driven at all times regardless of the state of the per-tributary OUTPUT_ENABLE bits in register 068H. When OUTGOING_OE is a logic 0, only the tributaries with their OUTPUT_ENABLE bit set will be driven. This bit only has an effect when in 19.44MHz SBI mode (TELECOM_BUS = ‘b0, 19M_BUSB = ‘b0 in the SBS Master Configuration Register). In all other modes, the outgoing bus is always driven.

OLOCK0

The OLOCK0 bit controls the position of the J1 byte in the Outgoing Telecom Bus. When OLOCK0 is a logic 1, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When OLOCK0 is a logic 0, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to pulse the OC1FP output when any part of STS1_OJ1EN[12:1] or STS1_OV1EN[12:1] are set. This bit only has an effect when in Telecom Bus mode (TELECOM_BUS = ‘b1 in the SBS Master Configuration Register).

INCLOC1FP[4:1]

The INCLOC1FP bits control whether the OC1FP output signal participates in the outgoing parity calculations. When INCLOC1FP[x] is set to a logic 1, the parity signal includes the OC1FP output. When INCLOC1FP[x] is set to a logic 0, parity is calculated without regard to the state of OC1FP. These bits only take effect when in Telecom bus mode. INCLOC1FP[4:2] are only valid when in 19MHz mode.

INCLOPL[4:1]

The INCLOPL bits control whether the OPL[x] output signal participates in the outgoing parity calculations. When INCLOPL[x] is set to a logic 1, the parity signal includes the OPL[x] output. When INCLOPL[x] is set to a logic 0, parity is calculated without regard to the state of OPL[x]. These bits only take effect when in Telecom bus mode. INCLOPL[4:2] are only valid when in 19MHz mode.

OOP

The outgoing odd parity bit (OOP) controls the parity generated on the outgoing bus. When OOP[x] is set to a logic 1, the parity on the ODP[x] output is odd. When OOP[x] is set to a logic 0, the parity is even. In SBI bus mode, the parity calculation encompasses the ODATA[x][7:0], OPL[x] and OV5[x] signals. In Telecom bus mode, the parity calculation encompasses the ODATA[x][7:0] and optionally OPL and OC1FP as determined by the INCLOPL[x] and INCLOC1FP[x] bits. OOP[4:2] are only valid when in 19MHz mode.

Register 061H: OSTA Outgoing J1 Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_OJ1EN[12]	0
Bit 10	R/W	STS1_OJ1EN[11]	0
Bit 9	R/W	STS1_OJ1EN[10]	0
Bit 8	R/W	STS1_OJ1EN[9]	0
Bit 7	R/W	STS1_OJ1EN[8]	0
Bit 6	R/W	STS1_OJ1EN[7]	0
Bit 5	R/W	STS1_OJ1EN[6]	0
Bit 4	R/W	STS1_OJ1EN[5]	0
Bit 3	R/W	STS1_OJ1EN[4]	0
Bit 2	R/W	STS1_OJ1EN[3]	0
Bit 1	R/W	STS1_OJ1EN[2]	0
Bit 0	R/W	STS1_OJ1EN[1]	0

STS1_OJ1EN[12:1]

The STS1_OJ1EN[12:1] bits may control the inclusion of the J1 byte identification on the OC1FP[4:1] output for each of the 12 STS/AUs. When STS1_OJ1EN[x] is a logic 1, the OC1FP[4:1] output will pulse high during the J1 byte position of the associated STS/AU along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the OLOCK0 bit. When STS1_OJ1EN[x] is a logic 0, the OC1FP[4:1] will not pulse high during the J1 byte position of the associated STS/AU. This bit only has an effect when in Telecom Bus mode (TELECOM_BUS = ‘b1 in the SBS Master Configuration Register). In 19MHz mode, the 12 STS/AUs are spread across the four outgoing buses. STS1_OJ1EN[1] controls the first STS/AU of the first bus, STS1_OJ1EN[2] controls the first STS/AU of the second bus, etc. These register bits should not be set if the receive serial link contains J1 characters (in serial mode) or the RC1FP input contain J1 indications (in parallel mode).

See section 13.12 for more information about J1/V1 insertion

Register 062H: OSTA Outgoing V1 Configuration

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_OV1EN[12]	0
Bit 10	R/W	STS1_OV1EN[11]	0
Bit 9	R/W	STS1_OV1EN[10]	0
Bit 8	R/W	STS1_OV1EN[9]	0
Bit 7	R/W	STS1_OV1EN[8]	0
Bit 6	R/W	STS1_OV1EN[7]	0
Bit 5	R/W	STS1_OV1EN[6]	0
Bit 4	R/W	STS1_OV1EN[5]	0
Bit 3	R/W	STS1_OV1EN[4]	0
Bit 2	R/W	STS1_OV1EN[3]	0
Bit 1	R/W	STS1_OV1EN[2]	0
Bit 0	R/W	STS1_OV1EN[1]	0

STS1_OV1EN[12:1]

The STS1_OV1EN[12:1] bit controls the inclusion of the byte following J1 identification on the OC1FP[4:1] output for each of the 12 STS/AUs. When STS1_OV1EN[x] is a logic 1, the OC1FP[4:1] output will pulse high during the byte following the J1 position of the associated STS/AU along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the OLOCK0 bit. When STS1_OV1EN is a logic 0, the OC1FP[4:1] will not pulse high during the byte following the J1 position of the associated STS/AU. This bit only has an effect when in Telecom Bus mode (TELECOM_BUS = ‘b1 in the SBS Master Configuration Register). In 19MHz mode, the 12 STS/AUs are spread across the four outgoing buses. STS1_OV1EN[1] controls the first STS/AU of the first bus, STS1_OV1EN[2] controls the first STS/AU of the second bus, etc. These bits should only be set when the associated STS/AU does not contain any high order pointer movements and the J1 bytes are in a fixed position relative to the C1 byte.

See section 13.12 for more information about J1/V1 insertion

Register 063H: OSTA H1-H2 Pointer Value

Bit	Type	Function	Default
Bit 15	R/W	H1[7]	0
Bit 14	R/W	H1[6]	0
Bit 13	R/W	H1[5]	0
Bit 12	R/W	H1[4]	0
Bit 11	R/W	H1[3]	0
Bit 10	R/W	H1[2]	0
Bit 9	R/W	H1[1]	0
Bit 8	R/W	H1[0]	0
Bit 7	R/W	H2[7]	0
Bit 6	R/W	H2[6]	0
Bit 5	R/W	H2[5]	0
Bit 4	R/W	H2[4]	0
Bit 3	R/W	H2[3]	0
Bit 2	R/W	H2[2]	0
Bit 1	R/W	H2[1]	0
Bit 0	R/W	H2[0]	0

H1[7:0]

The H1[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Outgoing Telecom bus when the STS1_PTR_SEL[x] bit is a logic 0 and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

H2[7:0]

The H2[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Outgoing Telecom bus when the STS1_PTR_SEL[x] bit is a logic 0 and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

Register 064H: OSTA Alternate H1-H2 Pointer Value

Bit	Type	Function	Default
Bit 15	R/W	H1_ALT[7]	0
Bit 14	R/W	H1_ALT[6]	0
Bit 13	R/W	H1_ALT[5]	0
Bit 12	R/W	H1_ ALT[4]	0
Bit 11	R/W	H1_ ALT[3]	0
Bit 10	R/W	H1_ ALT[2]	0
Bit 9	R/W	H1_ ALT[1]	0
Bit 8	R/W	H1_ ALT[0]	0
Bit 7	R/W	H2_ ALT[7]	0
Bit 6	R/W	H2_ ALT[6]	0
Bit 5	R/W	H2_ ALT[5]	0
Bit 4	R/W	H2_ ALT[4]	0
Bit 3	R/W	H2_ ALT[3]	0
Bit 2	R/W	H2_ ALT[2]	0
Bit 1	R/W	H2_ ALT[1]	0
Bit 0	R/W	H2_ ALT[0]	0

H1_ALT[7:0]

The H1_ALT[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Outgoing Telecom bus when the STS1_PTR_SEL[x] bit is a logic 1 and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

H2_ALT[7:0]

The H2_ALT[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Outgoing Telecom bus when the STS1_PTR_SEL[x] bit is a logic 1 and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

Register 065H: OSTA H1-H2 Pointer Selection

Bit	Type	Function	Default
Bit 15	R/W	OH1H2EN	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_PTR_SEL[12]	0
Bit 10	R/W	STS1_PTR_SEL[11]	0
Bit 9	R/W	STS1_PTR_SEL[10]	0
Bit 8	R/W	STS1_PTR_SEL[9]	0
Bit 7	R/W	STS1_PTR_SEL[8]	0
Bit 6	R/W	STS1_PTR_SEL[7]	0
Bit 5	R/W	STS1_PTR_SEL[6]	0
Bit 4	R/W	STS1_PTR_SEL[5]	0
Bit 3	R/W	STS1_PTR_SEL[4]	0
Bit 2	R/W	STS1_PTR_SEL[3]	0
Bit 1	R/W	STS1_PTR_SEL[2]	0
Bit 0	R/W	STS1_PTR_SEL[1]	0

OH1H2EN

The OH1H2EN bit enables the insertion of the H1 and H2 bytes in the transport overhead on the Outgoing Telecom bus. When OH1H2EN is a logic 1, the values in the internal registers is inserted into the H1 and H2 bytes of the Outgoing Telecom bus according to the STS1_PTR_SEL[12:1] bits. When OH1H2EN is a logic 0, the values from the internal registers is not inserted into the H1 and H2 bytes. This bit has no effect when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register). This bit should not be set if any of the STS/AUs are floating.

STS1_PTR_SEL[12:1]

The STS1_PTR_SEL[12:1] bits select which of the two H1-H2 Pointer registers is used for each of the 12 STS/AUs output on the Outgoing Telecom bus when the OH1H2EN bit is set. When STS1_PTR_SEL[x] is a logic 0, the SBS Transmit H1-H2 Pointer Value register is used for the associated STS/AU on the Outgoing bus. When STS1_PTR_SEL[x] is a logic 1, the SBS Transmit Alternate H1-H2 Pointer Value register is used for the associated STS/AU on the Outgoing bus. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM_BUS = ‘b0 in the Master Configuration Register).

Register 066H: OSTA Tributary Output Enable Indirect Access Address Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 tributary output enable register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.

Sequential SPE	SBI	SPE
1	1	1
2	2	1
3	3	1
4	4	1
5	1	2
6	2	2
7	3	2
8	4	2
9	1	3
10	2	3
11	3	3
12	4	3

Register 067H: OSTA Tributary Output Enable Indirect Access Control Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary output enable register. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Output Enable Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Tributary Output Enable Indirect Access Data Register.

HST_ADDR_ERR

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Tributary Output Enable Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Tributary Output Enable Indirect Access Data register or to determine when a new indirect write operation may commence.

Register 068H: OSTA Tributary Output Enable Indirect Access Data Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R	Unused	0
Bit 0	R/W	OUTPUT_ENABLE	0

OUTPUT_ENABLE

The OUTPUT_ENABLE bit controls whether or not the Outgoing bus is driven during the associated tributary. This bit only has an effect when the OUTGOING_OE bit in register 060H is a logic 0. When OUTPUT_ENABLE is a logic 1, the associated tributary is driven onto the Outgoing bus. When OUTPUT_ENABLE is a logic 0, the associated tributary is not driven and the Outgoing bus is held high impedance. Parity is only generated on enabled links. This bit is only used in 19MHz SBI mode. In all other modes, this bit is ignored.

Register 070h: WPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the WPP block. Writing to this register triggers an indirect register access.

PATH[3:0]

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	Time Division #
0000	Invalid STS-1/STM-0 path
0001-1100	STS-1/STM-0 path #1 to STS-1/STM-0 path #12
1101-1111	Invalid STS-1/STM-0 path

IADDR[3:0]

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor (IADDR[3] = ‘0’) : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1/STM-0 path Configuration page
0001	PRBS[22:7] page

IADDR[3:0]	RAM page
0010	PRBS[6:0] page
0011	Reserved
0100	Monitor error count page
0101	Reserved

Four pages are defined for the generator (IADDR [3] = '1') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page and the B1/E1 value.

IADDR[3:0]	RAM page
1000	STS-1/STM-0 path Configuration page
1001	PRBS[22:7] page
1010	PRBS[6:0] page
1011	Reserved

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 071h: WPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

Register 071h (IADDR = 0h): WPP Monitor STS-1/STM-0 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	AMODE	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 0h (IADDR[3:0] is “0h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured

MON_ENA

Monitor Enable register bit, enables the PRBS monitor for the STS-1/STM-0 path specified in the PATH[3:0] of register 070h (WPP Indirect Address). If MON_ENA is set to ‘1’, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the data at the input of the monitor is ignored.

AMODE

If AMODE is high, the monitor is in Autonomous mode, and the incoming SONET/SDH payload is compared to the internally generated one. In Autonomous mode, the beginning of the SPE is always place next to the H3 byte (zero offset), so the J1 pulses are ignored. When using the WPP in TelecomBus mode, this bit must be set high. When using the WPP in SBI mode, this bit must be set low.

INV_PRBS

This sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

RESYNC

This sets the monitor to re-initialize the PRBS sequence. When set high the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream.

SEQ_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Reserved

The reserved bits must be set low for correct operation of the SBS.

Register 071h (IADDR = 1h): WPP Monitor PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 1h (IADDR[3:0] is “1h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

PRBS[22:7]

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 071h (IADDR = 2h): WPP Monitor PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

PRBS[6:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 071h (IADDR = 4h): WPP Monitor Error count

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 4h (IADDR[3:0] is “4h” in register 070h).

ERR_CNT[15:0]

The ERR_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by writing to the WPP Performance Counters Transfer Trigger Register (07CH) or writing the SBS Master Signal Monitor #1, Accumulation Trigger Register (014H). The error counter is cleared and restarted after its value is transferred to the ERR_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value.

Register 071h (IADDR = 8h): WPP Generator STS-1/STM-0 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	LINKENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	LINKENA	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	Reserved	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	AMODE	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 8h (IADDR[3:0] is “8h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

AMODE

If AMODE is high, the generator is in Autonomous mode, and the SONET/SDH frame is generated using only the C1 pulse. The payload frame (J1) is at a fixed alignment as no pointer movements are generated. When using the WPP in TelecomBus mode, this bit must be set high. When using the WPP in SBI mode, this bit must be set low.

INV_PRBS

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

FORCE_ERR

The Force Error bit is used to force bit errors in the inserted pattern. When a logic one is written, the MSB of the next byte will be inverted, inducing a single bit error. The register clears itself when the operation is complete.

SEQ_PRBSB

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

LINKENA

These two bits specify if PRBS is to be inserted in the path through the TW8E. If LINKENA is high patterns are generated in the SONET/SDH frame to the TW8E, else no pattern is generated and the unmodified SONET/SDH input frame is passed to the TW8E.

Reserved

The reserved bits must be set low for correct operation of the SBS.

Register 071h (IADDR = 9h): WPP Generator PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 9h (IADDR[3:0] is “9h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

PRBS[22:7]

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 071h (IADDR = Ah): WPP Generator PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address Ah (IADDR[3:0] is “Ah” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

PRBS[6:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 072h: WPP Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[3]	0
Bit 2	R/W	GEN_STS3C[2]	0
Bit 1	R/W	GEN_STS3C[1]	0
Bit 0	R/W	GEN_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming bus for processing by the Working PRBS generator.

GEN_STS3C[0]

The STS-3c/VC-4 payload configuration (GEN_STS3C[0]) bit selects the payload configuration. When GEN_STS3C[0] is set to logic 1, the STS-1/VC-3 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When GEN_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[0] register bit.

GEN_STS3C[1]

The STS-3c/VC-4 payload configuration (GEN_STS3C[1]) bit selects the payload configuration. When GEN_STS3C[1] is set to logic 1, the STS-1/VC-3 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When GEN_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[1] register bit.

GEN_STS3C[2]

The STS-3c/VC-4 payload configuration (GEN_STS3C[2]) bit selects the payload configuration. When GEN_STS3C[2] is set to logic 1, the STS-1/VC-3 paths #3, #7 and #11 are part of a STS-3cVC-4 payload. When GEN_STS3C[2] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[2] register bit.

GEN_STS3C[4]

The STS-3c/VC-4 payload configuration (GEN_STS3C[3]) bit selects the payload configuration. When GEN_STS3C[3] is set to logic 1, the STS-1/VC-3 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When GEN_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[3] register bit.

GEN_STS12C

The STS-12c/VC-4-4c payload configuration (GEN_STS12C) bit selects the payload configuration. When GEN_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by GEN_MSSLEN. When GEN_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN_STS3C[3:0] register bit. The GEN_STS12C register bit has precedence over the GEN_STS3C[3:0] register bit.

Reserved

The Reserved bits must be set low for correct operation of the SBS.

Register 073h: WPP Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Receive Working Serial Link for processing by the PRBS monitor section.

MON_STS3C[0]

The STS-3c/VC-4 payload configuration (MON_STS3C[0]) bit selects the payload configuration. When MON_STS3C[0] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[0] register bit.

MON_STS3C[1]

The STS-3c/VC-4 payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[1] register bit.

MON_STS3C[2]

The STS-3c/VC-4 payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON_STS-3c/VC-4 payload. When MON_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The MON_STS12C register bit has precedence over the MON_STS3C[2] register bit.

MON_STS3C[4]

The STS-3c/VC-4 payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[3] register bit.

Reserved

The Reserved bits must be set low for correct operation of the SBS.

MON_STS12C

The STS-12c/VC-4-4c payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON_STS3C[3:0] register bit. The MON_STS12C register bit has precedence over the MON_STS3C[3:0] register bit.

Register 074h: WPP Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Receive Working Serial Link.

MON**x**_ERRI

The Monitor Byte Error Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1/STM-0 paths when an error has been detected. The MON**x**_ERRE is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1/STM-0 path **x**. This bit is independent of MON**x**_ERRE and is cleared after being read.

Register 075h: WPP Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Receive Working bus.

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1/STM-0 paths. When MON**x**_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt on INT.

Register 079h: WPP Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Receive Working Serial Link.

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1/STM-0 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. This bit is independent of MONx_SYNCE and is cleared after it's been read.

Register 07Ah: WPP Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Receive Working Serial Link.

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable register allows each individual STS-1/STM-0 path to generate an external interrupt on INT. When MON**x**_SYNCE is set high whenever a change occurs in the synchronization state of the monitor in STS-1/STM-0 path **x**, generates an interrupt on INT.

Register 07Bh: WPP Monitor Synchronization State

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Receive Working Serial Link.

MON**x**_SYNCV

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON**x**_SYNCV is set high the monitor's state machine is in synchronization for the STS-1/STM-0 Path **x**. When MON**x**_SYNCV is low the monitor is NOT in synchronization for the STS-1/STM-0 Path **x**.

When checking the state of MON**x**_SYNCV, you must also check the state of the WPP Monitor PRBS Accumulator Registers (Register 071H with IADDR=1H and 2H) of the associated STS-1/STM-0. If the value of MON**x**_SYNCV is a logic 1 and the value in the PRBS register is all zeros, then the associated STS-1/STM-0 path is NOT in synchronization. If the value of MON**x**_SYNCV is a logic 1 and the value in the PRBS register is non-zero, then the associated STS-1/STM-0 path is IN synchronization.

Register 07Ch: WPP Performance Counters Transfer Trigger

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

TIP

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

Register 080h: PPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the PPP block. Writing to this register triggers an indirect register access.

PATH[3:0]

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	Time Division #
0000	Invalid STS-1/STM-0 path
0001-1100	STS-1/STM-0 path #1 to STS-1/STM-0 path #12
1101-1111	Invalid STS-1/STM-0 path

IADDR[3:0]

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor (IADDR[3] = ‘0’) : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1/STM-0 path Configuration page
0001	PRBS[22:7] page

IADDR[3:0]	RAM page
0010	PRBS[6:0] page
0011	Reserved
0100	Monitor error count page
0101	Reserved

Four pages are defined for the generator (IADDR [3] = '1') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page and the B1/E1 value.

IADDR[3:0]	RAM page
1000	STS-1/STM-0 path Configuration page
1001	PRBS[22:7] page
1010	PRBS[6:0] page
1011	Reserved

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 081h: PPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

Register 081h (IADDR = 0h): PPP Monitor STS-1/STM-0 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	AMODE	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 0h (IADDR[3:0] is “0h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured

MON_ENA

Monitor Enable register bit, enables the PRBS monitor for the STS-1/STM-0 path specified in the PATH[3:0] of register 080h (PPP Indirect Address). If MON_ENA is set to ‘1’, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the data at the input of the monitor is ignored.

AMODE

If AMODE is high, the monitor is in Autonomous mode, and the incoming SONET/SDH payload is compared to the internally generated one. In Autonomous mode, the beginning of the SPE is always place next to the H3 byte (zero offset), so the J1 pulses are ignored. When using the PPP in TelecomBus mode, this bit must be set high. When using the PPP in SBI mode, this bit must be set low.

INV_PRBS

This sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

RESYNC

This sets the monitor to re-initialize the PRBS sequence. When set high the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream.

SEQ_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Reserved

The reserved bits must be set low for correct operation of the SBS.

Register 081h (IADDR = 1h): PPP Monitor PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 1h (IADDR[3:0] is “1h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

PRBS[22:7]

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 081h (IADDR = 2h): PPP Monitor PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

PRBS[6:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 081h (IADDR = 4h): PPP Monitor Error count

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the PPP Indirect Data register (Register 061h) when accessing Indirect Address 4h (IADDR[3:0] is “4h” in register 060h).

ERR_CNT[15:0]

The ERR_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by writing to the PPP Performance Counters Transfer Trigger Register (08CH) or by writing the SBS Master Signal Monitor #1, Accumulation Trigger Register (014H). The error counter is cleared and restarted after its value is transferred to the ERR_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value.

Register 081h (IADDR = 8h): PPP Generator STS-1/STM-0 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	LINKENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	X
Bit 8	R/W	LINKENA	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	Reserved	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	AMODE	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 8h (IADDR[3:0] is “8h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

AMODE

If AMODE is high, the generator is in Autonomous mode, and the SONET/SDH frame is generated using only the C1 pulse. The payload frame (J1) is at a fixed alignment as no pointer movements are generated. When using the PPP in TelecomBus mode, this bit must be set high. When using the PPP in SBI mode, this bit must be set low.

INV_PRBS

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

FORCE_ERR

The Force Error bit is used to force bit errors in the inserted pattern. When a logic one is written, the MSB of the next byte will be inverted, inducing a single bit error. The register clears itself when the operation is complete.

SEQ_PRBSB

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

LINKENA

These two bits specify if PRBS is to be inserted in the path through the TP8E. If LINKENA is high patterns are generated in the SONET/SDH frame to the TP8E, else no pattern is generated and the unmodified SONET/SDH input frame is passed to the TP8E.

Reserved

The reserved bits must be set low for correct operation of the SBS.

Register 081h (IADDR = 9h): PPP Generator PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 9h (IADDR[3:0] is “9h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

PRBS[22:7]

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 081h (IADDR = Ah): PPP Generator PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address Ah (IADDR[3:0] is “Ah” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

PRBS[6:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 082h: PPP Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[3]	0
Bit 2	R/W	GEN_STS3C[2]	0
Bit 1	R/W	GEN_STS3C[1]	0
Bit 0	R/W	GEN_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming bus for processing by the Protect PRBS generator.

GEN_STS3C[0]

The STS-3c/VC-4 payload configuration (GEN_STS3C[0]) bit selects the payload configuration. When GEN_STS3C[0] is set to logic 1, the STS-1/VC-3 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When GEN_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[0] register bit.

GEN_STS3C[1]

The STS-3c/VC-4 payload configuration (GEN_STS3C[1]) bit selects the payload configuration. When GEN_STS3C[1] is set to logic 1, the STS-1/VC-3 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When GEN_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[1] register bit.

GEN_STS3C[2]

The STS-3c/VC-4 payload configuration (GEN_STS3C[2]) bit selects the payload configuration. When GEN_STS3C[2] is set to logic 1, the STS-1/VC-3 paths #3, #7 and #11 are part of a STS-3cVC-4 payload. When GEN_STS3C[2] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[2] register bit.

GEN_STS3C[4]

The STS-3c/VC-4 payload configuration (GEN_STS3C[3]) bit selects the payload configuration. When GEN_STS3C[3] is set to logic 1, the STS-1/VC-3 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When GEN_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[3] register bit.

GEN_STS12C

The STS-12c/VC-4-4c payload configuration (GEN_STS12C) bit selects the payload configuration. When GEN_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by GEN_MSSLEN. When GEN_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN_STS3C[3:0] register bit. The GEN_STS12C register bit has precedence over the GEN_STS3C[3:0] register bit.

Reserved

The Reserved bits must be set low for correct operation of the SBS.

Register 083h: PPP Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Receive Protection Serial Link for processing by the PRBS monitor section.

MON_STS3C[0]

The STS-3c/VC-4 payload configuration (MON_STS3C[0]) bit selects the payload configuration. When MON_STS3C[0] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[0] register bit.

MON_STS3C[1]

The STS-3c/VC-4 payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[1] register bit.

MON_STS3C[2]

The STS-3c/VC-4 payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON_STS-3c/VC-4 payload. When MON_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The MON_STS12C register bit has precedence over the MON_STS3C[2] register bit.

MON_STS3C[4]

The STS-3c/VC-4 payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[3] register bit.

MON_STS12C

The STS-12c/VC-4-4c payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON_STS3C[3:0] register bit. The MON_STS12C register bit has precedence over the MON_STS3C[3:0] register bit.

Reserved

The Reserved bits must be set low for correct operation of the SBS.

Register 084h: PPP Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Receive Protection Serial Link.

MON**x**_ERRI

The Monitor Byte Error Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1/STM-0 paths when an error has been detected. The MON**x**_ERRE is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1/STM-0 path **x**. This bit is independent of MON**x**_ERRE and is cleared after being read.

Register 085h: PPP Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Receive Protection Serial Link.

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1/STM-0 paths. When MON**x**_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt on INT.

Register 089h: PPP Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Receive Protection Serial Link.

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1/STM-0 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. This bit is independent of MONx_SYNCE and is cleared after it's been read.

Register 08Ah: PPP Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Receive Protection Serial Link.

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable register allows each individual STS-1/STM-0 path to generate an external interrupt on INT. When MON**x**_SYNCE is set high whenever a change occurs in the synchronization state of the monitor in STS-1/STM-0 path **x**, generates an interrupt on INT.

Register 08Bh: PPP Monitor Synchronization State

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Receive Protection Serial Link.

MON**x**_SYNCV

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON**x**_SYNCV is set high the monitor's state machine is in synchronization for the STS-1/STM-0 Path **x**. When MON**x**_SYNCV is low the monitor is NOT in synchronization for the STS-1/STM-0 Path **x**.

When checking the state of MON**x**_SYNCV, you must also check the state of the PPP Monitor PRBS Accumulator Registers (Register 081H with IADDR=1H and 2H) of the associated STS-1/STM-0. If the value of MON**x**_SYNCV is a logic 1 and the value in the PRBS register is all zeros, then the associated STS-1/STM-0 path is NOT in synchronization. If the value of MON**x**_SYNCV is a logic 1 and the value in the PRBS register is non-zero, then the associated STS-1/STM-0 path is IN synchronization.

Register 08Ch: PPP Performance Counters Transfer Trigger

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

TIP

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

Register 090H: WILC Transmit FIFO Data High

Bit	Type	Function	Default
Bit 15	R/W	TDAT[31]	0
Bit 14	R/W	TDAT[30]	0
Bit 13	R/W	TDAT[29]	0
Bit 12	R/W	TDAT[28]	0
Bit 11	R/W	TDAT[27]	0
Bit 10	R/W	TDAT[26]	0
Bit 9	R/W	TDAT[25]	0
Bit 8	R/W	TDAT[24]	0
Bit 7	R/W	TDAT[23]	0
Bit 6	R/W	TDAT[22]	0
Bit 5	R/W	TDAT[21]	0
Bit 4	R/W	TDAT[20]	0
Bit 3	R/W	TDAT[19]	0
Bit 2	R/W	TDAT[18]	0
Bit 1	R/W	TDAT[17]	0
Bit 0	R/W	TDAT[16]	0

When writing data to the transmit FIFO, this register must be written to before register 091H.

TDAT[31:16]

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

Register 091H: WILC Transmit FIFO Data Low

Bit	Type	Function	Default
Bit 15	R/W	TDAT[15]	0
Bit 14	R/W	TDAT[14]	0
Bit 13	R/W	TDAT[13]	0
Bit 12	R/W	TDAT[12]	0
Bit 11	R/W	TDAT[11]	0
Bit 10	R/W	TDAT[10]	0
Bit 9	R/W	TDAT[9]	0
Bit 8	R/W	TDAT[8]	0
Bit 7	R/W	TDAT[7]	0
Bit 6	R/W	TDAT[6]	0
Bit 5	R/W	TDAT[5]	0
Bit 4	R/W	TDAT[4]	0
Bit 3	R/W	TDAT[3]	0
Bit 2	R/W	TDAT[2]	0
Bit 1	R/W	TDAT[1]	0
Bit 0	R/W	TDAT[0]	0

Writing to this register will initiate a transfer of TDAT[31:0] into the transmit FIFO.

TDAT[15:0]

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

Register 093H: WILC Transmit Control Register

Bit	Type	Function	Default
Bit 15	R/W	TX_AUX[7]	0
Bit 14	R/W	TX_AUX[6]	0
Bit 13	R/W	TX_AUX[5]	0
Bit 12	R/W	TX_AUX[4]	0
Bit 11	R/W	TX_AUX[3]	0
Bit 10	R/W	TX_AUX[2]	0
Bit 9	R/W	TX_AUX[1]	0
Bit 8	R/W	TX_AUX[0]	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R/W	TX_LINK[1]	0
Bit 4	R/W	TX_LINK[0]	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	TX_CRC_SWIZ_EN	0
Bit 0	R/W	TX_BYPASS	0

TX_BYPASS

When this bit is set to ‘1’, the blocks message transmit functions are bypassed. No messages are inserted into the Transmit data. The transmit message FIFO RAM is disabled and thus message data writes are ignored.

TX_CRC_SWIZ_EN

When this bit is set to ‘1’, the calculated CRC-16 is bit reversed before being transmitted. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality.

TX_LINK[1:0]

These bits are transmitted in the LINK bits of the message header of the next available message. On reads these bit return the last written value.

TX_AUX[7:0]

These bits form the input to an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developer’s discretion. Data written to this register will be transmitted in the AUX header byte of each subsequent message to the other end of the in-band link. A new value of TX_AUX will be transmitted at the next available message. Data read from this register will be the data previously written.

Register 095H: WILC Transmit Status and FIFO Synch Register

Bit	Type	Function	Default
Bit 15	R	TX_MSG_LVL_VALID	X
Bit 14	R	TX_LINK[1]	0
Bit 14	R	TX_LINK[0]	0
Bit 12	R	IPAGE[1]	X
Bit 11	R	IPAGE[0]	X
Bit 10	R	IUSER[2]	X
Bit 9	R	IUSER[1]	0
Bit 8	R	IUSER[0]	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	TX_MSG_LVL[3]	0
Bit 4	R	TX_MSG_LVL[2]	0
Bit 3	R	TX_MSG_LVL[1]	0
Bit 2	R	TX_MSG_LVL[0]	0
Bit 1	R	TX_FI_BUSY	0
Bit 0	W	TX_XFER_SYNC	0

TX_XFER_SYNC

Writing ‘1’ to this bit initializes the next write sequence to be to the beginning of the next message. After a ‘1’ had been written successive writes to the Transmit FIFO will be to location zero of the next available slot. If a partial message has been written, TX_XFER_SYNC indicates that the current message is complete and that subsequent writes will be to the next message. If more than 32 bytes are written, the 33rd byte will be the first byte of the next message. The purpose of this bit is to unambiguously align the message boundaries. Another use would be to abandon the current write and move the write pointer to the beginning of the next message. (Previous message data will remain in the unwritten portion of the message being abandoned, which will have to be ignored by the receiving software).

If the message FIFO pointers are already at a message boundary then writing this bit to a ‘1’ will have no affect.

On reads this bit is always returned as a ‘0’.

TX_FI_BUSY

This bit indicates that the internal hardware is transferring the data from the Transmit FIFO registers (TDAT) into the internal RAM. This bit need not be read by software if the time interval between successive 32 bit transfers is greater than 3 SYSCLK cycles.

TX_MSG_LVL[3:0]

This indicates the current number of messages in the TXFIFO.

TX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur. The number of free messages available in the FIFO is given by 8 – TX_MSG_LVL. The TX_MSG_LVL_VALID bit must be polled before reading these bits.

IUSER[2:0]

These bits are a reflection of the USER[2:0] bits output in the header of the in-band link on the Transmit Working Serial Link. IUSER[2] is sourced from the IUSER2 input to the SBS. IUSER[1:0] is sourced from the TXWUSER[1:0] bits of register 008H.

IPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits output in the header of the in-band link on the Transmit Working Serial Link. PAGE[1] reflects the current memory page used by the IMSU. PAGE[0] reflects the current memory page used by the OMSU.

TX_LINK[1:0]

These bits reflect the last written value of the TX_LINK[1:0] field of the WILC Transmit Control Register. The upper byte of this register therefore reflects all of the configurable bits of the message Header1 byte.

TX_MSG_LVL_VALID

This bit indicates that the value of TX_MSG_LVL is valid. When read with a logic 0 this register should be re-read until TX_MSG_LVL_VALID is a logic 1. This bit will be clear for only approximately 0.12% of the time. This bit must always be polled before reading the TX_MSG_LVL bits.

Register 096H: WILC Receive FIFO Data High

Bit	Type	Function	Default
Bit 15	R	RDAT[31]	0
Bit 14	R	RDAT[30]	0
Bit 14	R	RDAT[29]	0
Bit 12	R	RDAT[28]	0
Bit 11	R	RDAT[27]	0
Bit 10	R	RDAT[26]	0
Bit 9	R	RDAT[25]	0
Bit 8	R	RDAT[24]	0
Bit 7	R	RDAT[23]	0
Bit 6	R	RDAT[22]	0
Bit 5	R	RDAT[21]	0
Bit 4	R	RDAT[20]	0
Bit 3	R	RDAT[19]	0
Bit 2	R	RDAT[18]	0
Bit 1	R	RDAT[17]	0
Bit 0	R	RDAT[16]	0

When reading data out of the receive FIFO, this register must be read before register 097H.

RDAT[31:16]

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages. This register must be read before register 097H.

Register 097H: WILC Receive FIFO Data Low

Bit	Type	Function	Default
Bit 15	R	RDAT[15]	0
Bit 14	R	RDAT[14]	0
Bit 14	R	RDAT[13]	0
Bit 12	R	RDAT[12]	0
Bit 11	R	RDAT[11]	0
Bit 10	R	RDAT[10]	0
Bit 9	R	RDAT[9]	0
Bit 8	R	RDAT[8]	0
Bit 7	R	RDAT[7]	0
Bit 6	R	RDAT[6]	0
Bit 5	R	RDAT[5]	0
Bit 4	R	RDAT[4]	0
Bit 3	R	RDAT[3]	0
Bit 2	R	RDAT[2]	0
Bit 1	R	RDAT[1]	0
Bit 0	R	RDAT[0]	0

Reading this register initiates a read access to the next location in the receive FIFO.

RDAT[15:0]

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

Register 099H: WILC Receive FIFO Control Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RX_CRC_SWIZ_EN	0
Bit 0	R/W	RX_BYPASS	0

RX_BYPASS

When this bit is set to a logic 1. The WILC's message receive functions are bypassed and no messages are extracted from the Receive Working Serial Link. The receive message FIFO RAM is disabled and thus message data reads will return undefined data.

RX_CRC_SWIZ_EN

When this bit is set to a logic 1, the calculated CRC-16 is bit reversed before being compared with CRC-16 bytes of the received message. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality

Reserved

This bit should be set to a logic 1 for proper operation of the WILC.

Register 09AH: WILC Receive Auxiliary Register

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	RX_AUX[7]	0
Bit 6	R	RX_AUX[6]	0
Bit 5	R	RX_AUX[5]	0
Bit 4	R	RX_AUX[4]	0
Bit 3	R	RX_AUX[3]	0
Bit 2	R	RX_AUX[2]	0
Bit 1	R	RX_AUX[1]	0
Bit 0	R	RX_AUX[0]	0

RX_AUX[7:0]

These bits constitute the output from an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers' discretion. A read from this register will return the AUX header byte of the last message received (without a CRC-16 error).

RX_STTS_VALID

This bit indicates that the value of RX_AUX is valid. When read with a '0' this register should be re-read until RX_STTS_VALID is a '1'. This bit will be cleared for less than 0.15% of the time.

Register 09BH: WILC Receive Status and FIFO Synch Register

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14	R	RX_LINK[1]	0
Bit 13	R	RX_LINK[0]	0
Bit 12	R	OPAGE[1]	0
Bit 11	R	OPAGE[0]	0
Bit 10	R	OUSER[2]	0
Bit 9	R	OUSER[1]	0
Bit 8	R	OUSER[0]	0
Bit 7	R	CRC_ERR	0
Bit 6	R	HDR_CRC_ERR	0
Bit 5	R	RX_MSG_LVL[3]	0
Bit 4	R	RX_MSG_LVL[2]	0
Bit 3	R	RX_MSG_LVL[1]	0
Bit 2	R	RX_MSG_LVL[0]	0
Bit 1	R	RX_FI_BUSY	0
Bit 0	R	RX_SYNC_DONE	X
Bit 0	W	RX_XFER_SYNC	0

When this register is read, it returns the status for the Receive Message Channel. When a logic 1 is written into bit 0 of this register, it is used to synchronize the Receive FIFO to the start of a message boundary or perform a message skip.

RX_XFER_SYNC

Writing a logic 1 to this bit initiates a read sequence from the start of the next *unread* message. The hardware aligns the message read buffer address to the start of the next *unread* message and prefetches the first Dword from the *unread* message buffer so that it is ready to be read from the WILC Receive FIFO Data registers.

An *unread* message in this context means that the s/w has not read any of the message payload data by reading the WILC Receive FIFO Data registers.

After the RX XFER SYNC process has been completed successive reads from the Receive FIFO return the last Dword read from the Receive FIFO and prefetch the next Dword (when available).

This bit must be written to a logic 1 at the start of a message read sequence.

When multiple complete messages are being read (software knows that there is more than one message in the FIFO using the RX_MSG_LVL bits) this bit does not need to be written between individual message reads. It must be written for the 1st message.

When software uses a variable length message protocol it may want to abandon reading a message buffer before reading the entire message buffer of 8 DWords (16 Words). In this case this bit must be written with a '1' to move the message pointer to the start of the next message buffer before starting the read of that buffer.

After writing this bit with a logic 1 software should not start reading the FIFO until the RX_FI_BUSY bit has cleared. In the worst case this will take 4 SYSCLK cycles.

At this point the 1st DWORD of the message is available for reading and the CRC_ERR bit is valid. Software may abandon a CRC errored message without reading the message buffer by writing this bit with a logic 1 again.

Whenever the RW8D block is not in frame or character alignment, the WILC will be receiving random data and the WILC receive message FIFO will be filled with this random data. Once the RW8D is in character alignment and in frame alignment (OCAV and OFAV in register 0C0H are low), this bit should be written to 16 times before attempting to use the WILC. This will flush out the receive message FIFO.

On reads this bit always returns the RX_SYNC_DONE status.

RX_SYNC_DONE

This bit indicates the status of an RX_XFER_SYNC operation. When this bit is a logic 1 it indicates that an RX_XFER_SYNC has been done. S/W should check this bit at the start of a message read sequence or when attempting to perform a message skip sequence.

RX_FI_BUSY

This bit indicates that the internal hardware is transferring data from the Receive FIFO RAM into the Receive FIFO registers. The bit is set following a write to this register with the RX_XFER_SYNC bit set or following a read from the WILC Receive FIFO Data Low register.

Following an RX_XFER_SYNC write this bit need not be read by software if

the time interval to the successive Receive FIFO DATA register read is greater than approximately 4 SYSCLK cycles.

This bit need not be read by software if the time interval between successive Receive FIFO DATA register reads greater than approximately 3 SYSCLK cycles.

This means between a read access from the WILC Received FIFO Data Low register and a read from the WILC Received FIFO Data High register. Note that there is no time restriction between a read accesses from the WILC Received FIFO Data High register and a read from the WILC Received FIFO Data Low register

RX_MSG_LVL[3:0]

This indicates the current number of messages in the Receive FIFO.

RX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur.

HDR_CRC_ERR

If this bit is set to a logic 1, the last message slot received was received with an errored CRC-16 field. This bits is updated every message slot. This bit is provided as status only.

CRC_ERR

If this bit it set to ‘1’, the message at the head of the Receive FIFO has an errored CRC-16 field.

The usual sequence would be to read this register before reading the message buffer to check if the message buffer that will be read from next has been received with a CRC error. If a Receive FIFO Synchronization has been started the value of this bit is invalid until the RX_XFER_SYNC operation has completed. This bit is valid when RX_FI_BUSY is a logic 0 following a Receive FIFO Synchronization. The software must only check the status of this bit before reading the first word of a message from the receive FIFO.

OUSER[2:0]

These bits are a reflection of the USER[2:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link. OUSER[2] is output from the SBS on OUSER2 when the Working Serial Link is selected.

OPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link. When the Working Serial Link is selected, OPAGE[1] controls the active page of the IMSU and OPAGE[0] controls the active page of the OMSU.

RX_LINK[1:0]

These bits are a reflection of the LINK[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link.

RX_STTS_VALID

This bit indicates that the values of RX_MSG_LVL , RX_LINK, OPAGE, and OUSER are valid. When read with a logic 0 this register should be re-read until RX_STTS_VALID is a logic 1. This bit will be cleared for only approximately 0.15% of time.

Register 09DH: WILC Interrupt Enable and Control Register.

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R/W	RX_TIMEOUT_VAL[1]	0
Bit 11	R/W	RX_TIMEOUT_VAL[0]	0
Bit 10	R/W	RX_THRESHOLD_VAL[2]	1
Bit 9	R/W	RX_THRESHOLD_VAL[1]	0
Bit 8	R/W	RX_THRESHOLD_VAL[0]	1
Bit 7	R	Unused	0
Bit 6	R/W	RX_TIMEOUTE	0
Bit 5	R/W	RX_THRSHLDE	0
Bit 4	R/W	RX_OVFLWE	0
Bit 3	R/W	RX_LINK_CHGE	0
Bit 2	R/W	OPAGE_CHGE[1]	0
Bit 1	R/W	OPAGE_CHGE[0]	0
Bit 0	R/W	OUSER0_CHGE	0

OUSER0_CHGE

Writing a logic 1 to the RX_OUSER0_CHGE bit enables the generation of an interrupt on a change of state from a logic 0 to a logic 1 of received message header bit OUSER[0].

OPAGE_CHGE[1:0]

Writing a logic 1 to the OPAGE_CHGE[n] bit enables the generation of an interrupt on a change of state of the received PAGE bits. The OPAGE bits that changed value are indicated by a logic 1 in the corresponding OPAGE_CHGI[n].

RX_LINK_CHGE

Writing a logic 1 to the RX_LINK_CHGE bit enables the generation of an interrupt on a change of state of the received LINK bits. When either of the received LINK bits has changed value the RX_LINK_CHGI bit will be set to a logic 1.

RX_OVFLWE

Writing a logic 1 to the RX_OVFLWE bit enables the generation of an interrupt when RX_OVFLWI is a logic 1.

RX_THRSHLDE

Writing a logic 1 to the RX_THRSHLDE bit enables the generation of an interrupt when RX_THRSHLDI is a logic 1.

RX_TIMEOUTE

Writing a logic 1 to the RX_TIMEOUTE bit enables the generation of an interrupt when RX_TIMEOUTI is a logic 1.

RX_THRESHOLD_VAL[2:0]

Variable Threshold dictates the minimum number of messages required to be in the RXFIFO before an interrupt is generated. '000' = 1 message '111' = 8 messages.

RX_THRESHOLD_VAL[2:0]	Messages
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

RX_TIMEOUT_VAL[1:0]

These bits specify a variable delay, relative to a read from the receive message FIFO, in steps of 125 us, before an interrupt is generated, if the Receive FIFO level is greater than 0. The objective is to stop stale messages collecting in the RXFIFO.

RX_TIMEOUT_VAL[1:0]	Nominal Delay In Frames	Minimum Delay from Message Reception	Maximum Delay from Message Reception	Minimum Delay from FIFO read	Maximum Delay from FIFO read
00	1	152µs	222µs	125µs	250µs
01	2	277µs	347µs	250µs	375µs
10	3	402µs	472µs	375µs	500µs
11	4	527µs	597µs	500µs	625µs

Register 09FH: WILC Interrupt Reason Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	RX_TIMEOUTI	0
Bit 5	R	RX_THRSHLDI	0
Bit 4	R	RX_OVFLWI	0
Bit 3	R	RX_LINK_CHGI	0
Bit 2	R	OPAGE_CHGI[1]	0
Bit 1	R	OPAGE_CHGI[0]	0
Bit 0	R	OUSER0_CHGI	0

This register contains the status of events that may be enabled to generate interrupts..

All bits in this register are cleared on read.

OUSER0_CHGI

A logic 1 in this bit indicates that the last received value of the OUSER[0] header bit has changed from a ‘0’ to a ‘1’ from the previously received values. This bit is cleared on a read.

OPAGE_CHGI[1:0]

A logic 1 in these bits indicates that the last received value of the corresponding OPAGE[1:0] header bits has changed from the previously received values. These bits are cleared on read.

RX_LINK_CHGI

A logic 1 in this bit indicates that the last received value of the LINK[1:0] header bits has changed from the previously received values. This bit is cleared on a read.

RX_OVFLWI

A logic 1 in this bit indicates that a Receive FIFO Overflow has occurred. This bit is cleared on a read.

RX_THRSHLDI

A logic 1 in this bit indicates that the Receive FIFO Threshold has been reached. This bit is cleared on a read.

RX_TIMEOUTI

A logic 1 in this bit indicates a Receive FIFO Timeout. This bit is cleared on read.

Register 0A0H: PILC Transmit FIFO Data High

Bit	Type	Function	Default
Bit 15	R/W	TDAT[31]	0
Bit 14	R/W	TDAT[30]	0
Bit 13	R/W	TDAT[29]	0
Bit 12	R/W	TDAT[28]	0
Bit 11	R/W	TDAT[27]	0
Bit 10	R/W	TDAT[26]	0
Bit 9	R/W	TDAT[25]	0
Bit 8	R/W	TDAT[24]	0
Bit 7	R/W	TDAT[23]	0
Bit 6	R/W	TDAT[22]	0
Bit 5	R/W	TDAT[21]	0
Bit 4	R/W	TDAT[20]	0
Bit 3	R/W	TDAT[19]	0
Bit 2	R/W	TDAT[18]	0
Bit 1	R/W	TDAT[17]	0
Bit 0	R/W	TDAT[16]	0

When writing data to the transmit FIFO, this register must be written to before register 0A1H.

TDAT[31:16]

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

Register 0A1H: PILC Transmit FIFO Data Low

Bit	Type	Function	Default
Bit 15	R/W	TDAT[15]	0
Bit 14	R/W	TDAT[14]	0
Bit 13	R/W	TDAT[13]	0
Bit 12	R/W	TDAT[12]	0
Bit 11	R/W	TDAT[11]	0
Bit 10	R/W	TDAT[10]	0
Bit 9	R/W	TDAT[9]	0
Bit 8	R/W	TDAT[8]	0
Bit 7	R/W	TDAT[7]	0
Bit 6	R/W	TDAT[6]	0
Bit 5	R/W	TDAT[5]	0
Bit 4	R/W	TDAT[4]	0
Bit 3	R/W	TDAT[3]	0
Bit 2	R/W	TDAT[2]	0
Bit 1	R/W	TDAT[1]	0
Bit 0	R/W	TDAT[0]	0

Writing to this register will initiate a transfer of TDAT[31:0] into the transmit FIFO.

TDAT[15:0]

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

Register 0A3H: PILC Transmit Control Register

Bit	Type	Function	Default
Bit 15	R/W	TX_AUX[7]	0
Bit 14	R/W	TX_AUX[6]	0
Bit 13	R/W	TX_AUX[5]	0
Bit 12	R/W	TX_AUX[4]	0
Bit 11	R/W	TX_AUX[3]	0
Bit 10	R/W	TX_AUX[2]	0
Bit 9	R/W	TX_AUX[1]	0
Bit 8	R/W	TX_AUX[0]	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R/W	TX_LINK[1]	0
Bit 4	R/W	TX_LINK[0]	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	TX_CRC_SWIZ_EN	0
Bit 0	R/W	TX_BYPASS	0

TX_BYPASS

When this bit is set to ‘1’, the blocks message transmit functions are bypassed. No messages are inserted into the Transmit data. The transmit message FIFO RAM is disabled and thus message data writes are ignored.

TX_CRC_SWIZ_EN

When this bit is set to ‘1’, the calculated CRC-16 is bit reversed before being transmitted. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality.

TX_LINK[1:0]

These bits are transmitted in the LINK bits of the message header of the next available message. On reads these bit return the last written value.

TX_AUX[7:0]

These bits form the input to an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developer’s discretion. Data written to this register will be transmitted in the AUX header byte of each subsequent message to the other end of the in-band link. A new value of TX_AUX will be transmitted at the next available message. Data read from this register will be the data previously written.

Register 0A5H: PILC Transmit Status and FIFO Synch Register

Bit	Type	Function	Default
Bit 15	R	TX_MSG_LVL_VALID	X
Bit 14	R	TX_LINK[1]	0
Bit 13	R	TX_LINK[0]	0
Bit 12	R	IPAGE[1]	X
Bit 11	R	IPAGE[0]	X
Bit 10	R	IUSER[2]	X
Bit 9	R	IUSER[1]	0
Bit 8	R	IUSER[0]	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	TX_MSG_LVL[3]	0
Bit 4	R	TX_MSG_LVL[2]	0
Bit3	R	TX_MSG_LVL[1]	0
Bit 2	R	TX_MSG_LVL[0]	0
Bit 1	R	TX_FI_BUSY	0
Bit 0	W	TX_XFER_SYNC	0

TX_XFER_SYNC

Writing ‘1’ to this bit initializes the next write sequence to be to the beginning of the next message. After a ‘1’ had been written successive writes to the Transmit FIFO will be to location zero of the next available slot. If a partial message has been written, TX_XFER_SYNC indicates that the current message is complete and that subsequent writes will be to the next message. If more than 32 bytes are written, the 33rd byte will be the first byte of the next message. The purpose of this bit is to unambiguously align the message boundaries. Another use would be to abandon the current write and move the write pointer to the beginning of the next message. (Previous message data will remain in the unwritten portion of the message being abandoned, which will have to be ignored by the receiving software).

If the message FIFO pointers are already at a message boundary then writing this bit to a ‘1’ will have no affect.

On reads this bit is always returned as a ‘0’.

TX_FI_BUSY

This bit indicates that the internal hardware is transferring the data from the Transmit FIFO registers (TDAT) into the internal RAM. This bit need not be read by software if the time interval between successive 32 bit transfers is greater than 3 SYSCLK cycles.

TX_MSG_LVL[3:0]

This indicates the current number of messages in the TXFIFO.

TX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur. The number of free messages available in the FIFO is given by 8 – TX_MSG_LVL. The TX_MSG_LVL_VALID bit must be polled before reading these bits.

IUSER[2:0]

These bits are a reflection of the USER[2:0] bits output in the header of the in-band link on the Transmit Protection Serial Link. IUSER[2] is sourced from the IUSER2 input to the SBS. IUSER[1:0] is sourced from the TXPUSER[1:0] bits of register 008H.

IPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits output in the header of the in-band link on the Transmit Protection Serial Link. PAGE[1] reflects the current memory page used by the IMSU. PAGE[0] reflects the current memory page used by the OMSU.

TX_LINK[1:0]

These bits reflect the last written value of the TX_LINK[1:0] field of the PILC Transmit Control Register. The upper byte of this register therefore reflects all of the configurable bits of the message Header1 byte.

TX_MSG_LVL_VALID

This bit indicates that the value of TX_MSG_LVL is valid. When read with a logic 0 this register should be re-read until TX_MSG_LVL_VALID is a logic 1. This bit will be clear for only approximately 0.12% of the time. This bit must always be polled before reading the TX_MSG_LVL bits.

Register 0A6H: PILC Receive FIFO Data High

Bit	Type	Function	Default
Bit 15	R	RDAT[31]	0
Bit 14	R	RDAT[30]	0
Bit 13	R	RDAT[29]	0
Bit 12	R	RDAT[28]	0
Bit 11	R	RDAT[27]	0
Bit 10	R	RDAT[26]	0
Bit 9	R	RDAT[25]	0
Bit 8	R	RDAT[24]	0
Bit 7	R	RDAT[23]	0
Bit 6	R	RDAT[22]	0
Bit 5	R	RDAT[21]	0
Bit 4	R	RDAT[20]	0
Bit3	R	RDAT[19]	0
Bit 2	R	RDAT[18]	0
Bit 1	R	RDAT[17]	0
Bit 0	R	RDAT[16]	0

When reading data out of the receive FIFO, this register must be read before register 0A7H.

RDAT[31:16]

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages. This register must be read before register 097H.

Register 0A7H: PILC Receive FIFO Data Low

Bit	Type	Function	Default
Bit 15	R	RDAT[15]	0
Bit 14	R	RDAT[14]	0
Bit 13	R	RDAT[13]	0
Bit 12	R	RDAT[12]	0
Bit 11	R	RDAT[11]	0
Bit 10	R	RDAT[10]	0
Bit 9	R	RDAT[9]	0
Bit 8	R	RDAT[8]	0
Bit 7	R	RDAT[7]	0
Bit 6	R	RDAT[6]	0
Bit 5	R	RDAT[5]	0
Bit 4	R	RDAT[4]	0
Bit3	R	RDAT[3]	0
Bit 2	R	RDAT[2]	0
Bit 1	R	RDAT[1]	0
Bit 0	R	RDAT[0]	0

Reading this register initiates a read access to the next location in the receive FIFO.

RDAT[15:0]

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

Register 0A9H: PILC Receive FIFO Control Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit3	R	Unused	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RX_CRC_SWIZ_EN	0
Bit 0	R/W	RX_BYPASS	0

RX_BYPASS

When this bit is set to a logic 1. The PILC's message receive functions are bypassed and no messages are extracted from the Receive Working Serial Link. The receive message FIFO RAM is disabled and thus message data reads will return undefined data.

RX_CRC_SWIZ_EN

When this bit is set to a logic 1, the calculated CRC-16 is bit reversed before being compared with CRC-16 bytes of the received message. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality

Reserved

This bit should be set to a logic 1 for proper operation of the PILC.

Register 0AAH: PILC Receive Auxiliary Register

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	RX_AUX[7]	0
Bit 6	R	RX_AUX[6]	0
Bit 5	R	RX_AUX[5]	0
Bit 4	R	RX_AUX[4]	0
Bit 3	R	RX_AUX[3]	0
Bit 2	R	RX_AUX[2]	0
Bit 1	R	RX_AUX[1]	0
Bit 0	R	RX_AUX[0]	0

RX_AUX[7:0]

These bits constitute the output from an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers' discretion. A read from this register will return the AUX header byte of the last message received (without a CRC-16 error).

RX_STTS_VALID

This bit indicates that the value of RX_AUX is valid. When read with a '0' this register should be re-read until RX_STTS_VALID is a '1'. This bit will be cleared for less than 0.15% of the time.

Register 0ABH: PILC Receive Status and FIFO Synch Register

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14	R	RX_LINK[1]	0
Bit 13	R	RX_LINK[0]	0
Bit 12	R	OPAGE[1]	0
Bit 11	R	OPAGE[0]	0
Bit 10	R	OUSER[2]	0
Bit 9	R	OUSER[1]	0
Bit 8	R	OUSER[0]	0
Bit 7	R	CRC_ERR	0
Bit 6	R	HDR_CRC_ERR	0
Bit 5	R	RX_MSG_LVL[3]	0
Bit 4	R	RX_MSG_LVL[2]	0
Bit 3	R	RX_MSG_LVL[1]	0
Bit 2	R	RX_MSG_LVL[0]	0
Bit 1	R	RX_FI_BUSY	0
Bit 0	R	RX_SYNC_DONE	X
Bit 0	W	RX_XFER_SYNC	0

When this register is read, it returns the status for the Receive Message Channel. When a logic 1 is written into bit 0 of this register, it is used to synchronize the Receive FIFO to the start of a message boundary or perform a message skip.

RX_XFER_SYNC

Writing a logic 1 to this bit initiates a read sequence from the start of the next *unread* message. The hardware aligns the message read buffer address to the start of the next *unread* message and prefetches the first Dword from the *unread* message buffer so that it is ready to be read from the WILC Receive FIFO Data registers.

An *unread* message in this context means that the s/w has not read any of the message payload data by reading the WILC Receive FIFO Data registers.

After the RX XFER SYNC process has been completed successive reads from the Receive FIFO return the last Dword read from the Receive FIFO and prefetch the next Dword (when available).

This bit must be written to a logic 1 at the start of a message read sequence.

When multiple complete messages are being read (software knows that there is more than one message in the FIFO using the RX_MSG_LVL bits) this bit does not need to be written between individual message reads. It must be written for the 1st message.

When software uses a variable length message protocol it may want to abandon reading a message buffer before reading the entire message buffer of 8 DWords (16 Words). In this case this bit must be written with a '1' to move the message pointer to the start of the next message buffer before starting the read of that buffer.

After writing this bit with a logic 1 software should not start reading the FIFO until the RX_FI_BUSY bit has cleared. In the worst case this will take 4 SYSCLK cycles.

At this point the 1st DWORD of the message is available for reading and the CRC_ERR bit is valid. Software may abandon a CRC errored message without reading the message buffer by writing this bit with a logic 1 again.

Whenever the RP8D block is not in frame or character alignment, the PILC will be receiving random data and the PILC receive message FIFO will be filled with this random data. Once the RP8D is in character alignment and in frame alignment (OCAV and OFAV in register 0C8H are low), this bit should be written to 16 times before attempting to use the PILC. This will flush out the receive message FIFO.

On reads this bit always returns the RX_SYNC_DONE status.

RX_SYNC_DONE

This bit indicates the status of an RX_XFER_SYNC operation. When this bit is a logic 1 it indicates that an RX_XFER_SYNC has been done. S/W should check this bit at the start of a message read sequence or when attempting to perform a message skip sequence.

RX_FI_BUSY

This bit indicates that the internal hardware is transferring data from the Receive FIFO RAM into the Receive FIFO registers. The bit is set following a write to this register with the RX_XFER_SYNC bit set or following a read from the PILC Receive FIFO Data Low register.

Following an RX_XFER_SYNC write this bit need not be read by software if

the time interval to the successive Receive FIFO DATA register read is greater than approximately 4 SYSCLK cycles.

This bit need not be read by software if the time interval between successive Receive FIFO DATA register reads greater than approximately 3 SYSCLK cycles.

This means between a read access from the PILC Received FIFO Data Low register and a read from the PILC Received FIFO Data High register. Note that there is no time restriction between a read accesses from the PILC Received FIFO Data High register and a read from the PILC Received FIFO Data Low register

RX_MSG_LVL[3:0]

This indicates the current number of messages in the Receive FIFO.

RX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur.

HDR_CRC_ERR

If this bit is set to a logic 1, the last message slot received was received with an errored CRC-16 field. This bits is updated every message slot. This bit is provided as status only.

CRC_ERR

If this bit it set to ‘1’, the message at the head of the Receive FIFO has an errored CRC-16 field.

The usual sequence would be to read this register before reading the message buffer to check if the message buffer that will be read from next has been received with a CRC error. If a Receive FIFO Synchronization has been started the value of this bit is invalid until the RX_XFER_SYNC operation has completed. This bit is valid when RX_FI_BUSY is a logic 0 following a Receive FIFO Synchronization. The software must only check the status of this bit before reading the first word of a message from the receive FIFO.

OUSER[2:0]

These bits are a reflection of the USER[2:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Protection Serial Link. OUSER[2] is output from the SBS on OUSER2 when the Protection Serial Link is selected.

OPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Protection Serial Link. When the Protection Serial Link is selected, OPAGE[1] controls the active page of the IMSU and OPAGE[0] controls the active page of the OMSU.

RX_LINK[1:0]

These bits are a reflection of the LINK[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Protection Serial Link.

RX_STTS_VALID

This bit indicates that the values of RX_MSG_LVL , RX_LINK, OPAGE, and OUSER are valid. When read with a logic 0 this register should be re-read until RX_STTS_VALID is a logic 1. This bit will be cleared for only approximately 0.15% of time.

Register 0ADH: PILC Interrupt Enable and Control Register.

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R/W	RX_TIMEOUT_VAL[1]	0
Bit 11	R/W	RX_TIMEOUT_VAL[0]	0
Bit 10	R/W	RX_THRESHOLD_VAL[2]	1
Bit 9	R/W	RX_THRESHOLD_VAL[1]	0
Bit 8	R/W	RX_THRESHOLD_VAL[0]	1
Bit 7	R	Unused	0
Bit 6	R/W	RX_TIMEOUTE	0
Bit 5	R/W	RX_THRSHLDE	0
Bit 4	R/W	RX_OVFLWE	0
Bit 3	R/W	RX_LINK_CHGE	0
Bit 2	R/W	OPAGE_CHGE[1]	0
Bit 1	R/W	OPAGE_CHGE[0]	0
Bit 0	R/W	OUSER0_CHGE	0

OUSER0_CHGE

Writing a logic 1 to the RX_OUSER0_CHGE bit enables the generation of an interrupt on a change of state from a logic 0 to a logic 1 of received message header bit OUSER[0].

OPAGE_CHGE[1:0]

Writing a logic 1 to the OPAGE_CHGE[n] bit enables the generation of an interrupt on a change of state of the received PAGE bits. The OPAGE bits that changed value are indicated by a logic 1 in the corresponding OPAGE_CHGI[n].

RX_LINK_CHGE

Writing a logic 1 to the RX_LINK_CHGE bit enables the generation of an interrupt on a change of state of the received LINK bits. When either of the received LINK bits has changed value the RX_LINK_CHGI bit will be set to a logic 1.

RX_OVFLWE

Writing a logic 1 to the RX_OVFLWE bit enables the generation of an interrupt when RX_OVFLWI is a logic 1.

RX_THRSHLDE

Writing a logic 1 to the RX_THRSHLDE bit enables the generation of an interrupt when RX_THRSHLDI is a logic 1.

RX_TIMEOUTE

Writing a logic 1 to the RX_TIMEOUTE bit enables the generation of an interrupt when RX_TIMEOUTI is a logic 1.

RX_THRESHOLD_VAL[2:0]

Variable Threshold dictates the minimum number of messages required to be in the RXFIFO before an interrupt is generated. '000' = 1 message '111' = 8 messages.

RX_THRESHOLD_VAL[2:0]	Messages
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

RX_TIMEOUT_VAL[1:0]

These bits specify a variable delay, relative to a read from the receive message FIFO, in steps of 125 us, before an interrupt is generated, if the Receive FIFO level is greater than 0. The objective is to stop stale messages collecting in the RXFIFO.

RX_TIMEOUT_VAL[1:0]	Nominal Delay In Frames	Minimum Delay from Message Reception	Maximum Delay from Message Reception	Minimum Delay from FIFO read	Maximum Delay from FIFO read
00	1	152µs	222µs	125µs	250µs
01	2	277µs	347µs	250µs	375µs
10	3	402µs	472µs	375µs	500µs
11	4	527µs	597µs	500µs	625µs

Register 0AFH: PILC Interrupt Reason Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	RX_TIMEOUTI	0
Bit 5	R	RX_THRSHLDI	0
Bit 4	R	RX_OVFLWI	0
Bit 3	R	RX_LINK_CHGI	0
Bit 2	R	OPAGE_CHGI[1]	0
Bit 1	R	OPAGE_CHGI[0]	0
Bit 0	R	OUSER0_CHGI	0

This register contains the status of events that may be enabled to generate interrupts.

All bits in this register are cleared on read.

OUSER0_CHGI

A logic 1 in this bit indicates that the last received value of the OUSER[0] header bit has changed from a ‘0’ to a ‘1’ from the previously received values. This bit is cleared on a read.

OPAGE_CHGI[1:0]

A logic 1 in these bits indicates that the last received value of the corresponding OPAGE[1:0] header bits has changed from the previously received values. These bits are cleared on read.

RX_LINK_CHGI

A logic 1 in this bit indicates that the last received value of the LINK[1:0] header bits has changed from the previously received values. This bit is cleared on a read.

RX_OVFLWI

A logic 1 in this bit indicates that a Receive FIFO Overflow has occurred. This bit is cleared on a read.

RX_THRSHLDI

A logic 1 in this bit indicates that the Receive FIFO Threshold has been reached. This bit is cleared on a read.

RX_TIMEOUTI

A logic 1 in this bit indicates a Receive FIFO Timeout. This bit is cleared on read.

Register 0B0H: TW8E Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the TW8E.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the working transmit serial data stream. When this bit is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that SBI and Telecom Bus control characters are not affected by the DLCV bit but are passed unaltered.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

This bit must be set once CSU lock has been achieved.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the working transmit serial data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the transmit data stream. When TPINS is set low, no test pattern is inserted.

FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) enables FIFO overrun/underrun interrupts. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic 1. No interrupt is generated if FIFOERRE if is set to logic 0.

Reserved

These bits must be set low for correct operation of the SBS.

Register 0B1H: TW8E Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due the detection of FIFO error.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. FIFOERRI is set to logic 0 when this register is read.

Note: the default value would only be seen immediately after a digital reset performed while the CSU is running and locked. If the CSU is disabled, or is in the process of locking, FIFO errors will be generated continually and a “1” value will appear in FIFOERRI bit almost immediately.

Register 0B2H: TW8E Time-slot Configuration #1

Bit	Type	Function	Default
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

This register configures the path termination mode of time-slots 1 to 8 of the TW8E.

TMODE1[1:0]-TMODE8[1:0]

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the TW8E. Time-slots are numbered in order of transmission on the working transmit serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-8) determines which set of Telecom bus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in Telecom Bus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in Telecom Bus mode where valid V1/V2 tributary pointers must be preserved and the location of the J1 byte is indicated on the IC1FP input.
1	0	LPT level. This mode must be used for SBI336 mode and in Telecom Bus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

Register 0B3H: TW8E Time-slot Configuration #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

This register configures the path termination mode of time-slots 9 to 12 of the TW8E.

TMODE9[1:0]-TMODE12[1:0]

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the TW8E. Time-slots are numbered in order of transmission on the working transmit serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 9-12) determines which set of Telecom bus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in Telecom Bus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in Telecom Bus mode where valid V1/V2 tributary pointers must be preserved and the location of the J1 byte is indicated on the IC1FP input.
1	0	LPT level. This mode must be used for SBI336 mode and in Telecom Bus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

Register 0B4H: TW8E Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

This register contains the test pattern to be inserted into the working transmit serial data stream.

TP[9:0]

The Test Pattern registers (TP[9:0]) contains the test pattern that is used to insert into the working transmit serial data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the transmit data stream.

Register 0B5H: TW8E Analog Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	ARSTB	1

This registers controls the analog blocks.

ARSTB

Setting this bit low will reset the TWPS and TWLV blocks.

PISO_ENB

Setting this bit high will disable the TWPS circuitry.

TXLV_ENB

Setting this bit high will disable the TWLV circuitry.

Reserved

The Reserved bits should not be modified.

Register 0B8H: TP8E Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the TP8E.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the protection transmit serial data stream. When this bit is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that SBI and Telecom Bus control characters are not affected by the DLCV bit but are passed unaltered.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

This bit must be set once CSU lock has been achieved.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the protection transmit serial data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the transmit data stream. When TPINS is set low, no test pattern is inserted.

FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) enables FIFO overrun/underrun interrupts. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic 1. No interrupt is generated if FIFOERRE if is set to logic 0.

Reserved

These bits must be set low for correct operation of the SBS.

Register 0B9H: TP8E Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due the detection of FIFO error.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. FIFOERRI is set to logic 0 when this register is read.

Note: the default value would only be seen immediately after a digital reset performed while the CSU is running and locked. If the CSU is disabled, or is in the process of locking, FIFO errors will be generated continually and a “1” value will appear in FIFOERRI bit almost immediately.

Register 0BAH: TP8E Time-slot Configuration #1

Bit	Type	Function	Default
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

This register configures the path termination mode of time-slots 1 to 8 of the TP8E.

TMODE1[1:0]-TMODE8[1:0]

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the TP8E. Time-slots are numbered in order of transmission on the protection transmit serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-8) determines which set of Telecom bus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in Telecom Bus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in Telecom Bus mode where valid V1/V2 tributary pointers must be preserved and the location of the J1 byte is indicated on the IC1FP input.
1	0	LPT level. This mode must be used for SBI336 mode and in Telecom Bus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

Register 0BBH: TP8E Time-slot Configuration #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

This register configures the path termination mode of time-slots 9 to 12 of the TP8E.

TMODE9[1:0]-TMODE12[1:0]

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the TW8E. Time-slots are numbered in order of transmission on the working protection serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 9-12) determines which set of Telecom bus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in Telecom Bus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in Telecom Bus mode where valid V1/V2 tributary pointers must be preserved and the location of the J1 byte is indicated on the IC1FP input.
1	0	LPT level. This mode must be used for SBI336 mode and in Telecom Bus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

Register 0BCH: TP8E Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

This register contains the test pattern to be inserted into the protection transmit serial data stream.

TP[9:0]

The Test Pattern registers (TP[9:0]) contains the test pattern that is used to insert into the protection transmit serial data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the transmit data stream.

Register 0BDH: TP8E Analog Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	ARSTB	1

This register controls the analog blocks.

ARSTB

Setting this bit low will reset the TPPS and TPLV blocks.

PISO_ENB

Setting this bit high will disable the TPPS circuitry.

TXLV_ENB

Setting this bit high will disable the TPLV circuitry.

Reserved

The Reserved bits should not be modified.

Register 0C0H: RW8D Control and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	RX_INV	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the RW8D.

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due of LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUOE is set low.

RX_INV

The recive incoming data invert bit (RX_INV) controls the active polarity of the parallel incoming data stream. When RX_INV is set high, the data is complemented before further processing by the SBSLITE. When RX_INV is set low, the data is not complemented.

Reserved

These bits must be set low for correct operation of the SBS.

Register 0C1H: RW8D Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due to change of character alignment, change of frame alignment, detection of line code violations, and FIFO overrun or underrun events in the RW8D.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

LCVI:

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one byte of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUOE bit the FUOI remains valid and may be polled to detect underrun/overrun events.

This bit may be set when the Receive Working link is disconnected.

Register 0C2H: RW8D LCV Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

This register reports the number of line code violations in the previous accumulation period in the RW8D.

LCV[15:0]

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing this register or by writing to the SBS Master Clock Monitor, Accumulation Trigger register. The write access transfers the internally accumulated error count to the LCV register within 6 SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0C3H: RW8D Analog Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	ARSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls the WDRU and RWLV analog blocks. Please refer to their respective documents for a description of the functionality of these bits.

Note: THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE RW8D BLOCKS. FOR DISABLING THIS RECEIVER, THIS REGISTER SHOULD BE SET TO F834H

DRU_ENB

Setting this bit high will disable the WDRU.

RX_ENB

Setting this bit high will disable the RWLV.

ARSTB

Setting this bit low will reset the WDRU and RWLV blocks.

Reserved

The Reserved bits should be set as described above.

Register 0C8H: RP8D Control and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	RX_INV	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the RP8D.

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due of LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUOE is set low.

RX_INV

The recive incoming data invert bit (RX_INV) controls the active polarity of the parallel incoming data stream. When RX_INV is set high, the data is complemented before further processing by the SBSLITE. When RX_INV is set low, the data is not complemented.

Reserved

These bits must be set low for correct operation of the SBS.

Register 0C9H: RP8D Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due to change of character alignment, change of frame alignment, detection of line code violations, and FIFO overrun or underrun events in the RP8D.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

LCVI:

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one byte of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUOE bit the FUOI remains valid and may be polled to detect underrun/overrun events.

This bit may be set when the Receive Protection link is disconnected.

Register 0CAH: RP8D LCV Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

This register reports the number of line code violations in the previous accumulation period in the RP8D.

LCV[15:0]

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing this register or by writing to the SBS Master Clock Monitor, Accumulation Trigger register. The write access transfers the internally accumulated error count to the LCV register within 6 SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0CBH: RP8D Analog Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	ARSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls the PDRU and RPLV analog blocks. Please refer to their respective documents for a description of the functionality of these bits.

Note: THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE RP8D BLOCK. FOR DISABLING THIS RECEIVER, THIS REGISTER SHOULD BE SET TO F834H

DRU_ENB

Setting this bit high will disable the PDRU.

RX_ENB

Setting this bit high will disable the RPLV.

ARSTB

Setting this bit low will reset the PDRU and RPLV blocks.

Reserved

The Reserved bits should be set as described above.

Register 0D0H: CSTR Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	CSU_RSTB	1
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	1

Reserved

The Reserved bits must be set to their default values for proper operation.

CSU_RSTB

The CSU_RSTB signal is a software reset signal that forces the CSU1250 into a reset. In order to properly reset the CSU, CSU_RSTB should be held low for at least 1 ms.

CSU_ENB

The active low CSU enable control signal (CSU_ENB) bit can be used to force the CSU1250 into low power configuration if it is set to logic 1. For normal operation, it is set to logic 0.

Register 0D1H: CSTR Configuration and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	LOCKV	X
Bit 0	R/W	LOCKE	0

LOCKV

The CSU lock status bit (LOCKV) indicates whether the clock synthesis unit has successfully locked with the reference clock. LOCKV is set low when the CSU has not successfully locked with the reference SYSCLK. LOCKV is set high when the CSU has locked with the reference SYSCLK.

LOCKE

The CSU lock interrupt enable bit (LOCKE) controls the assertion of CSU lock state interrupts by the CSTR. When LOCKE is high, an interrupt is generated when the CSU lock state changes. Interrupts due to CSU lock state are masked when LOCKE is set low.

Register 0D2H: CSTR Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOCKI	0

LOCKI

The CSU lock interrupt status bit (LOCKI) responds to changes in the CSU lock state. Interrupts are to be generated as the CSU achieves lock with the reference clock, or loses its lock to the reference clock. As a result, the LOCKI register bit is set high when any of these changes occurs. LOCKI register bit will be cleared when it is read. When LOCKE is set high, LOCKI is used to produce the interrupt output that is reflected in the SBS Master Interrupt Source register. Whether or not the interrupt is masked by the LOCKE bit, the LOCKI bit itself remains valid and may be polled to detect change of lock status events.

Register 0E0H: REFDLL Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	LOCK	0

The REFDLL Configuration Register controls the basic operation of the DLL connected to the SREFCLK input. The REFDLL is only used when SREFCLK is operating at 77.76MHz. This register should be ignored when SREFCLK is operating at 19.44MHz.

LOCK

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the SREFCLK and the DLL's reference clock. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates of zero phase offset between the SREFCLK and the reference clock for the first time.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

Reserved

These bits must be set to set low for correct operation of the SBS.

Register 0E2H: REFDLL Reset

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

The REFDLL Reset Register is used to reset the REFDLL.

Writing any value to this register performs a software reset of the REFDLL. A software reset requires a maximum of 24*256 SREFCLK cycles for the REFDLL to regain lock.

Reserved

The Reserved bits are read only and should be ignored by the user.

Register 0E3H: REFDLL Control Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	0
Bit 0	R	RUN	0

The REFDLL Control Status Register provides information on the operation of the DLL connected to the SREFCLK input. The REFDLL is only used when SREFCLK is operating at 77.76MHz. This register should be ignored when SREFCLK is operating at 19.44MHz.

NOTE: Because the clear-on-read ERRORI bit is located in this register, polling the register to check the status of the RUN bit may inadvertently clear a pending ERRORI interrupt. Care should be taken to handle this possibility in software, perhaps by examining the ERRORI bit and responding appropriately during read accesses. Clearing the ERRORI bit will not change the status of the ERROR bit, so it is also possible to simply poll the ERROR bit and ignore ERRORI.

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the reference clock and the rising edge of SREFLCK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset (RSTB), an SBS software reset (in the SBS Master Reset Register), or a REFDLL software reset (writing to register 0E2H).

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a output clock phase that causes the rising edge of the reference clock to be aligned to the rising edge of SREFCLK. ERROR is set low, when the DLL captures lock again. To recover from this condition, the REFDLL software reset should be activated by writing to register 0E2H.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INT output is also asserted when ERRORI asserts. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Reserved

The Reserved bits are read only and should be ignored by the user.

Register 0E8H: SYSDLL Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	LOCK	0

The SYSDLL Configuration Register controls the basic operation of the DLL connected to the SYSCLK input.

LOCK

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the SYSCLK input and the DLL's reference clock. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates of zero phase offset between SYSCLK and the reference clock for the first time.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

Reserved

These bits must be set to set low for correct operation of the SBS.

Register 0EAH: SYSDLL Reset

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

The SYSDLL Reset Register is used to reset the SYSDLL.

Writing any value to this register performs a software reset of the SYSDLL. A software reset requires a maximum of 24*256 SYSCLK cycles for the SYSDLL to regain lock.

Reserved

The Reserved bits are read only and should be ignored by the user.

Register 0EBH: SYSDLL Control Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	0
Bit 0	R	RUN	0

The SYSDLL Control Status Register provides information on the operation of the DLL connected to the SYSCLK input.

NOTE: Because the clear-on-read ERRORI bit is located in this register, polling the register to check the status of the RUN bit may inadvertently clear a pending ERRORI interrupt. Care should be taken to handle this possibility in software, perhaps by examining the ERRORI bit and responding appropriately during read accesses. Clearing the ERRORI bit will not change the status of the ERROR bit, so it is also possible to simply poll the ERROR bit and ignore ERRORI.

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the reference clock and the rising edge of SYSCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset (RSTB), an SBS software reset (in the SBS Master Reset Register), or a SYSDLL software reset (writing to register 0EAH).

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a output clock phase that causes the rising edge of the reference clock to be aligned to the rising edge of SYSCLK. ERROR is set low, when the DLL captures lock again. To recover from this condition, the SYSDLL software reset should be activated by writing to register 0EAH.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INT output is also asserted when ERRORI asserts. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Reserved

The Reserved bits are read only and should be ignored by the user.

12 Test Feature Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the SBS. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[8]) is high.

In addition, the SBS also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

12.1 JTAG Test Port

The SBS JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 24 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 25 Identification Register

Length	32 bits
Version Number	1H
Part Number	8610H
Manufacturer's Identification Code	0CDH
Device Identification	186100CDH

Table 26 Boundary Scan Register

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
IV5[4]	291	IN_CELL	L
ITAIS[4]	290	IN_CELL	L
ITPL[4]	289	IN_CELL	L
IC1FP[4]	288	IN_CELL	H
IPL[4]	287	IN_CELL	H
IDP[4]	286	IN_CELL	L
IDATA[4][7]	285	IN_CELL	L
IDATA[4][6]	284	IN_CELL	L
IDATA[4][5]	283	IN_CELL	L
IDATA[4][4]	282	IN_CELL	H
IDATA[4][3]	281	IN_CELL	H
IDATA[4][2]	280	IN_CELL	L
IDATA[4][1]	279	IN_CELL	L
IDATA[4][0]	278	IN_CELL	L
ITAIS[2]	277	IN_CELL	L
ITPL[2]	276	IN_CELL	H
IC1FP[2]	275	IN_CELL	L
ALE	274	IN_CELL	L
RDB	273	IN_CELL	L
WRB	272	IN_CELL	L
CSB	271	IN_CELL	L
RWSEL	270	IN_CELL	L
RSTB	269	IN_CELL	L
RC1FP	268	IN_CELL	L
OEB_OACTIVE[4]	267	OUT_CELL	H
OACTIVE[4]	266	OUT_CELL	H
ODETECT[4]	265	IN_CELL	L
OEB_JUST_REQ[4]	264	OUT_CELL	L
JUST_REQ[4]	263	IO_CELL	H
OEB_OC1FP[4]	262	OUT_CELL	H
OC1FP[4]	261	OUT_CELL	L
OEB_OTAIS[4]	260	OUT_CELL	H
OTAIS[4]	259	OUT_CELL	-
OEB_OV5[4]	258	OUT_CELL	-
OV5[4]	257	OUT_CELL	-
OEB_OTPL[4]	256	OUT_CELL	-
OTPL[4]	255	OUT_CELL	-
OEB_OPL[4]	254	OUT_CELL	-
OPL[4]	253	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
OEB_ODP[4]	252	OUT_CELL	-
ODP[4]	251	OUT_CELL	-
OEB_D[15]	250	OUT_CELL	-
D[15]	249	IO_CELL	-
OEB_D[14]	248	OUT_CELL	-
D[14]	247	IO_CELL	-
OEB_ODATA[4][7]	246	OUT_CELL	-
ODATA[4][7]	245	OUT_CELL	-
OEB_ODATA[4][6]	244	OUT_CELL	-
ODATA[4][6]	243	OUT_CELL	-
OEB_ODATA[4][5]	242	OUT_CELL	-
ODATA[4][5]	241	OUT_CELL	-
OEB_ODATA[4][4]	240	OUT_CELL	-
ODATA[4][4]	239	OUT_CELL	-
OEB_ODATA[4][3]	238	OUT_CELL	-
ODATA[4][3]	237	OUT_CELL	-
OEB_ODATA[4][2]	236	OUT_CELL	-
ODATA[4][2]	235	OUT_CELL	-
OEB_ODATA[4][1]	234	OUT_CELL	-
ODATA[4][1]	233	OUT_CELL	-
OEB_ODATA[4][0]	232	OUT_CELL	-
ODATA[4][0]	231	OUT_CELL	-
USER_IN	230	IN_CELL	-
OEB_D[13]	229	OUT_CELL	-
D[13]	228	IO_CELL	-
OEB_D[12]	227	OUT_CELL	-
D[12]	226	IO_CELL	-
OEB_D[11]	225	OUT_CELL	-
D[11]	224	IO_CELL	-
OEB_D[10]	223	OUT_CELL	-
D[10]	222	IO_CELL	-
OEB_D[9]	221	OUT_CELL	-
D[9]	220	IO_CELL	-
IV5[2]	219	IN_CELL	-
IPL[2]	218	IN_CELL	-
IDP[2]	217	IN_CELL	-
IDATA[2][7]	216	IN_CELL	-
IDATA[2][6]	215	IN_CELL	-
IDATA[2][5]	214	IN_CELL	-
IDATA[2][4]	213	IN_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
IDATA[2][3]	212	IN_CELL	-
IDATA[2][2]	211	IN_CELL	-
IDATA[2][1]	210	IN_CELL	-
IDATA[2][0]	209	IN_CELL	-
OEB_D[8]	208	OUT_CELL	-
D[8]	207	IO_CELL	-
OEB_D[7]	206	OUT_CELL	-
D[7]	205	IO_CELL	-
IV5[3]	204	IN_CELL	-
ITAIS[3]	203	IN_CELL	-
ITPL[3]	202	IN_CELL	-
IC1FP[3]	201	IN_CELL	-
IPL[3]	200	IN_CELL	-
IDP[3]	199	IN_CELL	-
IDATA[3][7]	198	IN_CELL	-
OEB_D[6]	197	OUT_CELL	-
D[6]	196	IO_CELL	-
OEB_D[5]	195	OUT_CELL	-
D[5]	194	IO_CELL	-
OEB_D[4]	193	OUT_CELL	-
D[4]	192	IO_CELL	-
IDATA[3][6]	191	IN_CELL	-
IDATA[3][5]	190	IN_CELL	-
IDATA[3][4]	189	IN_CELL	-
IDATA[3][3]	188	IN_CELL	-
IDATA[3][2]	187	IN_CELL	-
OEB_D[3]	186	OUT_CELL	-
D[3]	185	IO_CELL	-
OEB_D[2]	184	OUT_CELL	-
D[2]	183	IO_CELL	-
OEB_D[1]	182	OUT_CELL	-
D[1]	181	IO_CELL	-
OEB_D[0]	180	OUT_CELL	-
D[0]	179	IO_CELL	-
A[8]	178	IN_CELL	-
A[7]	177	IN_CELL	-
A[6]	176	IN_CELL	-
A[5]	175	IN_CELL	-
A[4]	174	IN_CELL	-
A[3]	173	IN_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
A[2]	172	IN_CELL	-
A[1]	171	IN_CELL	-
IDATA[3][1]	170	IN_CELL	-
IDATA[3][0]	169	IN_CELL	-
OEB_JUST_REQ[3]	168	OUT_CELL	-
JUST_REQ[3]	167	IO_CELL	-
A[0]	166	IN_CELL	-
OEB_USER_OUT	165	OUT_CELL	-
USER_OUT	164	OUT_CELL	-
OEB_JUST_REQ[1]	163	OUT_CELL	-
JUST_REQ[1]	162	IO_CELL	-
OEB_OC1FP[3]	161	OUT_CELL	-
OC1FP[3]	160	OUT_CELL	-
OEB_OTAIS[3]	159	OUT_CELL	-
OTAIS[3]	158	OUT_CELL	-
OEB_OV5[3]	157	OUT_CELL	-
OV5[3]	156	OUT_CELL	-
OEB_OTPL[3]	155	OUT_CELL	-
OTPL[3]	154	OUT_CELL	-
OEB_OPL[3]	153	OUT_CELL	-
OPL[3]	152	OUT_CELL	-
OEB_ODP[3]	151	OUT_CELL	-
ODP[3]	150	OUT_CELL	-
OEB_OACTIVE[3]	149	OUT_CELL	-
OACTIVE[3]	148	OUT_CELL	-
OEB_ODATA[3][7]	147	OUT_CELL	-
ODATA[3][7]	146	OUT_CELL	-
OEB_ODATA[3][6]	145	OUT_CELL	-
ODATA[3][6]	144	OUT_CELL	-
OEB_ODATA[3][5]	143	OUT_CELL	-
ODATA[3][5]	142	OUT_CELL	-
OEB_ODATA[3][4]	141	OUT_CELL	-
ODATA[3][4]	140	OUT_CELL	-
OEB_ODATA[3][3]	139	OUT_CELL	-
ODATA[3][3]	138	OUT_CELL	-
OEB_ODATA[3][2]	137	OUT_CELL	-
ODATA[3][2]	136	OUT_CELL	-
OEB_ODATA[3][1]	135	OUT_CELL	-
ODATA[3][1]	134	OUT_CELL	-
OEB_ODATA[3][0]	133	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
ODATA[3][0]	132	OUT_CELL	-
ODETECT[3]	131	IN_CELL	-
OEB_INTB	130	OUT_CELL	-
INTB	129	OUT_CELL	-
OEB_OC1FP[2]	128	OUT_CELL	-
OC1FP[2]	127	OUT_CELL	-
OEB_OV5[2]	126	OUT_CELL	-
OV5[2]	125	OUT_CELL	-
OEB_OPL[2]	124	OUT_CELL	-
OPL[2]	123	OUT_CELL	-
OEB_ODP[2]	122	OUT_CELL	-
ODP[2]	121	OUT_CELL	-
OEB_ODATA[2][7]	120	OUT_CELL	-
ODATA[2][7]	119	OUT_CELL	-
OEB_ODATA[2][6]	118	OUT_CELL	-
ODATA[2][6]	117	OUT_CELL	-
OEB_ODATA[2][5]	116	OUT_CELL	-
ODATA[2][5]	115	OUT_CELL	-
OEB_ODATA[2][4]	114	OUT_CELL	-
ODATA[2][4]	113	OUT_CELL	-
OEB_ODATA[2][3]	112	OUT_CELL	-
ODATA[2][3]	111	OUT_CELL	-
OEB_ODATA[2][2]	110	OUT_CELL	-
ODATA[2][2]	109	OUT_CELL	-
OEB_ODATA[2][1]	108	OUT_CELL	-
ODATA[2][1]	107	OUT_CELL	-
OEB_ODATA[2][0]	106	OUT_CELL	-
ODATA[2][0]	105	OUT_CELL	-
ITAIS[1]	104	IN_CELL	-
IPL[1]	103	IN_CELL	-
IC1FP[1]	102	IN_CELL	-
IV5[1]	101	IN_CELL	-
ITPL[1]	100	IN_CELL	-
IDP[1]	99	IN_CELL	-
IDATA[1][7]	98	IN_CELL	-
IDATA[1][6]	97	IN_CELL	-
IDATA[1][5]	96	IN_CELL	-
IDATA[1][4]	95	IN_CELL	-
IDATA[1][3]	94	IN_CELL	-
IDATA[1][2]	93	IN_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
IDATA[1][1]	92	IN_CELL	-
IDATA[1][0]	91	IN_CELL	-
OEB_SREFCLK19	90	OUT_CELL	-
SREFCLK19	89	OUT_CELL	-
SREFCLK	88	IN_CELL	-
SYSCLK	87	IN_CELL	-
OEB_JUST_REQ[2]	86	OUT_CELL	-
JUST_REQ[2]	85	IO_CELL	-
OEB_OACTIVE[2]	84	OUT_CELL	-
OACTIVE[2]	83	OUT_CELL	-
ODETECT[2]	82	IN_CELL	-
OCMP	81	IN_CELL	-
ICMP	80	IN_CELL	-
OEB_OTAIS[2]	79	OUT_CELL	-
OTAIS[2]	78	OUT_CELL	-
OEB_OTPL[2]	77	OUT_CELL	-
OTPL[2]	76	OUT_CELL	-
RTAIS	75	IN_CELL	-
RTPL	74	IN_CELL	-
RV5	73	IN_CELL	-
RPL	72	IN_CELL	-
RDP	71	IN_CELL	-
RDATA[7]	70	IN_CELL	-
RDATA[6]	69	IN_CELL	-
RDATA[5]	68	IN_CELL	-
RDATA[4]	67	IN_CELL	-
RDATA[3]	66	IN_CELL	-
RDATA[2]	65	IN_CELL	-
RDATA[1]	64	IN_CELL	-
RDATA[0]	63	IN_CELL	-
RJUST_REQ	62	IN_CELL	-
OEB_OC1FP[1]	61	OUT_CELL	-
OC1FP[1]	60	OUT_CELL	-
OEB_OPL[1]	59	OUT_CELL	-
OPL[1]	58	OUT_CELL	-
OEB_OV5[1]	57	OUT_CELL	-
OV5[1]	56	OUT_CELL	-
OEB_OTPL[1]	55	OUT_CELL	-
OTPL[1]	54	OUT_CELL	-
OEB_OTAIS[1]	53	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
OTAIS[1]	52	OUT_CELL	-
OEB_ODATA[1][7]	51	OUT_CELL	-
ODATA[1][7]	50	OUT_CELL	-
OEB_ODATA[1][6]	49	OUT_CELL	-
ODATA[1][6]	48	OUT_CELL	-
OEB_ODATA[1][5]	47	OUT_CELL	-
ODATA[1][5]	46	OUT_CELL	-
OEB_ODATA[1][4]	45	OUT_CELL	-
ODATA[1][4]	44	OUT_CELL	-
OEB_ODATA[1][3]	43	OUT_CELL	-
ODATA[1][3]	42	OUT_CELL	-
ODETECT[1]	41	IN_CELL	-
OEB_OACTIVE[1]	40	OUT_CELL	-
OACTIVE[1]	39	OUT_CELL	-
OEB_TTAIS	38	OUT_CELL	-
TTAIS	37	OUT_CELL	-
OEB_TV5	36	OUT_CELL	-
TV5	35	OUT_CELL	-
Reserved	34	IN_CELL	-
OEB_TTPL	33	OUT_CELL	-
TTPL	32	OUT_CELL	-
OEB_TPL	31	OUT_CELL	-
TPL	30	OUT_CELL	-
OEB_TDP	29	OUT_CELL	-
TDP	28	OUT_CELL	-
OEB_ODATA[1][2]	27	OUT_CELL	-
ODATA[1][2]	26	OUT_CELL	-
OEB_ODATA[1][1]	25	OUT_CELL	-
ODATA[1][1]	24	OUT_CELL	-
OEB_ODATA[1][0]	23	OUT_CELL	-
ODATA[1][0]	22	OUT_CELL	-
OEB_ODP[1]	21	OUT_CELL	-
ODP[1]	20	OUT_CELL	-
OEB_TDATA[7]	19	OUT_CELL	-
TDATA[7]	18	OUT_CELL	-
OEB_TDATA[6]	17	OUT_CELL	-
TDATA[6]	16	OUT_CELL	-
OEB_TDATA[5]	15	OUT_CELL	-
TDATA[5]	14	OUT_CELL	-
OEB_TDATA[4]	13	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
TDATA[4]	12	OUT_CELL	-
OEB_TDATA[3]	11	OUT_CELL	-
TDATA[3]	10	OUT_CELL	-
OEB_TDATA[2]	9	OUT_CELL	-
TDATA[2]	8	OUT_CELL	-
OEB_TDATA[1]	7	OUT_CELL	-
TDATA[1]	6	OUT_CELL	-
OEB_TDATA[0]	5	OUT_CELL	-
TDATA[0]	4	OUT_CELL	-
OEB_TC1FP	3	OUT_CELL	-
TC1FP	2	OUT_CELL	-
OEB_TJUST_REQ	1	OUT_CELL	-
TJUST_REQ	0	OUT_CELL	-

Notes:

1. When set high, INTB will be set to high impedance.
2. Enable cell OEB_*pinname*, tristates pin *pinname* when set high.
3. IV5[4] is the first bit of the boundary scan chain.

12.1.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 11 Input Observation Cell (IN_CELL)

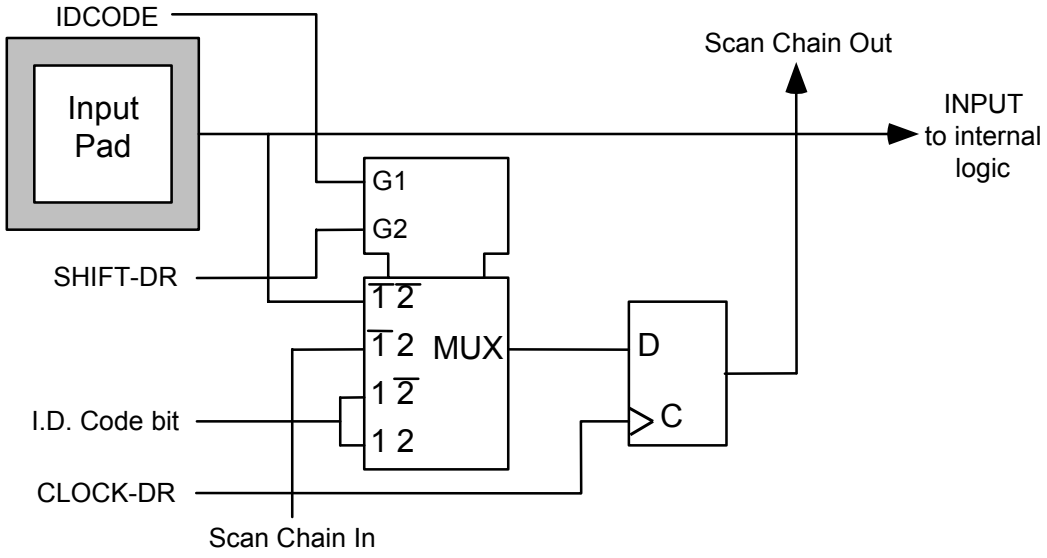


Figure 12 Output Cell (OUT_CELL)

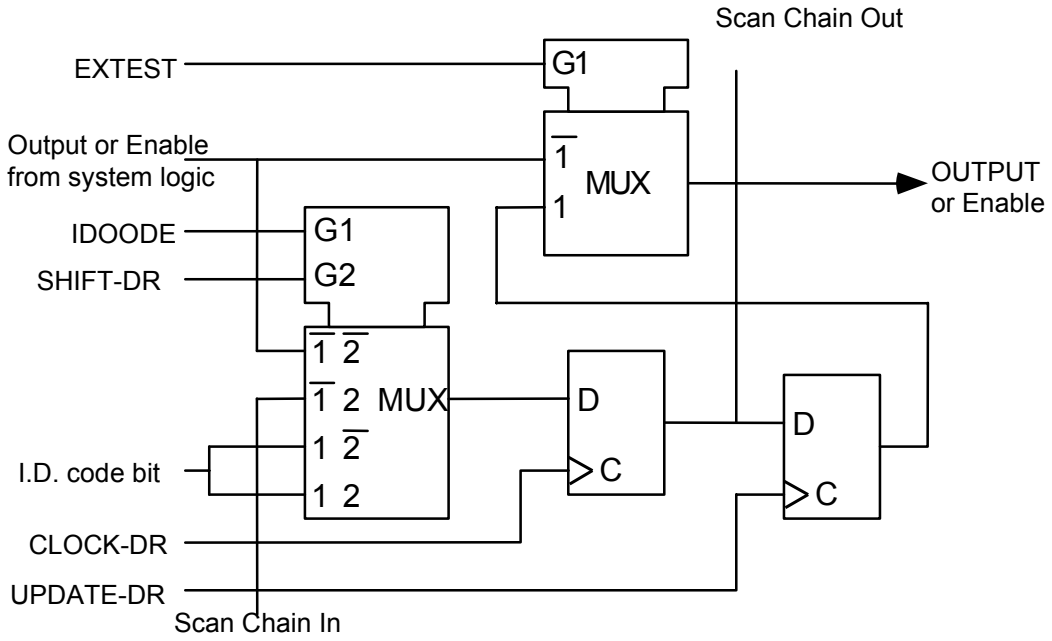


Figure 13 Bi-directional Cell (IO_CELL)

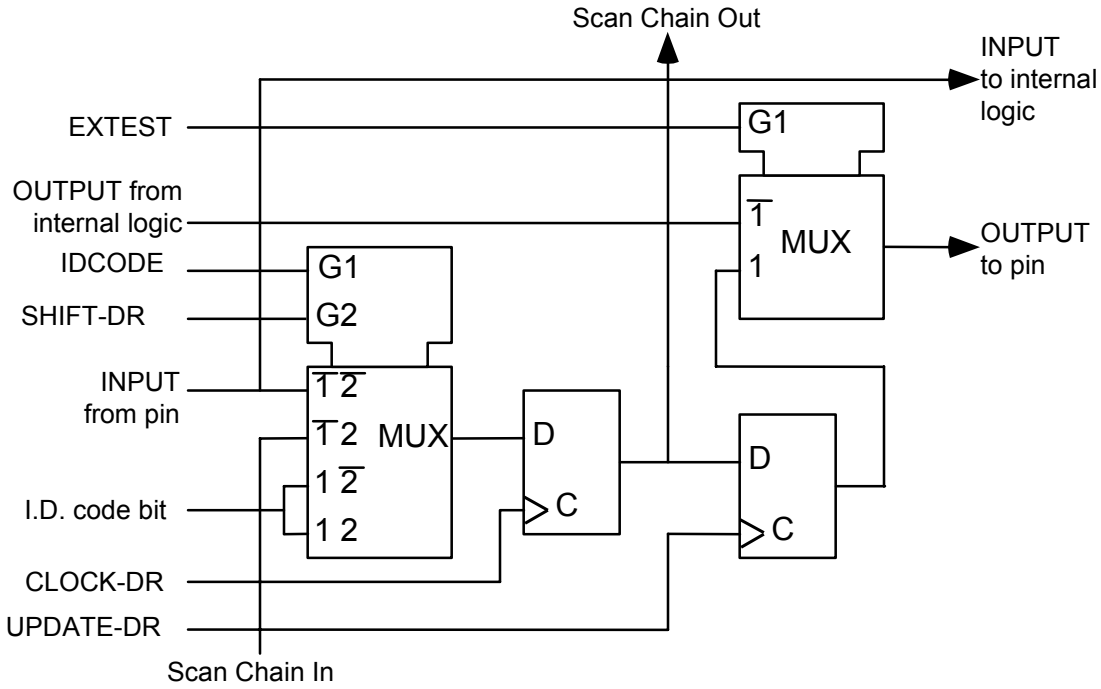
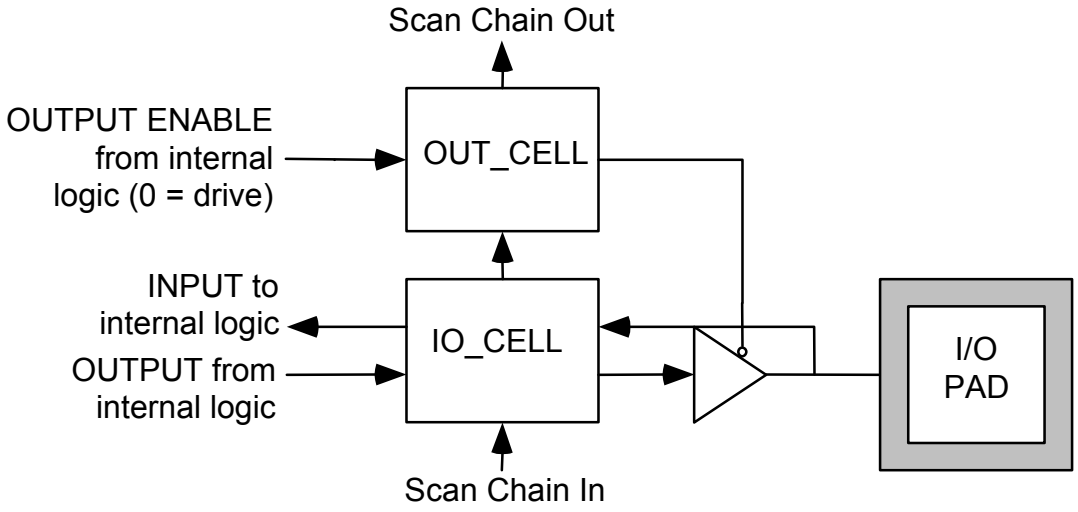


Figure 14 Layout of Output Enable and Bi-directional Cells



13 Operation

13.1 LVDS Optimizations

The LVDS interface implemented on the SBS and NSE follows the IEEE 1596.3-1996 specification with some minor exceptions. The changes are implemented to customize and optimize the LVDS interface for the system and are described in detail below. Even with these differences the LVDS interface should be compatible with the physical layer of other LVDS interfaces. The differences from the IEEE specification include:

1. Faster rise/fall times (200 – 400) ps versus the specified (300 - 500) ps. Faster edge rates are commonly used with higher speed LVDS interfaces in the industry to ease interfacing. The IEEE 1596.3-1996 edge rates are optimized for data rates below 400 Mbps.

2. Hysteresis is not implemented in the receive LVDS interface. Hysteresis is used in many implementations to negate the effect of noise that may exist on unused LVDS links. Hysteresis was not implemented in the SBS and NSE devices to minimize circuit complexity, power, and cost. Instead, the RX interfaces and the DRUs for unused links can be disabled (powered down) through register control in order to prevent sensitivity to noise on these links.

3. The LVDS transmitter contains an on-chip 100-ohm termination. Most implementations use a single 100-ohm termination on the receiver. By implementing a double termination (on both the LVDS receiver and transmitter) better signal integrity and matching is ensured.

4. Although not a difference with the Layer 1 IEEE 1596.3-1996 specification, the Layer 2 8B/10B encoding is discussed here for completeness. 8B/10B encoding guarantees transition density as compared to scrambled encoding, which provides only a certain probability of transition density. This guaranteed transition density allows a simpler and more power-effective data recovery unit, provides a more robust serial interface (greater trace or back-plane distance achievable). It also negates the need for complete SONET framing since the A1A2 and J0 bytes can be encoded into special escape characters of the LVDS data stream.

5. The device uses 20% resistors; not 10% as specified by the LVDS specification. They are 20% resistors since that was the highest tolerance resistor available for on-chip applications. However, because they are integrated on-chip, this LVDS interface can achieve much better signal integrity than one with off-chip terminations.

13.2 LVDS Hot Swapping

The LVDS electrical interface differs from a standard CMOS interface; there is no inherent problem in leaving the LVDS inputs floating. Note that the LVDS receiver consists of a differential amplifier with a wide common-mode range. The power dissipation is independent of the data transitions (that is, if the input is connected). There is an internal 100 Ω termination across the positive and negative input. Floating inputs will settle to an arbitrary voltage (between VDD and VSS) determined by leakage paths. Regardless of this arbitrary voltage, the input structure of the receiver will operate in its proper range and the receiver output will be logic 1 or 0 depending on internal offsets. Noise events (power supply noise, crosstalk) may induce the receiver to toggle randomly, generating "ambiguous" data. This ambiguous data will not result in any problems but is not a desirable condition since it simply wastes power.

Unused links should be disabled in software. This will ensure that the power consumption for those links will be reduced to nearly 0 mW. There is no requirement for how quickly the link should be disabled. Disabling the link simply results in lower power dissipation since the circuitry will be shut down. This action is not mandatory, but is good practice.

During a hot-swapping situation, there will be no electrical damage on the LVDS inputs provided that maximum ratings are not exceeded (see absolute maximum ratings section 15). There are no problems with hot-swapping. The “hot-swap” channel can be left enabled and the device will sync up once the far end transmitter is connected. There are no effects on other channels. Hot swapping of cards is still allowed by reprogramming of the links in software. The framing algorithm used in the receive framer blocks will keep the receiver in an out-of-frame state in the case of a link being hot swapped while still enabled. The device will pass on the random data received on this link, or the user may choose to pass on an AIS indication via register configuration. Despite passing on random data, control signals will be suppressed such that there will be no false J0 indications on the outgoing SBI or Telecom Bus.

13.3 Selecting Between the Receive Working and Protection Links

The data from only one of the two receive links is propagated to the Outgoing Bus on the SBS. The selection of which link, the working or protect, the SBS listens to is controlled by the RWSEL input or the RWSEL_VAL bit in register 001H. If the RWSEL_SRC bit in register 001H is set to a logic 0, the RWSEL_VAL bit is used to select the active link. If RWSEL_SRC is a logic 1, the RWSEL input is used to select the active link.

RWSEL is sampled at the C1 position of every frame, as marked by the RC1FP input, and when a change is detected the switching between the links is synchronized to the first byte of the following frame. This allows for a controlled switch between the working and protection links.

Note that both the working and protection PRBS monitors and in-band link controllers are active regardless of which link is selected by RWSEL. This provides a method to monitor the inactive link without disrupting the data on the active link.

13.4 Interrupt Service Routing

The SBS will assert the INTB output to a logic 0 when a condition that is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

Read the SBS Master Interrupt Source Register (010H) to find the functional block which caused the interrupt.

Find the register address of the corresponding block that caused the interrupt and read its Interrupt Status registers. The interrupt bits in the functional block and the interrupt source identification bits from step 1 are cleared once these register(s) have been read and the interrupt(s) identified.

Service the interrupt(s).

If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

Note that all interrupts in the SBS may be disabled by setting the INTE bit of the SBS Master Interrupt Enable Register (016H) to a logic 0. Interrupts may also be disabled on a block by block basis by setting the appropriate block enable bits in this register to a logic 0.

13.5 Accessing Indirect Registers

Indirect registers are used to conserve address space in the SBS.

13.5.1 Accessing Indirect Registers in the ICASM, OCASM, ISTT, OSTT and OSTA

When writing to an indirect register in the ICASM, OCASM, ISTT, OSTT or OSTA, the following procedure should be followed:

Read the BUSY bit in the Indirect Access Control Register. If it is a logic 0, continue to step 2. If it is a logic 1, continue polling the BUSY bit.

Write the desired configuration for the tributary into the Indirect Access Data Register.

Write the desired tributary number into the Indirect Access Address Register.

Write to the Indirect Access Control Register with RWB set to logic 0.

Read the BUSY bit. Once it is a logic 0, the indirect write has been completed.

When reading an indirect register from the ICASM, OCASM, ISTT, OSTT or OSTA, the following procedure should be followed:

Read the BUSY bit in the Indirect Access Control Register. If it is a logic 0, continue to step 2. If it is a logic 1, continue polling the BUSY bit.

Write the desired tributary number into the Indirect Access Address Register.

Write to the Indirect Access Control Register with RWB set to logic 1.

Read the BUSY bit. If it is a logic 0, continue to step 5. If it is a logic 1, continue polling the BUSY bit.

Read the Indirect Access Data Register to find the state of the register bits for the selected tributary.

13.5.2 Accessing Indirect Registers in the WPP and PPP

When writing to an indirect register in the WPP or PPP, the following procedure should be followed:

Read the BUSY bit in the Indirect Access Register. If it is a logic 0, continue to step 2. If it is a logic 1, continue polling the BUSY bit.

Write the desired configuration into the Indirect Data Register.

Write the desired path number and indirect address number into the Indirect Address Register with RDWRB set to logic 0.

Read the BUSY bit. Once it is a logic 0, the indirect write has been completed.

When reading an indirect register from the WPP or PPP, the following procedure should be followed:

Read the BUSY bit in the Indirect Access Register. If it is a logic 0, continue to step 2. If it is a logic 1, continue polling the BUSY bit.

Write the desired path number and indirect address number into the Indirect Address Register with RDWRB set to logic 1.

Read the BUSY bit. If it is a logic 0, continue to step 4. If it is a logic 1, continue polling the BUSY bit.

Read the Indirect Data Register to find the state of the register bits for the selected path and indirect address.

13.5.3 Software Design Notes:

Software should not attempt to write to indirect addresses other than those specifically mentioned in the register description. Other indirect addresses should be considered reserved.

Software should implement a timeout so that a BUSY bit which is stuck at 1 will not cause an infinite loop in the software. BUSY bits will no be stuck at 1 in normal operation, but may become stuck at 1 if an invalid access is attempted, or an access is attempted while the device is not being clocked.

13.6 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. All performance monitor counters have been sized to not saturate if polled at regular intervals. The counters will saturate and not roll over if they reach their maximum value.

Writing to the SBS Master Signal Monitor #1, Accumulation Trigger Register (014H) causes a device update of all the counters. If this register is written to, the TIP bit in the SBS Receive Synchronization Delay Register (007H) can be polled to determine when all the counter values have been transferred and are ready to be read. Alternately, software can wait the number of SYSCLK cycles shown in

Table 27 Maximum Performance Monitor Counter Transfer Time

Trigger Register Address	Block Name	SYSCLK cycles to complete transfer (MAX)
014H	All Blocks (WPP, PPP, RW8D and RP8D)	17
07CH	WPP	17
08CH	PPP	17
0C2H	RW8D	6
0CAH	RP8D	6

13.7 Configuring the Transmit Encoders (TW8E and TP8E)

The transmit encoder blocks (TW8E and TP8E) may be configured in one of three possible termination modes. The selection between the three modes is performed at the STS/AU level. The three modes are:

Low Order Path Termination Mode (LPT). This mode must be used when connecting the SBS to an SBI or SBI336 bus. This mode may also be used when connecting the SBS to a Telecom Bus where the V5 and TPL signals must be preserved across the Serial Telecom Bus. The ERDI[1:0] and REI bits of the V5 byte (bits 0, 4 and 5) will be preserved but the remaining bits will be set to zero by the receive decoder at the far end of the serial link. The V1 and V2 pointers will also be set to all zeros.

High Order Path Termination Mode (HPT). This mode may be used when connecting the SBS to a Telecom Bus where the V1 and V2 pointers must be preserved across the Serial Telecom Bus. Note that in this mode, the V5 signal will be zeroed out by the receive decoder at the far end of the serial link, but the data within the V5 byte will be preserved. In this mode the J1 byte will be overwritten with a control character on the serial link.

Multiplex Section Termination Mode (MST). This mode may be used when connecting the SBS to a Telecom Bus where H1 and H2 pointers must be preserved across the Serial Telecom Bus and the J1 byte cannot be overwritten. Note that in this mode, a receiving device must use the H1/H2 pointers to locate the J1 byte position.

The selection of the termination mode is contained in registers 0B2H and 0B3H for the TW8E, and in registers 0BAH and 0BBH for the TP8E.

13.8 Interpreting the Status of the Receive Decoders (RW8D and RP8D)

The receive decoded blocks (RW8D and RP8D) produce interrupts based on four receiver conditions or events: OCA (Out of Character Alignment), OFA (Out of Frame Alignment), FUO (FIFO Underrun/Overrun) and LCV (Line Code Violation). Understanding the relationship between these conditions can help to diagnose device status. These conditions have the following interrelationships:

OCA implies OFA until character alignment is re-achieved. OCA will most likely cause some LCVs but not necessarily a continual stream. Since character boundaries are not know, framing and disparity are meaningless.

OFA, by itself, does not cause any of the other conditions.

FUO may produce zero, one or many OCVs, depending on how the FIFO underrun/overrun occurs.

Persistent LCVs (five or more in any sequence of 15 characters) cause OCA.

13.9 Using the Memory Switch Units (IMSU and OMSU)

The Memory Switch Unit (MSU) blocks in the SBS (IMSU and OMSU) can be used to rearrange the position of the bytes (or columns) within the SBI336 or Telecom Bus frame. Each block buffers an entire frame (9720 bytes) or row (1080 columns) and rearranges them before outputting them.

13.9.1 Selection Between the Two Connection Memory Pages

The selection of which input byte (or column) is to be output at each output byte (or column) location is controlled by the settings in the connect memory pages. There are two connection memory pages, one of which is used to control the switching function while the other may be modified with new connections through the microprocessor interface.

The two pages can be swapped by changing the CMP value. There are three possible sources for the CMP value. They are the ICMP/OCMP input pins, the ICMP_VAL/OCMP_VAL bits in the SBS Master Configuration Register (001H), and the PAGE[1:0] bits from the ILC block on the active receive link. The selection of the source of CMP is controlled by the setting of the ICMP_SRC[1:0]/OCMP_SRC[1:0] bits in the SBS Master Configuration Register (001H).

13.9.2 Procedure for Writing to the Connection Memory Page

When writing to a location in the connection memory page in the IMSU or OMSU, the following procedure should be followed:

Write the desired configuration into the Indirect Time Switch Data Register.

Write to the desired address into the Indirect Time Switch Address Register with RWB set to logic 0.

Wait for a minimum of 4 SYSCLK cycles before repeating for the next address.

When reading from a location in the connection memory page in the IMSU or OMSU, the following procedure should be followed:

Write the desired address location into the Indirect Time Switch Address Register with RWB set to logic 1.

Wait a minimum of 8 SYSCLK cycles.

Read the value from the Indirect Time Switch Data Register and check the VALID bit. If the VALID bit is a logic 0, the data in the register is not valid and this register should be read again. If the VALID bit is a logic 1, the value in the IN_BYTE[13:0] bits is valid.

13.9.3 MSU Ram Address Map

Each ram location in the connection memory page corresponds to a byte (or column) in the SBI336 or Telecom Bus being output from the MSU. The data contained in the ram location points to the byte (or column) from the input SBI336 or Telecom Bus which is to be switched to the output. In byte mode, ram address 0 corresponds to the first byte in the frame, and ram address 9719 corresponds to the last byte in the frame. In column mode, ram address 0 corresponds to the first column in the frame and ram address 1079 corresponds to the last column in the frame.

13.9.4 Example Column Mode Addresses for TU-11 Tributaries (AU-3)

The following table shows the ram addresses for each column for AU-3 traffic containing TU-11 tributaries.

	Transport Overhead	VC-3 Path Overhead	TU-11 #1	TU-11 #2 - #336	Fixed Stuff	TU-11 #1	TU-11 #2 - #336	Fixed Stuff	TU-11 #1	TU-11 #2 - #336
Column	0 – 35	36 – 47	48	49 – 383	384 – 395	396	397 – 731	732 – 743	744	745 - 1079

13.9.5 Example Column Mode Addresses for TU-11 Tributaries (SDH AU-4 or SBI336)

The following table shows the ram addresses for each column for AU-4 traffic containing TU-11 tributaries. Note that for SBI336 traffic, columns 0 – 71 are all considered unused.

	Transport Overhead	VC-4 Path Overhead	Fixed Stuff	TU-11 #1	TU-11 #2 - #336	TU-11 #1	TU-11 #2 - #336	TU-11 #1	TU-11 #2 - #336
Column	0 – 35	36 – 39	40 – 71	72	73 – 407	408	409 – 743	744	745 - 1079

13.9.6 Example Byte Mode Addresses for TU-11 Tributaries (SDH AU-4 or SBI336)

The following table shows the ram addresses for each byte for AU-4 traffic containing TU-11 tributaries. Note that for SBI336 traffic, all bytes in the Transport Overhead, Path Overhead and Fixed Stuff columns are considered unused.

	Transport Overhead	VC-4 Path Overhead	Fixed Stuff	TU-11 #1	TU-11 #2 - #336	TU-11 #1	TU-11 #2 - #336	TU-11 #1	TU-11 #2 - #336
1	0 – 35	36 – 39	40 – 71	72	73 – 407	408	409 – 743	744	745 - 1079
2	1080 – 1115	1116 – 1119	1120 – 1151	1152	1153 – 1487	1488	1489 – 1823	1824	1825 – 2159
3	2160 – 2195	2196 – 2199	…						
4	3240 – 3275	3276 – 3279	…						
5	4320 – 4355	4356 – 4359	…						
6	5400 – 5435	5436 – 5439	…						
7	6480 – 6515	6516 – 6519	…						
8	7560 – 7595	7596 – 7599	…						
9	8640 – 8675	8676 – 8679	8680 – 8711	8712	8713 – 9047	9048	9049 – 9383	9384	9385 – 9719

13.10 Using the PRBS Generator and Monitors (WPP and PPP)

A pseudo-random (using the $X^{23}+X^{18}+1$ polynomial) or incrementing pattern can be inserted/extracted in the SONET/SDH payload. With PRBS data and incrementing data patterns, the payload envelope is filled with pseudo-random/incrementing bytes with the exception of POH and fixed stuff columns. In the case of the incrementing counts, the count starts at 0 and increments to FFh before the count starts over at 0 once again. The incrementing count is free to float within the payload envelope and therefore the 0 count is not associated with any fixed location within a payload envelope. This PRBS generator and monitor is compatible with the PRBS generators and monitors in other CHESS™ Set devices. It may not be compatible with external test equipment.

13.10.1 Mixed Payload (STS-12c/STM-4/AU4-4c, STS-3c/STM-1, and STS-1/STM-0)

The WPP and PPP are designed to process the payload of an STS-12/STM-4 frame in a time-multiplexed manner. Each time division (12 STS-1/STM-0 paths) can be programmed to a granularity of an STS-1/STM-0. It is possible to process one STS-12c/STM-4c, twelve STS-1/STM-0 or four STS-3c/STM-1 or a mix of STS-1/STM-0 and STS-3c/STM-1 as long as the aggregate data rate is not more than one STS-12/STM-4 equivalent. The mixed payload configuration can support the three STS-1/STM-0 and STS-3c/STM-1 combinations shown below:

- three STS-1/STM-0 with three STS-3c/STM-1
- six STS-1/STM-0 with two STS-3c/STM-1
- nine STS-1/STM-0 with one STS-3c/STM-1

The STS-1/STM-0 path that each one of the payload occupies, cannot be chosen randomly. They must be placed on STS-3c/STM-1 boundaries (group of three STS-1/STM-0).

13.10.2 Synchronization

Before being able to monitor the correctness of the PRBS payload, the monitor must synchronize to the incoming PRBS. The process of synchronization involves synchronizing the monitoring LFSR to the transmitting LFSR. Once the two are synchronized the monitoring LFSR is able to generate the next expected PRBS bytes. When receiving sequential PRBS bytes (STS-12c/VC-4-4c), the LFSR state is determined after receiving 3 PRBS bytes (24 bits of the sequence). The last 23 of 24 bits (excluding MSB of first received byte) would give the complete LFSR state. The 8 newly generated LFSR bits after a shift by 8 (last 8 XOR products) will produce the next expected PRBS byte.

The implemented algorithm requires four PRBS bytes of the same payload to ascertain the LFSR state. From this recovered LFSR state the next expected PRBS byte is calculated.

Out of Synchronization and Synchronized states are defined for the monitor. While in progress of synchronizing to the incoming PRBS stream, the monitor is out of synchronization and remains in this state until the LFSR state is recovered and the state has been verified by receiving 4 consecutive PRBS bytes without error. The monitor will then change to the Synchronized State and remains in that state until forced to resynchronize via the RESYNC register bit or upon receiving 3 consecutive bytes with errors. When forced to resynchronize, the monitor changes to the Out of Synchronization State and tries to regain synchronization. It is important to note however that the monitor can falsely synchronize to an all zero pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 pattern. It is therefore recommended that users poll the monitor's LFSR value after synchronization has been declared, to confirm that the value is neither all 1s or all 0s.

Upon detecting 3 consecutive PRBS byte errors, the monitor will enter the Out of Synchronization State and automatically try to resynchronize to the incoming PRBS stream. Once synchronized to the incoming stream, it will take 4 consecutive non-erred PRBS bytes to change back into the Synchronized State. The auto synchronization is useful when the input frame alignment of the monitored stream changes. The realignment will affect the PRBS sequence causing all input PRBS bytes to mismatch and forcing the need for a resynchronization of the monitor. The auto resynchronization does this, detecting a burst of errors and automatically re-synchronizing.

13.10.3 Error Detection and Accumulation

By comparing the received PRBS byte with the calculated PRBS byte, the monitor is able to detect byte errors in the payload. A byte error is detected on a comparison mismatch of the two bytes. Only a single byte error is counted regardless of the number of erroneous bits in the byte. All byte errors are accumulated in a 16 bit byte error counter. The error counter will saturate at its maximum value of FFFFh, i.e. it will not wrap around to 0000h if further PRBS byte errors are encountered. The counter is readable via the WPP Monitor Error Count Register or the PPP Monitor Error Count Register. The error counter is cleared when transferred into the registers and the accumulation restarts at zero. When reading error counts for concatenated payloads of STS-3c /STM-1c or STS-12c/STM-3c sizes, it is necessary to read the error count in all slices (all associated STS-1/STM-0s). For each independent STS-1/STM-0 monitored by a PRGM, the error count register for each individual STS-1/STM-0 must be read.

Byte errors are accumulated only when the monitor is in synchronized state. To enter the synchronize state, the monitor must have synchronized to the incoming PRBS stream and received 4 consecutive bytes without errors. Once synchronized, the monitor falls out of synchronization when forced to by programming the RESYNC register bit high, or once it detects 3 consecutive PRBS byte errors. When out of synchronization, detected errors are not accumulated.

13.11 Using the In-Band Link Controller (WILC and PILC)

The In-Band Link Controllers provides a mechanism for communication between devices over the serial interface. The ILC inserts and retrieves messages from the transport overhead of the SBI336 or Telecom Bus frame. The messages are 36 bytes each and 4 messages are transmitter each frame. These messages are inserted into the Data Communication Channel (DCC) bytes, in rows 3,6,7 and 8. Each message contains 2 header bytes, 32 bytes containing the free format information, and 2 bytes for a CRC-16. There is an independent in-band link controller for working and the protection links (WILC for the working link and PILC for the protection link).

If no information bytes are available to transmit, the ILC will continue to send messages but will insert all zeros into the information bytes and will set the VALID bit in the header to zero. The header and CRC bytes will be transmitted normally. When the receive link recognizes that the VALID bit is a zero, it will not write the all zero message into the receive FIFO.

13.11.1 Transmitting Messages

When writing to the transmit FIFO in the WILC or PILC, the following procedure should be followed:

Write a logic 1 to the TX_XFER_SYNC bit of the Transmit Status and FIFO Synch Register (095H or 0A5H). This will ensure the subsequent writes to the FIFO start at the beginning of a message.

Write to the Transmit Data High Register (090H or 0A0H).

Write to the Transmit Data Low Register (091H or 0A1H). Writing to this register will initiate a transfer of the Transmit Data High Register and Transmit Data Low Register into the transmit FIFO.

Read the TX_FI_BUSY bit in the Transmit Status and FIFO Synch Register (095H or 0A5H) or wait a minimum of 3 SYSCLK cycles. If TX_FI_BUSY is a logic 0, continue to step 5. If it is a logic 1, continue polling the TX_FI_BUSY bit.

Loop back to Step 2 until the entire message has been written in to the FIFO.

When transmitting multiple 32 byte messages, the TX_XFER_SYNC bit does not have to be written to between each message.

When transmitting a message shorter than 32 bytes, the TX_XFER_SYNC bit should be set after writing the last byte of the message into the FIFO. This will allow the short message to be transmitted and move the FIFO to the next 32 byte partition.

13.11.2 Retrieving Messages

When reading messages from the receive FIFO in the WILC or PILC, the following procedure should be followed:

Write a logic 1 to the RX_XFER_SYNC bit of the Receive Status and FIFO Synch Register (09BH or 0ABH). This will initiate a read from the receive FIFO.

Read the RX_FI_BUSY bit in the Receive Status and FIFO Synch Register (09BH or 0ABH) or wait a minimum of 4 SYSCLK cycles. If RX_FI_BUSY is a logic 0, continue to step 3. If it is a logic 1, continue polling the RX_FI_BUSY bit.

Read the Receive Status and FIFO Synch Register (09BH or 0ABH) and check the state of the CRC_ERR. If this bit is a logic 1, the current message in the FIFO had a CRC error and the data is not reliable and the user may want to skip to the next message. This may be done by writing logic 1 to the RX_XFER_SYNC bit (09BH or 0ABH), then returning to step 1.

Read the Receive FIFO Data High Register (096H or 0A6H).

Read the Receive FIFO Data Low Register (097H or 0A7H).

Read the RX_FI_BUSY bit in the Receive Status and FIFO Synch Register (09BH or 0ABH) or wait a minimum of 4 SYSCLK cycles. If RX_FI_BUSY is a logic 0, continue to step 7. If it is a logic 1, continue polling the RX_FI_BUSY bit.

Loop back to Step 4 until the entire message has been read out of the FIFO.

When reading more than one message from the receive FIFO, the RX_XFER_SYNC does not have to be set between each message.

Before reading the any messages, the software may want to check how many messages are contained in the receive FIFO. This can be done by reading the RX_MSG_LVL[3:0] bits in the Receive Status and FIFO Synch Register (09BH or 0ABH). When reading these bits, the RX_STTS_VALID bit must also be checked. If RX_STTS_VALID is a logic 1, the RX_MSG_LVL[3:0] bits are valid. If RX_STTS_VALID is a logic 0, the RX_MSG_LVL[3:0] bits are not valid and this register should be read again until RX_STTS_VALID is a logic 1.

13.11.3 Transmit Message Header Bytes

LINK[1:0]: These bits reflect the state of the TX_LINK[1:0] bits in the Transmit Control Register (093H or 0A3H).

PAGE[1:0]: These bits reflect the state of the CMP value used by each of the MSU blocks. PAGE[1] reflects the current memory page used by the IMSU. PAGE[0] reflects the current memory page used by the OMSU.

USER[2:0]: The USER[2] bit reflects the state of the IUSER2 input to the SBS. The USER[1:0] bits transmitted by the WILC reflects the state of the TXWUSER[1:0] bits in register 008H. The USER[1:0] bits transmitted by the PILC reflects the state of the TXPUSER[1:0] bits in register 008H.

AUX[7:0]: These bits reflect the state of the TX_AUX[7:0] bits in the Transmit Control Register (093H or 0A3H).

13.11.4 Receive Message Header Bytes

LINK[1:0]: The LINK[1:0] bits from the latest received message are reflected in the RX_LINK[1:0] bits of the Receive Status and FIFO Synch Register (09DH or 0ADH). These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value. A change in state of either of these bits can be configured to cause an interrupt by setting the RX_LINK_CHGE bit in the Interrupt Enable and Control Register (09DH or 0ADH).

PAGE[1:0]: The PAGE[1:0] bits from the latest received message are reflected in the OPAGE[1:0] bits of the Receive Status and FIFO Synch Register (09DH or 0ADH). The PAGE[1:0] bits on the active link (as selected by RWSEL) may be used to control the connection memory pages of the MSU blocks. PAGE[1] will control the CMP value for the IMSU when the ICMP_SRC[1:0] bits in register 001H are set to "10". PAGE[0] will control the CMP value for the OMSU when the OCMP_SRC[1:0] bits in register 001H are set to "10". These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value. A change in state in either of these bits can be configured to cause an interrupt by setting the OPAGE_CHGE[1:0] bits in the Interrupt Enable and Control Register (09DH or 0ADH).

USER[2:0]: The USER[2:0] bits from the latest received message are reflected in the OUSER[2:0] bits of the Receive Status and FIFO Synch Register (09DH or 0ADH). The USER[2] from the active link (as selected by RWSEL) will also be output on the OUSER2 output of the SBS. These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value.

AUX[7:0]: The AUX[7:0] bits from the latest received message are reflected in the RX_AUX[7:0] bits of the Receive Auxiliary Register (09AH or 0AAH). These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value.

13.11.5 Disabling the ILC

The functions of the WILC and PILC blocks may be disabled. When disabled, no messages are inserted or retrieved. All data passes through the ILC unmodified.

The TX_BYPASS bit in the Transmit Control Register (093H or 0A3H) will disable the transmit half of the ILC. The RX_BYPASS bit in the Receive FIFO Control Register (099H or 0A9H) will disable the receive half of the ILC.

13.12 Using J1 and V1 insertion registers

Registers 061H and 062H allow for the insertion of J1 and V1 indicators on the OC1FP signal. By using these registers, it is possible to insert J1 and V1 indicators at STS/AU granularity. The OLOCK0 bit in register 060H controls the position of the J1 indicators, which may either follow C1 (Z0) or H3. On the multiframe, V1 indicators always follow the J1 indicator.

These registers should not be used in SBI mode. In TelecomBus mode, the registers act as an OR function with existing J1 indicators, and should not be used with STS/AUs where J1 is floating. When J1 is fixed to 0 or 522, the incoming J1 from the serial link will still propagate through the device, and setting the appropriate J1 indicator will have no additional effect; however, V1 insertion may be used in this case to mark the multiframe.

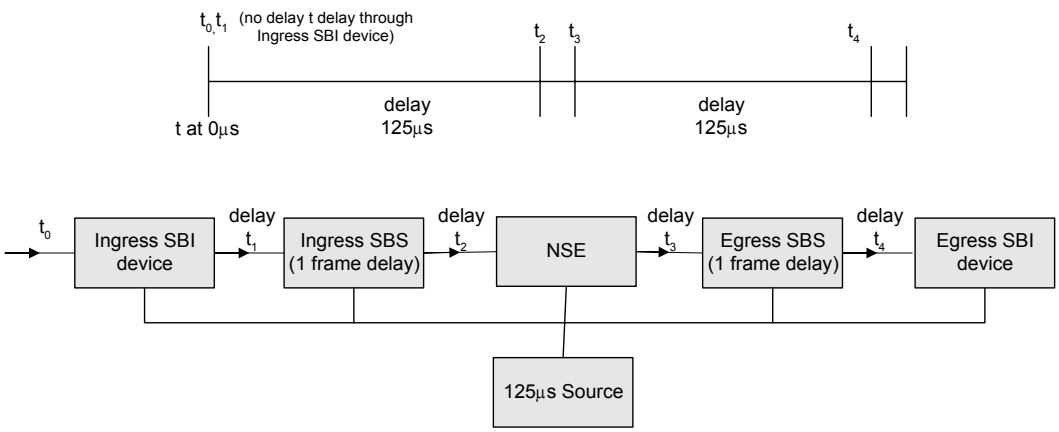
13.13 "C1" Synchronization

Any NSE/SBS fabric can be viewed as a collection of five "columns" of devices: column 0 consists of the ingress flow from the load devices (e.g., some SBI device); column 1 consists of the ingress flow through the SBS devices; column 2 consists of the NSE-20G device; column 3 consists of the egress flow through the SBS devices; and column 4 consists of the egress flow through the load devices (e.g. some SBI device). Note that the devices in columns 0 and 4 are SBI bus devices while columns 1 and 3 are SBS or SBSLITE devices. The dual column references refer to their two separate simplex flows. Path-aligned STS-12/STM-4 frames are pipelined through this structure in a regular fashion, under control of a single clock source and frame pulse. There are latencies between these columns, and these latencies may vary from path to path. The following design is used to accommodate these latencies.

A timing pulse for SBI frames (2kHz, 500 µs) is generated and fed to each device in the fabric. Each chip has a *FrameDelay* register (RC1DLY) which contains the count of 77.76 MHz clock ticks that device should delay from the reference timing pulse before expecting the C1 characters of the ingress STS-12/STM-4 frames to have arrived. The base timing pulse is called t. The delays from t based on the settings of the RC1DLY registers in the successive columns of the devices are called $t_0, \ldots t_4$. The first signal, t_1(equal to t_0), determines the start of an STS-12/STM-4 frame; this signal is used to instruct the ingress load devices (column 0) to start emitting an STS-12/STM-4 frame (with its special "C1" control character) at that time. t_i is determined by the customer, based on device and wiring delays to be approximately the earliest time that all "C1" characters will have arrived in the ingress FIFOs of the t_i column of devices. t_i is selected to provide assurance that all "C1" characters have arrived at the i^{th} column. The i^{th} column of devices use the t_i signal to synchronize emission of the STS-12/STM-4 frames. The ingress FIFOs permit a variable latency in C1 arrival of up to 24 clock cycles.

Note: the SBS device, being a memory switch adds a latency of one complete frame plus a few clock ticks to the data in DS0 switching mode. In column switching mode, the latency is one row plus a few clock ticks.

Figure 15 "C1" Synchronization Control



13.14 Synchronized Control Setting Changes

The NSE-20G and SBS support dual switch control settings. These dual settings permit one bank of settings to be operational while the other bank is updated as a result of some new connection requests. The CMP input selects the current operational switch control settings. CMP is sampled by the SBS and the NSE-20G on the base timing pulse *t*. The internal blocks sample the registered CMP value as they receive the next C1 character –at least a delay of RC1DLY. The new CMP value is applied on the first A1 character of the following STS-12/STM-4 frame or multi-frame. This switchover is hitless; the control change does not disrupt the user data flow in any way. This feature is required for the addition of arbitrary new connections, as existing connections may need to be rerouted (see the discussion of the connection routing algorithm in this document).

The DS0-granularity switch settings RAM is organized into two control settings banks, these are switched by the above mechanisms on C1 boundaries. The NSE also has to coordinate the switching of the connected SBS devices (if using the In-Band link facility), so a broader understanding of the issues is required.

To illustrate the system, the following describes actual examples:

13.14.1 SBS/NSE Systems with DS0 and CAS switching

When building a DS0 and Channel Associated Signaling switching system with the SBS, SBSLITE and NSE devices the overall timing is based on the CAS signaling multi-frame on the SBI bus. In this configuration the delay through the SBS devices is a single 125uS SBI frame plus a few 77.76MHz clocks and the delay through the NSE is a few 77.76MHz clocks. A single C1FP frame synchronization signal is distributed around the system. Internal to the SBS and NSE devices are programmable offsets used to account for propagation delays through the system. The key constraint is that all SBI frames are aligned going into the NSE device.

Compatible devices are TEMUX84, FREEDM336, FREEDM336-84, IMA84, and other future SBI336 devices.

The SBS and NSE devices have two configuration pages controlling the switching of each DS0 with CAS. The SBS has independent configuration pages for each direction of data flow through the device. The NSE has one set of configuration pages. System configuration changes are made by writing to the offline configuration page in all affected devices and then swapping from the old configuration page to the new configuration page. The ICMP and OCMP signals control the current configuration page of the SBS and the CMP signal controls the current configuration page of the NSE. Swapping of configuration pages must be aligned to frame switching through the system to avoid any possible data corruption. The ICMP, OCMP and CMP signals are sampled with the SBS IC1FP and RC1FP signals and the NSE RC1FP signals respectively. The CMP signals can be connected together at the expense of having to ensure all device configuration pages are current.

The following diagram shows how the devices are connected together. The following timing diagrams show the external signals and the internal device frame alignment signal generated from the programmed delays. Although the CMP signals are sampled externally with the C1FP signals they are also delayed internally to coincide with the internally delayed frame signals. These are also shown in the timing diagram. All internal signals are identified by the .INT suffix.

Figure 16 Temux84/SBS/NSE/SBS/AALIGATOR32 System DS0 Switching with CAS

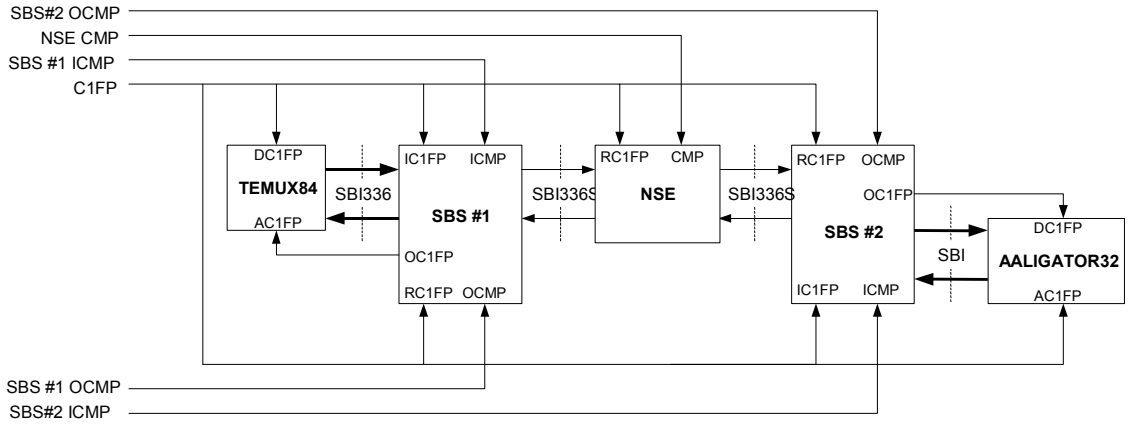


Figure 17 CAS Multi-frame Timing

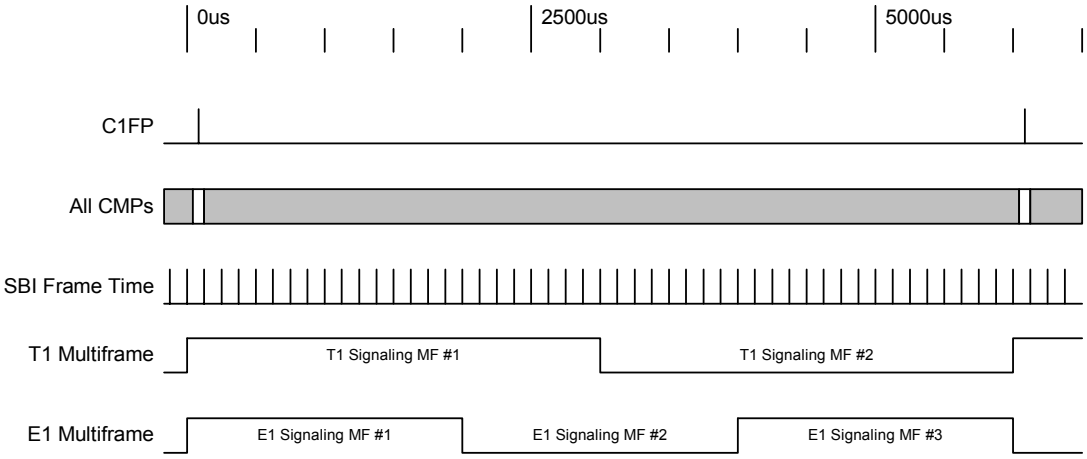
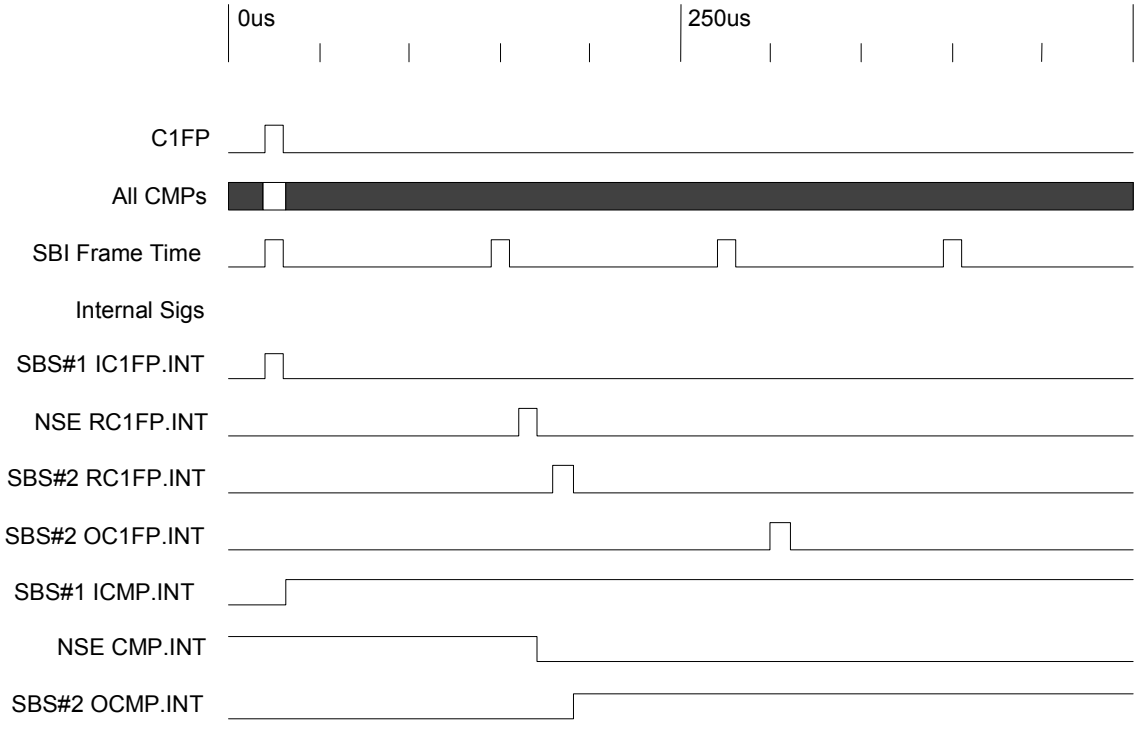


Figure 18 Switch Timing DSOs with CAS

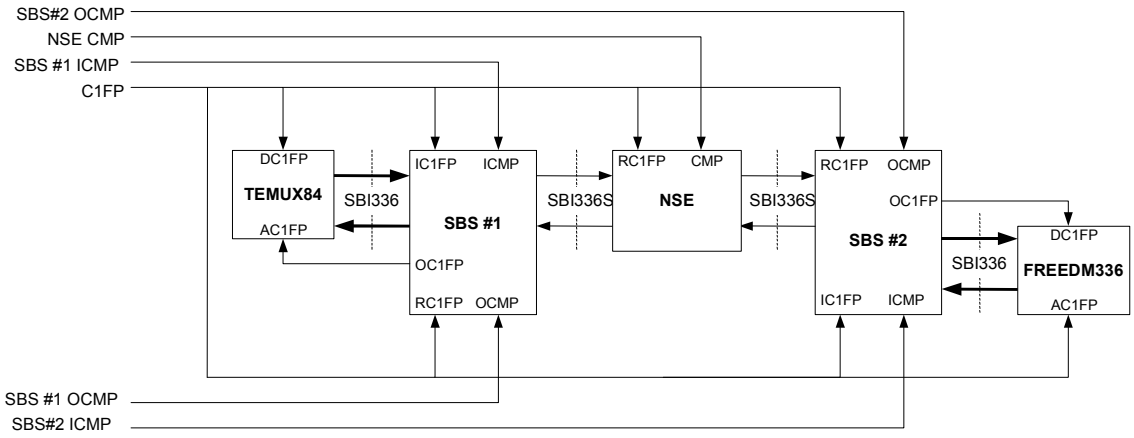


13.14.2 SBS/NSE Systems Switching DS0s Without CAS

This is very similar to the DS0 switching system configuration with CAS described in the previous section. The only difference is that in this system the global C1FP can be reduced to every SBI multi-frame rather than the longer 48 frame SBI bus signaling multi-frame. The advantage is that there is less latency when making switch configuration changes via the CMP signals.

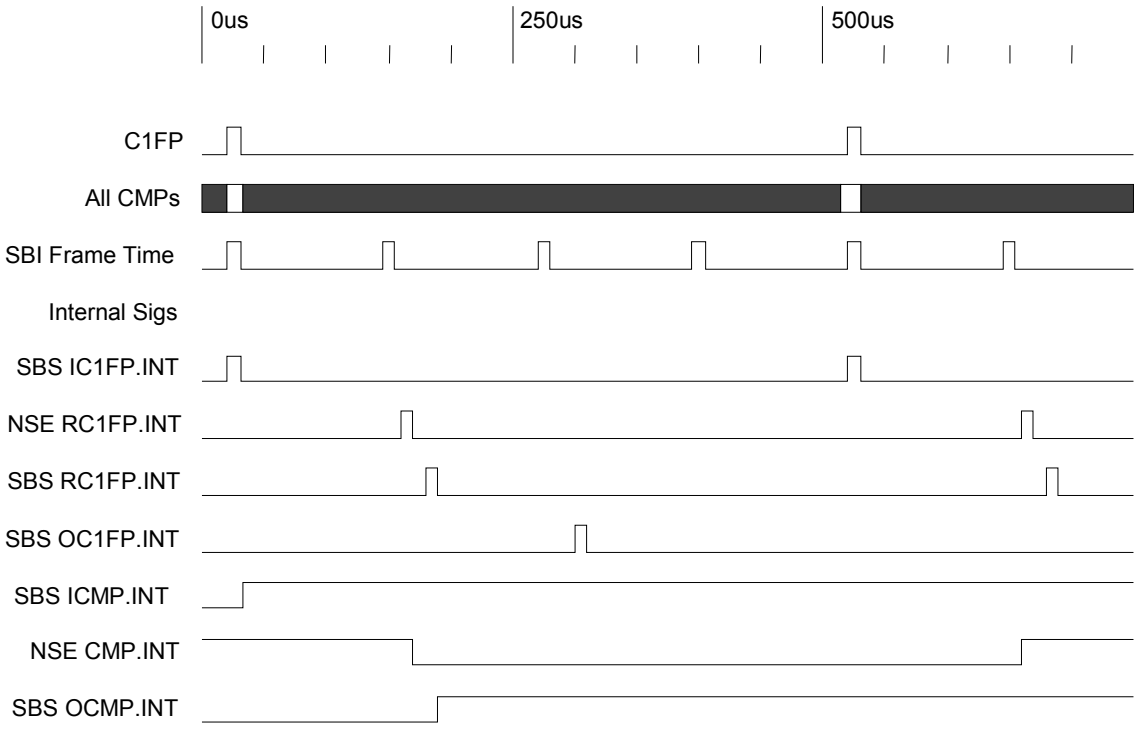
The following diagram shows the system with the FREEDM336 which does not require Channel Associated Signaling. Notice that the data latency through the system is the same as the case when switching DS0s with CAS.

Figure 19 Temux84/SBS/NSE/SBS/FREEDM336 System DS0 Switching no CAS



The following timing diagram shows the system timing when in this configuration.

Figure 20 Switch Timing - DSOs Without CAS



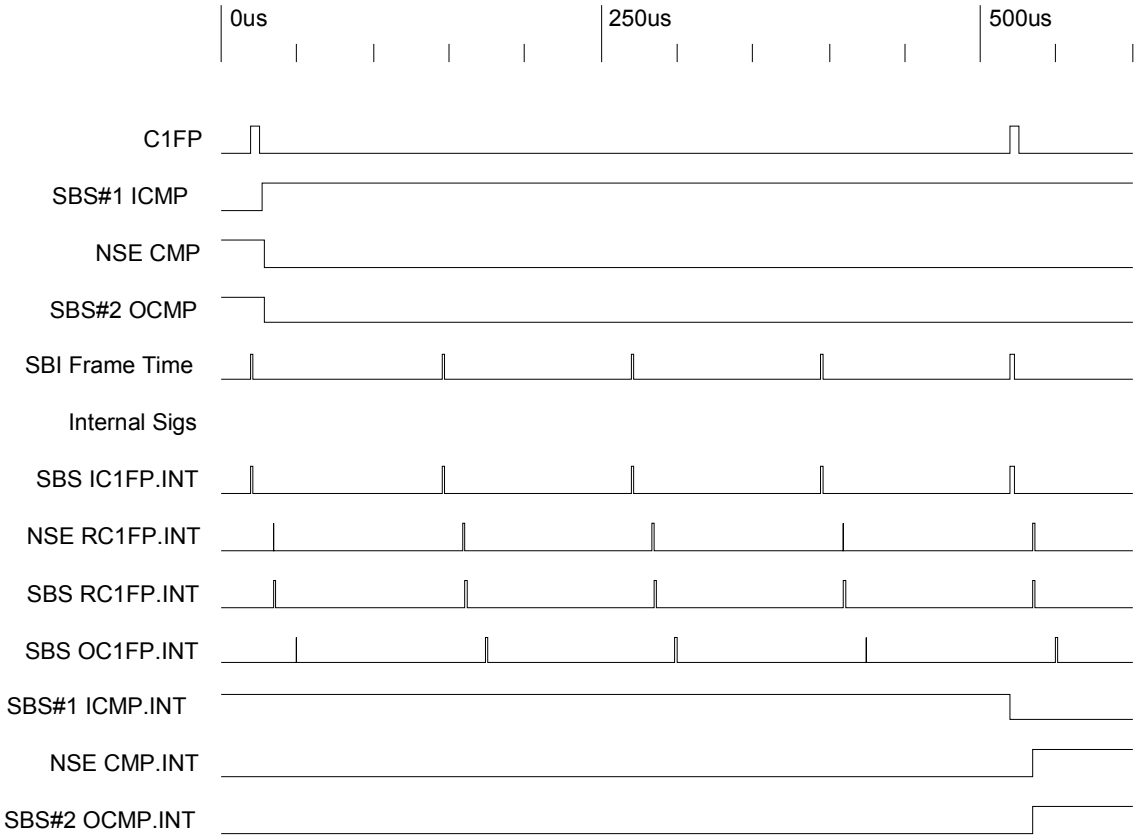
13.14.3 SBS/NSE non-DS0 Level Switching With SBI336 Devices

The SBS and NSE supports another mode of operation that has lower latency and lower power when not switching at the DS0 level. In this mode both of these devices become a column switch rather than a DS0 switch. This also saves SW configuration since only one row of the switch configuration rams has to be configured rather than all nine rows.

When switching DS0 through the system the SBS must store an entire frame of DS0s before routing them to the destination to allow for the last DS0 of a frame to be switched to the first DS0 of the output. When doing column switching only one row of the SBI structure needs to be stored before switching can take place.

The same diagram from the previous section can be used here. The following timing diagram shows the system timing for this mode of operation.

Figure 21 Non DS0 Switch Timing



13.15 Device Latency

The following table is a list of the approximate latency of the SBS in various operating modes. No blocks are bypassed (see register 004H)

Mode	Latency (SYSCLK cycles)
TX Serial: 77MHz DS0 switching mode, TX FIFO centered	9752
TX Serial: 77MHz Column switching mode, TX FIFO centered	1112
RX Serial: 77MHz DS0 switching mode, RC1DLY centre of range	9748
RX Serial: 77MHz Column switching mode, RC1DLY centre of range	1108
TX Parallel : 77MHz SBI DS0 switching mode	9741
TX Parallel: 77MHz SBI Column switching mode	1101
TX Parallel : 19MHz SBI DS0 switching mode	9743
RX Parallel: 77MHZ DS0 switching mode	9742
RX Parallel: 77MHz Column switching mode	1102
RX Parallel: 19MHz DS0 switching mode	9744

13.16 Switch Setting Algorithm.

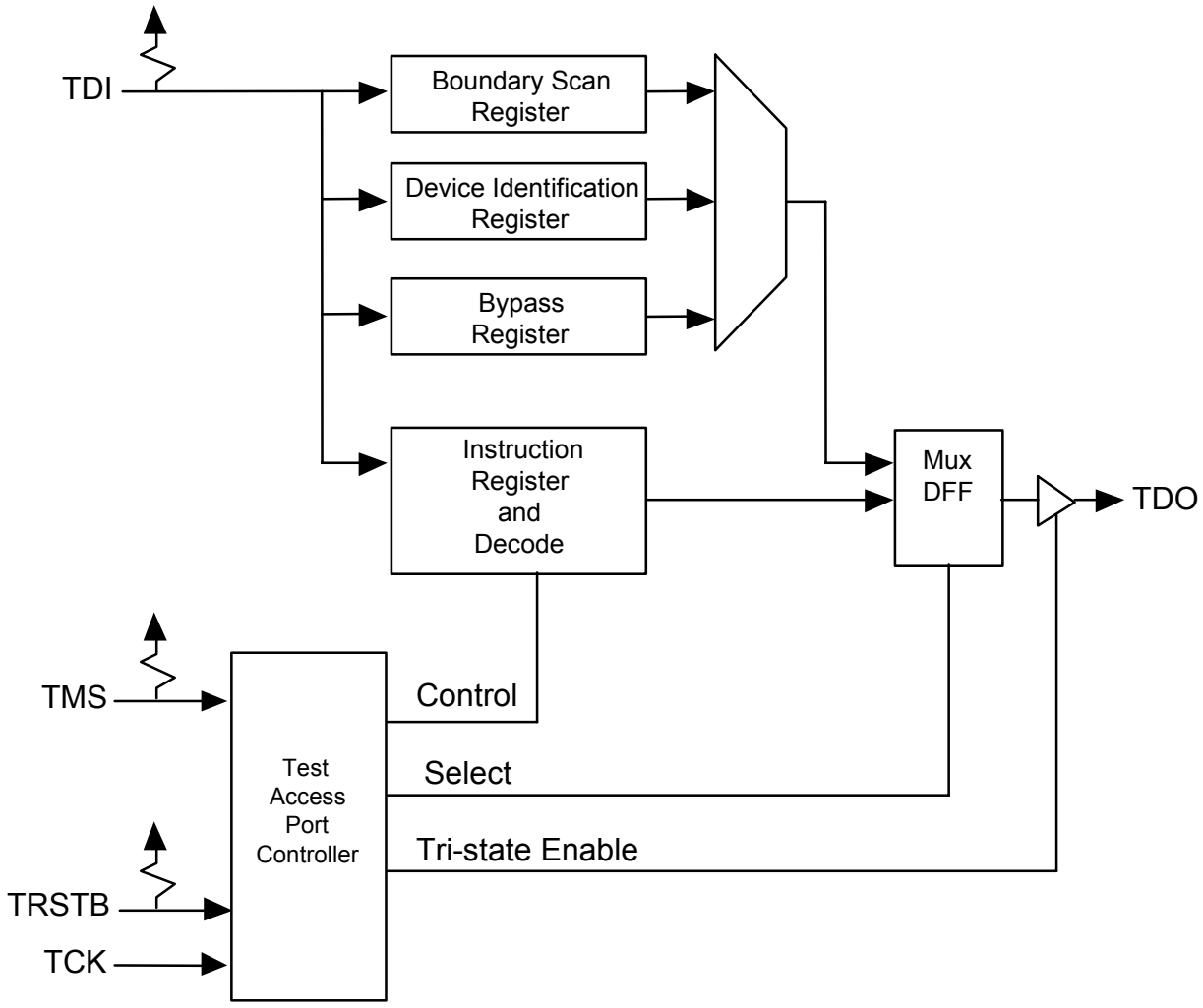
Please see the Open Path Algorithm (OPA), Chip Set Driver (CSD) and the related CHESS-Narrowband application notes for more information on the switch setting algorithms and software support.

CHESS-Narrowband Open Path Algorithm API Design Specification (PMC-2010601)
Open Path Algorithm Application Note (PMC-2012161)
NSE/SBS Narrowband Chipset Driver Design Specification (PMC-2002294)

13.17 JTAG Support

The SBS supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins; TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 28 Boundary Scan Architecture



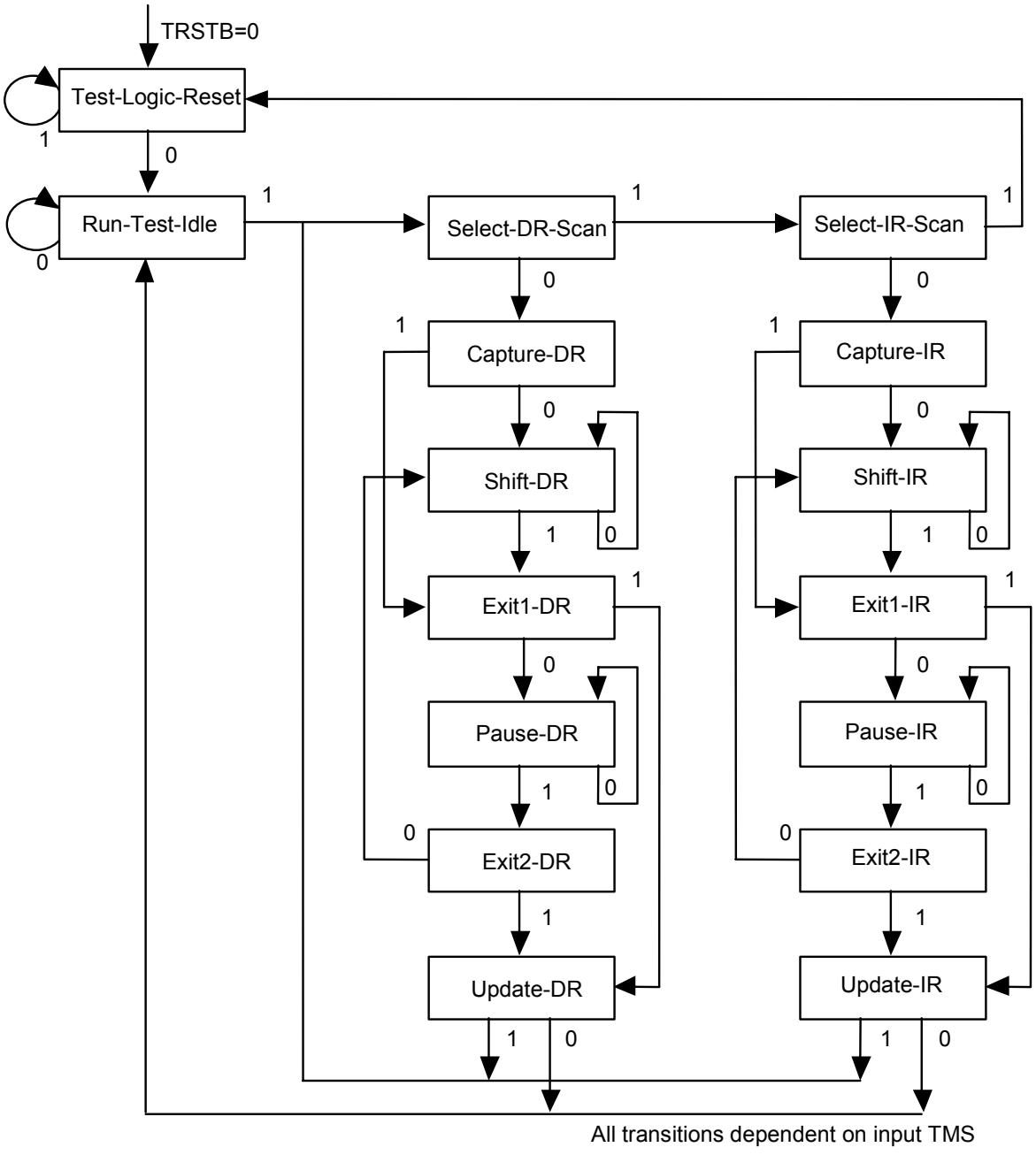
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.17.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 29 TAP Controller Finite State Machine



13.17.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

13.17.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

14 Functional Timing

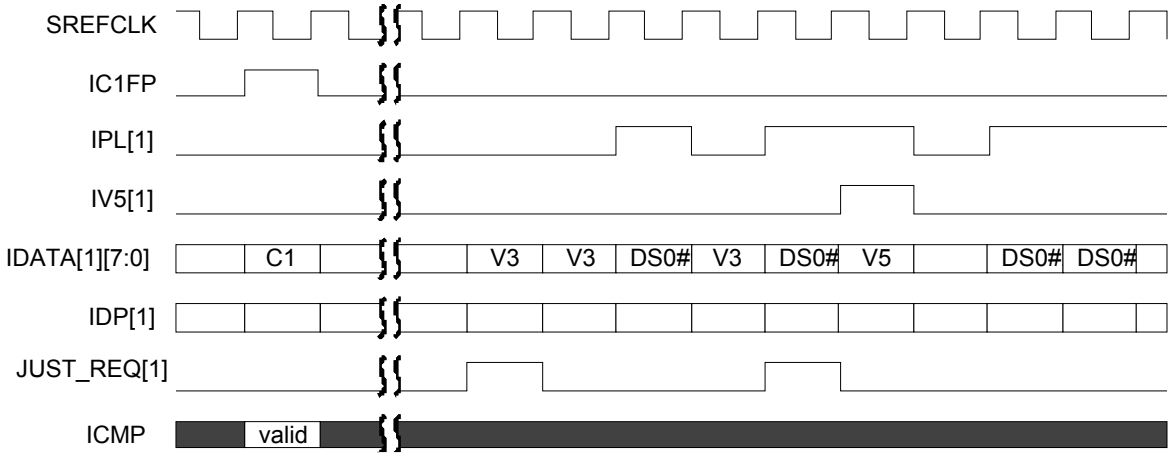
14.1 Incoming SBI336 Bus Functional Timing

Figure 30 shows the functional timing for the incoming SBS 77.76MHz SBI336 bus configured for connection to a physical layer device. When configured for the SBI336 bus timing is provided by a 77.76MHz SREFCLK which is also connected to SYSCLK. When connecting to a physical layer device the justification request signal, JUST_REQ, is used by the physical layer device to control link timing from a slave link layer device and is an input to the SBS.

Figure 30 shows a number of capabilities of the SBI bus. IC1FP is a 2KHz pulse that indicates the SBI336 frame alignment from which all control signals and data are synchronized. The payload signal indicates valid tributary data as well as positive and negative tributary timing adjustments. In Figure 30 the first occurrence of IPL[1] high shows a negative timing adjustment where valid data is carried in the V3 location. The last cycle with IPL[1] low indicates a positive timing adjustment in the tributary octet after V3 where there is no valid data. The IV5[1] signal indicates that the current data octet is the V5 octet used for tributary framing alignment. The JUST_REQ[1] signal is only valid during the V3 octets and the tributary octets following the V3 octets. The first occurrence of JUST_REQ[1] high during the V3 octet indicates to the slave link layer device that it should speed next frame by performing a negative timing adjustment. The second occurrence of JUST_REQ[1] high during the tributary octet after the V3 octet indicates to the slave link layer device that it should slow down by performing a positive timing adjustment during the next frame. The last V3 in the diagram is meant to be the last V3 for all the tributaries.

The ICMP signal selects the active connection memory page in the memory switch. It is sampled at the C1 byte position in every multi-frame. ICMP is ignored at all other positions within the SBI frame. The connection memory page is switched on the next SBI bus multi-frame boundary after ICMP is sampled. The SBI multi-frame can be either 4 or 48 frames, depending on the value of MF_48 in the SBS Master Configuration Register.

Figure 30 Incoming SBI336 Functional Timing



When configured as connecting to a link layer device the JUST_REQ[1] signal is an output synchronized to OC1FP rather than IC1FP as shown in Figure 30. With the exception of the JUST_REQ[1] signal, the functional timing of the incoming SBI336 bus is the same when connecting to a Link Layer device as connecting to a physical layer device.

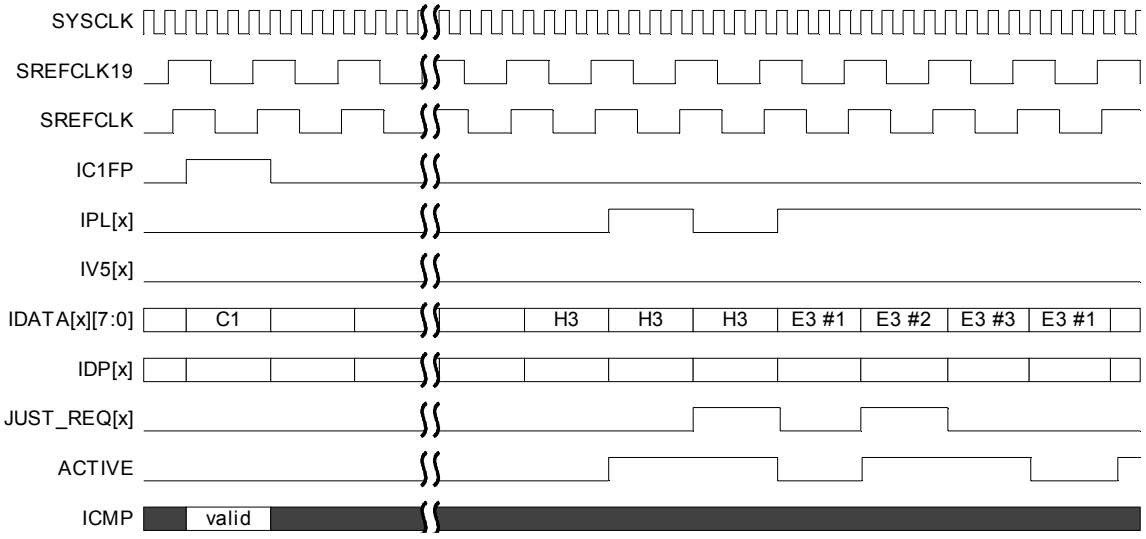
14.2 Incoming SBI Bus Functional Timing

Figure 31 shows the functional timing for the four incoming SBI buses. When in SBI mode SREFCLK is a 19.44MHz clock sourced from SREFCLK19 which is generated from SYSCLK. Figure 31 shows the timing for a 19.44MHz SBI bus configured as connecting to a link layer device carrying three E3 links. When configured for SBI mode connecting to a link layer device the JUST_REQ[x] signal is an output synchronized to IC1FP. All other signals in Figure 31 are inputs.

The first occurrence of IPL[x] in Figure 31 shows a negative timing justification during the H3 octet. During this H3 octet there would be actual data for E3#2. The IV5[x] signal would be asserted during any octet carrying a V5 payload indicator. JUST_REQ[x] in this timing diagram indicates to the link layer device that it should do a positive timing justification on tributary E3#3 and a negative timing justification on tributary E3#2 during the next SBI frame.

With the SBI bus there is also an ACTIVE signal that indicates when a particular SBI device is driving the bus. In Figure 31 the link layer device is configured for E3#2 and E3#3 as indicated by ACTIVE going high during these tributaries.

Figure 31 Incoming SBI Functional Timing



When configured as connecting to physical layer device, JUST_REQ[x] is an input synchronized to OC1FP, therefore JUST_REQ[x] would not be included in the incoming SBI functional timing diagram when configured for connecting to a physical layer device.

Some SBI devices share a common SBI C1FP signal which locks both the incoming and outgoing SBI buses together. The SBS is not able to support this mode and requires separate incoming IC1FP and outgoing OC1FP SBI frame alignment. This is necessary due to the propagation times through the SBS devices. If these C1FP pulses were to align significant buffering and latency would be added to the system.

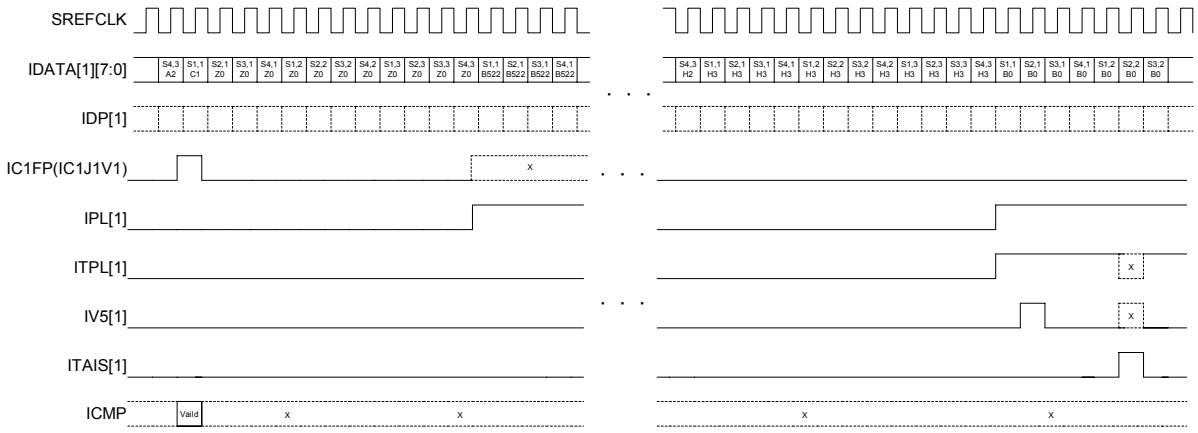
14.3 Incoming 77MHz Telecom Bus Functional Timing

Figure 32 shows the timing of the Incoming Telecom bus stream when configured for 77.76MHz mode. Timing is provided by SREFCLK. SONET/SDH data is carried in the IDATA[1][7:0]. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The IPL[1] signal is set high to mark payload bytes and is set low at all other bytes. Similarly, ITPL[1] is set high to mark tributary payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal IC1J1V1 is equivalent to the IC1FP in SBI mode and is set high with IPL[1] set low to mark the C1 byte of a transport frame. IC1J1V1/IC1FP is set high with IPL[1] set high to mark the J1 bytes and V1 multi-frame of all the streams within IDATA[1][7:0]. For locked STS/AUs, the SBS requires that all J1s follow immediately after the C1(Z0) or the H3 overhead bytes. The SBS also requires that all H4 multi-frames be aligned forcing all V1 bytes to follow the J1 bytes as shown in Figure 33. Multi-frame alignment is based on the first V1 indication by IC1J1V1 after the twelve J1 bytes. Tributary path frame boundaries are marked by a logic high on the IV5[1] signal. Tributaries in AIS alarm are indicated by the ITAIS[1] signal.

The ICMP signal selects the active connection memory page in the memory switch. It is only valid at the C1 byte position and is ignored at all other positions within the transport frame. The connection memory page is switched on the next telecom bus frame boundary after ICMP is sampled at the C1 byte.

In Figure 32 below, STS-3/STM-1 numbers 1, 2, and 4 are configured for STS-3/AU3 operation. STS-3/STM-1 number 3 is configured for STS-3c/AU4 operation. All streams are shown to have an active offset of 522 by the high level on IPL[1] and IC1J1V1/IC1FP at byte Sx,y/B522. No pointer justifications are shown nor permitted by the SBS. All stream are configured to carry virtual tributaries/tributary units. The payload frame boundary of one such tributary is located at byte S2,1/B0, as marked by a high level on IV5[1]. At byte S2,2/B0, the tributary carried in stream S2,2 (2 (STM-1 #2, AU3 #2) is shown to be in tributary path AIS by the high level on ITAIS[1] signal. The arrangement shown in Figure 32 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

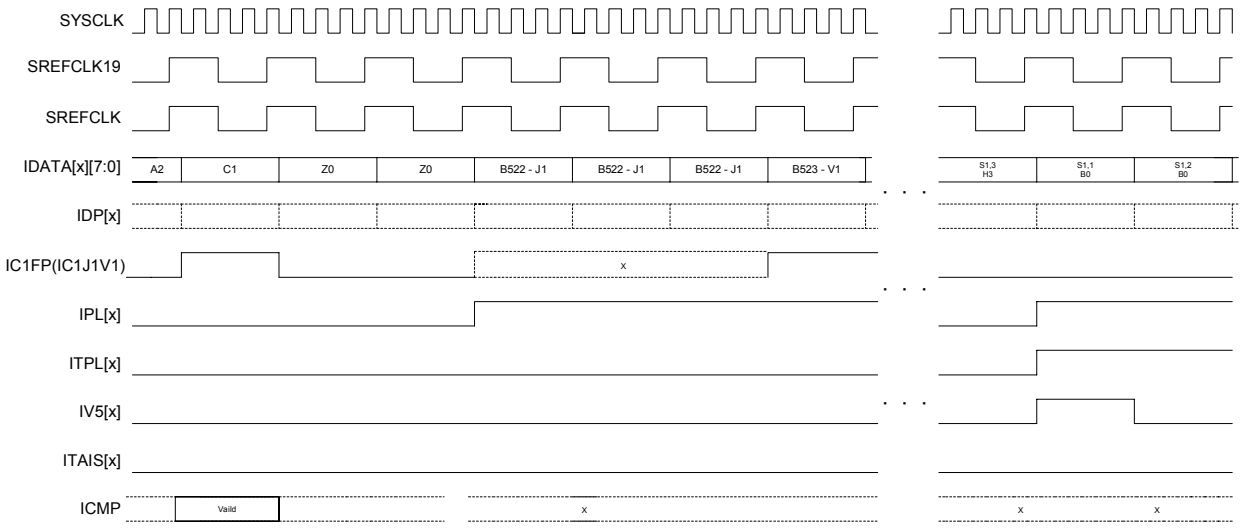
Figure 32 Incoming 77MHz Telecom Bus Functional Timing



14.4 Incoming 19MHz TelecomBus Functional Timing

Figure 33 shows the Incoming Telecom bus interface configured for 19.44MHz mode. The figure is very similar to Figure 32 with one quarter the number of synchronous payload envelopes. Timing is provided by a 19.44MHz SREFCLK sourced from SREFCLK19 which is generated by the SBS from the 77.76MHz SYSCLK.

Figure 33 Incoming 19MHz Telecom Bus Functional Timing

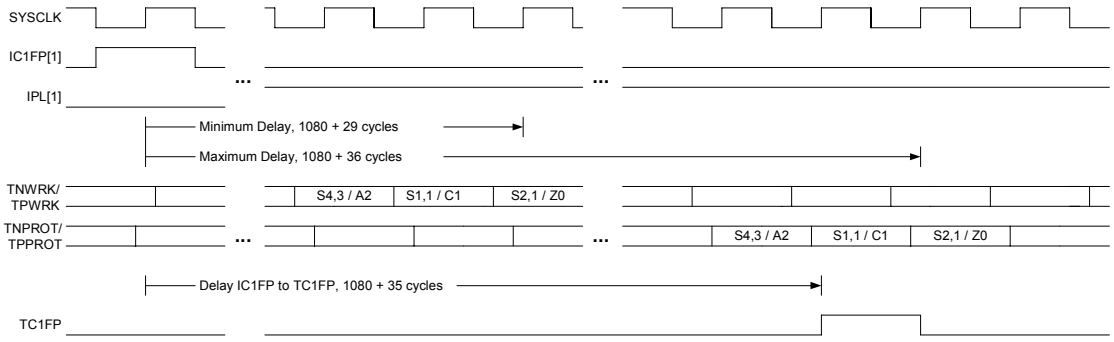


14.5 Transmit Serial LVDS Functional Timing

The delay through the SBS is dependent on the operating mode. The timing from the Incoming Telecom or SBI bus to the LVDS link differs between telecom bus mode and SBI mode. The timing when in SBI mode is also dependent on whether the SBS is switching at the DS0 level and above or is switching only at the tributary level. When switching only tributaries in SBI mode we have the same delay through the SBS as when switching tributaries in telecom bus mode.

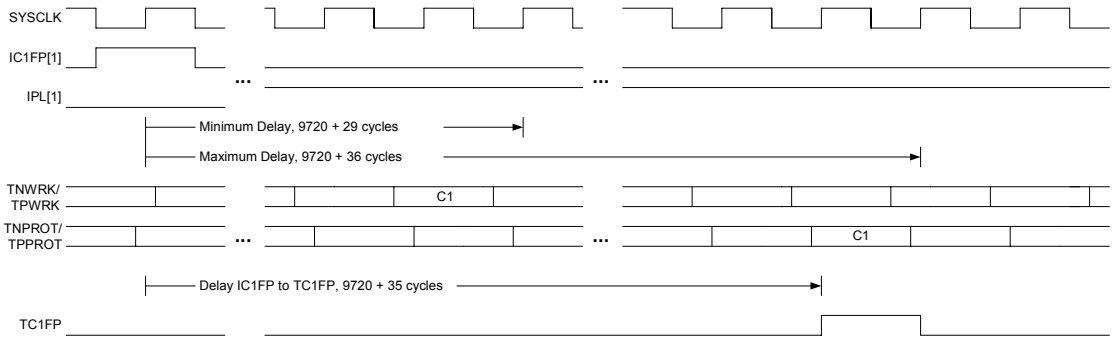
When switching tributaries in SBI mode or when in telecom bus mode the SBS is acting as a column switch. Due to the presence of FIFOs in the data path, the delay to the various links can differ by up to 7 SYSCLK cycles. The minimum delay (1109 SYSCLK cycles) is shown in Figure 34 to be incurred by the transmit working serial data link (TPWRK/TNWRK). This is equivalent to one row (1080 clock cycles) in a 77.76MHz Telecom Bus structure or SBI336 bus structure plus 29 clock cycles through the data path. The maximum delay (1116 SYSCLK cycles) is shown to be incurred by the transmit protection serial data link (TPPROT/TNPROT). The TC1FP output is provided as a reference to indicate the approximate time the C1 characters are being output on the serial link. The relative phases in Figure 34 are shown for illustrative purposes only. Links may have different delays relative the each other than what is shown.

Figure 34 Incoming 77.76MHz Telecom Bus to LVDS Functional Timing



When switching DS0s in SBI mode the delay through the SBS increases. Due to the presence of FIFOs in the data path, the delay to the various links can differ by up to 7 SYSCLK cycles. The minimum delay (9749 SYSCLK cycles) is shown in Figure 35 to be incurred by the transmit working serial data link (TPWRK/TNWRK). This is equivalent to one complete SBI336 frame (9720 clock cycles) plus 29 clock cycles through the data path. The maximum delay (9756 SYSCLK cycles) is shown to be incurred by the transmit protection serial data link (TPPROT/TNPROT). The TC1FP output is provided as a reference to indicate the approximate time the C1 characters are being output on the serial link. The relative phases in Figure 35 are shown for illustrative purposes only. Links may have different delays relative the each other than what is shown.multi-frame

Figure 35 Incoming SBI336 Bus to LVDS Timing with DS0 Switching



When operating in Incoming Bus at 19.44MHz, the delay through the SBS increases by 5 SYSCLK cycles. In column mode, the minimum delay is 1114 SYSCLK cycles and the maximum delay is 1121 SYSCLK cycles. In DS0 mode, the minimum delay is 9754 SYSCLK cycles and the maximum delay is 9761 SYSCLK cycles.

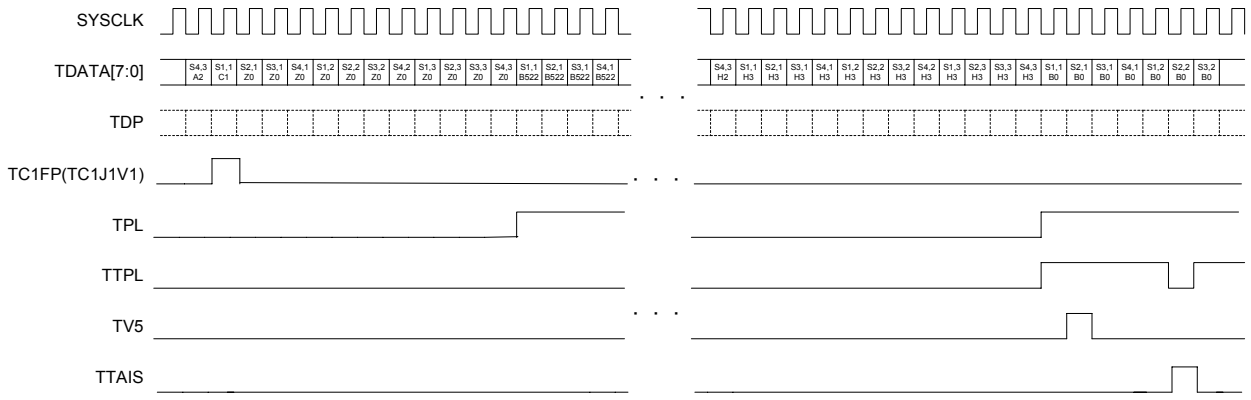
Although Figure 34 and Figure 35 show IC1FP relative to SYSCLK, IC1FP is sampled by SREFCLK.

14.6 Transmit Telecom Bus Functional Timing

The delay from the Incoming telecom bus, either four by 19.44MHz buses or one 77.76MHz bus, to the transmit telecom bus is the same as the delay to the serial LVDS interface. There is a slight difference in the overall delay since the FIFOs of the serial LVDS link are no longer in the path and therefore the absolute delay is more controlled. The total delay is from the incoming telecom bus to the transmit telecom bus is 1080+12 77.76MHz SYSCLK cycles.

Figure 36 shows the transmit telecom bus functional timing. The transmit telecom bus has only a couple of small differences from the incoming 77.76MHz telecom bus, in fact without column switching they could be identical. The main functional difference is in how the TC1FP(TC1J1V1) signal is handled. TC1J1V1 will pulse during the C1 byte position, but must be configured to pulse during the J1 and V1 positions if desired. This is shown in Figure 36.

Figure 36 Transmit Telecom Bus Functional Timing



14.7 Transmit SBI336 Bus Functional Timing

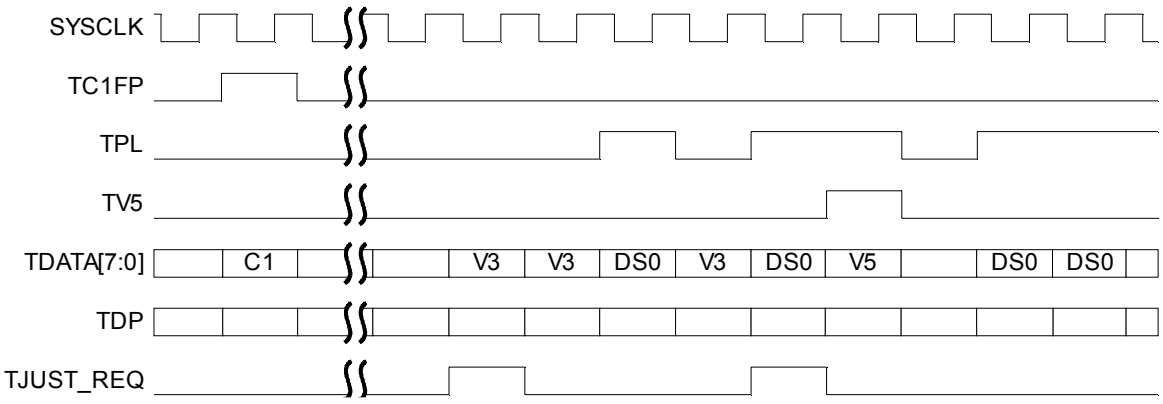
The delay from the Incoming SBI/SBI336 bus to the transmit SBI336 bus is the same as the delay to the serial LVDS interface. There is a slight difference in the overall delay since the FIFOs of the serial LVDS link are no longer in the path and therefore the absolute delay is more controlled.

When switching SBI tributaries the total delay is 1080+12 SYSCLK cycles. When switching DS0s the data delay is 9720+12 SYSCLK cycles and the CAS delay is the T1 or E1 multi-frame + 12 clocks.

The transmit SBI336 interface is functionally the same as the incoming 77.76MHz SBI336 interface. Figure 37 shows the transmit SBI336 bus timing. Like Figure 30 it shows positive and negative timing adjustments via the TPL signal, a V5 tributary frame alignment and positive and negative justification requests via TJUST_REQ.

The use of TJUST_REQ on the transmit SBI336 interface is dependent on whether the SBS is configured as connecting to a physical layer device or link layer device. The interface connection type refers to the Incoming and Outgoing SBI buses therefore the configuration of the transmit SBI336 interface is opposite to that of the Incoming SBI336 bus. In Figure 37 TJUST_REQ is shown as a transmit SBI336 bus output which is consistent with the SBS configured for connection to a physical layer device, meaning that the transmit SBI336 interface is expected to connect to a link layer type device. When the SBS is configured for connection to a link layer device, TJUST_REQ is not used and is held low.

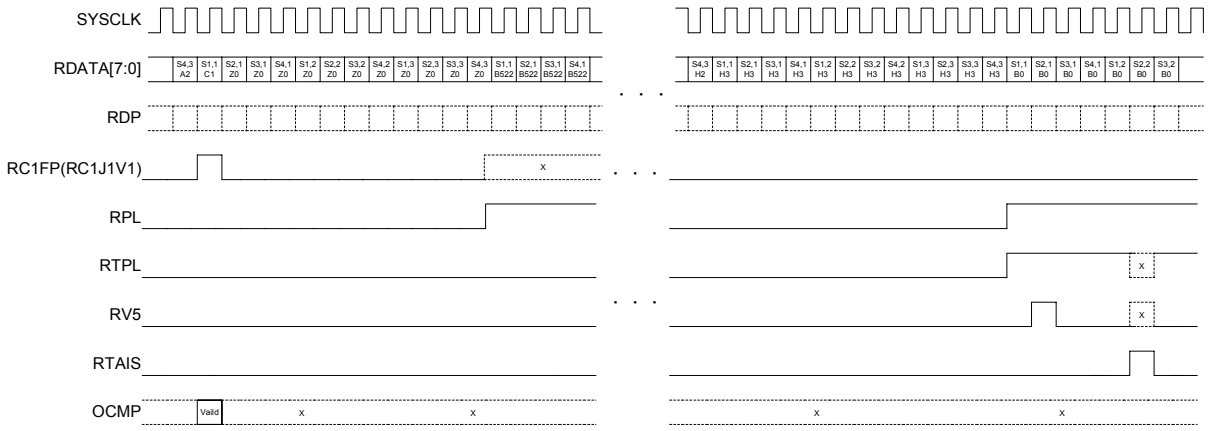
Figure 37 Transmit SBI336 Functional Timing Diagram



14.8 Receive Telecom Bus Functional Timing

Figure 38 shows the receive telecom bus functional timing. This figure is very similar to the Incoming 77.76MHz Telecom Bus Functional Timing shown in Figure 32. The main difference is that the timing is provided by the 77.76MHz SYSCLK.

Figure 38 Receive Telecom Bus Functional Timing

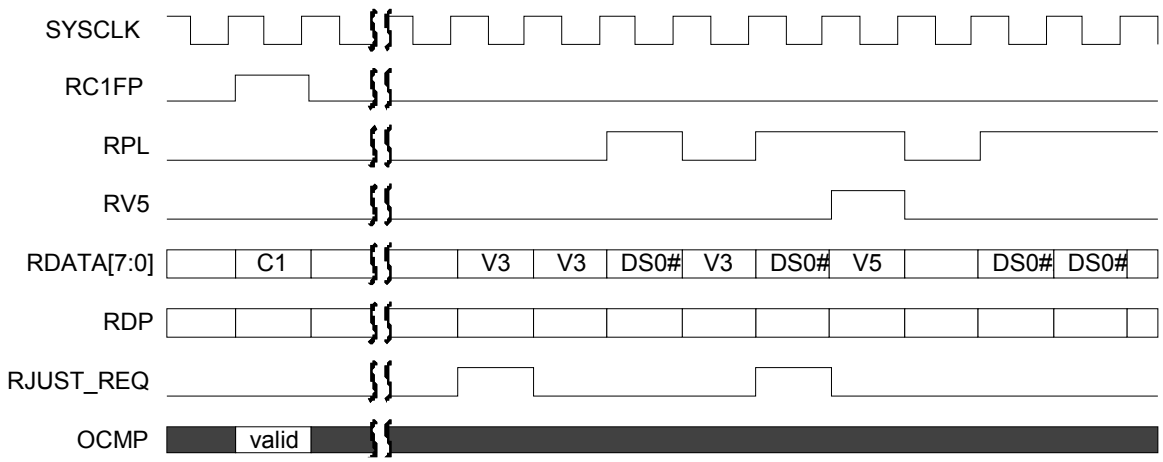


14.9 Receive SBI336 Functional Timing

Figure 39 shows the receive telecom bus functional timing. This figure is very similar to the Incoming SBI336 Functional Timing shown in Figure 30. The main difference is that the timing is provided by the 77.76MHz SYSCLK.

The use of RJUST_REQ on the receive SBI336 interface is dependent on whether the SBS is configured as connecting to a physical layer device or link layer device. The interface connection type refers to the Incoming and Outgoing SBI buses therefore the configuration of the receive SBI336 interface is opposite to that of the Outgoing SBI336 bus. In Figure 39 RJUST_REQ is shown as a receive SBI336 bus input which is consistent with the SBS configured for connection to a link layer device, meaning that the receive SBI336 interface is expected to connect to a physical layer type device. When the SBS is configured for connection to a physical layer device, RJUST_REQ is not used.

Figure 39 Receive SBI336 Functional Timing



14.10 Receive Serial LVDS Functional Timing

Figure 40 below shows the relative timing of the receive LVDS links. Links carry SONET/SDH or SBI336 frame octets that are encoded in 8B/10B characters. Frame boundaries, tributary justification events and tributary alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the Receive Serial Interface Frame Pulse signal (RC1FP). Due to phase noise of clock multiplication circuits and backplane routing discrepancies, the links will not be phase aligned to each other (within a tolerance level of 24 byte times) but are frequency locked The delay from RC1FP being sampled high to the first and last C1 character is shown in Figure 40. In this example, the first C1 is delivered by the working link (RNWRK/RPWRK). The delay to the last C1 represents the time when both links have delivered their C1 character. The minimum value for the internal programmable delay (RC1FPDLY[13:0]) is the delay to the last C1 character plus 15. The maximum value is the delay to the first C1 character plus 31. Consequently, the external system must ensure that the relative delays between all the receive LVDS links be less than 16 bytes. The relative phases of the links in Figure 40 are shown for illustrative purposes only.

Figure 40 Receive LVDS Link Timing

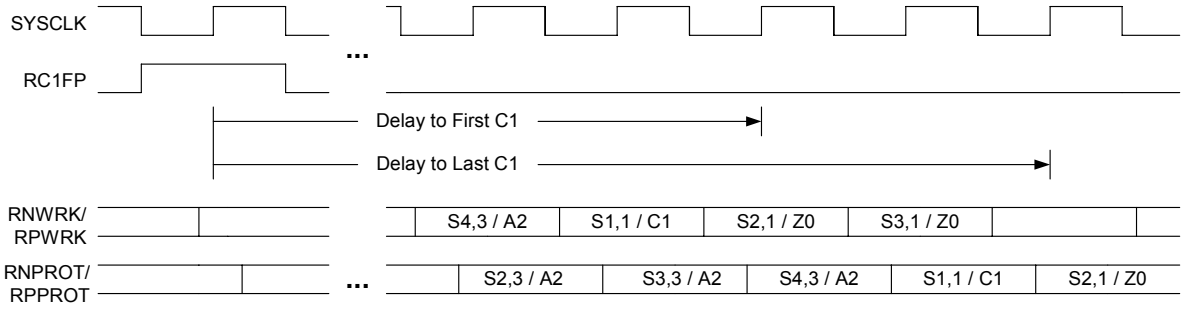
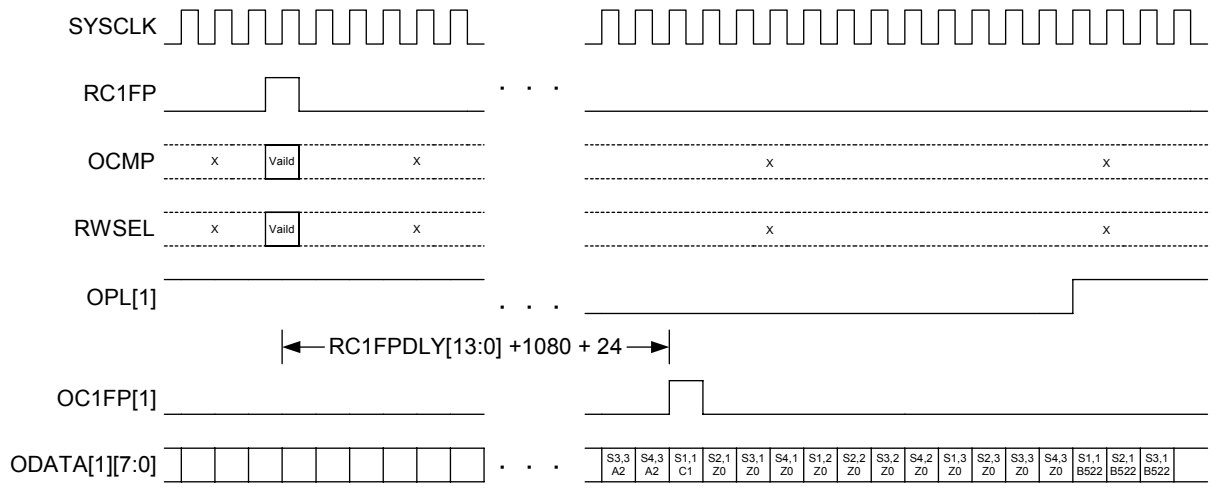


Figure 41 shows the timing relationships around the RC1FP signal. The Outgoing Memory Page selection signal (OCMP) and the Receive Working Serial Data Select signal (RWSEL) are only valid at the SYSCLK cycle at the C1 location as indicated by RC1FP. They are ignored at all other locations within the transport frame. In column switching mode, the delay from RC1FP to the C1 byte on the outgoing Telecom or SBI336 bus stream is the sum of the value programmed into the RC1FPDLY[13:0] register, the OMSU switching latency of 1080 SYSCLK cycles and the processing delay of 24 SYSCLK cycles. In DS0 switching mode, the delay from RC1FP to the C1 byte on the outgoing SBI336 bus stream is the sum of the value programmed into the RC1FPDLY[13:0] register, the OMSU switching latency of 9720 SYSCLK cycles and the processing delay of 24 SYSCLK cycles.

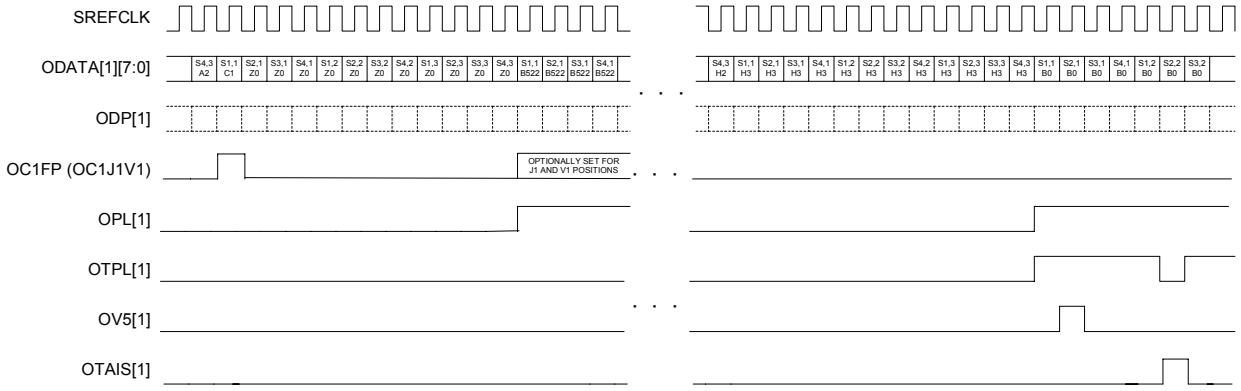
Figure 41 Outgoing Synchronization Timing (77.76MHz Telecom Bus)



14.11 Outgoing 77.76MHz TelecomBus Functional Timing

Figure 42 shows the timing of the Outgoing Telecom bus stream. Timing is provided by SREFCLK. SONET/SDH data is carried on the ODATA[1][7:0] signals. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The OPL[1] signal is set high to mark payload bytes and is set low at all other bytes. Similarly, OTPL[1] is set high to mark tributary payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal, OC1FP[1] (OC1J1V1[1]), is set high with OPL[1] set low to mark the C1 byte of a transport frame. OC1J1V1[1] is optionally set high with OPL[1] also set high to mark the J1 byte and the byte following J1 of all the streams within ODATA[1][7:0]. Tributary path frame boundaries are marked by a logic high on the OTV5[1] signal. Tributaries in AIS alarm are indicated by the OTAIS[1] signal.

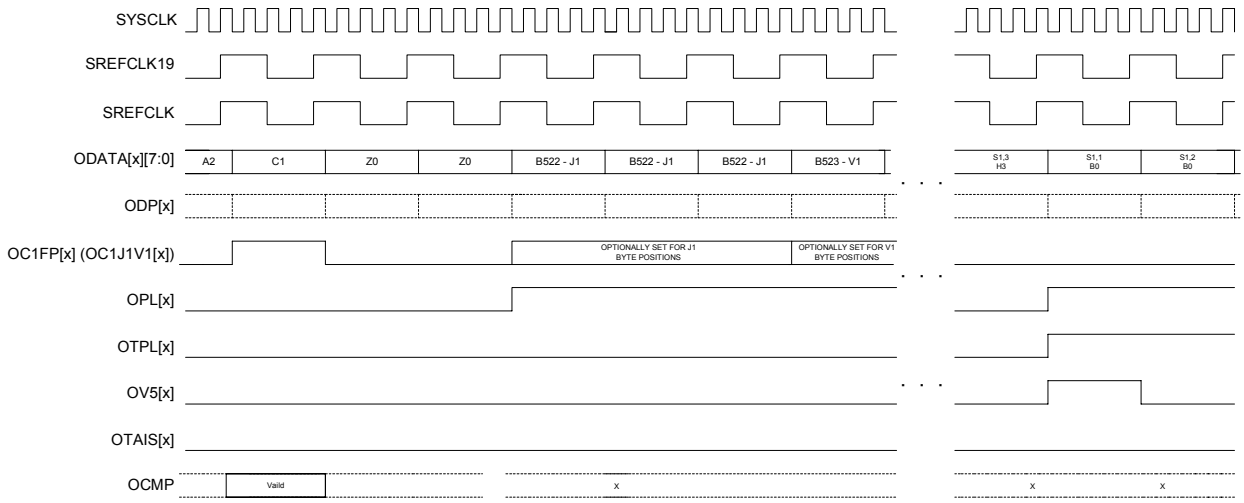
Figure 42 Outgoing 77.76MHz TelecomBus Functional Timing



14.12 Outgoing 19.44MHz TelecomBus Functional Timing

Figure 43 shows the Outgoing Telecom bus interface configured for 19.44MHz mode. The figure is very similar to Figure 42 with one quarter the number of synchronous payload envelopes. Timing is provided by a 19.44MHz SREFCLK sourced from SREFCLK19 which is generated by the SBS from the 77.76MHz SYSCLK.

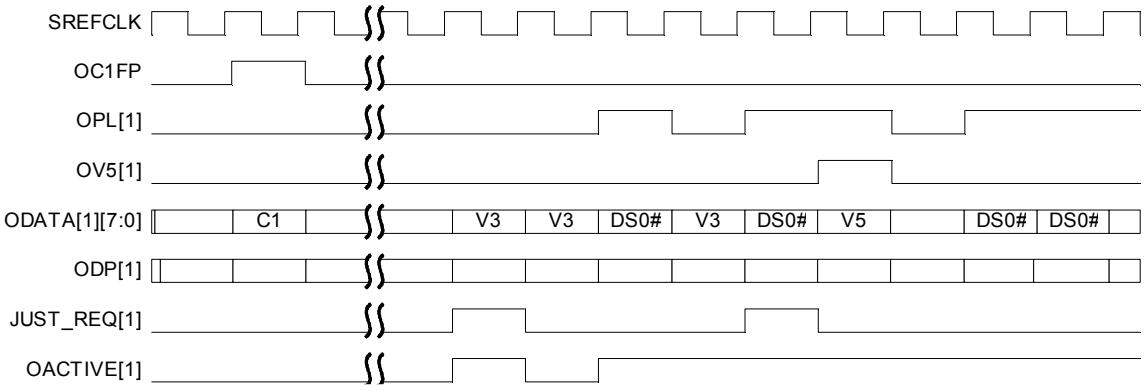
Figure 43 Outgoing 19.44MHz TelecomBus Functional Timing



14.13 Outgoing SBI336 Functional Timing

Figure 44 shows the functional timing for the outgoing 77.76MHz SBI336 bus configured for connection to a link layer device. When configured for the SBI336 bus, timing is provided by a 77.76MHz SREFCLK which is also connected to SYSCLK. When connecting to a link layer device the justification request signal, JUST_REQ[1], is output from the SBS and is used to control the link timing. If the SBS is connected to a physical layer device the JUST_REQ[1] signal is an input synchronized to IC1FP rather than OC1FP. With the exception of the JUST_REQ[1] signal, the functional timing of the outgoing SBI336 bus is the same when connecting to a physical layer device as connecting to a link layer device.

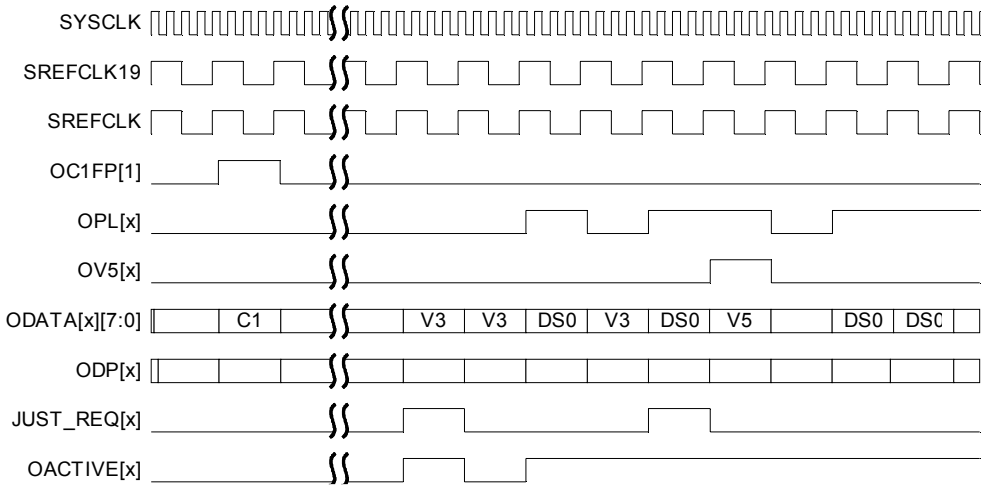
Figure 44 Outgoing SBI336 Functional Timing



14.14 Outgoing SBI Bus Functional Timing

Figure 45 shows the functional timing for 4 outgoing 19.44MHz SBI buses. When configured for the SBI bus, timing is provided by a 19.44MHz SREFCLK sourced from SREFCLK19 which is generated by the SBS from the 77.76MHz SYSCLK. Figure 45 shows the timing for a 19.44MHz SBI bus configured to connect to a physical layer device. In this figure the JUST_REQ[x] signal is an input to the SBS aligned to OC1FP and is used by the physical layer device to control the link timing of a slave link layer device. If the SBS is connected to a link layer device, the JUST_REQ[x] signal would be an output aligned to IC1FP. With the exception of the JUST_REQ[x] signal, the functional timing of the outgoing SBI bus is the same when connecting to a physical layer device as connecting to a link layer device.

Figure 45 Outgoing SBI Bus Functional Timing



15 Absolute Maximum Ratings

Maximum ratings are the worst-case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions. Note: if a voltage is applied to an input pin when the device is powered down, the current needs to be limited below 20mA and the maximum voltage rating does not apply.

Table 28 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
1.8V Supply Voltage (DVDDO, AVDH, CSU_AVDH)	-0.3V to +4.6V
3.3V Supply Voltage (DVDDI, AVDL, CSU_AVDL)	-0.3V to +2.5V
Input Pad Tolerance	-2V < VDDO < +2V for 10ns, 100mA max
Output Pad Overshoot Limits	-2V < VDDO < +2V for 10ns, 20mA max
Voltage on Any Digital Pin	-0.5V to DVDDO+0.5V
Voltage on LVDS Pin	-0.5V to AVDH+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA except RESK, TPWRK, TNWRK, TPPROT, TNPROT, RPWRK, RNWRK, RPPROT and RNPROT
Latch-Up Current on TPWRK, TNWRK, TPPROT, TNPROT, RPWRK, RNWRK, RPPROT and RNPROT	±90 mA
Latch-Up Current on RESK pin	±50 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

16 Power Information

16.1 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
PM8610 (SBS) 4x19.44MHz Incoming/Outgoing interface with Parallel Tx/Rx interface	IDDOP (VDDI)	0.199	—	0.233	A
	IDDOP (VDDO)	0.063	—	0.103	A
	IDDOP (AVDL)	0.078	—	0.123	A
	IDDOP (AVDH)	0.009	—	0.019	A
	Total Power	0.74	0.93	—	W
PM8610 (SBS) 77.76MHz Incoming Outgoing interface with Serial LVDS Tx/Rx interface	IDDOP (VDDI)	0.243	—	0.277	A
	IDDOP (VDDO)	0.078	—	0.132	A
	IDDOP (AVDL)	0.110	—	0.168	A
	IDDOP (AVDH)	0.038	—	0.049	A
	Total Power	1.02	1.28	—	W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T_J=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30 pF, unless otherwise specified)
3. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system
4. High power values are a “normal high power” estimate and are calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T_J=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics

16.2 Power Sequencing

Due to ESD protection structures in the SBS pads it is necessary to exercise caution when powering the IC up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

The 1.8 V supplies can be brought up at the same time or after the 3.3 V supplies as long as the 1.8V supplies never exceed the 3.3V supplies by more than 0.3V.

Analog supplies must not exceed digital supplies of the same nominal voltage by more than 0.3V.

Data applied to I/O pins must not exceed VDDO by more than 0.3V unless the data is current-limited to 20 mA *.

There are no power-up ramp rate restrictions.

The SBS must be powered down according to the same restrictions above.

* These rules are intended to allow for hot-swap of LVDS signals, as the differential links are appropriately current-limited.

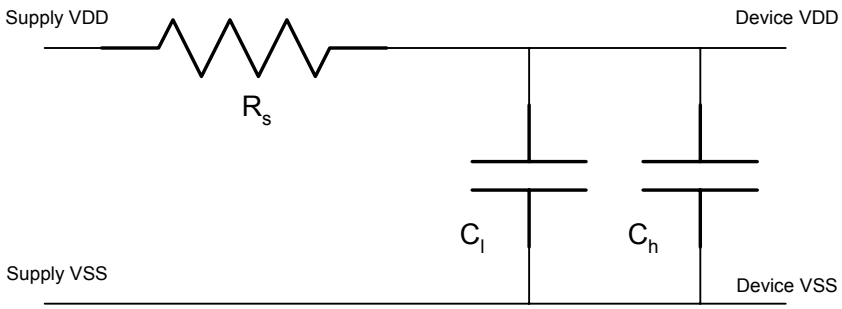
16.3 Analog Power Filtering Recommendations

To achieve best performance of the LVDS links, an analog filter network should be installed between the power balls and the supply.

Table 29 Analog Power Filters

	R_s	C_l	C_h	Notes
CSU_AVDH (1 ball)	3.3-ohm	100nF	10nF	One Filter network per VDD ball.
CSU_AVDL (3 balls)	0.47-ohm	4.7uF	10nF	One Filter network per VDD ball.
AVDH (7 balls)	3.3-ohm	1.0uF	10nF	Two VDD balls per filter network
AVDL (1 ball)	0-ohm	100nF	10nF	One Filter network per VDD ball.

Figure 46 Analog Power Filter Circuit



17 D. C. Characteristics

T_A = -40°C to T_J = +125°C, V_{DDO} = 3.3V ± 5%, V_{DDI} = 1.8V ± 5%
(Typical Conditions: T_C = 25°C, V_{DDO} = 3.3V, V_{DDI} = 1.8V)

Table 30 D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDVDDO	Power Supply	3.14	3.3	3.47	Volts	
VDVDDI	Power Supply	1.71	1.8	1.89	Volts	
VAVDH	Power Supply	3.14	3.3	3.47	Volts	
VCSU_AVDH	Power Supply	3.14	3.3	3.47	Volts	
VAVDL	Power Supply	1.71	1.8	1.89	Volts	
VCSU_AVDL	Power Supply	1.71	1.8	1.89	Volts	
VIL	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
VIL_TCK	Input Low Voltage	0		0.75	Volts	Guaranteed Input Low voltage – TCK only.
VIH	Input High Voltage	2.0		VDDO +0.5	Volts	Guaranteed Input High voltage.
VOL	Output or Bi-directional Low Voltage		0.1	0.4	Volts	Guaranteed output Low voltage at VDDO =3.14V and IOL= maximum rated for pad.
VOH	Output or Bi-directional High Voltage	2.4	2.7		Volts	Guaranteed output High voltage at VDDO =3.14V and IOH= maximum rated for pad.
VT+	Reset Input High Voltage	2.2		VDDO +0.5	Volts	Applies to RSTB and TRSTB only.
VT-	Reset Input Low Voltage	-0.5		0.8	Volts	Applies to RSTB and TRSTB only.
VTH	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB and TRSTB only.
IILPU	Input Low Current	-200	-50	-4	µA	VIL = GND. Notes 1 and 3.
IIHPU	Input High Current	-10	0	+10	µA	VIH = VDDO. Notes 1 and 3.
IIL	Input Low Current	-10	0	+10	µA	VIL = GND. Notes 2 and 3.
IIH	Input High Current	-10	0	+10	µA	VIH = VDDO. Notes 2 and 3.
VICM	LVDS Input Common-Mode Range	0		2.4	V	

Symbol	Parameter	Min	Typ	Max	Units	Conditions
|VIDM|	LVDS Input Differential Sensitivity			100	mV	
RIN	LVDS Differential Input Impedance	85	100	115	Ω	
VLOH	LVDS Output voltage high		1375	1475	mV	RLOAD=100Ω ±1%
VLOL	LVDS Output voltage low	925	1025		mV	RLOAD=100Ω ±1%
VODM	LVDS Output Differential Voltage	300	350	400	mV	RLOAD=100Ω ±1%
VOCM	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	RLOAD=100Ω ±1%
RO	LVDS Output Impedance, Differential	85	110	115	Ω	
|ΔVODM|	Change in |VODM| between “0” and “1”			25	mV	RLOAD=100Ω ±1%
ΔVOCM	Change in VOCM between “0” and “1”			25	mV	RLOAD=100Ω ±1%
ISP, ISN	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
ISPN	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together
CIN	Input Capacitance		5		pF	tA=25°C, f = 1 MHz
COUT	Output Capacitance		5		pF	tA=25°C, f = 1 MHz
CIO	Bi-directional Capacitance		5		pF	tA=25°C, f = 1 MHz

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

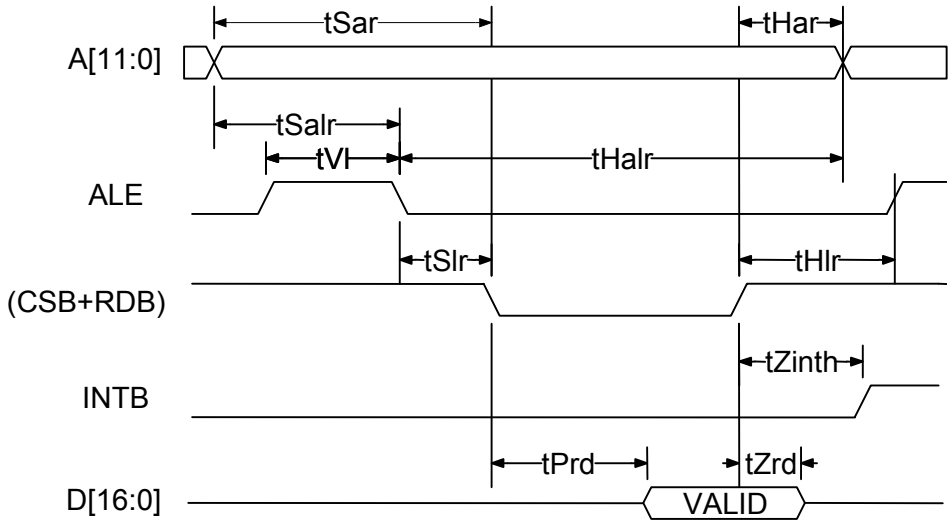
18 Microprocessor Interface Timing Characteristics

(T_A = -40°C to T_J = +125°C, V_{DDO} = 3.3V ± 5%, V_{DDI} = 1.8V ± 5%)

Table 31 Microprocessor Interface Read Access (Figure 47)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	5		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	5		ns
tH_{ALR}	Address to Latch Hold Time	5		ns
tV_{L}	Valid Latch Pulse Width	2		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		15	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		15	ns
tZ_{INTH}	Valid Read Negated to INTB High		20	ns

Figure 47 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

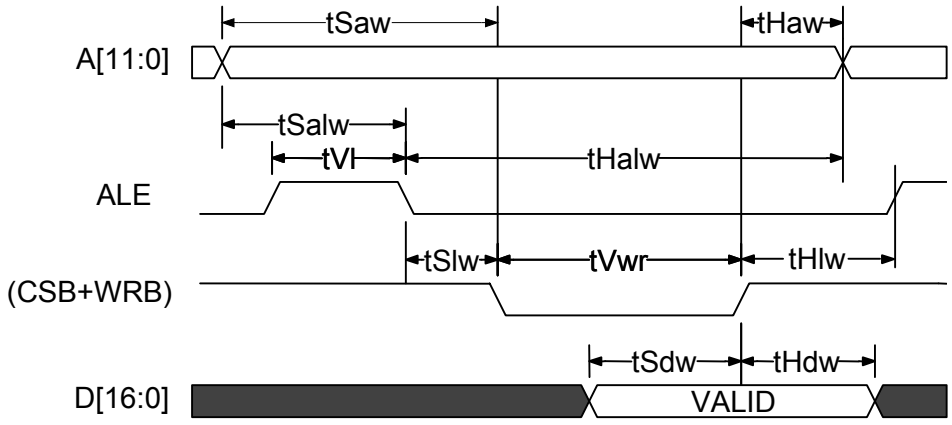
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_{L}, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 32 Microprocessor Interface Write Access (Figure 48)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	5		ns
tS_{DW}	Data to Valid Write Set-up Time	10		ns
tS_{ALW}	Address to Latch Set-up Time	5		ns
tH_{ALW}	Address to Latch Hold Time	5		ns
tV_{L}	Valid Latch Pulse Width	2		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	15		ns

Figure 48 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

19 A.C. timing Characteristics

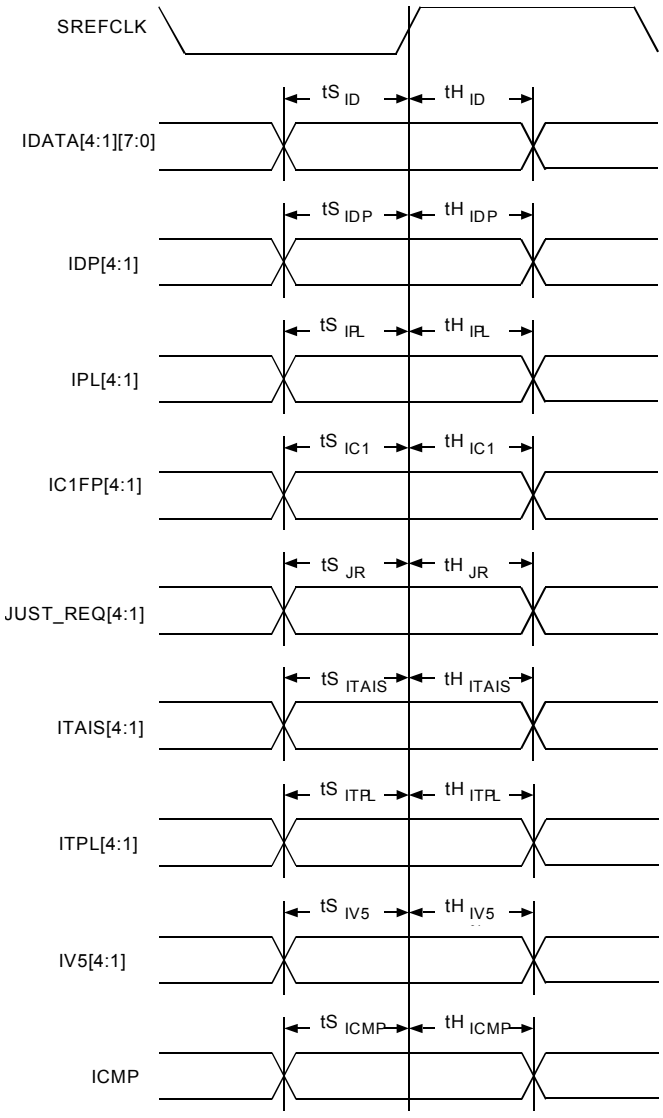
(T_A = -40°C to T_J = +125°C, V_{DDO} = 3.3V ± 5%, V_{DDI} = 1.8V ± 5%)

19.1 SBS Incoming Bus Timing

Table 33 SBS Incoming Timing (Figure 49)

Symbol	Description	Min	Max	Units
	SREFCLK Frequency (nominally 19.44 MHz or 77.76MHz)	-50	+50	ppm
	SREFCLK Duty Cycle	40	60	%
tS_{ID}	IDATA[4:1][7:0] Set-up Time	3		ns
tH_{ID}	IDATA[4:1][7:0] Hold Time	0		ns
tS_{IDP}	IDP[4:1] Set-up Time	3		ns
tH_{IDP}	IDP[4:1] Hold Time	0		ns
tS_{IPL}	IPL[4:1] Set-Up Time	3		ns
tH_{IPL}	IPL[4:1] Hold Time	0		ns
tS_{IC1}	IC1FP[4:1] Set-Up Time	3		ns
tH_{IC1}	IC1FP[4:1] Hold Time	0		ns
tS_{JR}	JUST_REQ[4:1] Set-Up Time	3		ns
tH_{JR}	JUST_REQ[4:1] Hold Time	0		ns
tSITAIS	ITAIS[4:1] Set-Up Time	3		ns
tHITAIS	ITAIS[4:1] Hold Time	0		ns
tSITPL	ITPL[4:1] Set-Up Time	3		ns
tHITPL	ITPL[4:1] Hold Time	0		ns
tS_{IV5}	IV5[4:1] Set-Up Time	3		ns
tH_{IV5}	IV5[4:1] Hold Time	0		ns
tSICMP	ICMP Set-Up Time	3		ns
tHICMP	ICMP Hold Time	0		ns

Figure 49 SBS Incoming Timing



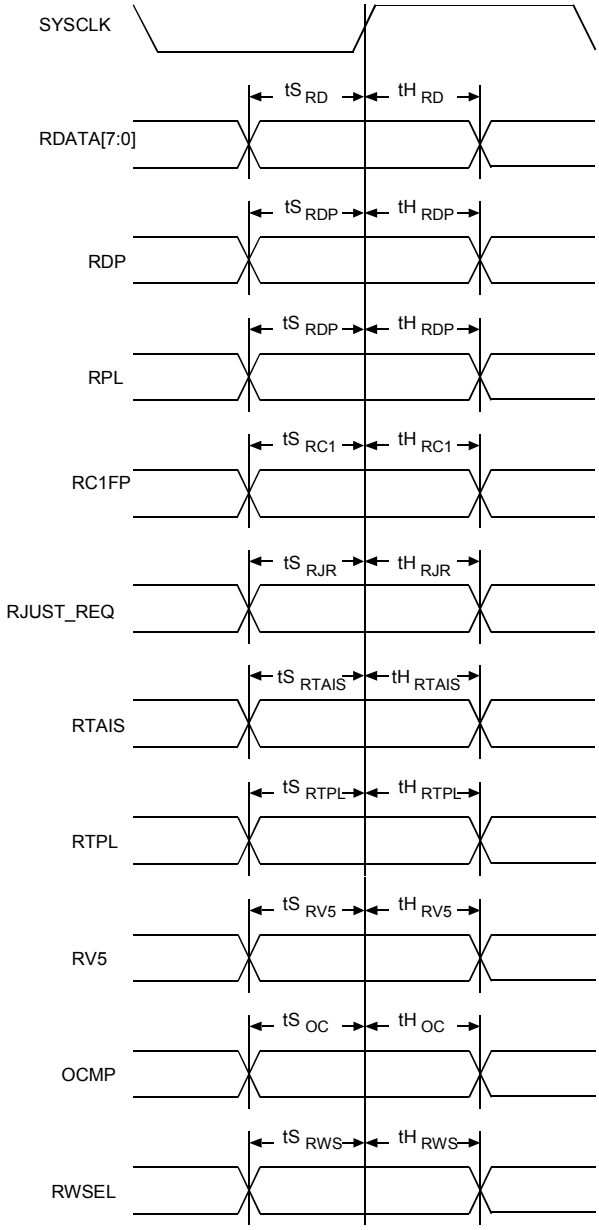
19.2 SBS Receive Bus Timing

Table 34 SBS Receive Timing (Figure 50)

Symbol	Description	Min	Max	Units
	SYSCLK Frequency (nominally 77.76 MHz)	-50	+50	ppm
	SYSCLK Duty Cycle	40	60	%
tS_{RD}	RDATA[7:0] Set-up Time	3		ns
tH_{RD}	RDATA[7:0] Hold Time	0		ns
tS_{RDP}	RDP Set-up Time	3		ns

Symbol	Description	Min	Max	Units
tH_{RDP}	RDP Hold Time	0		ns
tS_{RPL}	RPL Set-Up Time	3		ns
tH_{RPL}	RPL Hold Time	0		ns
tS_{RC1}	RC1FP Set-Up Time	3		ns
tH_{RC1}	RC1FP Hold Time	0		ns
tS_{RJR}	RJUST_REQ Set-Up Time	3		ns
tH_{RJR}	RJUST_REQ Hold Time	0		ns
tS_{RTAIS}	RTAIS Set-Up Time	3		ns
tH_{RTAIS}	RTAIS Hold Time	0		ns
tS_{RPL}	RTPL Set-Up Time	3		ns
tH_{RPL}	RTPL Hold Time	0		ns
tS_{RV5}	RV5 Set-Up Time	3		ns
tH_{RV5}	RV5 Hold Time	0		ns
tS_{OC}	OCMP Set-Up Time	3		ns
tH_{OC}	OCMP Hold Time	0		ns
tS_{RWS}	RWSEL Set-Up Time	3		ns
tH_{RWS}	RWSEL Hold Time	0		ns

Figure 50 SBS Receive Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

19.3 SBS Outgoing Bus Timing

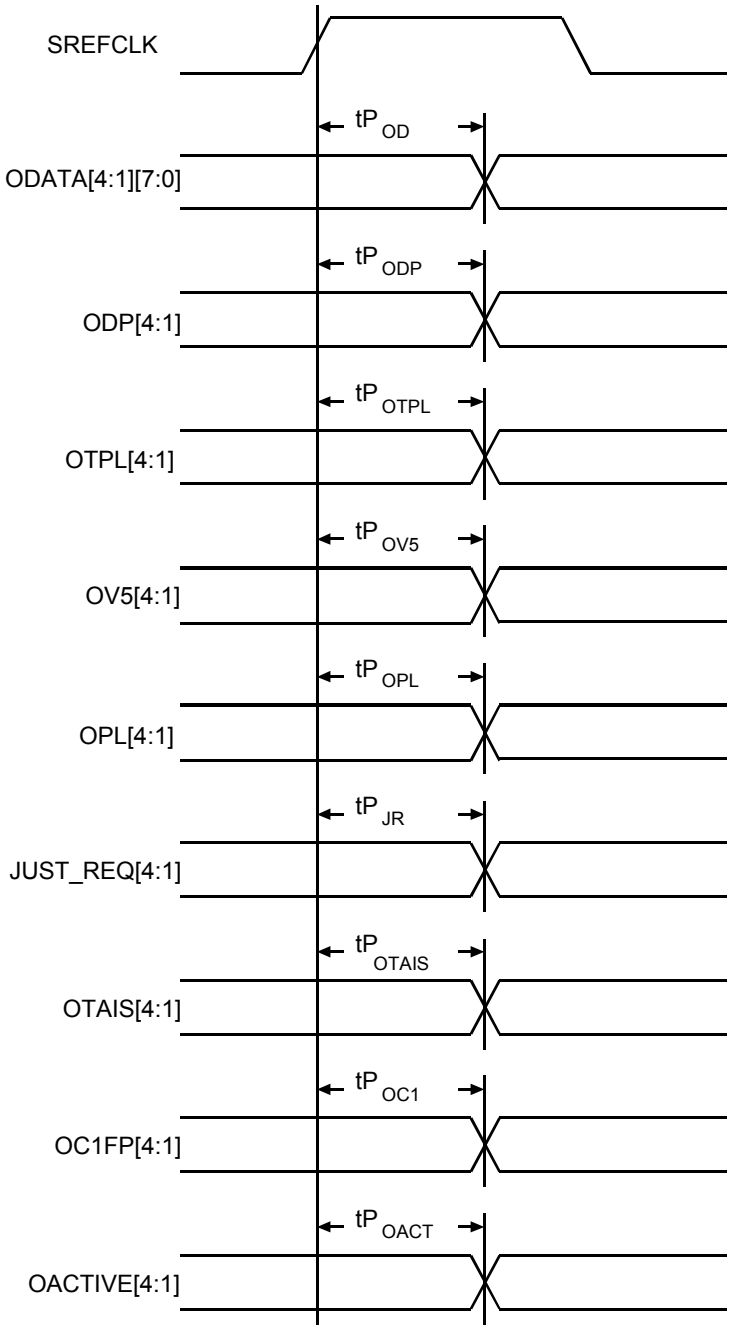
Table 35 SBS Outgoing Timing with 77.76MHz SREFCLK (Figure 51)

Symbol	Description	Min	Max	Units
tP_{OD}	SREFCLK High to ODATA[1][7:0] Valid (77.76MHz SREFCLK)	1	7	ns
tP_{ODP}	SREFCLK High to ODP[1] Valid (77.76MHz SREFCLK)	1	7	ns
tP_{OTPL}	SREFCLK High to OTPL[1] Valid (77.76MHz SREFCLK)	1	7	ns
tP_{OV5}	SREFCLK High to OV5[1] Valid (77.76MHz SREFCLK)	1	7	ns
tP_{OPL}	SREFCLK High to OPL[1] Valid (77.76MHz SREFCLK)	1	7	ns
tP_{JR}	SREFCLK High to JUST_REQ[1] Valid (77.76MHz SREFCLK)	1	7	ns
tP_{OTAIS}	SREFCLK High to OTAIS[1] Valid (77.76MHz SREFCLK)	1	7	ns
tP_{OC1}	SREFCLK High to OC1FP[4:1] Valid (77.76MHz SREFCLK)	1	7	ns

Table 36 SBS Outgoing Timing with 19.44MHz SREFCLK (Figure 51)

Symbol	Description	Min	Max	Units
tP_{OD}	SREFCLK High to ODATA[4:1][7:0] Valid (19.44MHz SREFCLK)	2	20	ns
tP_{ODP}	SREFCLK High to ODP[4:1] Valid (19.44MHz SREFCLK)	2	20	ns
tP_{OTPL}	SREFCLK High to OTPL[4:1] Valid (19.44MHz SREFCLK)	2	20	ns
tP_{OV5}	SREFCLK High to OV5[4:1] Valid (19.44MHz SREFCLK)	2	20	ns
tP_{OPL}	SREFCLK High to OPL[4:1] Valid (19.44MHz SREFCLK)	2	20	ns
tP_{JR}	SREFCLK High to JUST_REQ[4:1] Valid (19.44MHz SREFCLK)	2	20	ns
tP_{OTAIS}	SREFCLK High to OTAIS[4:1] Valid (19.44MHz SREFCLK)	2	20	ns
tP_{OC1}	SREFCLK High to OC1FP[4:1] Valid (19.44MHz SREFCLK)	2	20	ns
tP_{OACT}	SREFCLK High to OACTIVE[4:1] Valid (19.44MHz SREFCLK)	2	20	ns

Figure 51 SBS Outgoing Timing

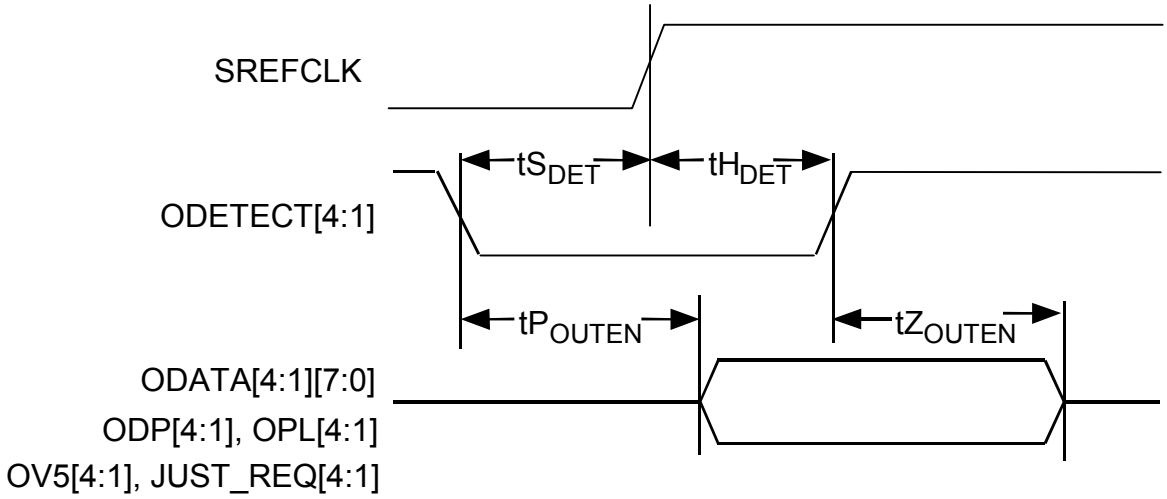


19.4 SBS Outgoing Bus Collision Avoidance Timing

Table 37 SBS Outgoing Bus Collision Avoidance Timing (Figure 52)

Symbol	Description	Min	Max	Units
tS_{DET}	ODETECT[4:1] Set-Up Time	3		ns
tH_{DET}	ODETECT[4:1] Hold Time	3.2		ns
tP_{OUTEN}	ODETECT[4:1] low to all Outgoing Bus Outputs Valid	0	12	ns
tZ_{OUTEN}	ODETECT[4:1] high to all Outgoing Bus Outputs Tristate	0	12	ns

Figure 52 SBS Outgoing Bus Collision Avoidance Timing

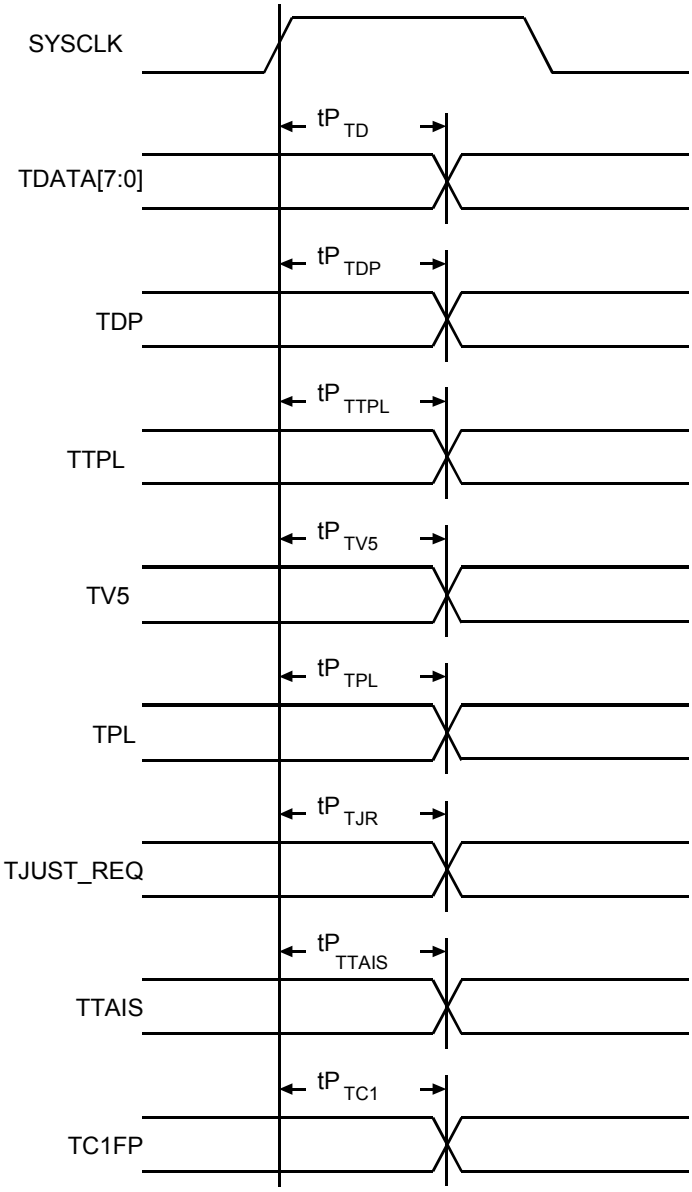


19.5 SBS Transmit Bus Timing

Table 38 SBS Transmit Timing (Figure 53)

Symbol	Description	Min	Max	Units
tP_{TD}	SYSCLK High to TDATA[7:0] Valid	1	7	ns
tP_{TDP}	SYSCLK High to TDP Valid	1	7	ns
tP_{TTPL}	SYSCLK High to TTPL Valid	1	7	ns
tP_{TV5}	SYSCLK High to TV5 Valid	1	7	ns
tP_{TPL}	SYSCLK High to TPL Valid	1	7	ns
tP_{TJR}	SYSCLK High to TJUST_REQ Valid	1	7	ns
tP_{TTAIS}	SYSCLK High to TTAIS Valid	1	7	ns
tP_{TC1}	SYSCLK High to TC1FP Valid	1	7	ns

Figure 53 SBS Transmit Timing



Notes on Output Timing:

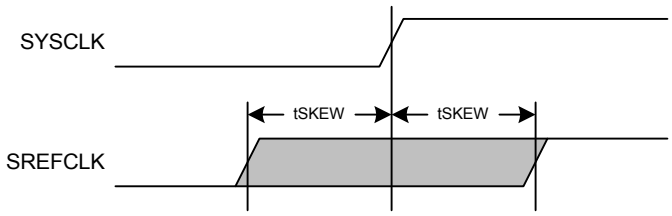
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 50 pF load on the outputs operating at 77.76MHz except where indicated.
3. Output propagation delays are measured with a 100 pF load on the outputs operating at 19.44MHz except where indicated.

19.6 SYSCLK / REFCLK Skew Requirement (77.76MHz mode)

Table 39 SYSCLK / REFCLK Skew Requirement – 77.76MHz mode

Symbol	Description	Min	Max	Units
tSKEW	SREFCLK to SYSCLK Skew (SREFCLK at 77.76MHz)	-1	1	ns

Figure 54 SYSCLK / REFCLK Skew Requirement

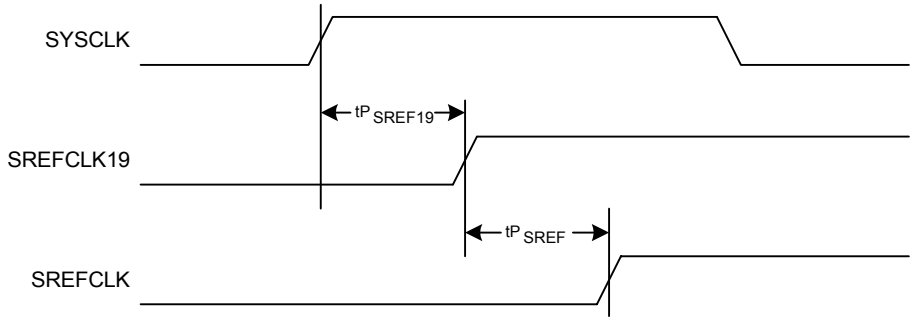


19.7 SYSCLK / SREFCLK Timing (19.44MHz mode)

Table 40 SYSCLK / SREFCLK Timing – 19.44MHz mode

Symbol	Description	Min	Max	Units
tP_{SREF19}	SYSCLK high to valid SREFCLK19	1	7	ns
tP_{SREF}	SREFCLK19 output to SREFCLK input (19.44MHz mode)	0	20	ns

Figure 55 SYSCLK / SREFCLK Timing – 19.44MHz mode



19.8 Serial Interface

Table 41 Serial Interface Timing

Symbol	Description	Min	Typical	Max	Units
fRLVDS	RPWRK, RNWRK, RPPROT, RNPROT Bit Rate	$10f_{SYSCLK}$	$10f_{SYSCLK}$	$10f_{SYSCLK}$	Mbps
tFALL	VODM fall time, 80%-20%,	200	300	400	ps

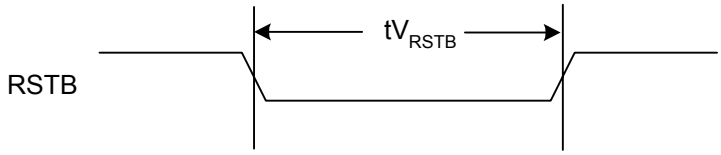
Symbol	Description	Min	Typical	Max	Units
	(RLOAD=100Ω ±1%)				
tRISE	VODM rise time, 20%-80%, (RLOAD=100Ω ±1%)	200	300	400	ps
tSKEW	Differential Skew			50	ps

19.9 RSTB Timing

Table 42 RSTB Timing (Figure 56)

Symbol	Description	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Figure 56 RSTB Timing

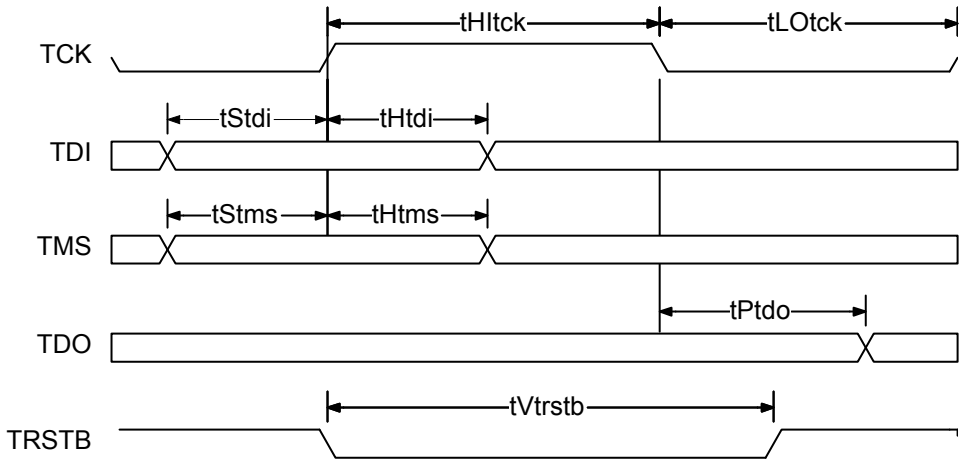


19.10 JTAG Port Interface

Table 43 JTAG Port Interface (Figure 57)

Symbol	Description	Min	Max	Units
FTCK	TCK Frequency		4	MHz
THITCK	TCK HI Pulse Width	100		ns
THITCK	TCK LO Pulse Width	100		ns
TSTMS	TMS Set-up time to TCK	25		ns
THTMS	TMS Hold time to TCK	25		ns
TSTDI	TDI Set-up time to TCK	25		ns
THTDI	TDI Hold time to TCK	25		ns
TPTDO	TCK Low to TDO Valid	2	35	ns
TVTRSTB	TRSTB Pulse Width	100		ns

Figure 57 JTAG Port Interface Timing



20 Ordering Information

Part No.	Description
PM8610-BI	352-pin Ball Grid Array (UBGA)

21 Thermal Information

The SBS is designed to operate over a wide temperature range and is suited for outside plant equipment[1].

Table 44 Outside Plant Thermal Information

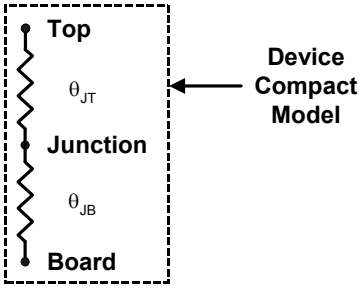
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when local ambient reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 45 Thermal Resistance vs. Air Flow[3]

Airflow	Natural Convection	200 LFM	400 LFM
θ_{JA} (°C/W)	16.7	11.45	10.14

Table 46 Device Compact Model[4]

Junction-to-Top Thermal Resistance, θ_{JT}	0.3 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	7.08 °C/W



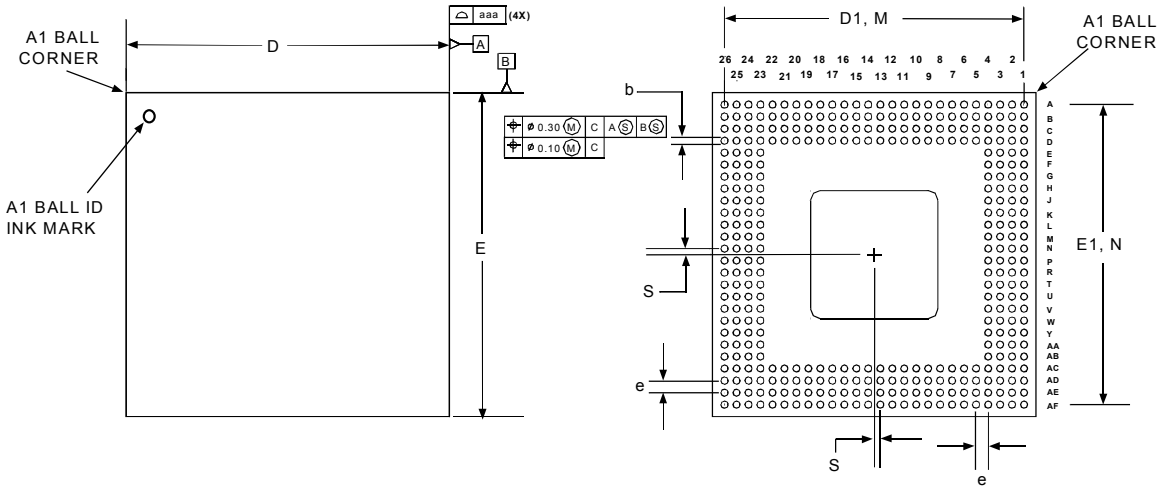
Power depends upon the operating mode. To obtain power information, refer 'High' power values in section 16 Power Requirements.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core.
3. θ_{JA}, the total junction to ambient thermal resistance, is measured according to JEDEC Standard JESD51 (2S2P).
4. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8 and θ_{JT}, the junction-to-top thermal resistance, is obtained by simulating conditions described in SEMI Standard G30-88.

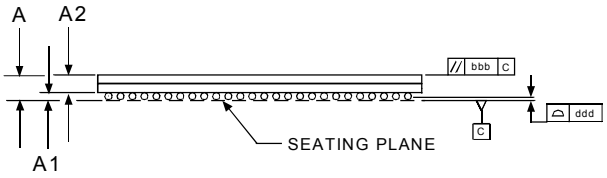
22 Mechanical Information

Figure 58 352 Pin UBGA 27x27mm Body



TOP VIEW

BOTTOM VIEW



SIDE VIEW

NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 352 THERMALLY ENHANCED BALL GRID ARRAY - UBGA																
BODY SIZE : 27 x 27 x 1.41 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	d	e	aaa	bbb	ddd	S	
Min.	1.26	0.40	0.86	26.90	-	26.90	-	-	0.50	-	-	-	-	-	0.45	
Nom.	1.41	0.50	0.91	27.00	25.00	27.00	25.00	26x26	0.63	-	1.00	-	-	-	0.56	
Max.	1.56	0.60	0.96	27.10	-	27.10	-	-	0.70	0.20	-	0.20	0.25	0.20	0.55	

Notes