

P10C68/P11C68

(Previously PNC10C68 and PNC11C68)

CMOS/SNOS NVSRAM

HIGH PERFORMANCE 8 K x 8 NON-VOLATILE STATIC RAM

(Supersedes DS3159-1.3, DS3160-1.3, DS3234-1.1, DS3235-1.1)

The P10C68 and P11C68 are fast static RAMs (35 and 45 ns) with a non-volatile electrically-erasable PROM (EEPROM) cell incorporating in each static memory cell. The SRAM can be read and written an unlimited number of times while independent non-volatile data resides in PROM.

On the P10C68 data may easily be transferred from the SRAM to the EEPROM (STORE) and from the EEPROM back to the SRAM (RECALL) using the NE (bar) pin. The Store and Recall cycles are initiated through software sequences on the P11C68. These devices combine the high performance and ease of use of a fast SRAM with the data integrity of non-volatility.

The P10C68 and P11C68 feature the industry standard pinout for non-volatile RAMs in a 28-pin 0.3-inch plastic and ceramic dual-in-line packages.

FEATURES

- Non-Volatile Data Integrity
- 10 year Data Retention in EEPROM
- 35ns and 45ns Address and Chip Enable Access Times
- 20ns and 25ns Output Enable Access
- Unlimited Read and Write to SRAM
- Unlimited Recall Cycles from EEPROM
- 10⁴ Store Cycles to EEPROM
- Automatic Recall on Power up
- Automatic Store Timing
- Hardware Store Protection
- Single 5V ± 10% Operation
- Available in Standard Package 28-pin 0.3-inch DIL plastic and ceramic
- Commercial and Industrial temperature ranges

ORDERING INFORMATION

(See back page)

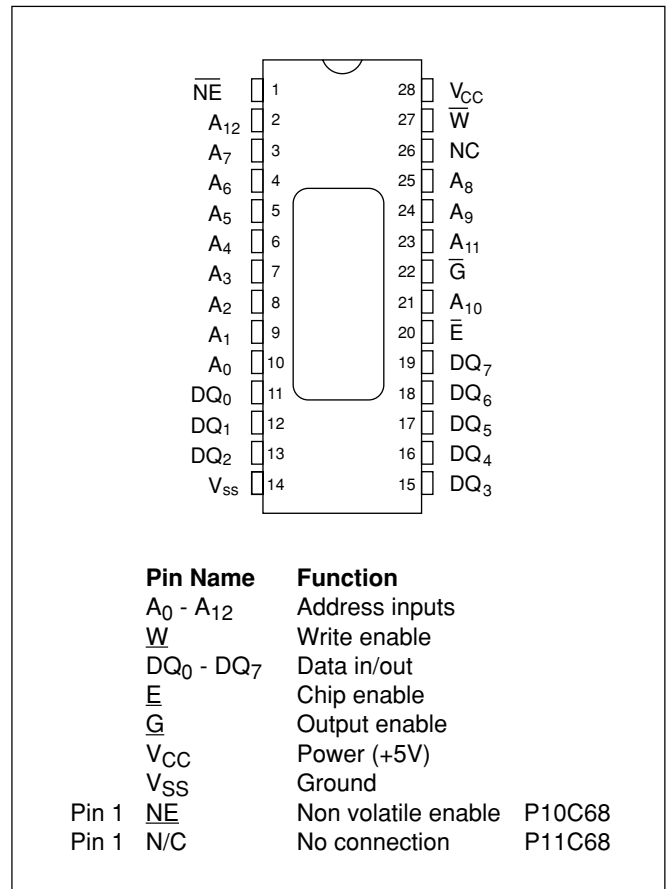


Figure 1. Pin connections - top view.

P10C68/P11C68

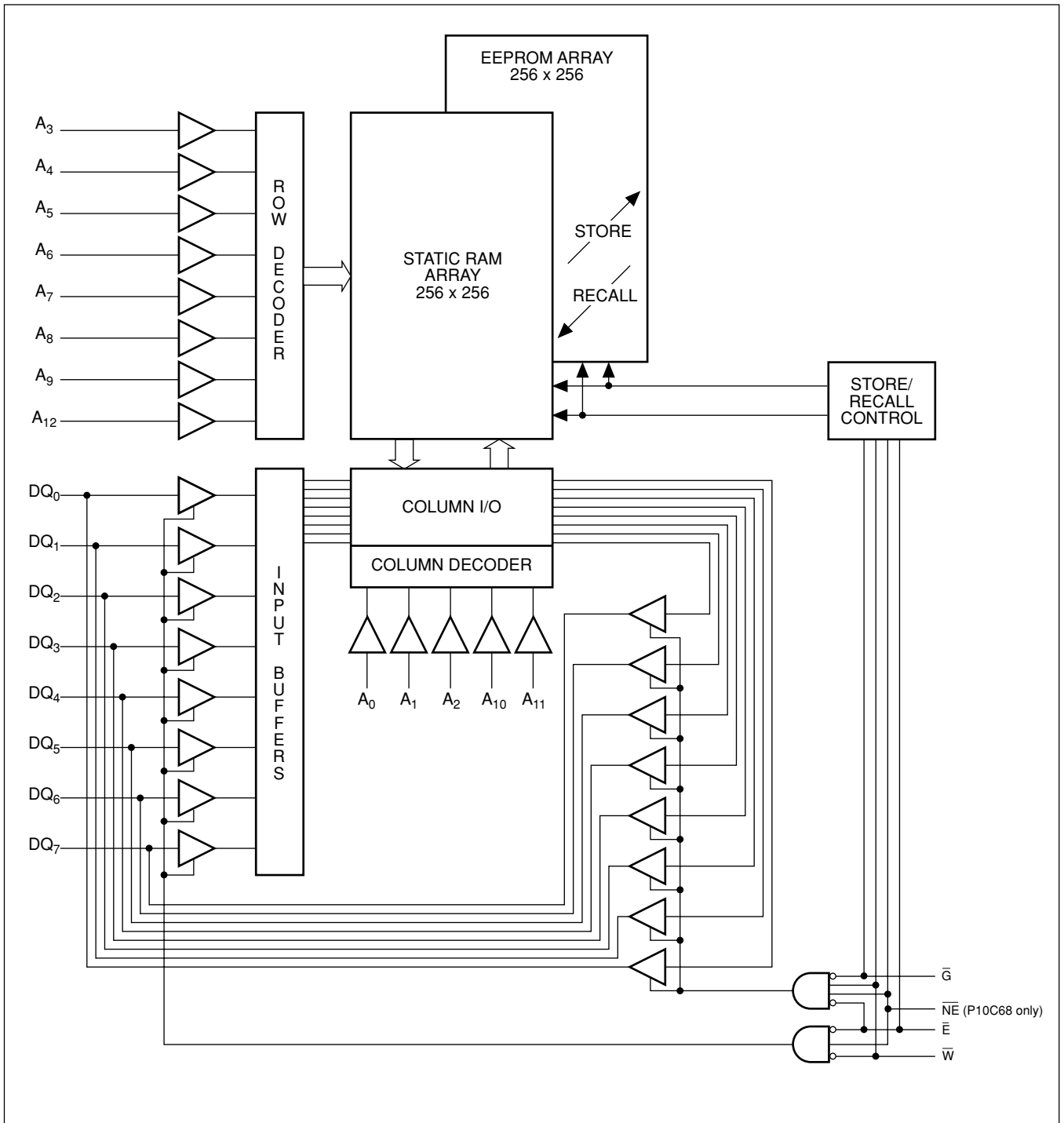


Figure 2. Logic block diagram.

ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------------|
| Voltage on typical input relative to VSS | -0.6V to 7.0V |
| Voltage on DQ0-7 and G(bar) | -0.5V to (V _{CC} + 0.5V) |
| Temperature under Bias | -55°C to + 125°C |
| Storage temperature | -65°C to + 150°C |
| Power dissipation | 1W |
| DC output current | 15mA |
| (one output at a time, one second duration) | |

NOTE

Stresses greater than those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at any other conditions than those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Units | Conditions |
|--|------------------|----------------------|------|----------------------|-------|------------|
| | | Min. | Typ. | Max. | | |
| Supply voltage | V _{CC} | | 5.0 | | V | |
| Input logic '1' voltage | V _{IH} | 2.2 | | V _{CC} +0.5 | V | All inputs |
| Input logic '0' voltage | V _{IL} | V _{SS} -0.5 | | 0.8 | V | All inputs |
| Ambient operating temperature commercial | T _{amb} | 0 | | +70 | °C | |
| industrial | T _{amb} | -40 | | +85 | °C | |

DC ELECTRICAL CHARACTERISTICS

Commercial temperature range

Test conditions (unless otherwise stated):

T_{amb} = 0°C to 70°C, V_{CC} = +5V (See notes 1, 2 and 3)

| Characteristic | Symbol | Value | | Units | Conditions |
|--|------------------|-------|----------|----------|--|
| | | Min. | Max. | | |
| Average power supply current | I _{CC1} | | 75 65 | mA mA | t _{AVAV} = 35ns t _{AVAV} = 45ns |
| Average power supply current during STORE cycle | I _{CC2} | | 50 | mA | All inputs at V _{IN} ≤ 0.2V |
| Average power supply current (standby, cycling TTL input levels) | I _{SB1} | | 23 20 | mA mA | t _{AVAV} = 35ns t _{AVAV} = 45ns E(bar) ≥ V _{IH} , all other inputs cycling |
| Average power supply current (standby, stable CMOS input levels) | I _{SB2} | | 1 | mA | E (bar) ≥ (V _{CC} - 0.2V), all other inputs at V _{IN} ≤ 0.2V or ≥ (V _{CC} - 0.2V) |
| Input leakage current (any input) | I _{ILK} | | ±1 | µA | V _{CC} = max, V _{IN} = V _{SS} to V _{CC} |
| Off state output leakage current | I _{OLK} | | ±5 | µA | V _{CC} = max, V _{IN} = V _{SS} to V _{CC} |
| Output logic '1' voltage | V _{OH} | 2.4 | | V | I _{OUT} = 4mA |
| Output voltage '0' voltage | V _{OL} | | 0.4 | V | I _{OUT} = 8mA |

NOTES

- I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
- Bringing E (bar) ≥ V_{IH} will not produce standby currents levels until any non-volatile cycle in progress has timed out. See Mode Selection table.
- I_{CC2} is the average current required for the duration of the STORE cycle (t_{STORE}) after the sequence that initiates the cycle.

P10C68/P11C68

Industrial temperature range

Test conditions (unless otherwise stated):

T_{amb} = -40°C to 70°C, V_{cc} = +5V ± 10% (See notes 4, 5 and 6)

| Characteristic | Symbol | Value | | Units | Conditions |
|--|------------------|-------|----------|----------|--|
| | | Min. | Max. | | |
| Average power supply current | I _{CC1} | | 80 75 | mA mA | t _{AVAV} = 35ns t _{AVAV} = 45ns |
| Average power supply current during STORE cycle | I _{CC2} | | 50 | mA | All inputs at V _{IN} ≤ 0.2V |
| Average power supply current (standby, cycling TTL input levels) | I _{SB1} | | 27 23 | mA mA | t _{AVAV} = 35ns t _{AVAV} = 45ns E(bar) ≥ V _{IH} , all other inputs cycling |
| Average power supply current (standby, stable CMOS input levels) | I _{SB2} | | 1 | mA | E (bar) ≥ (V _{CC} - 0.2V), all other inputs at V _{IN} ≤ 0.2V or ≥ (V _{CC} - 0.2V) |
| Input leakage current (any input) | I _{ILK} | | ±1 | μA | V _{CC} = max, V _{IN} = V _{SS} to V _{CC} |
| Off state output leakage current | I _{OLK} | | ±5 | μA | V _{CC} = max, V _{IN} = V _{SS} to V _{CC} |
| Output logic '1' voltage | V _{OH} | 2.4 | | V | I _{OUT} = 4mA |
| Output voltage '0' voltage | V _{OL} | | 0.4 | V | I _{OUT} = 8mA |

NOTES

- I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
- Bringing E (bar) ≥ V_{IH} will not produce standby currents levels until any non-volatile cycle in progress has timed out. See Mode Selection table.
- I_{CC2} is the average current required for the duration of the STORE cycle (t_{STORE}) after the sequence that initiates the cycle.

AC TEST CONDITIONS

| | |
|--|-----------------------|
| Input pulse levels | V _{SS} to 3V |
| Input rise and fall times | ≤5ns |
| Input and output timing reference levels | 1.5V |
| Output load | See Figure 3 |

CAPACITANCE T_{amb} = 25°C, f = 1.0MHz (see note 7)

| Parameter | Symbol | Max. | Units | Conditions |
|--------------------|------------------|------|-------|------------|
| Input capacitance | C _{IN} | 5 | pF | ΔV=0 to 3V |
| Output capacitance | C _{OUT} | 7 | pF | ΔV=0 to 3V |

NOTE

- These parameters are characterised but not 100% tested.

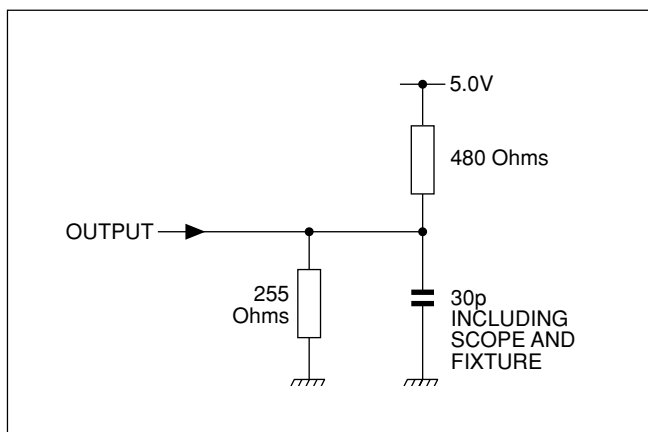


Figure 3. AC output loading.

SRAM MEMORY OPERATION

Test conditions (unless otherwise stated):
Commercial and Industrial Temperature Range
 Tamb = -40°C to + 85°C, Vcc = + 5V ± 10%

READ CYCLES 1 AND 2 (See note 8)

| Symbol | | Parameter | P10C68-35 P11C68-35 | | P10C68-45 P11C68-45 | | Units | Notes |
|---------------------|------------------|-----------------------------------|------------------------|------|------------------------|------|-------|-------|
| Standard | Alternative | | Min. | Max. | Min. | Max. | | |
| t _{ELQV} | t _{ACS} | Chip enable access time | | 35 | | 45 | ns | |
| t _{AVAV} | t _{RC} | Read cycle time | 35 | 35 | 45 | 45 | ns | 9 |
| t _{AVQV} | t _{AA} | Address access time | | 35 | | 45 | ns | 10 |
| t _{GLQV} | t _{OE} | Output enable to data valid | | 20 | | 25 | ns | |
| t _{AXQX} | t _{OH} | Output hold after address change | 5 | | 5 | | ns | |
| t _{ELQX} | t _{LZ} | Chip enable to output active | 5 | | 5 | | ns | |
| t _{EHQZ} | t _{OHZ} | Chip disable to output inactive | | 20 | | 25 | ns | 11 |
| t _{GLQX} | t _{OLZ} | Output enable to output active | 0 | | 0 | | ns | |
| t _{GHQZ} | t _{HZ} | Output disable to output inactive | | 15 | | 20 | ns | 11 |
| t _{ELICCH} | t _{PA} | Chip enable to power active | 0 | | 0 | | ns | 12 |
| t _{EHICCL} | t _{PS} | Chip disable to power standby | | 25 | | 25 | ns | 12 |
| t _{WHQV} | t _{WR} | Write recovery time | | 45 | | 55 | ns | |

NOTES

8. E (bar), G (bar) and W (bar) must make the transition between VIH(min) to VIL(max), or VIL(max) to VIH(min) in a monotonic fashion. NE (bar) must be ≥ VIH during entire cycle.
9. For READ CYCLE 1 and 2, W (bar) and NE (bar) must be high for entire cycle.
10. Device is continuously selected with E (bar) low, and G (bar) low.
11. Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
12. Parameter guaranteed but not tested.

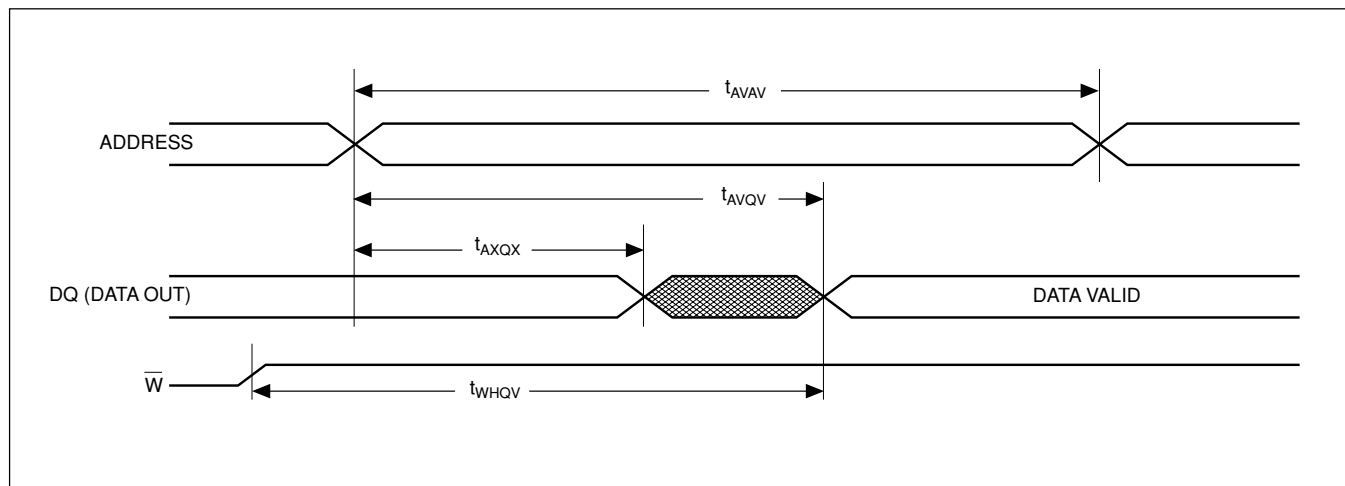


Figure 4. READ CYCLE 1 timing diagram (see notes 9 and 10).

P10C68/P11C68

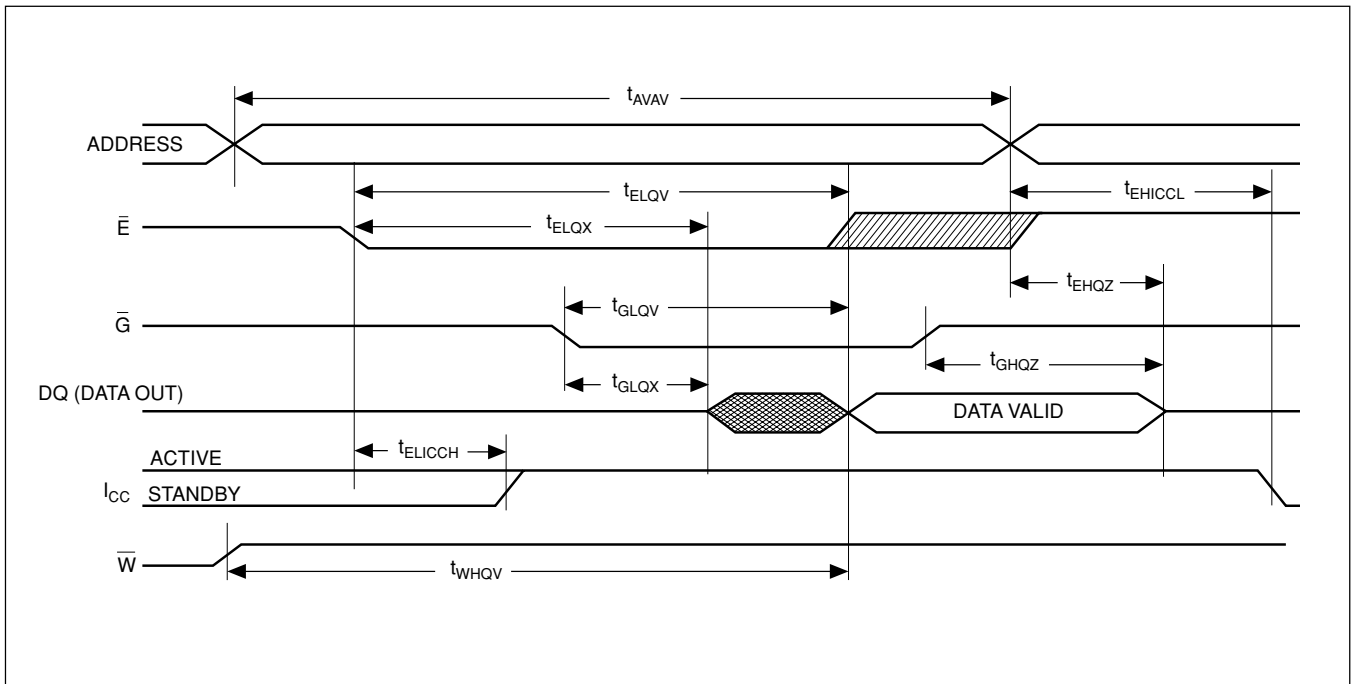


Figure 5. READ CYCLE 2 timing diagram (see note 9).

WRITE CYCLE 1 : W (BAR) CONTROLLED (See notes 8 and 13) Commercial and Industrial Temperature Range

| Symbol | | Parameter | P10C68-35 P11C68-35 | | P10C68-45 P11C68-45 | | Units | Notes |
|----------|-------------|----------------------------------|------------------------|------|------------------------|------|-------|--------|
| Standard | Alternative | | Min. | Max. | Min. | Max. | | |
| tAVAV | tWC | Write cycle time | 45 | | 45 | | ns | |
| tWLWH | tWP | Write pulse width | 35 | | 35 | | ns | |
| tELWH | tCW | Chip enable to end of write | 35 | | 35 | | ns | |
| tDVWH | tDW | Data set-up to end of write | 30 | | 30 | | ns | |
| tWHDX | tDH | Data hold after end of write | 0 | | 0 | | ns | |
| tAVWH | tAW | Address set-up to end of write | 35 | | 35 | | ns | |
| tAVWL | tAS | Address set-up to start of write | 0 | | 0 | | ns | |
| tWHAX | tWR | Address hold after end of write | 0 | | 0 | | ns | |
| tWLQZ | tWZ | Write enable to output disable | | 35 | | 35 | ns | 11, 14 |
| tWHQZ | tOW | Output active after end of write | 5 | | 5 | | ns | |

NOTES

13. E (bar) or W (bar) must be $\geq V_{IH}$ during address transitions.
14. If W (bar) is low when E (bar) goes low, the outputs remain in the high impedance state.

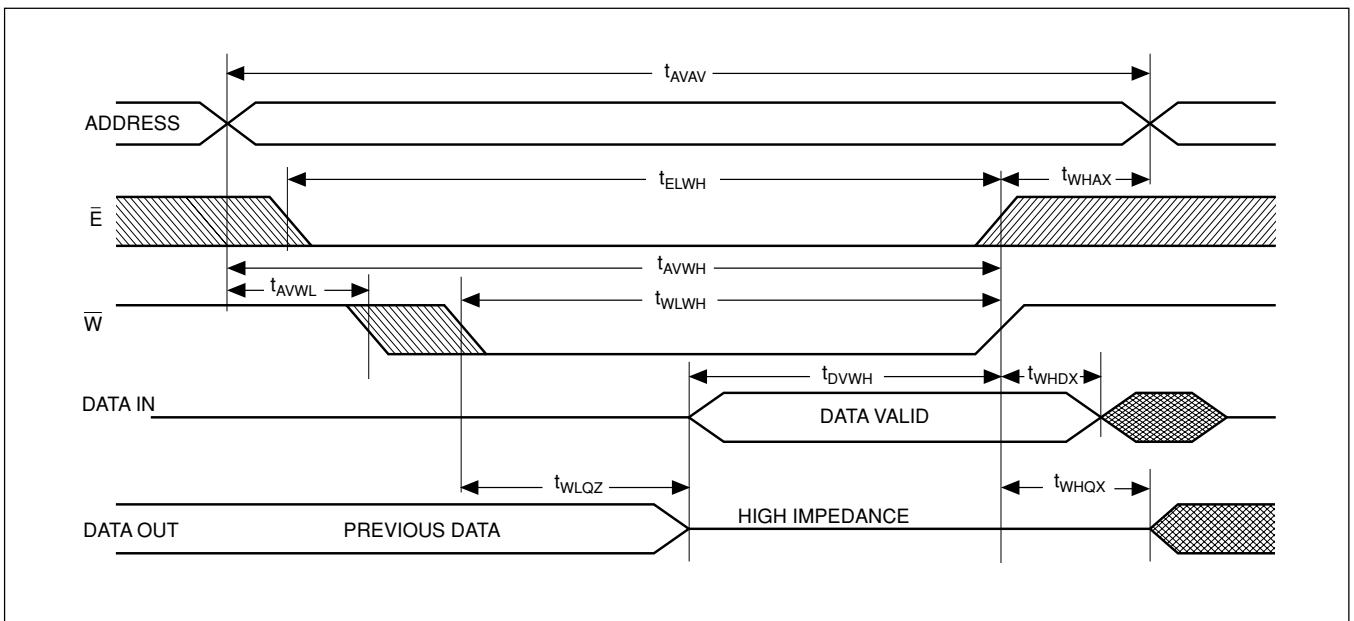


Figure 6. WRITE CYCLE 1: \bar{W} (bar) controlled timing diagram (see notes 8 and 13).

WRITE CYCLE 2 : \bar{E} (BAR) CONTROLLED (See notes 8 and 13)

| Symbol | | Parameter | P10C68-35 P11C68-35 | | P10C68-45 P11C68-45 | | Units | Notes |
|------------|-------------|----------------------------------|------------------------|------|------------------------|------|-------|-------|
| Standard | Alternative | | Min. | Max. | Min. | Max. | | |
| t_{AVAV} | t_{WC} | Write cycle time | 45 | | 45 | | ns | |
| t_{WLEH} | t_{WP} | Write pulse width | 35 | | 35 | | ns | |
| t_{ELEH} | t_{CW} | Chip enable to end of write | 35 | | 35 | | ns | |
| t_{DVEH} | t_{DW} | Data set-up to end of write | 30 | | 30 | | ns | |
| t_{EHDX} | t_{DH} | Data hold after end of write | 0 | | 0 | | ns | |
| t_{AVEH} | t_{AW} | Address set-up to end of write | 35 | | 35 | | ns | |
| t_{EHAX} | t_{WR} | Address hold after end of write | 0 | | 0 | | ns | |
| t_{AVWL} | t_{AS} | Address set-up to start of write | 0 | | 0 | | ns | |

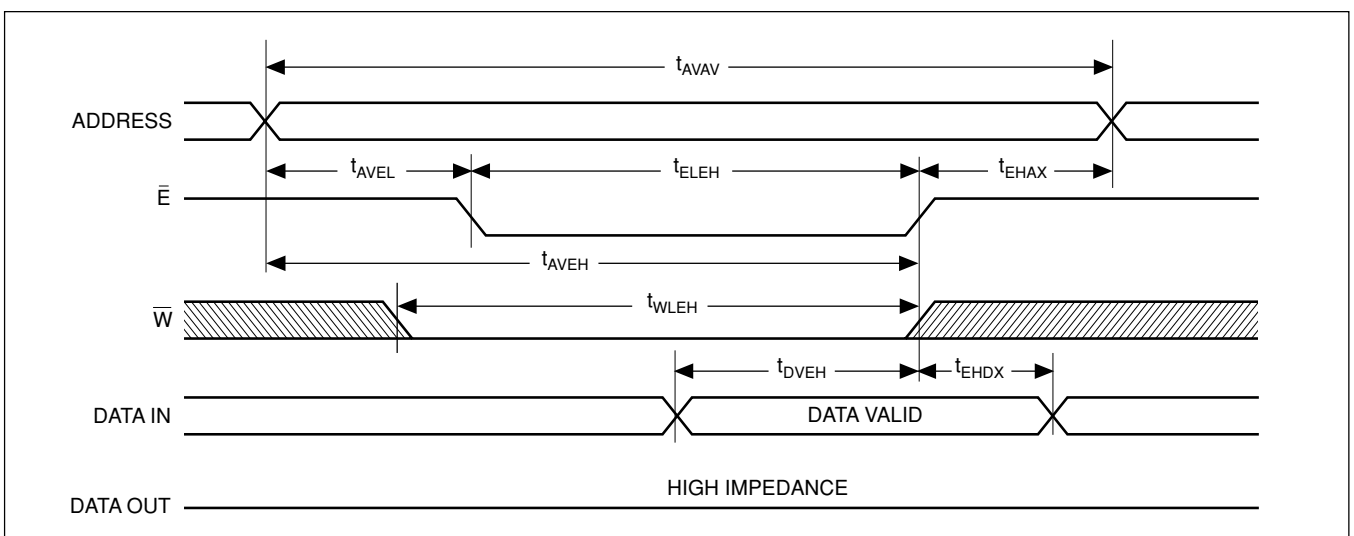


Figure 7. WRITE CYCLE 2: \bar{E} (bar) controlled timing diagram (see notes 8 and 13).

P10C68/P11C68

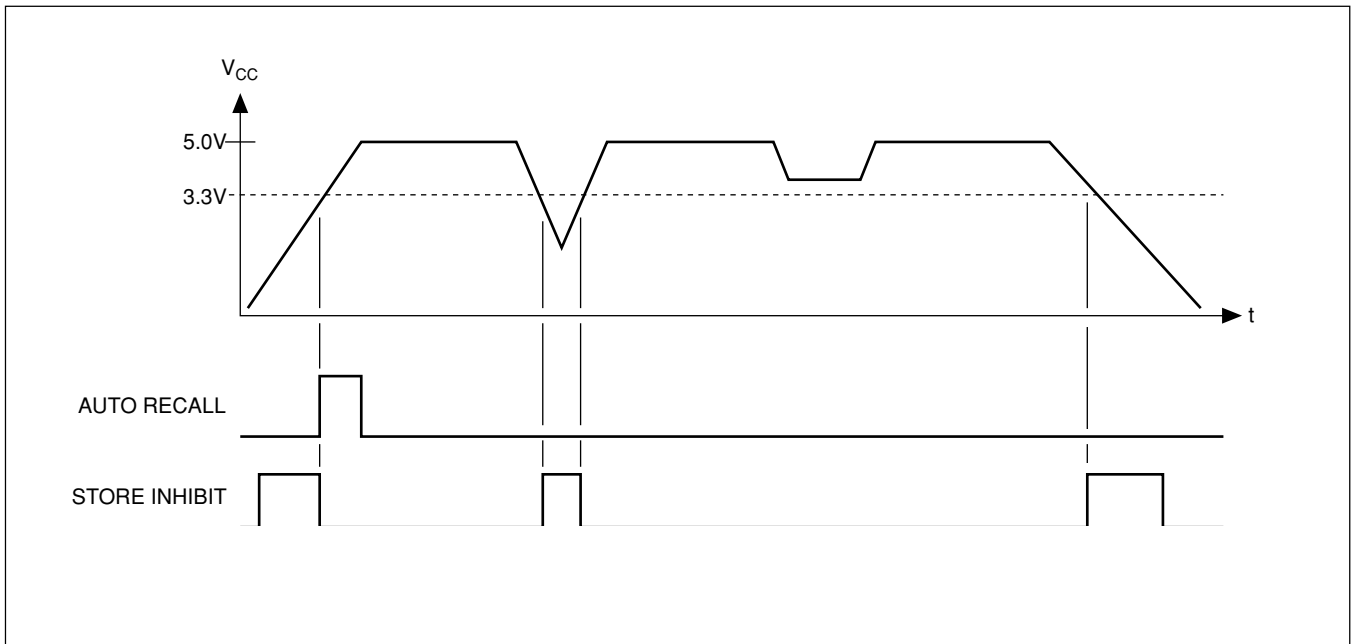


Figure 8. Automatic RECALL and STORE inhibit.

NON-VOLATILE MEMORY OPERATION OF P10C68 MODE SELECTION

| <u>E</u> | <u>W</u> | <u>G</u> | <u>NE</u> | Mode | Power |
|----------|----------|----------|-----------|-------------------------------|------------------|
| H | X | X | X | Not selected | Standby |
| L | H | L | H | Read RAM | Active |
| L | L | X | H | Write RAM | Active |
| L | H | L | L | Non-volatile recall (Note 15) | Active |
| L | L | H | L | Non-volatile store | I _{CC2} |
| L | L | L | L | No operation | Active |
| L | H | H | X | | |

NOTE

15. An automatic RECALL also takes place on chip power-up, starting when V_{CC} exceeds 3.3V, and taking t_{RECALL} from the time at which V_{CC} exceeds 3.3V. V_{CC} must not drop below 3.3V once it has exceeded it for the RECALL to function properly.

STORE CYCLE 1 : W (BAR) CONTROLLED (See note 16)

| Symbol | | Parameter | P10C68-35 | | P10C68-45 | | Units | Notes |
|-------------------|--------------------|--|-----------|------|-----------|------|-------|-------|
| Standard | Alternative | | Min. | Max. | Min. | Max. | | |
| t _{WLQX} | t _{STORE} | Store cycle time | | 10 | | 10 | ms | 17 |
| t _{GHNL} | | Output disable set-up to NE (bar) fall | 0 | | 0 | | ns | |
| t _{NLWL} | t _{WC} | Non-volatile set-up to write low | 0 | | 0 | | ns | 18 |
| t _{WLNH} | | Write low to NE (bar) rise | 45 | | 45 | | ns | |
| t _{ELWL} | | Chip enable SET-UP | 0 | | 0 | | ns | |

STORE CYCLE 2 : E (BAR) CONTROLLED (See note 13)

| Symbol | | Parameter | P10C68-35 | | P10C68-45 | | Units | Notes |
|-------------|-------------|---------------------------------------|-----------|------|-----------|------|-------|-------|
| Standard | Alternative | | Min. | Max. | Min. | Max. | | |
| t_{ELQX1} | t_{STORE} | Store cycle time | | 10 | | 10 | ms | 17 |
| t_{NLEL} | | NE (bar) set-up to chip enable | 0 | | 0 | | ns | |
| t_{WLEL} | | Write enable wet-up to chip enable | 0 | | 0 | | ns | |
| t_{ELNH} | t_{WC} | Chip enable to NE (bar) rise | 45 | | 45 | | ns | 18 |
| t_{GHEL} | | Output disable set-up to E (bar) fall | 0 | | 0 | | ns | |

NOTES

16. E (bar), G (bar), NE (bar) and W (bar) must make the transition between VIH(max) to VIL(max), or VIL(max) to VIH(min) in a monotonic fashion.

17. Measured with W (bar) and NE (bar) both returned high, and G (bar) returned low. Note that store cycles are inhibited/aborted by $V_{CC} < 3.3V$ (STORE inhibit).

18. Once t_{wc} has been satisfied by NE (bar), G (bar), W (bar) and E (bar) the store cycle is completed automatically, ignoring all inputs. Any of NE (bar), G (bar), W (bar) or E (bar) may be used to terminate the store initiation cycle.

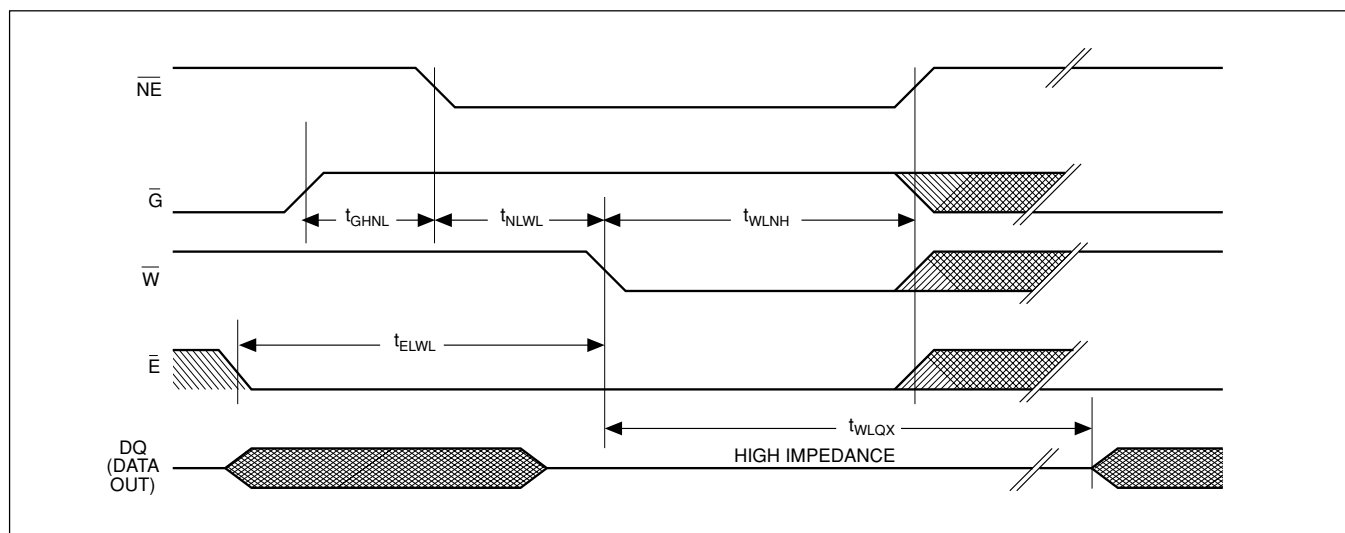


Figure 9. STORE CYCLE 1: W (bar) controlled timing diagram (see note 16).

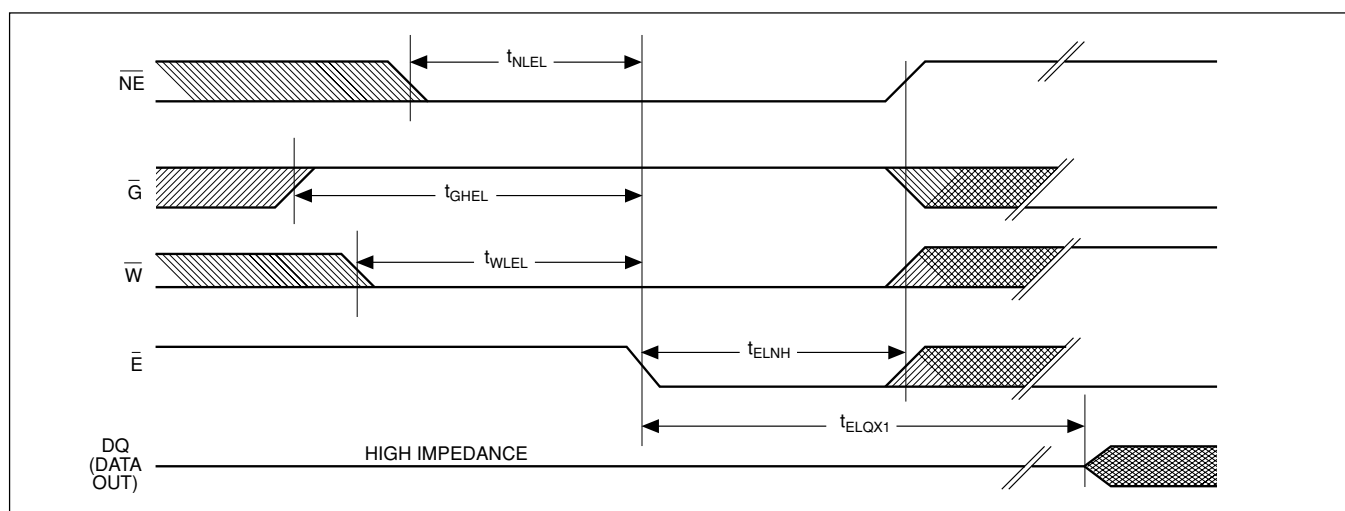


Figure 10. STORE CYCLE 2: E (bar) controlled timing diagram (see note 16).

P10C68/P11C68

P10C68 RECALL CYCLE 1 : NE (BAR) CONTROLLED (See note 16)

| Symbol | | Parameter | P10C68-35 | | P10C68-45 | | Units | Notes |
|-------------------|---------------------|----------------------------------|-----------|------|-----------|------|-------|-------|
| Standard | Alternative | | Min. | Max. | Min. | Max. | | |
| t _{NLQX} | t _{RECALL} | Recall cycle time | | 20 | | 20 | μs | 19 |
| t _{NLNH} | t _{RC} | Recall initiation cycle time | 25 | | 25 | | μs | 20 |
| t _{GLNL} | | Output enable set-up | 0 | | 0 | | ns | |
| t _{WHNL} | | Write enable set-up | 0 | | 0 | | ns | |
| t _{ELNL} | | Chip enable set-up | 0 | | 0 | | ns | |
| t _{NLQZ} | | NE (bar) fall to output inactive | | 25 | | 25 | ns | |

P10C68 RECALL CYCLE 2 : E (BAR) CONTROLLED (See note 16)

| Symbol | | Parameter | P10C68-35 | | P10C68-45 | | Units | Notes |
|--------------------|---------------------|------------------------------|-----------|------|-----------|------|-------|-------|
| Standard | Alternative | | Min. | Max. | Min. | Max. | | |
| t _{ELQX2} | t _{RECALL} | Recall cycle time | | 20 | | 20 | μs | 19 |
| t _{ELNH} | t _{RC} | Recall initiation cycle time | 25 | | 25 | | ns | 20 |
| t _{NLEL} | | NE (bar) set-up | 0 | | 0 | | ns | |
| t _{GLEL} | | Output enable set-up | 0 | | 0 | | ns | |
| t _{WHEL} | | Write enable set-up | 0 | | 0 | | ns | |

P10C68 RECALL CYCLE 3 : G (BAR) CONTROLLED (See note 16)

| Symbol | | Parameter | P10C68-35 | | P10C68-45 | | Units | Notes |
|--------------------|---------------------|------------------------------|-----------|------|-----------|------|-------|-------|
| Standard | Alternative | | Min. | Max. | Min. | Max. | | |
| t _{GLQX2} | t _{RECALL} | Recall cycle time | | 20 | | 20 | μs | 19 |
| t _{GLNH} | t _{RC} | Recall initiation cycle time | 25 | | 25 | | ns | 20 |
| t _{NLGL} | | NE (bar) set-up | 0 | | 0 | | ns | |
| t _{WHGL} | | Write enable set-up | 0 | | 0 | | ns | |
| t _{ELGL} | | Chip enable set-up | 0 | | 0 | | ns | |

NOTES

- Measured with W (bar) and NE (bar) both returned high, and G (bar) returned low. Address transitions may not occur on any address pin during this time.
- Once t_{RC} has been satisfied by NE (bar), G (bar), W (bar) and E (bar) the RECALL cycle is completed automatically. Any of NE (bar), G (bar) or E (bar) may be used to terminate the RECALL initiation cycle.

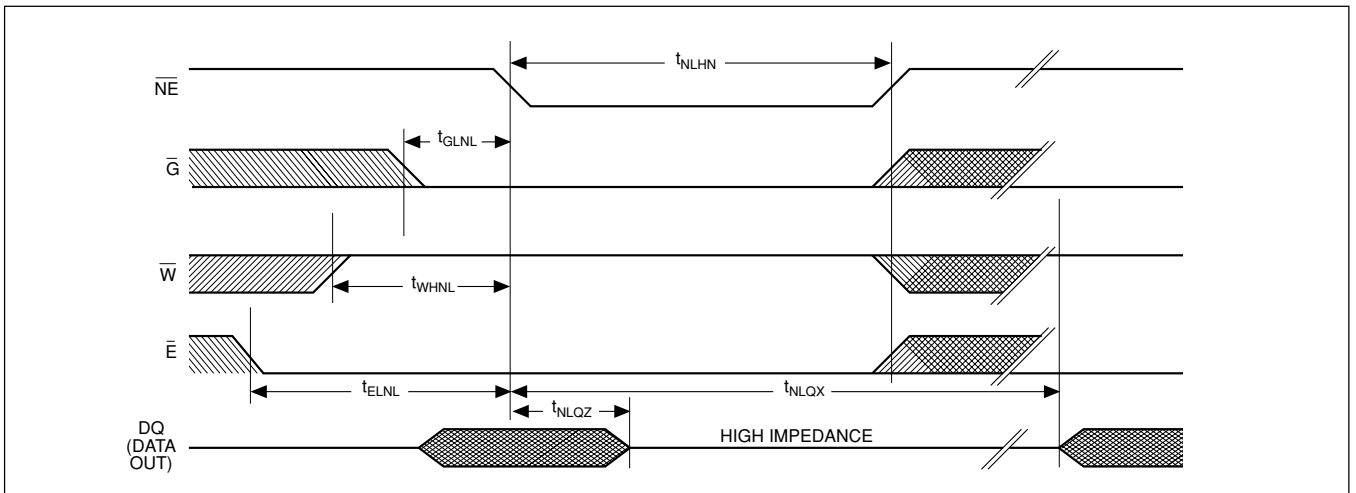


Figure 11. P10C68 RECALL CYCLE 1: NE (bar) controlled timing diagram (see note 16).

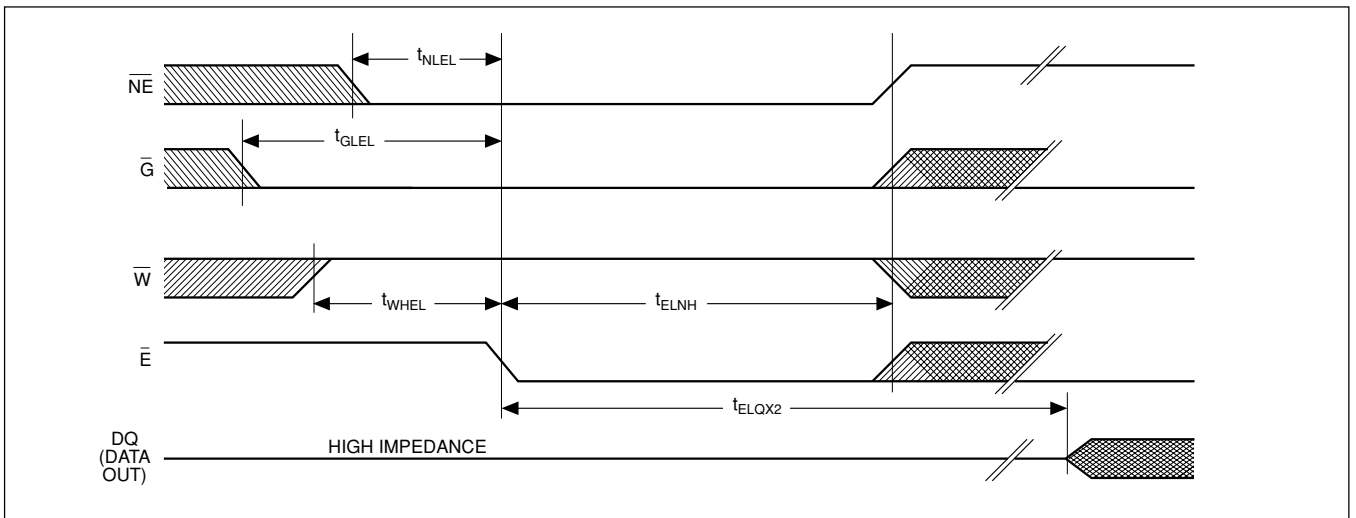


Figure 12. P10C68 RECALL CYCLE 2: E (bar) controlled timing diagram (see note 16).

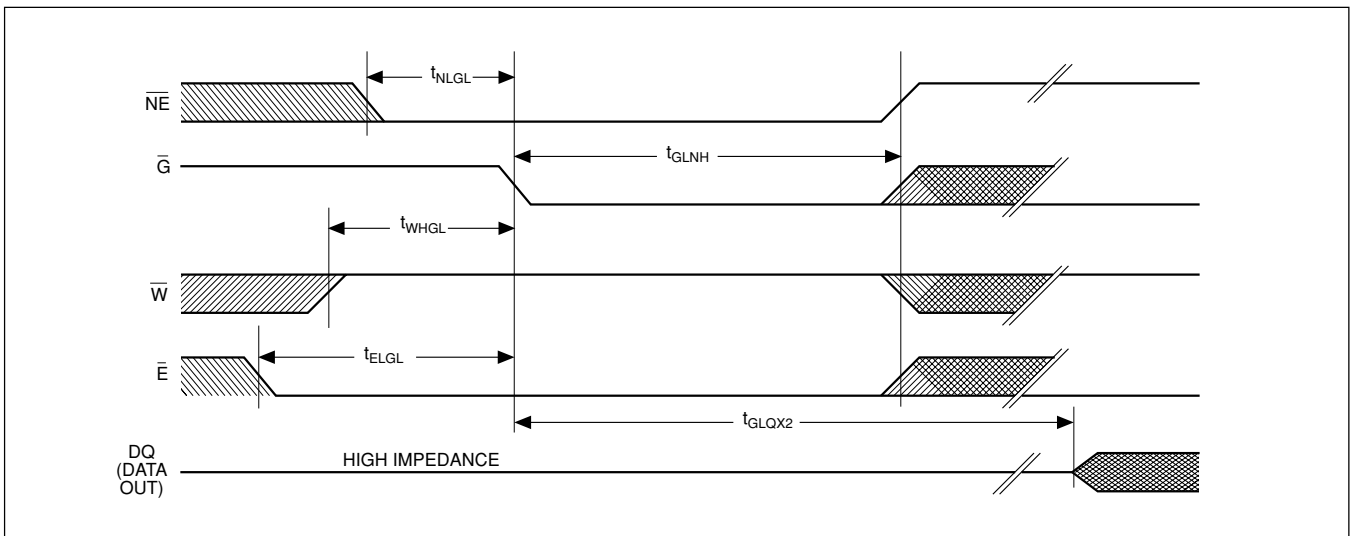


Figure 13. P10C68 RECALL CYCLE 3: E (bar) controlled timing diagram (see note 16).

P10C68/P11C68

NON-VOLATILE MEMORY OPERATION OF P11C68 MODE SELECTION

| E | W | A ₁₂ -A ₀ (hex) | Mode | I/O | Power | Notes |
|---|---|---------------------------------------|---------------------|---------------|---------|------------------|
| H | X | X | Not selected | Output High Z | Standby | |
| L | H | X | Read RAM | Output data | Active | 22 |
| L | L | X | Write RAM | Input Data | Active | |
| L | H | 0000 | Read RAM | Output Data | Active | 21, 22 |
| | | 1555 | Read RAM | Output Data | | 21, 22 |
| | | 0AAA | Read RAM | Output Data | | 21, 22 |
| | | 1FFF | Read RAM | Output Data | | 21, 22 |
| | | 10F0 | Read RAM | Output Data | | 21, 22 |
| | | 0F0F | Non-volatile STORE | Output High Z | | I _{CC2} |
| L | H | 0000 | Read RAM | Output Data | Active | 21, 22 |
| | | 1555 | Read RAM | Output Data | | 21, 22 |
| | | 0AAA | Read RAM | Output Data | | 21, 22 |
| | | 1FFF | Read RAM | Output Data | | 21, 22 |
| | | 10F0 | Read RAM | Output Data | | 21, 22 |
| | | 0F0E | Non-volatile RECALL | Output High Z | | |

NOTES

- The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. W (bar) must be high during all six consecutive cycles. See STORE CYCLE and RECALL CYCLE tables and diagrams for further details.
- I/O state assumes that G (bar) $\geq V_{IL}$. Activation of non-volatile cycles does not depend on the state of G (bar).

STORE / RECALL CYCLES 1 AND 2 (See notes 24 and 29)

| Symbol | | Parameter | P11C68-35 | | P11C68-45 | | Units | Notes |
|-------------------|---------------------|--|-----------|------|-----------|------|-------|--------|
| Standard | Alternative | | Min. | Max. | Min. | Max. | | |
| t _{AVAV} | t _{ACS} | Read cycle time | 35 | | 45 | | ns | |
| t _{AXAV} | t _{SKEW} | Skew between sequentially adjacent addresses | | 5 | | 5 | ns | 23 |
| t _{AVQZ} | t _{ELQZ} | Address valid to output inactive | | 75 | | 75 | ns | 25 |
| | t _{STORE} | Store cycle time | | 10 | | 10 | ms | 26 |
| | t _{RECALL} | Recall cycle time | | 20 | | 20 | μs | 26, 30 |
| t _{AVEL} | t _{AE} | Address set-up to chip enable | 0 | | 0 | | ns | 27 |
| t _{ELEH} | t _{EP} | Chip enable pulse width | 35 | | 45 | | ns | 27 |
| t _{EHAX} | t _{EA} | Chip disable to address change | 0 | | 0 | | ns | 27 |

NOTES

- Skew spec may be avoided by using E (bar) (STORE/RECALL CYCLE 2).
- W (bar) $\geq V_{IH}$ during entire address sequence to initiate a non-volatile cycle. Required address sequences are shown in the Mode Selection table.
- Once the software STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.
- Measured with W (bar) high, G (bar) low and E (bar) low. Note that STORE cycles (but not RECALLS) are aborted by V_{CC} < 3.3V (STORE Inhibit).
- E (bar) must make the transition between V_{IH}(max) to V_{IL}(max), or V_{IL}(max) to V_{IH}(min) in a monotonic fashion.
- Chip is continuously selected with E (bar) low.
- Addresses 1 through 6 are found in the Mode Selection table. Address 6 determines whether the P11C68 performs a STORE or RECALL. A RECALL cycle is performed automatically at power up when V_{CC} exceeds 3.3V. V_{CC} must not drop below 3.3V once it has exceeded it for the RECALL to function properly, t_{RECALL} is measured from the point at which V_{CC} exceeds 3.3V.
- Address transitions may not occur on any address pin during this time.

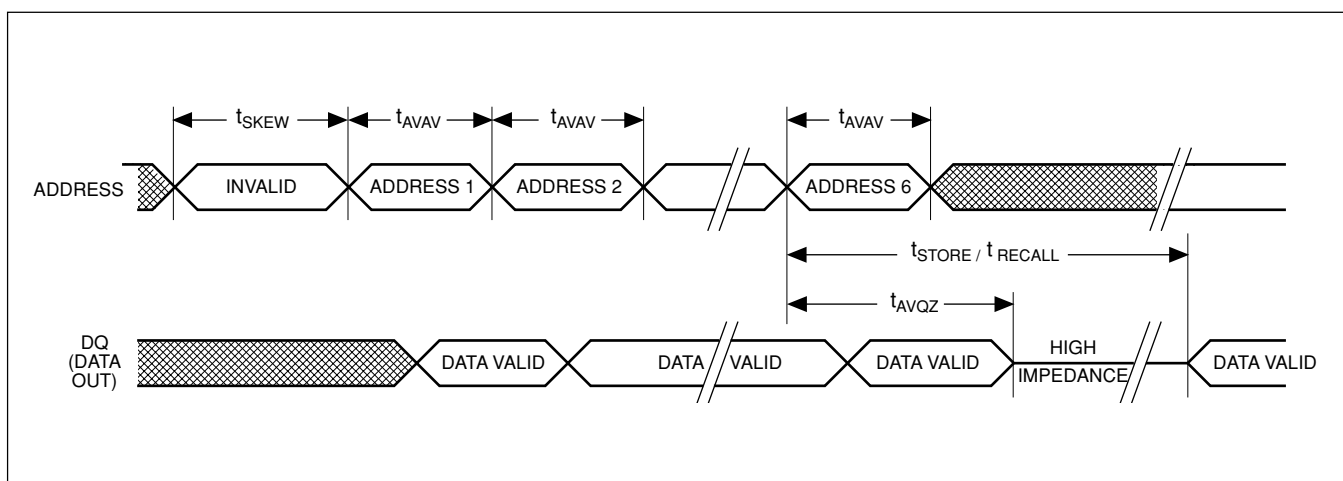


Figure 14. STORE/RECALL cycle 1. Address controlled timing diagram (see notes 22, 26 and 27).

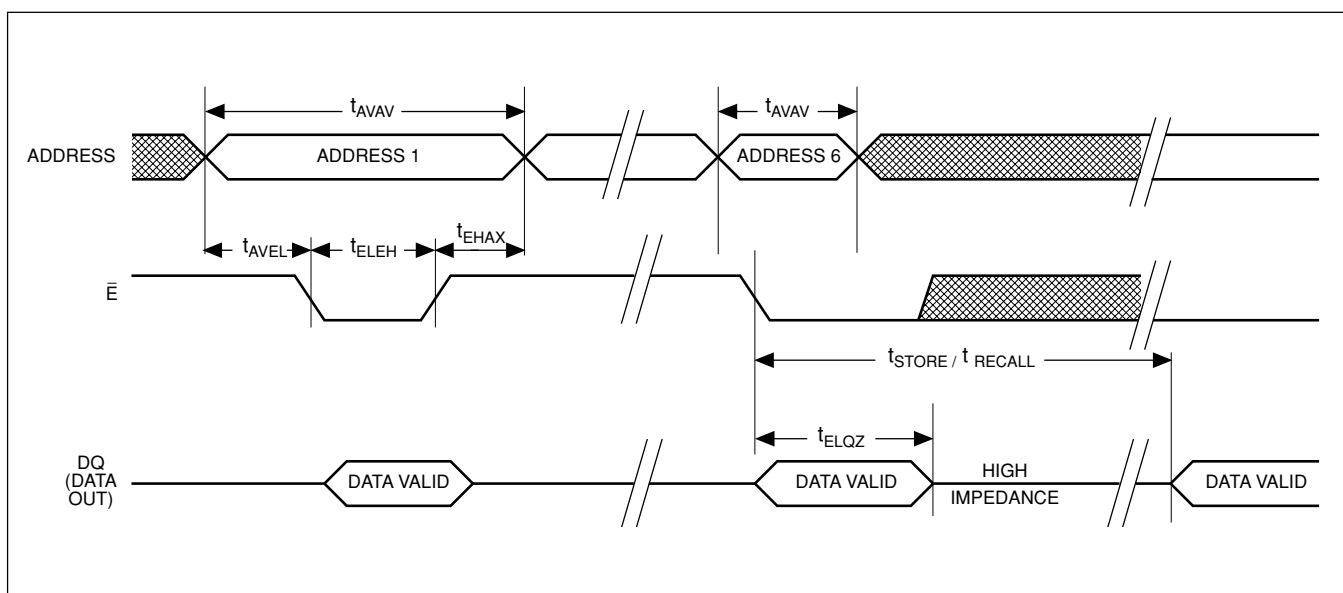


Figure 15. STORE/RECALL cycle 2. E (bar) controlled timing diagram (see notes 22, 25 and 27).

OPERATING NOTES

Note: References to NE (bar) should be taken as applying to P10C68 only and can be ignored for P11C68.

The devices have two separate modes of operation: SRAM mode and non-volatile mode. In SRAM mode, the memory operates as an ordinary static RAM. While in non-volatile mode, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM.

SRAM READ

The devices perform a read cycle when ever E (bar) and G (bar) are LOW and NE (bar) and W (bar) are HIGH. The address specified by the thirteen address pins A₀₋₁₂ determine which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE 1).

If the READ is initiated by E (bar) or G (bar), the outputs will be valid at t_{ELQV} or t_{GLQV}, whichever is later. (READ CYCLE 2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins and will remain valid until another address change or until E (bar) or G (bar) is brought HIGH or W (bar) or NE (bar) is brought LOW.

SRAM WRITE

A write cycle is performed whenever E (bar) and W (bar) are LOW and NE (bar) is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either E (bar) or W (bar) go HIGH at the end of the cycle. The data on the eight pins DQ₀₋₇, will be written into the memory location specified by the address inputs if valid t_{DVWH} before the end of a W (bar) controlled WRITE or t_{DVEH} before the end of an E (bar) controlled WRITE.

P10C68/P11C68

It is recommended that G (bar) be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If G (bar) is left LOW, internal circuitry will turn off the output buffers t_{WHQZ} after W (bar) goes LOW.

Non-Volatile STORE - P10C68

A STORE cycle is performed when NE, (bar) E (bar) and W (bar) are LOW and G (bar) is HIGH. While any sequence to achieve this state will initiate a STORE, only W(bar) initiation (STORE CYCLE 1) and E (bar) initiation (STORE CYCLE 2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During the STORE cycle, previous non-volatile data is erased and the SRAM contents are then programmed into non-volatile elements. Once a STORE cycle is initiated, further input and output is disabled and the DQ₀₋₇ pins are tri-stated until the cycle is completed.

If E (bar) and G (bar) are LOW and W (bar) and NE (bar) are HIGH at the end of the cycle, a READ will be performed and the outputs will go active, signalling the end of the STORE.

The P10C68 will not be activated into either a STORE or RECALL cycle by the software sequence required for the P11C68.

Hardware Protect - P10C68

The P10C68 offers two levels of protection to suppress inadvertent STORE cycles. If the clock signals remain in the STORE condition at the end of a STORE cycle, a second STORE cycle will not be started. The STORE will be initiated only after a HIGH to LOW transition on NE (bar) Because the STORE cycle is initiated by an NE (bar) transition, powering-up the chip with NE (bar) Low will not initiate a STORE cycle either.

In addition to multi-trigger protection, the P10C68 offers hardware protection through Vcc Sense. A STORE cycle will not be initiated, and one in progress will discontinue, if Vcc goes below 3.3V.

Non-Volatile RECALL - P10C68

A RECALL cycle is performed when E (bar), G (bar) and NE (bar) are LOW and W (bar) is HIGH. Like the STORE cycle, RECALL is initiated when the last of the four clock signals goes to the RECALL state. Once initiated, the RECALL cycle will take t_{NLQX} to complete, during which all inputs are ignored. When the RECALL completes, any READ or WRITE state on the input pins will take effect.

Internally, RECALL is a two step procedure. First the SRAM data is cleared and second, the non-volatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the non-volatile cells. The non-volatile data can be recalled an unlimited number of times. Address transitions may not occur during the RECALL cycle. Like the STORE cycle, a transition must occur on the NE (bar) pin to cause a RECALL, preventing inadvertent multi-triggering. On power-up, once Vcc exceeds Vcc sense voltage of 3.3V, a RECALL cycle is automatically initiated. The voltage on the Vcc pin must not drop below 3.3V once it has risen above it in order for the RECALL to operate properly. Due to the automatic RECALL, SRAM operation cannot commence until t_{NLQX} after Vcc exceeds 3.3V.

The P11C68 STORE cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the P11C68 implements non-volatile operation while remaining pin-for-pin compatible with standard 8Kx8 SRAMs. During the STORE cycle, an erase of the previous non-volatile data is first performed, followed by a program of the non-volatile elements. The program operation copies the SRAM data into non-volatile storage. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed. Because a sequence of addresses is used for STORE initiation, it is critical that no invalid address states intervene in the sequence or the sequence will be aborted. The maximum skew between address inputs A0-12 for each address state is t_{SKEW} (STORE CYCLE 1).

If t_{SKEW} is exceeded it is possible that the transitional data state will be interpreted as a valid address and the sequence will be aborted. If E (bar) controlled READ cycles are used for the sequence (STORE CYCLE 2), address skew is no longer a concern.

To enable the STORE cycle the following READ sequence must be performed.

1. Read address 0000 (hex) Valid READ
2. Read address 1555 (hex) Valid READ
3. Read address 0AAA (hex) Valid READ
4. Read address 1FFF (hex) Valid READ
5. Read address 10F0 (hex) Valid READ
6. Read address 0F0F (hex) Initiate STORE Cycle

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that G (bar) be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

Once the first of the six reads has taken place, the read sequence must either complete or terminate with an incorrect address (other than 0000 hex) before it may be started anew.

The P11C68 offers hardware protection against inadvertent STORE cycles through Vcc Sense. A STORE cycle will not be initiated, and one in progress will discontinue, if Vcc goes below 3.3V.

A RECALL of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the STORE initiation. To initiate the RECALL cycle the following sequence of READ operations must be performed:

1. Read address 0000 (hex) Valid READ
2. Read address 1555 (hex) Valid READ
3. Read address 0AAA (hex) Valid READ
4. Read address 1FFF (hex) Valid READ
5. Read address 10F0 (hex) Valid READ
6. Read address 0F0E (hex) Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second the non-volatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the EEPROM cells. The non-volatile data can be recalled an unlimited number of times. Address transitions may not occur during the RECALL cycle.

On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 3.3V, a RECALL cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below 3.3V once it has risen above it in order for the RECALL to operate properly. Due to this automatic RECALL, SRAM operation cannot commence until t_{RECALL} after V_{CC} exceeds 3.3V.

The automatic RECALL feature can be adversely affected by factors such as supply rise time, temperature and elapsed time since the last STORE cycle. For this reason it is recommended that the user initiate a RECALL cycle after power-up for critical applications.

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information please contact your local Customer Service Centre.

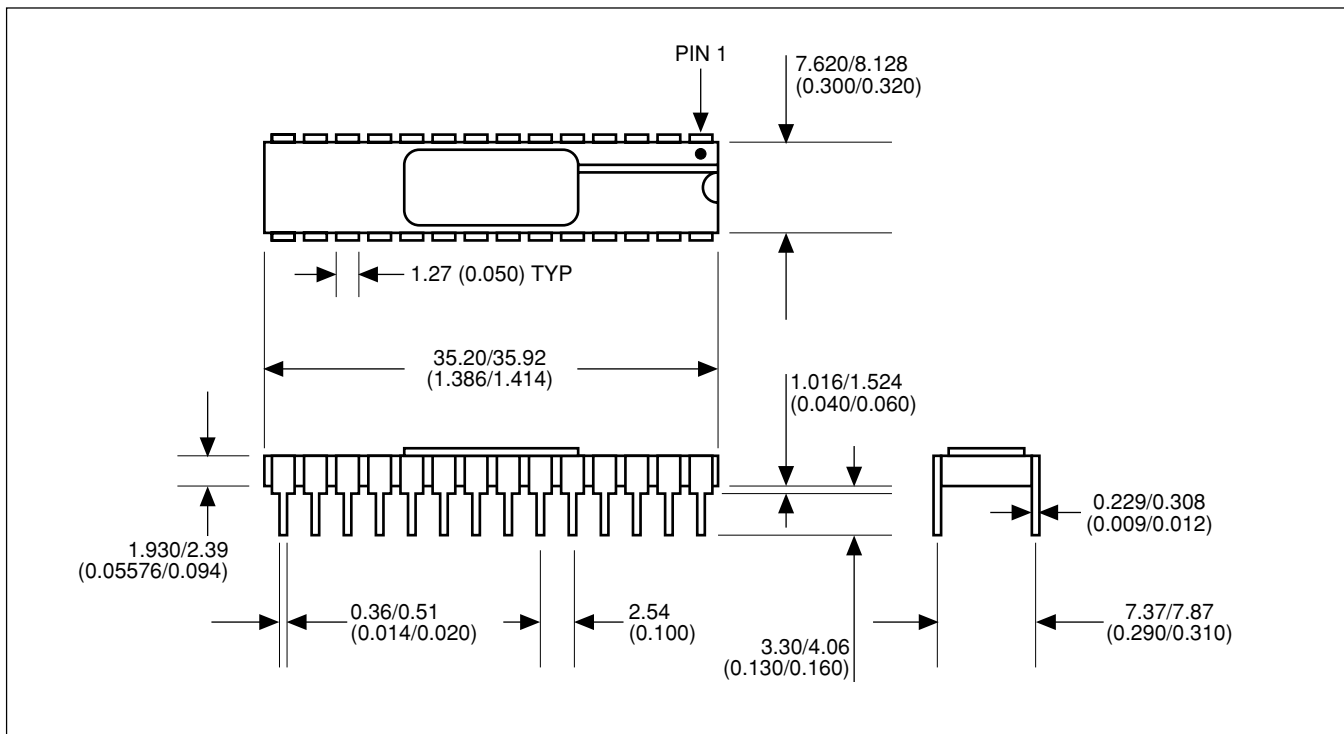


Figure 16, 28-lead sidebraced ceramic DIL (0.3in) DCB

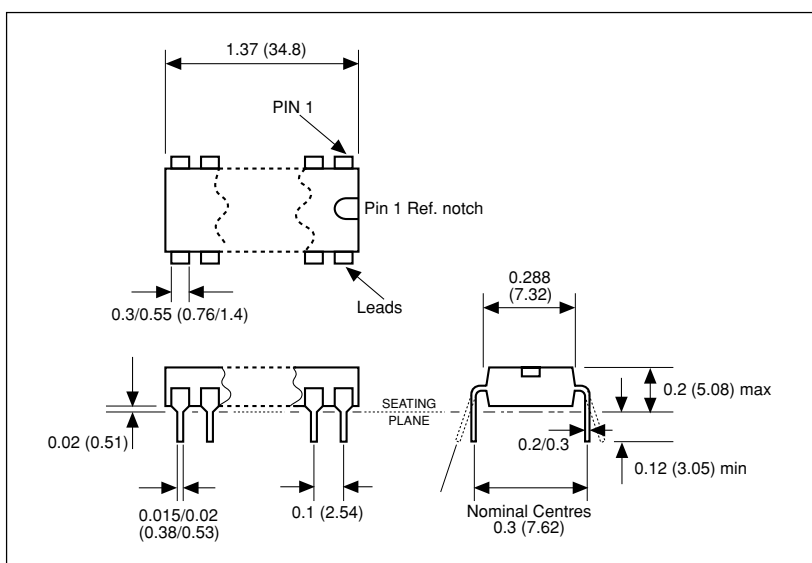
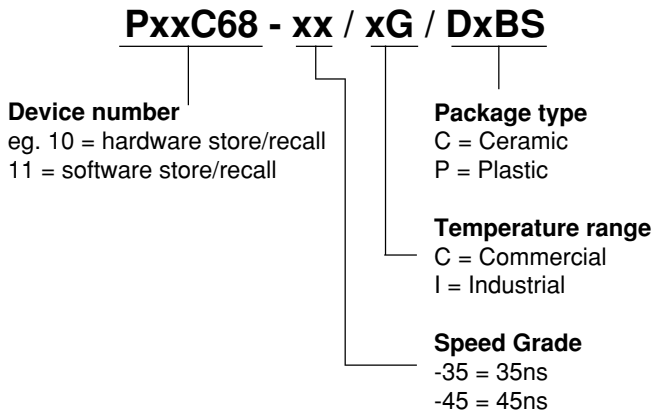


Figure 17, 28 plastic DIL Package (0.3in) DPB

P10C68/P11C68

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