1 PRODUCT OVERVIEW

OVERVIEW

The KS57C21516 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With an up-to-896-dot LCD direct drive capability, 8-bit and 16-bit timer/counter, and serial I/O, the KS57C21516 offers an excellent design solution for a wide variety of applications which require LCD functions.

Up to 39 pins of the 100-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the KS57C21516's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The KS57C21516 microcontroller is also available in OTP (One Time Programmable) version, KS57P21516. KS57P21516 microcontroller has an on-chip 16K-byte one-time-programable EPROM instead of masked ROM. The KS57P21516 is comparable to KS57C21516, both in function and in pin configuration.

FEATURES SUMMARY

Memory

- 768 × 4-bit RAM
- 16,384 × 8-bit ROM

39 I/O Pins

- I/O: 35 pins
- Input only: 4 pins

LCD Controller/Driver

- 56 segments and 16 common terminals
- 8 and 16 common selectable
- Internal resistor circuit for LCD bias
- All dot can be switched on/off

8-bit Basic Timer

- 4 interval timer functions
- Watch-dog timer

8-bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider
- Serial I/O interface clock generator

16-Bit Timer/Counter

- Programmable 16-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Memory-Mapped I/O Structure

- Data memory bank 15

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 32768 Hz
- 4 frequency outputs to BUZ pin
- Clock source generation for LCD

Interrupts

- Four internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system oscillation stops)
- Subsystem clock stop mode

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 0.4 – 6 MHz
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.67, 1.33, 10.7 µs at 6 MHz
- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 122 µs at 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 2.0 V to 5.5 V

Package Type

- 100-pin QFP

BLOCK DIAGRAM

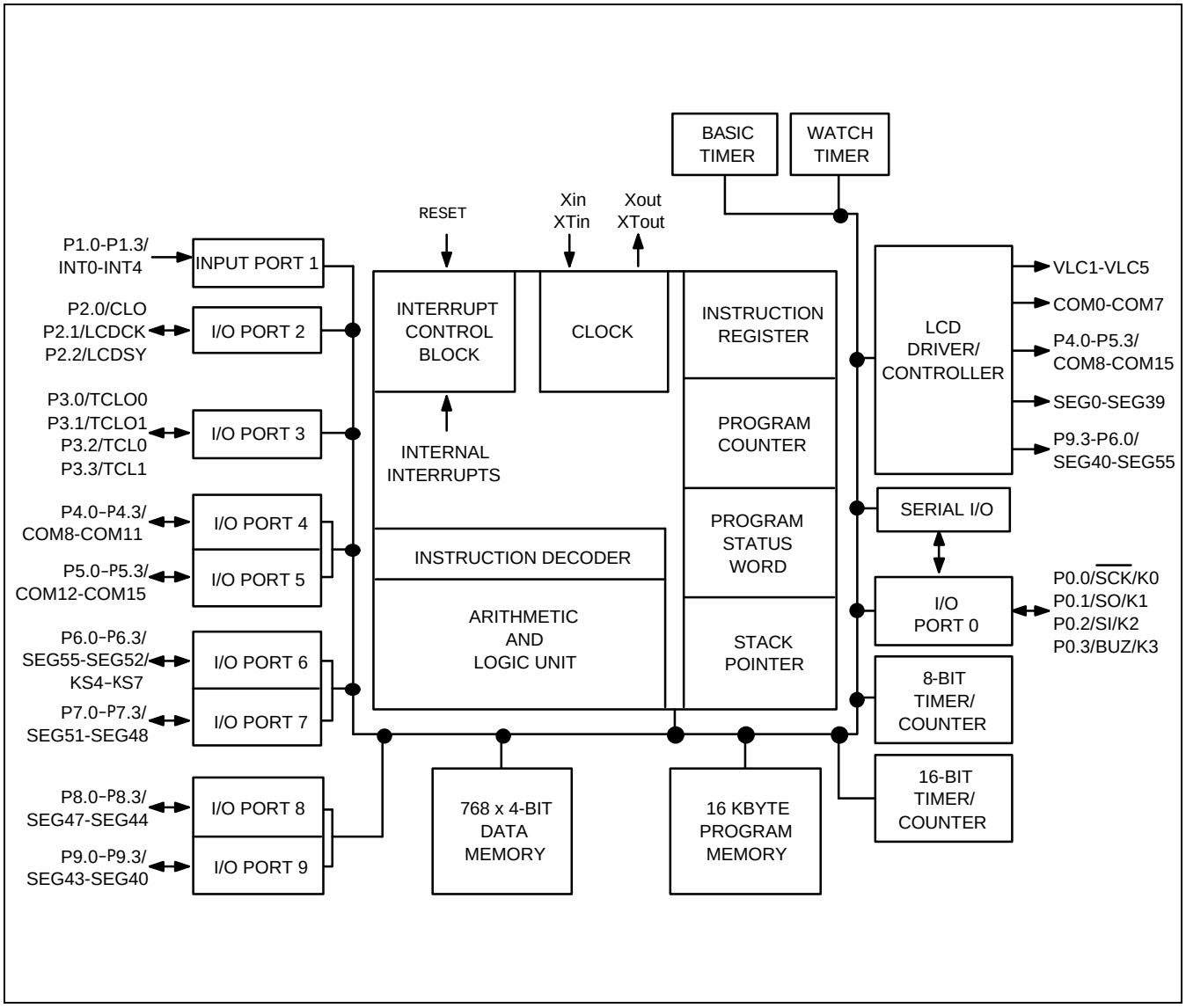

Figure 1–1. KS57C21516 Simplified Block Diagram

PIN ASSIGNMENTS

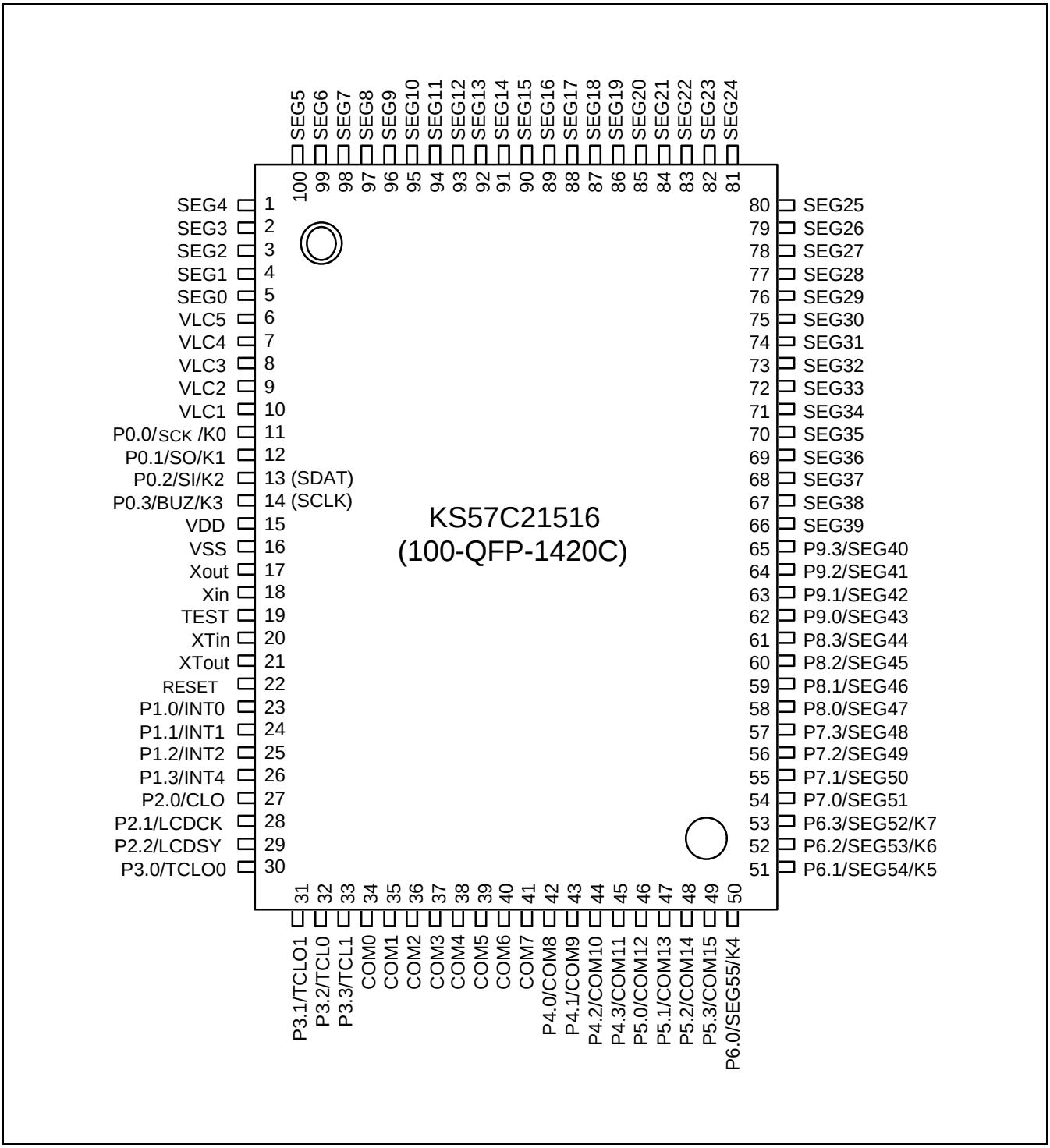

Figure 1–2. KS57C21516 100-QFP Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1–1. KS57C21516 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. Individual pins are software configurable as open-drain or push-pull output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	11 12 13 14	SCK/K0 SO/K1 SI/K2 BUZ/K3
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 4-bit pull-up resistors are assignable by software.	23 24 25 26	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2	I/O	Same as port 0 except that port 2 is 3-bit I/O port.	27 28 29	CLO LCDCK LCDSY
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0.	30 31 32 33	TCLO0 TCLO1 TCL0 TCL1
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-, 4-bit or 8-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	42–45 46–49	COM8–COM11 COM12–COM15
P6.0–P6.3 P7.0–P7.3	I/O	Same as P4, P5.	50–53 54–57	SEG55/K4–SEG52/K7 SEG51–SEG48
P8.0–P8.3 P9.0–P9.3	I/O	Same as P4, P5.	58–61 62–65	SEG47–SEG44 SEG43–SEG40
SCK	I/O	Serial I/O interface clock signal.	11	P0.0/K0
SO	I/O	Serial data output.	12	P0.1/K1
SI	I/O	Serial data input.	13	P0.2/K2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz or 16 kHz frequency output for buzzer signal.	14	P0.3/K3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	23, 24	P1.0, P1.1

Table 1–1. KS57C21516 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
INT2	I	Quasi-interrupt with detection of rising or falling edges.	25	P1.2
INT4	I	External interrupt with detection of rising or falling edges.	26	P1.3
CLO	I/O	Clock output .	27	P2.0
LCDCK	I/O	LCD clock output for display expansion.	28	P2.1
LCDSY	I/O	LCD synchronization clock output for display expansion.	29	P2.2
TCLO0	I/O	Timer/counter 0 clock output.	30	P3.0
TCLO1	I/O	Timer/counter 1 clock output.	31	P3.1
TCL0	I/O	External clock input for timer/counter 0.	32	P3.2
TCL1	I/O	External clock input for timer/counter 1.	33	P3.3
COM0–COM7	O	LCD common signal output.	34–41	–
COM8–COM11	I/O		42–45	P4.0–P4.3
COM12–COM15			46–49	P5.0–P5.3
SEG0–SEG39	O	LCD segment signal output.	5–1, 100–66	–
SEG40–SEG43	I/O		65–62	P9.3–P9.0
SEG44–SEG47			61–58	P8.3–P8.0
SEG48–SEG51			57–54	P7.3–P7.0
SEG52–SEG55			53–50	P6.3/K7–P6.0/K4
K0–K3	I/O	External interrupt. The triggering edge is selectable.	11–14	P0.0–P0.3
K4–K7			50–53	P6.0–P6.3
V_{DD}	–	Main power supply.	15	–
V_{SS}	–	Ground.	16	–
RESET	I	Reset signal.	22	–
V_{LC1}–V_{LC5}	–	LCD power supply.	10–6	–
X_{in}, X_{out}	–	Crystal, Ceramic or RC oscillator pins for system clock.	18, 17	–
XT_{in}, XT_{out}	–	Crystal oscillator pins for subsystem clock.	20, 21	–
TEST	I	Test signal input. (must be connected to V_{SS})	19	–

NOTE: Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.

Table 1–2. Overview of KS57C21516 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P0.1–P0.3	SO/K1, BUZ/K3	I/O	Input	E-1
P0.0–P0.2	SCK/K0, SI/K2	I/O	Input	E-2
P1.0–P1.3	INT0–INT2, INT4	I	Input	A-3
P2.0–P2.2	CLO, LCDCK, LCDSY	I/O	Input	E
P3.0–P3.1	TCLO0, TCLO1	I/O	Input	E
P3.2–P3.3	TCL0, TCL1	I/O	Input	E-1
P4.0–P4.3 P5.0–P5.3	COM8–COM11 COM12–COM15	I/O	Input	H-13
P6.0–P6.3	SEG55/K4–SEG52/K7	I/O	Input	H-16
P7.0–P7.3	SEG51–SEG48	I/O	Input	H-13
P8.0–P8.3 P9.0–P9.3	SEG47–SEG44 SEG43–SEG40	I/O	Input	H-13
COM0–COM7	–	O	High	H-3
SEG0–SEG39	–	O	High	H-15
V_{DD}	–	–	–	–
V_{SS}	–	–	–	–
RESET	–	I	–	B
V_{LC1}–V_{LC5}	–	–	–	–
X_{in}, X_{out}	–	–	–	–
XT_{in}, XT_{out}	–	–	–	–
TEST	–	I	–	–