



HIGH-SPEED CMOS QUAD 2-INPUT MULTIPLEXER

IDT74FCTL2257T

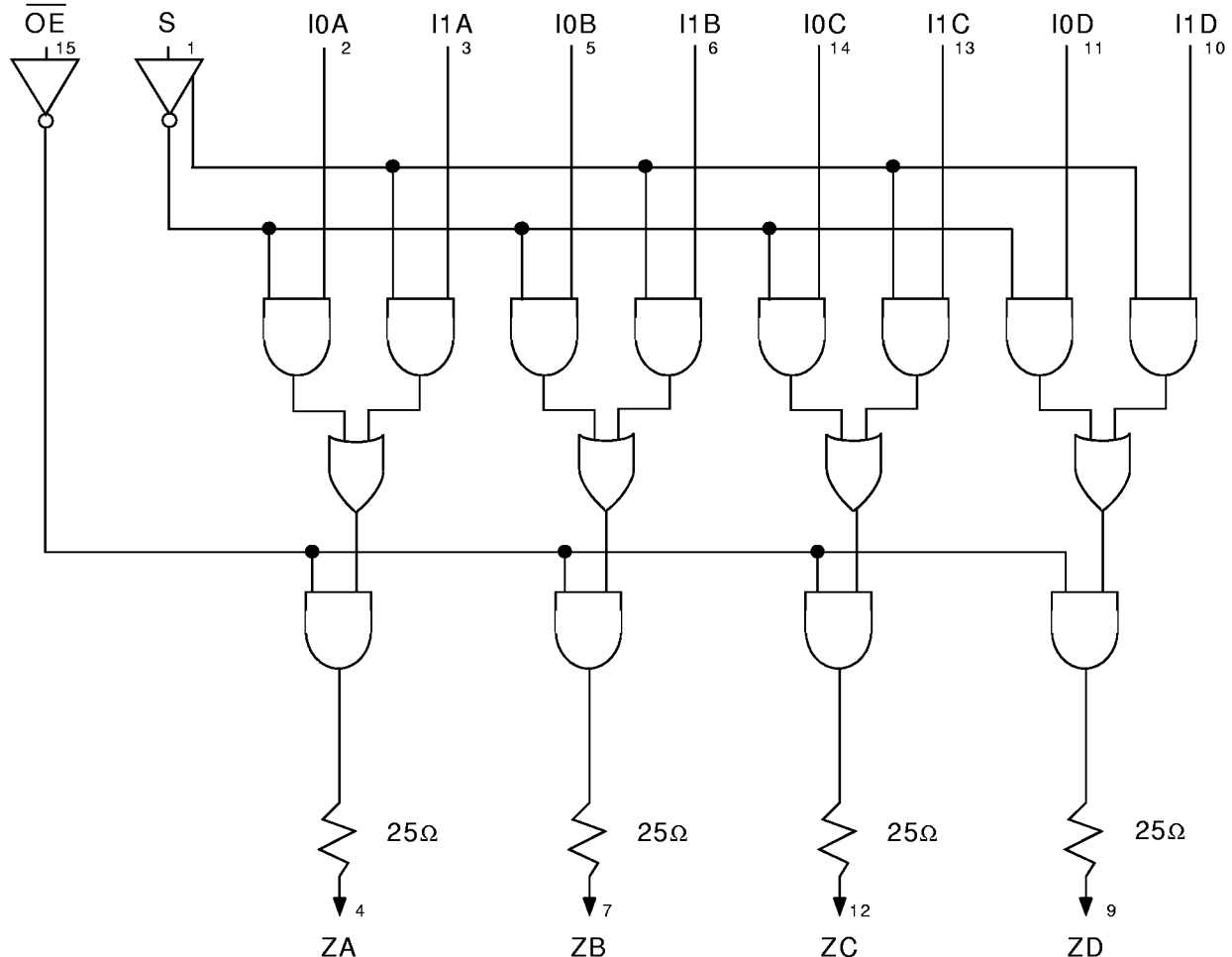
FEATURES:

- Pin and function compatible to the Quality QS74FCT Family
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- CMOS power levels: $<7.5\text{mW}$ static
- Available in PDIP, SOIC and QSOP packages
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A and C speed grades with 4.3ns for C
- $\text{IOL} = 12\text{mA}$

DESCRIPTION:

The IDT74FCTL2257T is a 25Ω resistor output version of a high-speed CMOS TTL-compatible, quad, 2-input multiplexer, useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when V_{CC} is removed from the device.

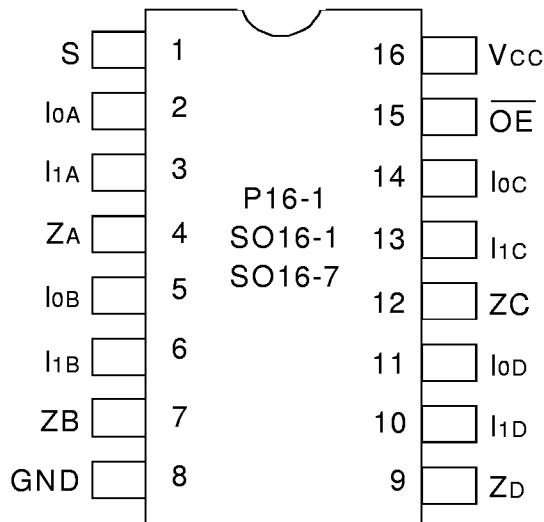
FUNCTIONAL BLOCK DIAGRAM



EXTENDED COMMERCIAL TEMPERATURE RANGE

SEPTEMBER 1999

PIN CONFIGURATION



PDIP/ SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to +7	V
TSTG	Storage Temperature	– 65 to +150	°C
IOUT	DC Output Current	120	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _O < 0	– 20	mA
I _{OK}		– 50	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

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NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
IoA - IoD	Source O Data Inputs
I1A - I1D	Source I Data Inputs
$\overline{OE}$	Enable Input (Active LOW)
S	Select Input
ZA - ZD	Outputs

FUNCTION TABLE⁽¹⁾

Inputs				Outputs
$\overline{OE}$	S	Io	Ii	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

NOTE:

- H = High Voltage Level
X = Don't Care
L = Low Voltage Level
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Extended Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for all inputs		—	0.2	—	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} < V_{CC}$	—	—	5	μA
I_{IL}	Input LOW Current						
I_{OZ}	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	5	μA
I_{OR}	Current Drive	$V_{CC} = \text{Max.}$, $V_{OUT} = 2.0\text{V}^{(2)}$		50	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$, $T_A = 25^{\circ}\text{C}$		—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -15\text{mA}$	2.4	—	—	V
V_{OL}	Output LOW Voltage (25 Ω)	$V_{CC} = \text{Min.}$	$I_{OL} = 12\text{mA}$	—	—	0.5	V
R_{OUT}	Output Resistance (25 Ω)	$V_{CC} = \text{Min.}$	$I_{OL} = 12\text{mA}$	20	28	40	Ω

NOTES:

1. Typical values are at $V_{CC} = 5.0\text{V}$, $T_A = 25^{\circ}\text{C}$.

2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

Extended Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ freq = 0	—	2	mA
I_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/MHz

NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.

2. Per TLL driven input ($V_{IN} = 3.4\text{V}$).

3. For flip-flops, I_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.

4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} \text{ DHNT} + I_{CCD} (\text{fcp}/2 + \text{fiNi})$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4\text{V}$)

DH = Duty Cycle for TTL Inputs High

NT = Number of TTL Inputs at DH

I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)

fcp = Clock Frequency for Register Devices (Zero for Non-Register Devices)

fi = Input Frequency

Ni = Number of Inputs at fi

All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Following Conditions Apply Unless Otherwise Specified:

Extended Commercial: TA = -40°C to +85°C, VCC = 5.0V ± 5%

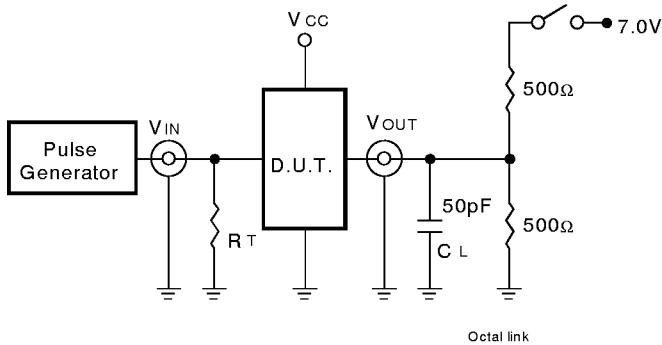
Symbol	Parameter	74FCTL2257T		74FCTL2257AT		74FCTL2257CT		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay Ixx to Zx	1.5	6	1.5	5	1.5	4.3	ns
tPLH tPHL	Propagation Delay S to Zx	1.5	10.5	1.5	7	1.5	5.2	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to Zx	1.5	8.5	1.5	7	1.5	6	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Zx	1.5	6	1.5	5.5	1.5	5	ns

NOTES:

1. CLOAD = 50pF, RLOAD = 500Ω unless otherwise noted.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

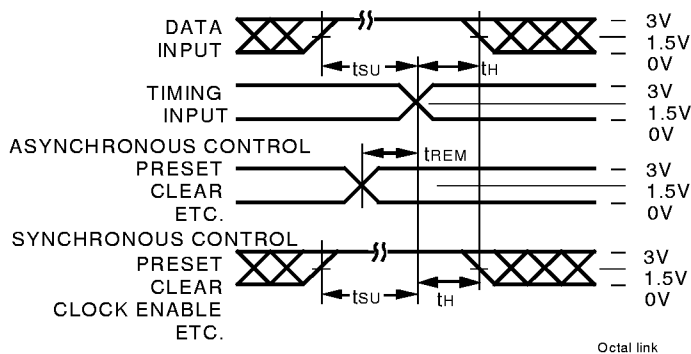
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DEFINITIONS:

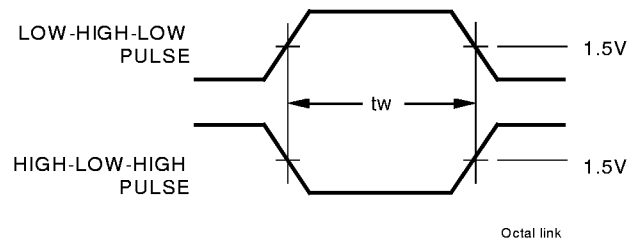
C_L = Load capacitance; includes jig and probe capacitance.

R_T = Termination resistance; should be equal to Z_{OUT} of the Pulse Generator.

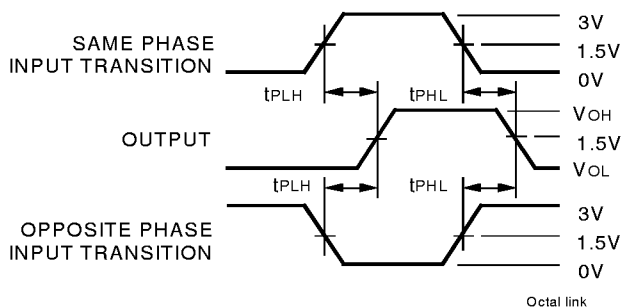
SET-UP, HOLD, AND RELEASE TIMES



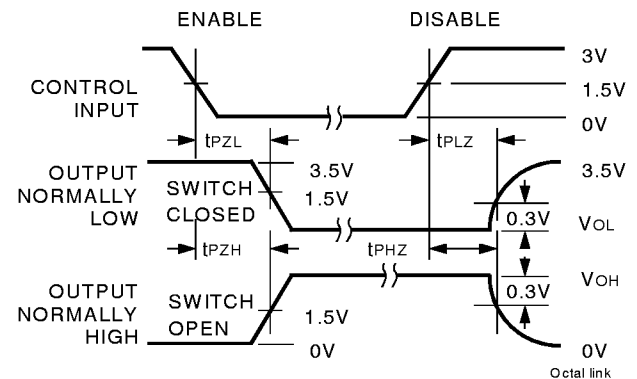
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT	XX	FCTL	XXXX	XX	
Temp. Range			Device Type	Package	
				P	Plastic DIP (P16-1)
				SO	Small Outline IC (gull wing) (SO16-1)
				Q	Quarter Size Small Outline Package (SO16-7)
				2257T	High-Speed CMOS Quad 2-Input Multiplexer
				2257AT	
				2257CT	
				74	−40 °C to +85 °C



CORPORATE HEADQUARTERS

2975 Stender Way
 Santa Clara, CA 95054

for SALES:

800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com*

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