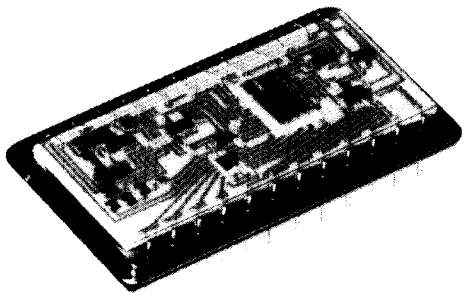
12 BIT HYBRID D/A CONVERTER WIDE OPERATING TEMPERATURE RANGE 100ns Current Settling; 3 μs Voltage Settling



DESCRIPTION

The DDC DAC87 is a 12 bit, wide temperature range (-55°C to +125°C) and high accuracy digital to analog hybrid converter. Its features include form-fit-function replacement for DAC87, linearity error of ±½ LSB, throughput rates up to 6MHz* and guaranteed monotonicity. The voltage output version, DDC DAC87-CBI-V has five pin programmable output ranges, while the current output unit, DDC DAC87-CBI-I, may be used either for direct current drive or with an external op-amp. The DDC DAC87's input is TTL compatible, requiring 1 standard TTL load drive capability and will accept complementary binary and complementary offset binary codes. The unit is packaged in a hermetically sealed 24 pin Double DIP.

APPLICATIONS

Because of its high performance, pin programmable features, and relatively low cost the DDC DAC87 has many applications. These include portable instrumentation, aircraft and shipboard displays, and the D/A in a successive approximation type analog to digital converter. These converters are rugged devices, which can be used in remotely located and hard to access equipment where small size and high MTBF are important.

*Throughput rate for 1 LSB change.

FEATURES

- *GUARANTEED SPECIFICATIONS FROM −55° C TO +125° C*
- *3,000,000 HOUR MTBF*
- *PIN COMPATIBLE WITH DAC87, DAC85*
- *HERMETICALLY SEALED 24 PIN DOUBLE DIP PACKAGE*
- *VOLTAGE AND CURRENT OUTPUT MODELS*
- *MIL-STD-883B SCREENING AVAILABLE*

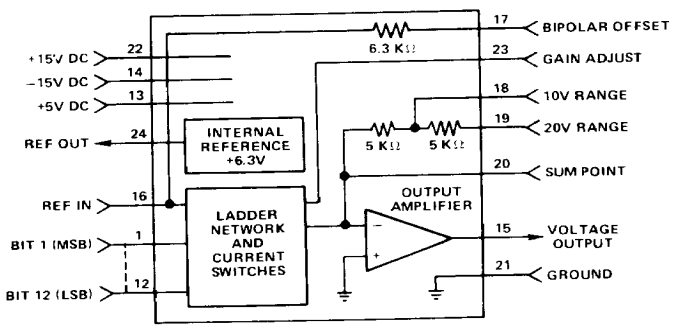


FIGURE 1. BLOCK DIAGRAM FOR VOLTAGE OUTPUT (DDC DAC87-CBI-V)

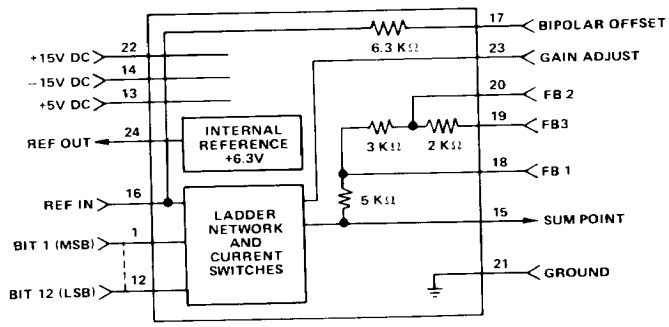


FIGURE 2. BLOCK DIAGRAM FOR CURRENT OUTPUT (DDC DAC87-CBI-I)

SPECIFICATIONS

Typical Values at 25°C and at nominal power supply voltages unless otherwise indicated:

PARAMETER	UNIT	VALUE		
RESOLUTION	bits	12		
ACCURACY		MIN	TYP	MAX
Linearity Error (+25°C)	LSB			±½
—55°C to +125°C	LSB			±1
Differential Linearity Error	LSB			+1 −¾
Gain Error (Trimmable to zero)	%		±0.1	±0.2
Gain Tempco (Using internal feedback resistors)	ppm/°C			±15
Offset Error (Trimmable to zero)	%FSR		±0.05	±0.1
Offset Tempco (Using internal feedback resistors)				
Unipolar Ranges	ppm FSR/°C		±1	±3
Bipolar Ranges	ppm FSR/°C		±5	±15
Monotonicity	bits	12		
DYNAMIC CHARACTERISTICS				
Voltage Output (DDC DAC87-CBI-V)				
Settling Time to ±0.01%FSR				
For Full Scale Change				
With 10k ohm feedback	µs			5
With 5k ohm feedback	µs			3
For 1 LSB Change	µs			1.5
Slew Rate	V/µs		20	
Current Output (DDC DAC87-CBI-I)				
Settling Time to ±0.01%FSR				
Full Scale Change				
With 10 to 100 ohm load	ns			100
With 1k ohm load	ns			500
For 1 LSB Change	ns		50	
DIGITAL INPUT				
Type (TTL Compatible)		12 parallel data bits, positive logic		
Coding		Unipolar ranges: Complementary Binary Bipolar ranges: Complementary Offset Binary and Two's Complement if the MSB Complement is supplied		
Loading		1 std. TTL load		
Maximum Logic Input Voltage Without Damage		Do not exceed voltage of +5 power supply		
ANALOG OUTPUT				
Voltage Output (DDC DAC87-CBI-V)				
Ranges (Typical Values)	V	±2.5 ±5 ±10 0 to +10 0 to +5		
Output Current	mA	±5 min		
Output Impedance		0.05 typ		
Short Circuit Protection		Fully protected		
Current Output (DDC DAC87-CBI-I)		BIPOLAR | UNIPOLAR		
Ranges (Typical Values)	ma	±1 | 0 to -2		
Output Impedance	kΩ	4.4 | 15		
Compliance	V	±2.5 max | ±2.5 max		
REFERENCE		MIN	TYP	MAX
Internal Reference				
Voltage	V		+6.3	
Current Capability	µA			200
Reference Input				
Voltage/Regulation	V		+6.3 ±10%	
Voltage Without Damage	V			+10
Current Requirements	mA		1.1	
POWER SUPPLIES				
Power Supply Requirements				
Voltages	V	+15 ±0.5	-15 ±0.5	+5 ±0.25
Maximum Voltage Without Damage	V	+18	-18	+7
Current**	mA	20 typ 25 max	20 typ 25 max	10 typ 20 max
Power Supply Sensitivity	%FSR/%P.S.	±0.002	±0.002	±0.002
** Plus load current for +15V and -15V power supplies				
TEMPERATURE RANGES (Ambient)				
Operating	°C	-55 to +125		
Storage	°C	-55 to +150		
PHYSICAL CHARACTERISTICS				
Size (24 Pin Double DIP)	in	0.8 x 1.4 x 0.2 (20 x 36 x 5 mm)		
Weight	oz	0.4 (11.3g)		

INTRODUCTION

Figure 1 and Figure 2 are block diagrams of the voltage output and current output models, respectively, of the DDC DAC87. Note that the two models have different feedback resistors and different pin connections in the output section. In both models the resistor network generates currents which are discrete fractions of the reference voltage. The fractions are determined by the digital inputs which control the current switches. The DDC DAC87 is calibrated with its own internal reference, but an external reference can be used instead. When the internal reference is used, pin 16 must be connected to pin 24.

CODING

The coding for both voltage and current output models is as shown in Figure 3. The full scale voltage (F.S.) and LSB values for all voltage and current ranges are:

RANGE	FULL SCALE (FS)	1 LSB
±2.5V	2.50000V	0.00122V
±5V	5.00000V	0.00244V
±10V	10.00000V	0.00488V
0 to +5V	5.00000V	0.00122V
0 to +10V	10.00000V	0.00244V
±1 mA	1.00000 mA	0.00049 mA
0 to —2 mA	2.00000 mA	0.00049 mA

ANALOG OUTPUT VOLTAGE		DIGITAL BIT INPUTS											
UNIPOLAR COMPLEMENTARY BINARY	BIPOLAR COMPLEMENTARY OFFSET BINARY	1	2	3	4	5	6	7	8	9	10	11	12
+F.S — 1 LSB	+F.S. — 1 LSB	0	0	0	0	0	0	0	0	0	0	0	0
+3/4 F.S.	+1/2 F.S.	0	0	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. + 1 LSB	+ 1 LSB	0	1	1	1	1	1	1	1	1	1	1	0
+1/2 F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. — 1 LSB	—1 LSB	3	0	0	0	0	0	0	0	0	0	0	0
1/4 F.S.	—1/2 F.S.	1	0	1	1	1	1	1	1	1	1	1	1
+ 1 LSB	—F.S. + 1 LSB	1	1	1	1	1	1	1	1	1	1	1	0
0	—F.S.	1	1	1	1	1	1	1	1	1	1	1	1

Notes:
1. For current output models (DDC DAC87-CBI-I), the current direction is defined as positive for currents entering the output.
2. For Complementary Two's Complement coding, the bit values are identical to those for Complementary Offset Binary coding in the above table, except that the MSB is reversed (MSB bits "1" become "0" and bits "0" become "1") using an external inverter.

FIGURE 3. BIT WEIGHT TABLE

OFFSET AND GAIN TRIM

The offset and gain errors are trimmed at the factory to within the limits listed in the specifications table. If both errors are trimmed to zero, the over-all accuracy will be equal to the linearity. Figure 4 shows trim adjustment circuits that apply to both the voltage and current output models of the DDC DAC87. The 3.9MΩ and 18MΩ fixed resistors should be located close to the converter pins to reduce noise, and the two potentiometers should have a temperature coefficient of 100 ppm/°C or less.

To trim the offset, apply the all one's digital code, which corresponds to 0 input for a unipolar range and —F.S. for a bipolar range (see Figure 3). Adjust the offset potentiometer for the proper value of analog output.

After trimming the offset, trim the gain by applying the all zero's digital code. This corresponds to +F.S. — 1 LSB, and the output should be adjusted to this value with the gain trim potentiometer.

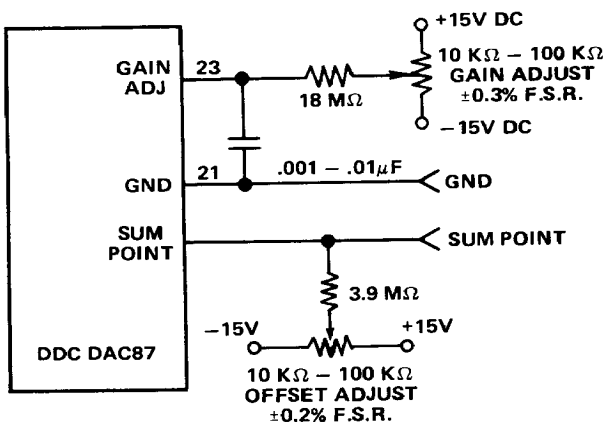


FIGURE 4. OFFSET AND GAIN TRIM CIRCUITS

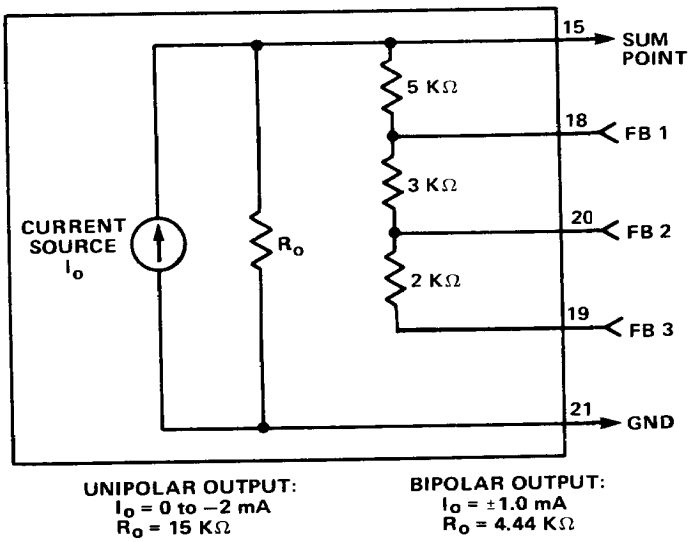


FIGURE 5. EQUIVALENT CIRCUIT FOR (DDC DAC87-CBI-I)

OUTPUT CONNECTIONS FOR (DDC DAC87-CBI-V)

The following table shows pin connections for the five voltage ranges of voltage output model of the DDC DAC87.

Voltage Range	Load Feedback Connection	Bipolar Offset Connection	Other Pin Connections
±2.5V	15 to 18	17 to 20	19 to 20
±5V	15 to 18	17 to 20	—
±10V	15 to 19	17 to 20	19 to 15
0 to +5V	15 to 18	17 to 21	19 to 20
0 to +10V	15 to 18	17 to 21	—

The output load in all cases is connected to pin 15, the voltage output. The feedback connection from pin 15 should be made as close to the load as possible to minimize the effects of line and contact impedance.

OUTPUT CONNECTIONS FOR DDC DAC87-CBI-I

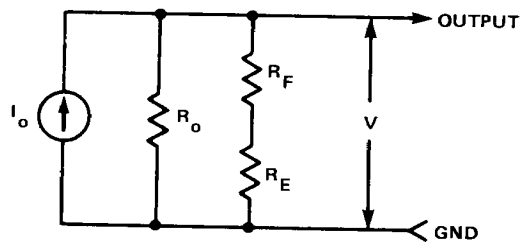
Figure 5 shows the equivalent circuit for the current output model of the DDC DAC87. The converter is represented by a current source with a parallel resistance R_o and a chain of three feedback resistors. The output is unipolar if the Bipolar Offset is connected to ground, and bipolar if it is connected to the Sum Point.

Three configurations for using the DDC DAC87-CBI-I will be discussed. In the first, the converter output current is used to drive a resistive load directly, and the internal feedback resistors are used to scale the output voltage. In the second, the internal resistors are used to provide feedback for an external op-amp. In the third, an external op-amp is used with an external feedback resistor.

1. Driving a Resistive Load. An equivalent diagram for driving a resistive load and using the internal resistors to regulate the load voltage is shown in Figure 6. I_O and R_O have the values given in Figure 5. R_F represents the pin programmed internal feedback resistance and R_E represents additional external resistance in series with R_F. The equations in Figure 6 show the relationship between the voltage V across the load and $R_F + R_E$. Two examples will be discussed, unipolar coding with an output voltage range of 0 to —2V, and bipolar coding with a voltage range of ±1V. To obtain the least temperature drift, R_F should be made as large as possible relative to R_E.

For a 0 to —2V range:

$$R_F + R_E = \frac{(15{,}000)\ (2)}{(15{,}000)\ (.002) - 2} = 1071.4\Omega$$



$$V = \frac{I_o R_o (R_F + R_E)}{R_o + R_F + R_E} \quad \text{OR} \quad R_F + R_E = \frac{R_o V}{R_o I_o - V}$$

R_E = EXTERNAL METAL FILM RESISTOR

FIGURE 6. EQUIVALENT CIRCUIT FOR DRIVING A RESISTIVE LOAD

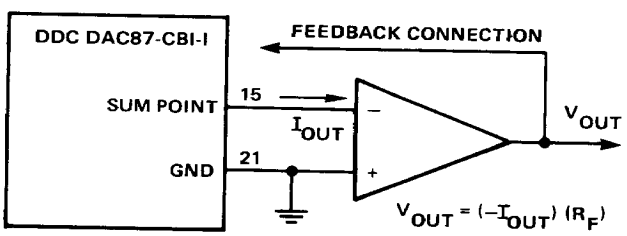


FIGURE 7. CONNECTIONS FOR EXTERNAL OP-AMP USING INTERNAL FEEDBACK RESISTOR

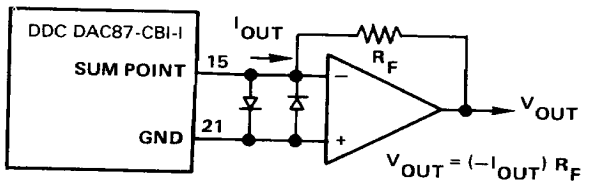


FIGURE 8. CONNECTIONS FOR EXTERNAL OP-AMP USING AN EXTERNAL FEEDBACK RESISTOR

PIN CONNECTION TABLE

FUNCTION		FUNCTION		
PIN	BOTH MODELS	PIN	DDC DAC87-CBI-V	DDC DAC87-CBI-I
1	Bit 1 (MSB)	13	+5 V DC	
2	Bit 2	14	—15 V DC	
3	Bit 3	15	Voltage Out	Sum Point
4	Bit 4	16	Ref In	
5	Bit 5	17	Bipolar Offset	
6	Bit 6	18	10V Range	FB 1
7	Bit 7	19	20V Range	FB 3
8	Bit 8	20	Sum Point	FB 2
9	Bit 9	21	Ground	
10	Bit 10	22	+15V DC	
11	Bit 11	23	Gain Adjust	
12	Bit 12 (LSB)	24	Ref Out	

The three feedback resistors can be programmed for a total resistance of 967.7 Ω by connecting all three of them in parallel. The following pin connections will accomplish this:

17 to 21; 15 to 20; 18 to 19; output from pin 18

The required value of for the external resistance will be

$$R_E = 1071.4 - 967.7 = 103.7\ \Omega$$

For a ±1V range:

$$R_F + R_E = \frac{(4440)\ (1)}{(4440)\ (.001) - 1} = 1290.6\ \Omega$$

A value of $R_F = 1200\ \Omega$ can be obtained by connecting the 2KΩ and 3KΩ resistors in parallel with the following pin connections:

17 to 15; 15 to 18; 18 to 19; output from pin 20

The required value of R_E will be:

$$R_E = 1290.6 - 1200 = 90.6\ \Omega$$

2. External Op-Amp Using Internal Feedback Resistors. Figure 7 shows how to connect an external op-amp to the DDC DAC87-CBI-I when the internal feedback resistors are used. Pin connections for various voltage ranges are as follows:

Voltage Range	Connect Feedback to Pin	Offset Pin Conn.	Other Pin Connection	Feedback Resistance R_F
±2.5V	18	15	19 to 15	2.5KΩ
±5V	18	15	—	5KΩ
±10V	19	15	—	10 KΩ
0 to +5V	18	21	19 to 15	2.5 KΩ
0 to +10V	18	21	—	5 KΩ

3. External Op-Amp With External Feedback Resistor. For output voltage ranges greater than ±10V, an external feedback resistor must be used, as shown in Figure 8. External feeback resistors will generally give poorer gain accuracy over temperature. The internal resistors may be used in series with the external resistors to minimize this effect. When high voltage op-amps are used, diodes should be installed to protect the DDC DAC87 as indicated in Figure 8.

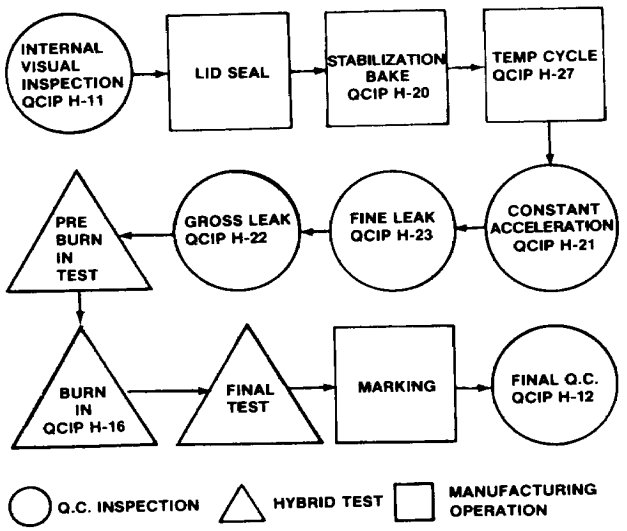
POWER SUPPLY DECOUPLING

Power supply decoupling capacitors should be used to improve noise rejection. Install two capacitors at each of the three power supply input pins, as close to the module as possible. Tie the other ends of the capacitors to ground, preferably to a ground plane underneath the module. One capacitor at each pin should be a 1 — 10μ F tantalum or electrolytic type; the second capacitor can be 0.01μF ceramic for high frequency bypassing.

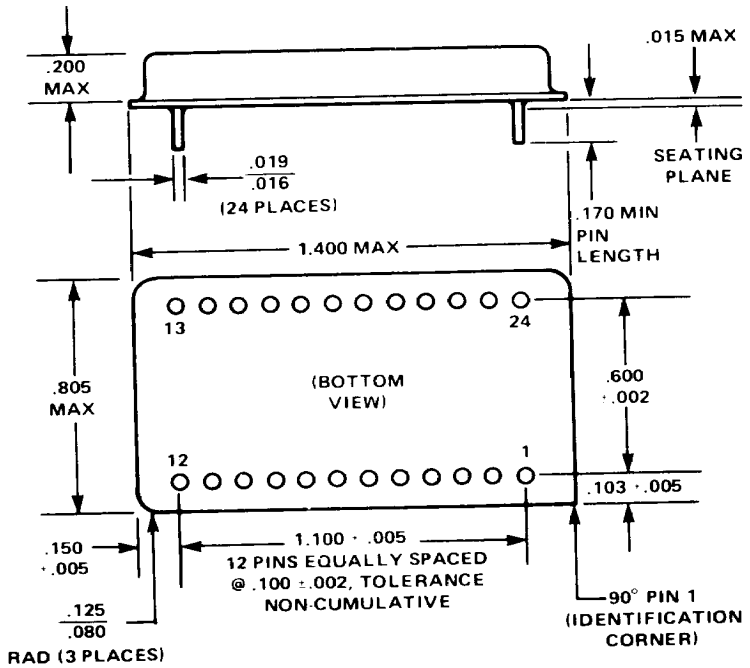
RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTFB values. Summaries of MTFB calculations are available on request. The computed MTBF value for DDC DAC87, with MIL-STD-883 processing, (including burn in) is 3,400,000 hours, Ground Fixed, at 25°C.

DDC Processing to MIL-STD-883 is Optional as follows:



MECHANICAL OUTLINE
24 Pin Double Dip



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

MIL-STD-883 REQUIREMENT	DDC CONTROL PROCEDURE	TITLE	REMARKS
2017	QCIP H-11	Internal Visual	
None	Welded	Lid Seal	DDC Procedure
1008	QCIP H-20	Stabilization Bake	Condition B 24 hrs. @ 125°C.
1010	QCIP H-27	Temperature Cycling	Condition B 10 Cycles +25, -55, +25, +125°C.
2001	QCIP H-21	Constant Acceleration	5000g Condition A
1014	QCIP H-23	Fine Leak	883 Test Condition A
	QCIP H-22	Gross Leak	883 Test Condition C
None	QCIP H-16	Burn In	DDC Procedure
2009	QCIP H-12	Final QC	External Visual

ORDERING INFORMATION

DDC DAC87 -CBI-V -883B

MIL-STD-883 Processing: Optional
883B = Conforms to MIL-STD-883B, DDC procedures.
Blank = Same, except pre burn in test and burn in are omitted.

Output Type:
V = Voltage output
I = Current output