T-46-13-25

CY7C265

CYPRESS SEMICONDUCTOR 64K Registered PROM

Features

- CMOS for optimum speed/power
- High speed
  - 15 ns max. set-up
  - 12 ns clock to output
- Low power
  - 770 mW (commercial)
  - 965 mW (military)
- On-chip edge-triggered registers
  - Ideal for pipelined microprogrammed systems
- EPROM technology
  - 100% programmable
  - Reprogrammable (7C265W)
- 5V ±10% V_{CC}, commercial and military
- Capable of withstanding >2001V static discharge
- Slim 28-pin, 300-mil plastic or hermetic DIP

Functional Description

The CY7C265 is a 64K registered PROM. It is organized as 8,192 words by 8 bits wide, and has a pipeline output register. In addition, the device features a programmable initialize byte that may be loaded into the pipeline register with the initialize signal. The programmable initialize byte is the 8,193rd byte in the PROM and its value is programmed at the time of use.

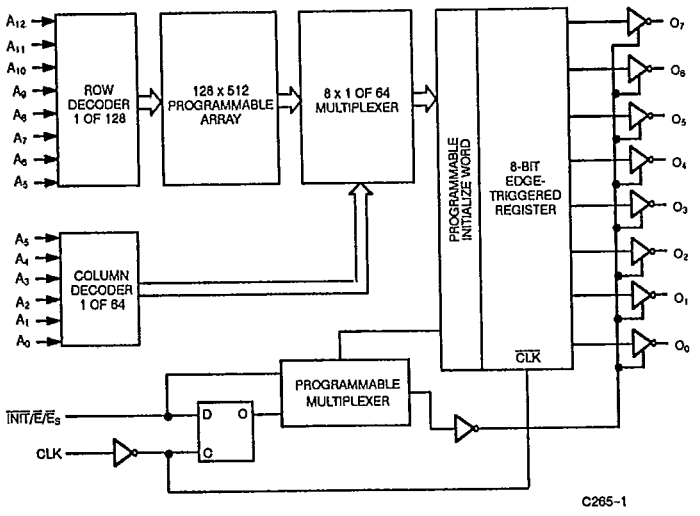
Packaged with 28 pins, the PROM has 13 address signals (A_0 through A_{12}), 8 data out signals (O_0 through O_7), $\overline{E}/\overline{I}$ (enable or initialize), and CLOCK.

CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the pipeline register on each rising edge. The data will appear on the outputs if they are enabled. One pin on the CY7C265 is programmed to perform either the enable or the initialize function.

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C265 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

Logic Block Diagram



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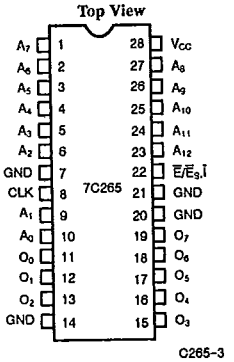
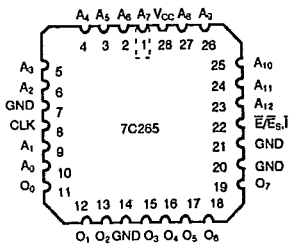
Pin Configurations

DIP
Top View



C265-3

LCC
Top View



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Functional Description (continued)

If the $\overline{E}/I$ pin is used for $\overline{INIT}$ (asynchronous), then the outputs are permanently enabled. The initialize function is useful during power-up and time-out sequences, and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user programmed 8193rd 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1's and 0's into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register clear (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register preset (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the pipeline register and onto the outputs. The $\overline{INIT}$ LOW disables clock and must return HIGH to enable clock independent of all other inputs, including the clock.

Selection Guides

		7C265-15	7C265-18	7C265-25	7C265-40	7C265-50	7C265-60
Maximum Set-Up Time (ns)		15	18	25	40	50	60
Maximum Clock to Output (ns)		12	15	20	20	25	25
Maximum Operating Current (mA)	Com'l	140	140		100	80	80
	Mil		175	175		120	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage to Ground Potential ..... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to + 7.0V

DC Input Voltage ..... – 3.0V to + 7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C265-15 Min.	7C265-15 Max.	7C265-18 Min.	7C265-18 Max.	7C265-25 Min.	7C265-25 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4		0.4		0.4	V
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil		0.4		0.4		0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+ 10	– 10	+ 10	– 10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		– 40	+ 40	– 40	+ 40	– 40	+ 40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		140		140			mA
			Mil				175		175	

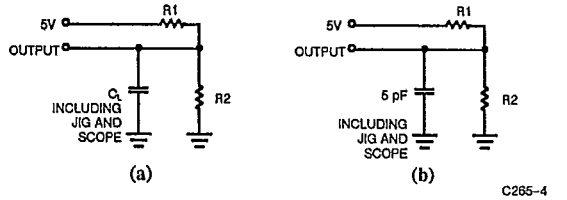
Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C265-40 Min.	7C265-40 Max.	7C265-50 Min.	7C265-50 Max.	7C265-60 Min.	7C265-60 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA	Com'l		0.4		0.4		0.4	V
		V_{CC} = Min., I_{OL} = 8.0 mA	Mil		0.4		0.4		0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+ 10	– 10	+ 10	– 10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		– 40	+ 40	– 40	+ 40	– 40	+ 40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		100		80		80	mA
			Mil				120		100	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveform



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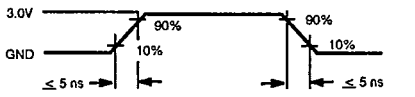
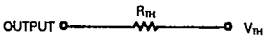


C265-5

Equivalent to: THÉVENIN EQUIVALENT



I_{OH}/I_{OL}		–2 mA/8 mA	–2 mA/12 mA
R1		500Ω (658Ω Mil)	250Ω
R2		333Ω (403Ω Mil)	167Ω
R_{TH}		200Ω (250Ω Mil)	100Ω
C_L		30 pF	50 pF
V_{TH}	Com'l	2.0V	2.11
	Mil	1.9V	2.0

CYPRESS SEMICONDUCTOR

Switching Characteristics Over the Operating Range[2]

Parameters	Description	7C265-15		7C265-18		7C265-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	15		18		25		ns
t_{HA}	Address Hold from Clock	0		0		0		ns
t_{CO}	Clock to Output Valid		12		15		20	ns
t_{PW}	Clock Pulse Width	12		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync. Enable Only)	12		15		20		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		7		10		ns
t_{DI}	$\overline{INIT}$ to Output Valid		15		18		25	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	12		15		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	12		15		20		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		12		15		20	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		12		15		20	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Async. Mode)		12		15		20	ns
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		12		15		20	ns

Parameters	Description	7C265-40		7C265-50		7C265-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	40		50		60		ns
t_{HA}	Address Hold from Clock	0		0		0		ns
t_{CO}	Clock to Output Valid		20		25		25	ns
t_{PW}	Clock Pulse Width	15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync. Enable Only)	15		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		ns
t_{DI}	$\overline{INIT}$ to Output Valid		25		35		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	20		25		25		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	25		35		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		20		25		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		20		25		25	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Async. Mode)		20		25		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		20		25		25	ns

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.

Switching Waveform

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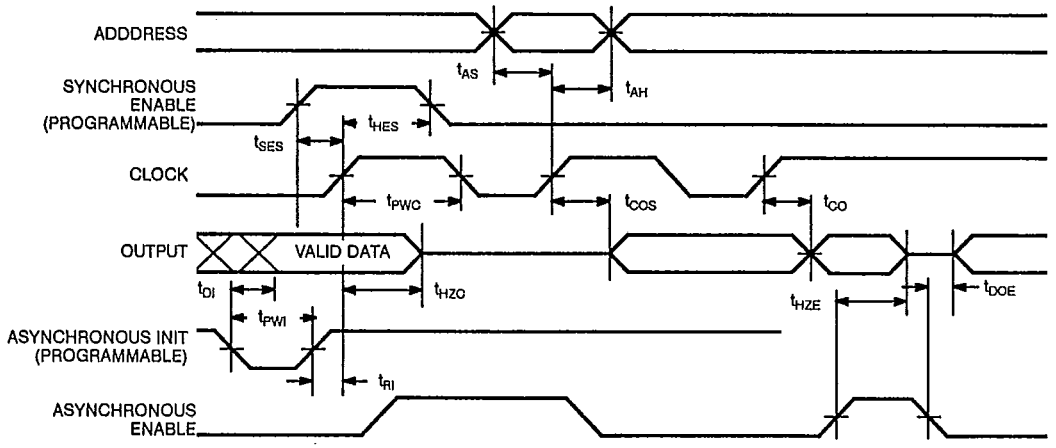


Notes on Testing:

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

A. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1-μF or larger capacitor and a 0.01-μF or smaller capactor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.

B. Do not leave any inputs disconnected (floating) during any tests.

C. Do not attempt to perform threshold tests under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. These transients, which flow through the parasitic inductance between the device ground pin and the test system ground, can create significant reductions in observable input noise immunity.

D. Output levels are measured at 1.5V reference levels.

E. Transition is measured at steady-state HIGH level - 500 mV or steady-state LOW level + 500 mV on the output from the 1.5V level on inputs with load as shown in (b) of AC Test Loads and Waveforms.

Programming Algorithm for the Architecture

The 7C265 offers a limited selection of programmed architecture. Programming these features should be done with a single 10-ms-wide pulse in place of the intelligent algorithm, mainly because these features are verified operationally, not with the $\overline{VFY}$ pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C265 architecture, V_{PP} is applied to pins 3, 9, and 22. The choice of a particular mode depends on the states of the other pins during programming, so it is important that the condition of the other pins be met as set forth in the mode table. The considerations that apply with respect to power-up and power-down during intelligent programming also apply during architecture programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling $\overline{PGM}$ from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C265 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity • exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C265 needs to be within one inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Mode Table

Mode Select	P2 A_6	P3 A_5	P26 A_9	P6 A_2	P7 $\overline{PGM}$	P8 CLK	P9 A_1	P10 A_0	P20 $\overline{VFY}$	P24 A_{11}	P22 $\overline{E/I}$ V_{PP}	P23 A_{12}
Normal Read	A_6	A_5	A_9	A_2	L	L/H	A_1	A_0	HIZ	A_{11}	H/L	A_{12}
Program (Memory)	A_6	A_5	A_9	A_2	L	L	A_1	A_0	H	A_{11}	V_{PP}	A_{12}
Program Verify	A_6	A_5	A_9	A_2	H	L	A_1	A_0	L	A_{11}	V_{PP}	A_{12}
Program Inhibit	A_6	A_5	A_9	A_2	H	L	A_1	A_0	H	A_{11}	V_{PP}	A_{12}
Async. Enable Read	A_6	A_5	A_9	A_2	L	L	A_1	A_0	HIZ	A_{11}	L	A_{12}
Sync. Enable Read	A_6	A_5	A_9	A_2	L	L/H	A_1	A_0	HIZ	A_{11}	L	A_{12}
Async. Init. Read	A_6	A_5	A_9	A_2	L	L	A_1	A_0	HIZ	A_{11}	L	A_{12}
Program Sync. Enable[4]	H	V_{PP}	A_9	H	L	L	V_{PP}	L	H	H	V_{PP}	H
Program Initialize[5]	H	V_{PP}	A_9	L	L	L	V_{PP}	L	H	H	V_{PP}	L
Program Initial Byte	H	V_{PP}	A_9	L	L	L	V_{PP}	H	H	L	V_{PP}	A_{12}

Notes:
4. Default is asynchronous enable.
5. Default is enable.

Bit Map Data

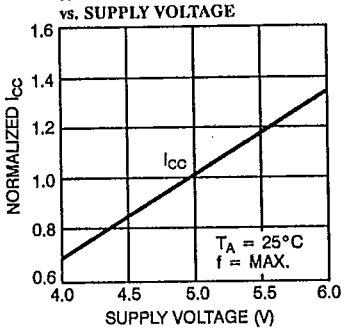
Programmer Address (Hex.)		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
.	.	.
8191	1FFF	Data
8192	2000	INIT Byte
8193	2001	Control Byte

Control Byte

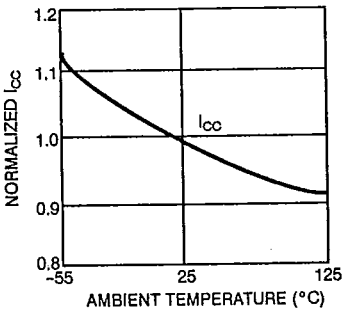
00 Asynchronous output enable (default condition)
01 Synchronous output enable
02 Asynchronous initialize

Typical DC and AC Characteristics

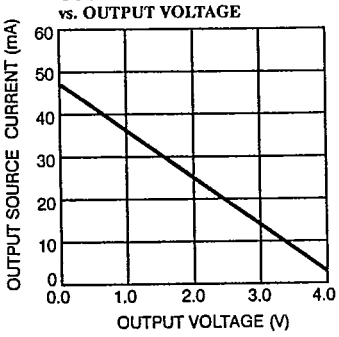
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



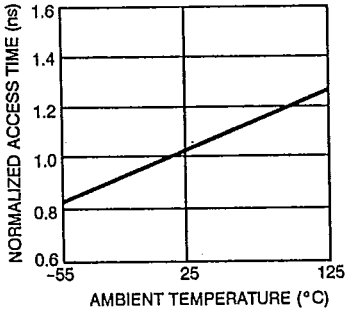
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



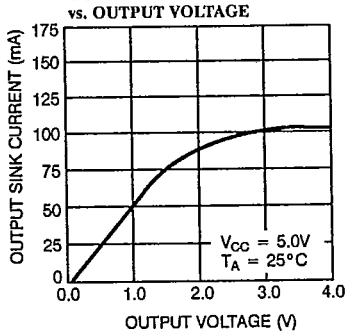
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



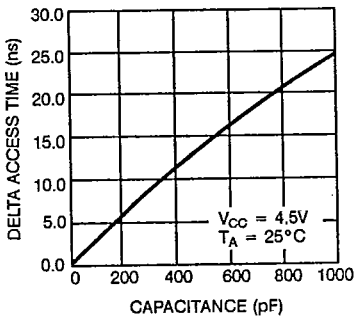
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
15	140	CY7C265-15PC	P21	Commercial
		CY7C265-15DC	D22	
		CY7C265-15LC	L64	
		CY7C265-15QC	Q64	
		CY7C265-15WC	W22	
18	140	CY7C265-18PC	P21	Commercial
		CY7C265-18DC	D22	
		CY7C265-18LC	L64	
		CY7C265-18QC	Q64	
		CY7C265-18WC	W22	
	175	CY7C265-18DMB	D22	Military
		CY7C265-18WMB	W22	
		CY7C265-18LMB	L64	
		CY7C265-18QMB	Q64	
25	175	CY7C265-25DMB	D22	Military
		CY7C265-25WMB	W22	
		CY7C265-25LMB	L64	
		CY7C265-25QMB	Q64	
40	100	CY7C265-40PC	P21	Commercial
		CY7C265-40DC	D22	
		CY7C265-40LC	L64	
		CY7C265-40QC	Q64	
		CY7C265-40WC	W22	
50	80	CY7C265-50PC	P21	Commercial
		CY7C265-50DC	D22	
		CY7C265-50LC	L64	
		CY7C265-50QC	Q64	
		CY7C265-50WC	W22	
	175	CY7C265-50DMB	D22	Military
		CY7C265-50WMB	W22	
		CY7C265-50LMB	L64	
		CY7C265-50QMB	Q64	
60	80	CY7C265-60PC	P21	Commercial
		CY7C265-60DC	D22	
		CY7C265-60LC	L64	
		CY7C265-60QC	Q64	
		CY7C265-60WC	W22	
	100	CY7C265-60DMB	D22	Military
		CY7C265-60WMB	W22	
		CY7C265-60LMB	L64	
		CY7C265-60QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{PW}	7, 8, 9, 10, 11
t_{SES}	7, 8, 9, 10, 11
t_{HES}	7, 8, 9, 10, 11
t_{COS}	7, 8, 9, 10, 11

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