



M.S.KENNEDY CORP.

HIGH POWER DUAL OPERATIONAL AMPLIFIER

101

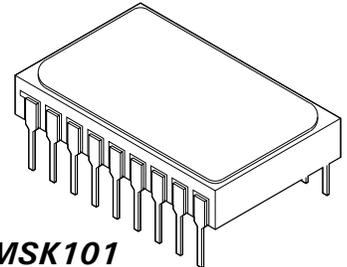
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FEATURES:

- Operates In Class AB Or Class C Mode
- Low Cost
- High Voltage Operation : 150V
- Low Quiescent Current : ± 8.0 mA Total Typ. In Class "C" Mode
- High Output Current : 5A Min. Per Amplifier
- No Second Breakdown
- High Speed : 27V/ μ S Typ.
- External Compensation For Optimum Gain-Bandwidth

MIL-PRF-38534 QUALIFIED

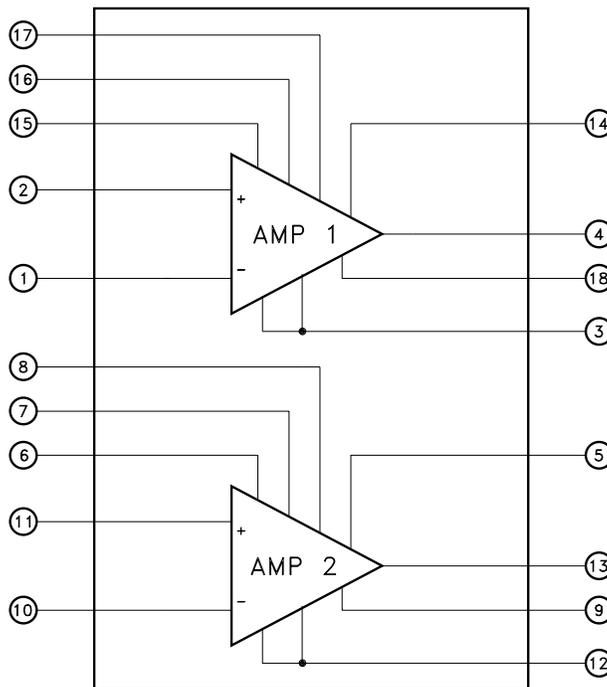


MSK101

DESCRIPTION:

The MSK 101 is a dual high power monolithic MOSFET operational amplifier ideally suited for high power amplification and magnetic deflection applications. With a total supply voltage rating of 150 volts and 5A of output current available from each amplifier, the MSK 101 is also an excellent low cost choice for motor drive circuits. The MOSFET output frees the MSK 101 from secondary breakdown limitations and power dissipation is kept to a minimum with a typical quiescent current rating of only ± 8.0 mA total in class "C" mode. Power saving class "C" mode is enabled by the user externally. The MSK 101 is packaged in a hermetically sealed 18 pin ceramic dip which has two external compensation pins for each amplifier.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- PA Audio
- Magnetic Deflection
- Bridge Motor Drive
- Noise Cancellation

PIN-OUT INFORMATION

1 Inverting Input 1	18 Current Sense 1
2 Non-Inverting Input 1	17 Amp 1 Comp 2
3 -Vcc 1	16 Amp 1 Comp 1
4 Output Drive 1	15 Quiescent Current Adjust 1
5 +Vcc 2	14 +Vcc 1
6 Quiescent Current Adjust 2	13 Output Drive 2
7 Amp 2 Comp 1	12 -Vcc 2
8 Amp 2 Comp 2	11 Non-Inverting Input 2
9 Current Sense 2	10 Inverting Input 2

ABSOLUTE MAXIMUM RATINGS

V_{CC} ②	Total Supply Voltage	150V
$\pm I_{OUT}$	Output Current (within S.O.A.)	$\pm 5A$
V_{IND}	Input Voltage (Differential)	$\pm 16V$
V_{IN}	Input Voltage (Common Mode)	$\pm V_{CC}$
T_J	Junction Temperature	150°C

T_{ST}	Storage Temperature	-65°C to +150°C
T_{LD}	Lead Temperature	300°C
T_C	Case Operating Temperature (MSK101B)	-55°C to +125°C
	(MSK101)	-40°C to +85°C
R_{TH}	Thermal Resistance (DC) Junction to Case	5.0°C/W

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions ①	Group A Subgroup	MSK101B			MSK101			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
STATIC									
Supply Voltage Range ② ④		-	± 15	± 50	± 75	± 15	± 50	± 75	V
Quiescent Current	$V_{IN} = 0V$	1	-	± 30	± 50	-	± 30	± 50	mA
		2	-	± 20	± 45	-	-	-	mA
		3	-	± 35	± 65	-	-	-	mA
Quiescent Current (Class 'C')	$V_{IN} = 0V$	1	-	± 4	± 6		± 4	± 6	mA
INPUT									
Offset Voltage	$V_{IN} = 0V$	1	-	± 5	± 10	-	± 5	± 15	mV
Offset Voltage Drift ④	$V_{IN} = 0V$	2,3	-	± 10	± 50	-	± 10	-	$\mu V/^\circ C$
Offset Voltage vs $\pm V_{CC}$ ④	$V_{IN} = 0V$	1	-	± 8	± 15	-	± 8	± 15	$\mu V/V$
Input Bias Current ④	$V_{CM} = 0V$	1,3	-	± 20	± 100	-	± 20	± 100	pA
		2	-	-	± 50	-	-	-	nA
Input Impedance ④	(DC)	-	-	10^{11}	-	-	10^{11}	-	Ω
Input Capacitance ④		-	-	5	-	-	5	-	pF
Common Mode Rejection ④	$V_{CM} = \pm 30VDC$	-	90	106	-	90	106	-	dB
Noise	10KHz BW	-	-	10	-	-	10	-	$\mu VRMS$
OUTPUT									
Output Voltage Swing	$I_{OUT} = \pm 5A$ Peak	4	± 40	± 42	-	± 40	± 42	-	V
Output Current	$V_{OUT} = MAX$	4	± 5	± 5.5	-	± 5	± 5.5	-	A
Power Bandwidth ④	$V_{OUT} = 80V_{PP}$	-	-	66	-	-	66	-	KHz
Settling Time to 0.1% ③ ④	10V Step	-	-	2	-	-	2	-	μS
Capacitive Load ④	$A_v = +1V/V$ $C_c = 68pF$	-	10	-	-	10	-	-	nF
TRANSFER CHARACTERISTICS									
Slew Rate	$C_c = Open$	4	20	27	-	20	27	-	$V/\mu S$
Open Loop Voltage Gain ④	$F = 15Hz$	4	94	106	-	94	106	-	dB

NOTES:

- ① Unless otherwise noted $C_c = 10pF$, $R_c = 1.0K\Omega$, $\pm V_{CC} = \pm 50VDC$ and specifications apply to each amplifier.
- ② Derate maximum supply voltage 0.5V/°C below $T_c = +25^\circ C$. No derating is needed above $T_c = 25^\circ C$.
- ③ $A_v = -10V/V$ measured in false summing junction circuit.
- ④ Devices shall be capable of meeting the parameter, but need not be tested. Typical parameters are for reference only.
- ⑤ Industrial grade devices shall be tested to subgroups 1 and 4 unless otherwise requested.
- ⑥ Military grade devices ('B' suffix) shall be 100% tested to subgroups 1,2,3 and 4.
- ⑦ Subgroup 5 and 6 testing available upon request.
- ⑧ Subgroup 1,4 $T_c = +25^\circ C$
Subgroup 2,5 $T_c = +125^\circ C$
Subgroup 3,6 $T_A = -55^\circ C$

APPLICATION NOTES

CURRENT LIMIT (SEE TYPICAL CONNECTION DIAGRAM)

A value of current limit resistance can be calculated as follows:

$$R_{CL} = (0.83 - (0.05 * I_{CL})) / I_{CL}$$

Where:

R_{CL} is the current limit resistor value

I_{CL} is the current limit

$0.05 * I_{CL}$ is the voltage dropped in the current limit path across internal impedances other than the actual current limit resistor

0.83 volts is the voltage drop that must be developed across the current limit connections to activate the current limit circuit

The maximum practical value of current limit resistance is 16 ohms. The current limit resistor will decrease available output voltage swing in the following manner:

$$V_R = I_O * R_{CL}$$

V_R is the reduction in output voltage swing due to the current limit resistor. It is recommended the user limit output current to a value as close to the required output current as possible, without clipping output voltage swing. Current limit will vary with case temperature. Refer to the typical performance curves to predict current limit drift. If current limit is not required replace the resistor with a short.

STABILITY

The MSK 101 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10nF. However, it is recommended that the parallel sum of the input and feedback resistor be 1000 ohms or less for closed loop gains of ten or less to minimize phase shift caused by the R-C network formed by the input resistor, feedback resistor and input capacitance. The user can tailor the performance of the MSK 101 to their application using the external compensation pins. The graphs of small signal gain and phase as well as the graphs of slew rate and power response demonstrate the effect of various forms of compensation. The compensation capacitor must be rated at 150 volts working voltage if maximum power supply voltages are used. The compensation resistor and capacitor lead lengths must be kept as short as possible to minimize spurious oscillations. A high quality NPO capacitor is recommended for the compensation capacitor. An effective method of checking amplifier stability is to apply the worst case capacitive load to the output of the amplifier and drive a small signal square wave across it. If overshoot is less than 25%, the system will typically be stable.

INPUT PROTECTION

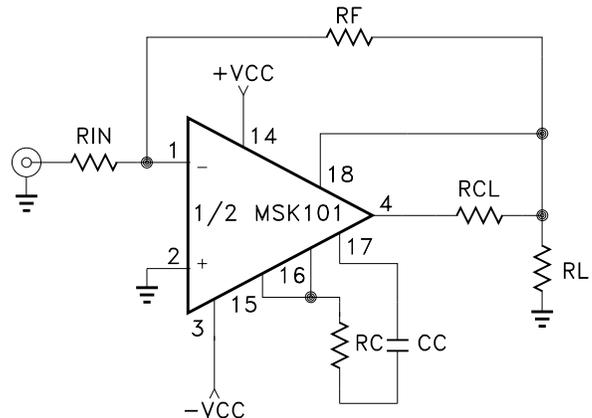
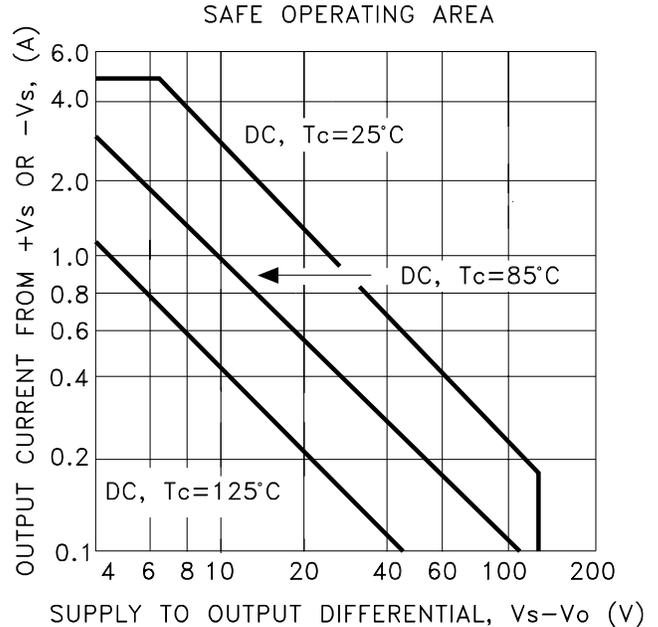
Input protection circuitry within the MSK 101 will clip differential input voltages greater than 16 volts. The inputs are also protected against common mode voltages up to the supply rails as well as static discharge. There are 300 ohm current limiting resistors in series with each input. These resistors may become damaged in the event the input overload is capable of driving currents above 1mA. If severe overload conditions are expected, external input current limiting resistors are recommended.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the die metallization.
2. The junction temperature of the output MOSFET's.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery reverse biased diodes should be connected from the output to ground.



TYPICAL CONNECTION DIAGRAM

CLASS "C" MODE

The user can enable class "C" mode by simply connecting pin 15 to pin 16 and pin 6 to pin 7. This connection will disable the bias control network in the output stage of each amplifier. Quiescent current will drop to ± 8 mA total typically and a small amount of crossover distortion will appear on the output waveforms. This mode of operation is recommended for switching type applications where distortion is not a critical specification and quiescent power dissipation must be minimized. Disconnecting the pin 15 to pin 16 and pin 6 to pin 7 shorts will enable the bias control network and the outputs will be biased in class AB mode again. Pins 15 and 6 should be left unconnected when using class AB mode. (Do not ground or pull high).

TYPICAL PERFORMANCE CURVES

