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**Document Title**

**512Kx36 & 1Mx18-Bit Pipelined NtRAM™**

**Revision History**

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial document.	Mar. 23, 2004	Advance
0.1	1. Update the current spec(Icc, Isb)	May. 13, 2004	Preliminary
0.2	1. Change the ISB, ISB1, ISB2 - ISB ; from 120mA to 170mA - ISB1 ; from 80mA to 150mA - ISB2 ; from 80mA to 130mA	Sep. 21. 2004	Preliminary
0.3	1. Remove the 1.8V Vdd voltage level	Oct. 18, 2004	Preliminary
0.4	1. Remove the -20 and -13 speed bin	Jan. 04, 2005	Preliminary

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The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

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**16Mb NtRAM(Flow Through / Pipelined) Ordering Information**

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7M161835B-QC(I)65	FlowThrough	3.3/2.5	6.5ns	Q : 100TQFP F : 165FBGA	C ; Commercial Temp.Range I ; Industrial Temp.Range
	K7N161831B-Q(F)C(I)25/16	Pipelined	3.3/2.5	250/167MHz		
512Kx36	K7M163635B-QC(I)65	FlowThrough	3.3/2.5	6.5ns		
	K7N163631B-Q(F)C(I)25/16	Pipelined	3.3/2.5	250/167MHz		

**512Kx36 & 1Mx18-Bit Pipelined NtRAM™**

**FEATURES**

- $V_{DD}$  = 2.5 or 3.3V +/- 5% Power Supply.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data-contention .
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- 100-TQFP-1420A
- 165FBGA(11x15 ball array) with body size of 13mmx15mm.
- Operating in commercial and industrial temperature range.

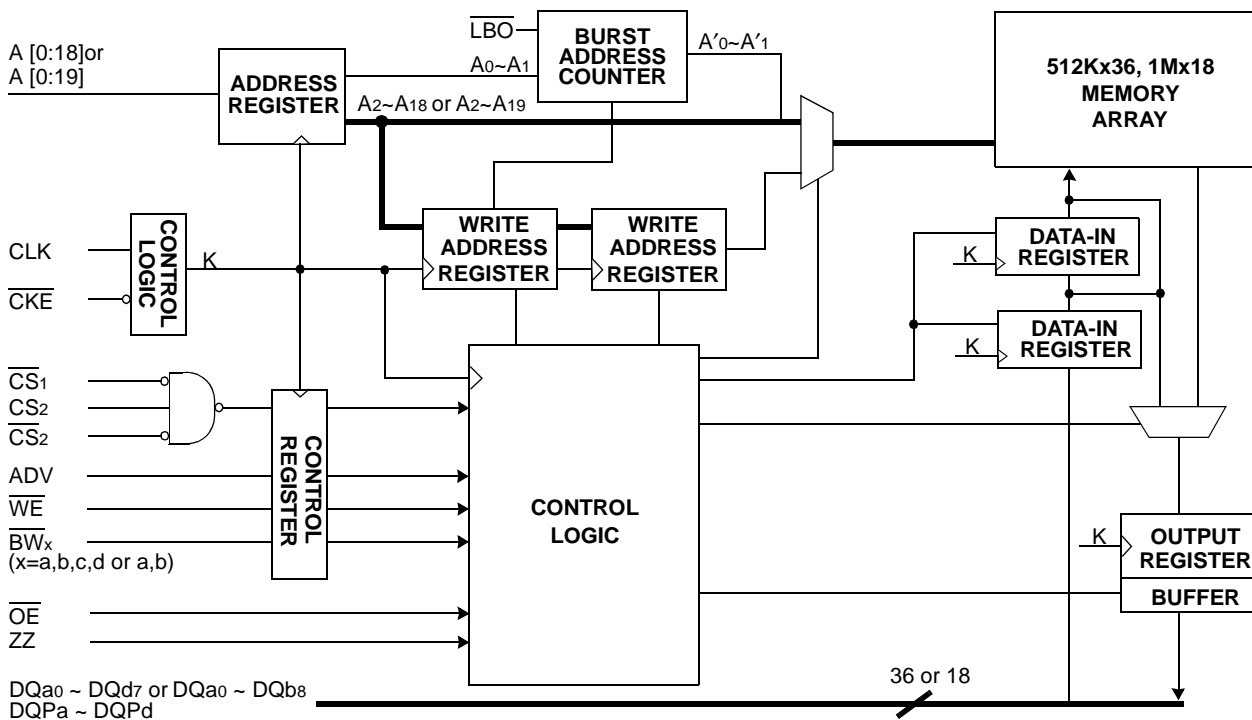
**GENERAL DESCRIPTION**

The K7N163631B and K7N161831B are 18,874,368-bits Synchronous Static SRAMs. The NtRAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low". Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock. The K7N163631B and K7N161803B are implemented with SAMSUNG's high performance CMOS technology and is available in 100pin TQFP and 165FBGA packages. Multiple power and ground pins minimize ground bounce.

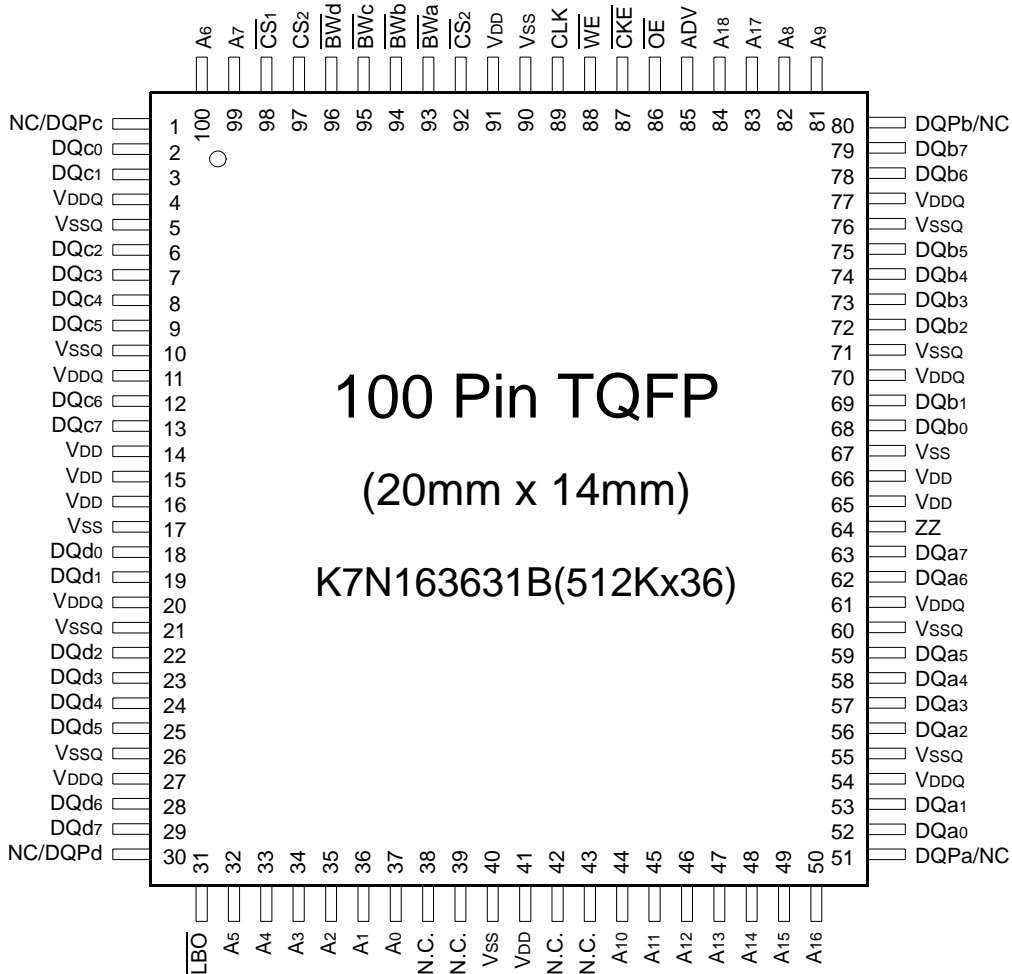
**FAST ACCESS TIMES**

PARAMETER	Symbol	-25	-16	Unit
Cycle Time	tCYC	4.0	6.0	ns
Clock Access Time	tCD	2.6	3.5	ns
Output Enable Access Time	tOE	2.6	3.5	ns

**LOGIC BLOCK DIAGRAM**



**PIN CONFIGURATION(TOP VIEW)**

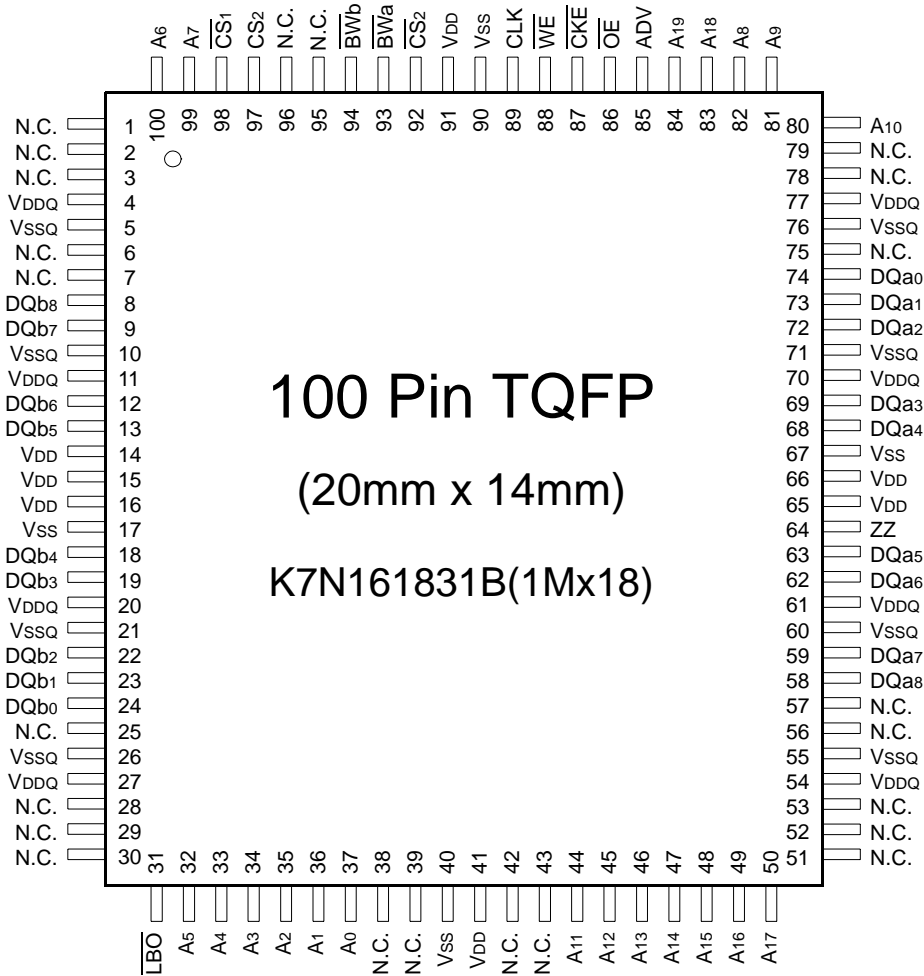


**PIN NAME**

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,81 82,83,84,99,100	VDD	Power Supply(+3.3V)	14,15,16,41,65,66,91
			VSS	Ground	17,40,67,90
ADV	Address Advance/Load	85	N.C.	No Connect	38,39,42,43
WE	Read/Write Control Input	88			
CLK	Clock	89	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CKE	Clock Enable	87	DQb0~b7	Data Inputs/Outputs	68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0~c7	Data Inputs/Outputs	2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0~d7	Data Inputs/Outputs	18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd or NC	Data Inputs/Outputs	51,80,1,30
BWx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
ZZ	Power Sleep Mode	64	VSSQ	Output Ground	5,10,21,26,55,60,71,76
LBO	Burst Mode Control	31			

**Note :** 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

**PIN CONFIGURATION(TOP VIEW)**



**PIN NAME**

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,80 81,82,83,84,99,100	VDD	Power Supply(+3.3V)	14,15,16,41,65,66,91
			VSS	Ground	17,40,67,90
ADV	Address Advance/Load	85	N.C.	No Connect	1,2,3,6,7,25,28,29,30, 38,39,42,43,51,52,53, 56,57,75,78,79,95,96
WE	Read/Write Control Input	88	DQa0~a8	Data Inputs/Outputs	58,59,62,63,68,69,72,73,74
CLK	Clock	89	DQb0~b8	Data Inputs/Outputs	8,9,12,13,18,19,22,23,24
CKE	Clock Enable	87			
CS1	Chip Select	98	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
CS2	Chip Select	97	VSSQ	Output Ground	5,10,21,26,55,60,71,76
CS2	Chip Select	92			
BWx(x=a,b)	Byte Write Inputs	93,94			
OE	Output Enable	86			
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

**NOTE :** A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

**165-PIN FBGA PACKAGE CONFIGURATIONS(TOP VIEW)**

**K7N163631B(512Kx36)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC	A	$\overline{CS1}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CS2}$	$\overline{CKE}$	ADV	A	A	NC
<b>B</b>	NC	A	CS2	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
<b>C</b>	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
<b>D</b>	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
<b>E</b>	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
<b>F</b>	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
<b>G</b>	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
<b>H</b>	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
<b>J</b>	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
<b>K</b>	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
<b>L</b>	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
<b>M</b>	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
<b>N</b>	DQPd	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQPd
<b>P</b>	NC	NC	A	A	TDI	A <sub>1</sub> *	TDO	A	A	A	NC
<b>R</b>	$\overline{LBO}$	NC	A	A	TMS	A <sub>0</sub> *	TCK	A	A	A	A

**Note :** \* A<sub>0</sub> and A<sub>1</sub> are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

**PIN NAME**

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
A <sub>0</sub> ,A <sub>1</sub>	Burst Address Inputs	VSS	Ground
ADV	Address Advance/Load	N.C.	No Connect
WE	Read/Write Control Input		
CLK	Clock	DQa	Data Inputs/Outputs
CKE	Clock Enable	DQb	Data Inputs/Outputs
CS <sub>1</sub>	Chip Select	DQc	Data Inputs/Outputs
CS <sub>2</sub>	Chip Select	DQd	Data Inputs/Outputs
CS <sub>x</sub>	Chip Select	DQPa~Pd	Data Inputs/Outputs
BW <sub>x</sub>	Byte Write Inputs		
(x=a,b,c,d)		VDDQ	Output Power Supply
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
LBO	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

**165-PIN FBGA PACKAGE CONFIGURATIONS(TOP VIEW)**

**K7N161831B(1Mx18)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC	A	$\overline{CS1}$	$\overline{BWb}$	NC	$\overline{CS2}$	$\overline{CKE}$	ADV	A	A	A
<b>B</b>	NC	A	CS2	NC	$\overline{BWa}$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
<b>C</b>	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQP <sub>a</sub>
<b>D</b>	NC	DQ <sub>b</sub>	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQ <sub>a</sub>
<b>E</b>	NC	DQ <sub>b</sub>	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQ <sub>a</sub>
<b>F</b>	NC	DQ <sub>b</sub>	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQ <sub>a</sub>
<b>G</b>	NC	DQ <sub>b</sub>	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQ <sub>a</sub>
<b>H</b>	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
<b>J</b>	DQ <sub>b</sub>	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ <sub>a</sub>	NC
<b>K</b>	DQ <sub>b</sub>	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ <sub>a</sub>	NC
<b>L</b>	DQ <sub>b</sub>	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ <sub>a</sub>	NC
<b>M</b>	DQ <sub>b</sub>	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ <sub>a</sub>	NC
<b>N</b>	DQP <sub>b</sub>	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC
<b>P</b>	NC	NC	A	A	TDI	A <sub>1</sub> *	TDO	A	A	A	NC
<b>R</b>	$\overline{LBO}$	NC	A	A	TMS	A <sub>0</sub> *	TCK	A	A	A	A

**Note :** \* A<sub>0</sub> and A<sub>1</sub> are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

**PIN NAME**

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
A <sub>0</sub> ,A <sub>1</sub>	Burst Address Inputs	VSS	Ground
ADV	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock		
$\overline{CKE}$	Clock Enable	DQ <sub>a</sub>	Data Inputs/Outputs
$\overline{CS1}$	Chip Select	DQ <sub>b</sub>	Data Inputs/Outputs
$\overline{CS2}$	Chip Select	DQP <sub>a</sub> , P <sub>b</sub>	Data Inputs/Outputs
$\overline{CS2}$	Chip Select		
$\overline{BWx}$ (x=a,b)	Byte Write Inputs	VDDQ	Output Power Supply
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

**FUNCTION DESCRIPTION**

The K7N163631B and K7N161831B are NtRAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of  $\overline{OE}$ ,  $\overline{LBO}$  and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable( $\overline{CKE}$ ) pin allows the operation of the chip to be suspended as long as necessary. When  $\overline{CKE}$  is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

NtRAM™ latches external address and initiates a cycle, when  $\overline{CKE}$ , ADV are driven to low and all three chip enables( $\overline{CS1}$ , CS2,  $\overline{CS2}$ ) are active .

Output Enable( $\overline{OE}$ ) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register,  $\overline{CKE}$  is driven low, all three chip enables( $\overline{CS1}$ , CS2,  $\overline{CS2}$ ) are active, the write enable input signals  $\overline{WE}$  are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. Also during read operation  $\overline{OE}$  must be driven low for the device to drive out the requested data.

Write operation occurs when  $\overline{WE}$  is driven low at the rising edge of the clock.  $\overline{BW}[d:a]$  can be used for byte write operation. The pipelined NtRAM™ uses a late-late write cycle to utilize 100% of the bandwidth.

At the first rising edge of the clock,  $\overline{WE}$  and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the  $\overline{LBO}$  pin. When this pin is low, linear burst sequence is selected.

And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

**BURST SEQUENCE TABLE**

(Interleaved Burst,  $\overline{LBO}$ =High)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

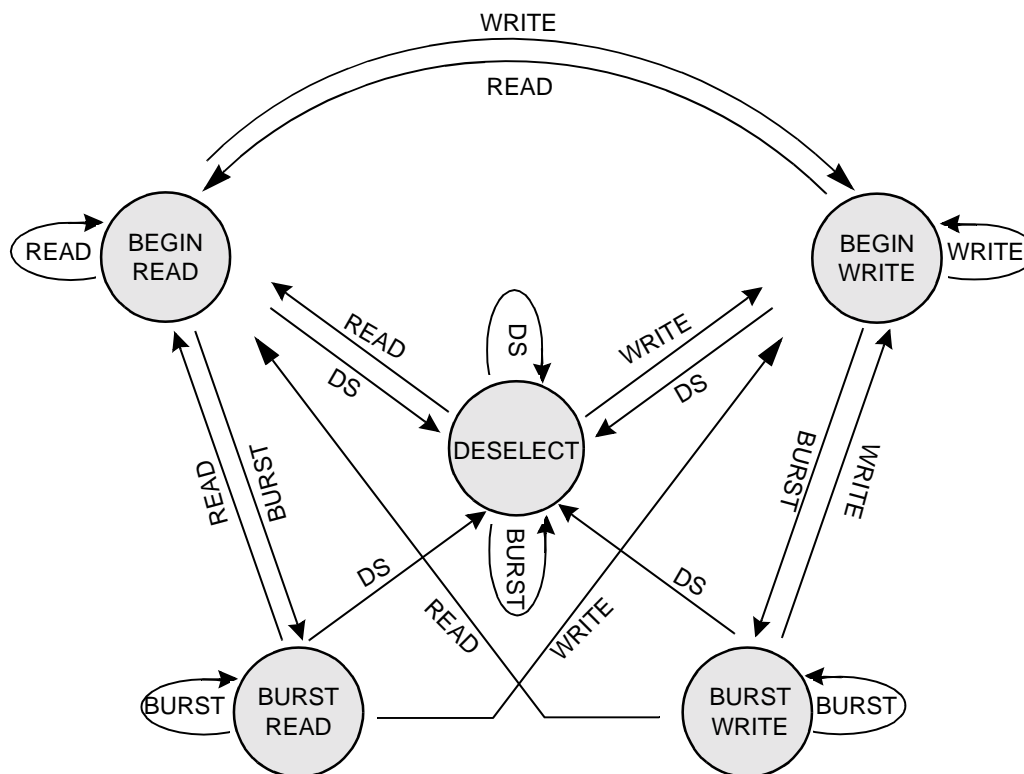
(Linear Burst,  $\overline{LBO}$ =Low)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

**Note** : 1.  $\overline{LBO}$  pin must be tied to High or Low, and Floating State must not be allowed.



STATE DIAGRAM FOR NtRAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.  
2. States change on the rising edge of the clock(CLK)

**TRUTH TABLES**

**SYNCHRONOUS TRUTH TABLE**

$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_2$	ADV	$\overline{WE}$	$\overline{BW}_x$	$\overline{OE}$	$\overline{CKE}$	CLK	ADDRESS ACCESSED	Operation
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by (↑).  
 3. A continue deselect cycle can only be entered if a deselect cycle is executed first.  
 4.  $\overline{WRITE} = L$  means Write operation in WRITE TRUTH TABLE.  
 $\overline{WRITE} = H$  means Read operation in WRITE TRUTH TABLE.  
 5. Operation finally depends on status of asynchronous input pins(ZZ and  $\overline{OE}$ ).

**WRITE TRUTH TABLE(x36)**

$\overline{WE}$	$\overline{BW}_a$	$\overline{BW}_b$	$\overline{BW}_c$	$\overline{BW}_d$	OPERATION
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTES
L	H	H	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".  
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

**WRITE TRUTH TABLE(x18)**

$\overline{WE}$	$\overline{BW}_a$	$\overline{BW}_b$	OPERATION
H	X	X	READ
L	L	H	WRITE BYTE a
L	H	L	WRITE BYTE b
L	L	L	WRITE ALL BYTES
L	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".  
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

**ASYNCHRONOUS TRUTH TABLE**

OPERATION	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

**Notes**

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V <sub>DD</sub> Supply Relative to V <sub>SS</sub>	V <sub>DD</sub>	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to V <sub>SS</sub>	V <sub>IN</sub>	-0.3 to V <sub>DD</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	1.6	W
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	Commercial	T <sub>OPR</sub>	0 to 70
	Industrial	T <sub>OPR</sub>	-40 to 85
Storage Temperature Range Under Bias	T <sub>BIAS</sub>	-10 to 85	°C

\*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING CONDITIONS (0°C ≤ T<sub>A</sub> ≤ 70°C)**

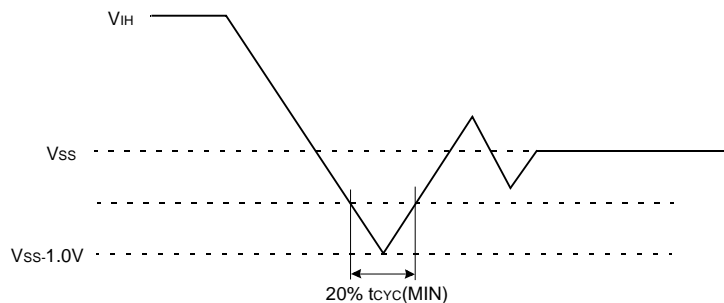
PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V <sub>DD1</sub>	2.375	2.5	2.625	V
	V <sub>DDQ1</sub>	2.375	2.5	2.625	V
	V <sub>DD2</sub>	3.135	3.3	3.465	V
	V <sub>DDQ2</sub>	3.135	3.3	3.465	V
Ground	V <sub>SS</sub>	0	0	0	V

- Notes: 1. The above parameters are also guaranteed at industrial temperature range.  
2. It should be V<sub>DDQ</sub> ≤ V<sub>DD</sub>

**CAPACITANCE\* (T<sub>A</sub>=25°C, f=1MHz)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	TBD	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> =0V	-	TBD	pF

\*Note : Sampled not 100% tested.



**DC ELECTRICAL CHARACTERISTICS**

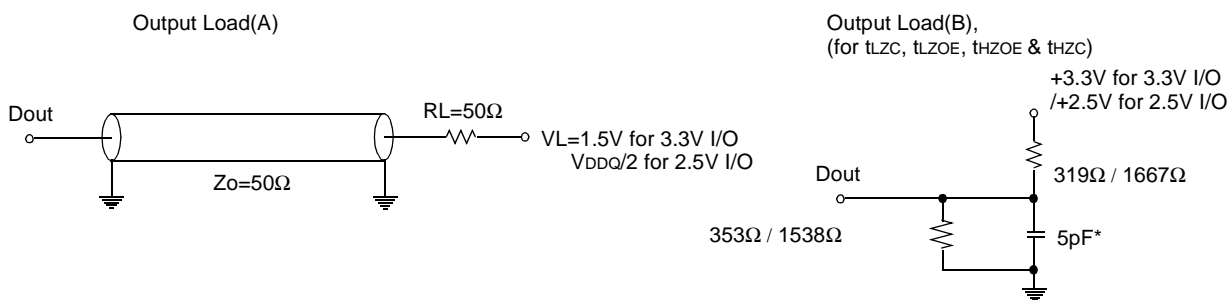
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES	
Input Leakage Current(except ZZ)	IIL	VDD=Max ; VIN=VSS to VDD	-2	+2	μA		
Output Leakage Current	IOL	Output Disabled, Vout=VSS to VDDQ	-2	+2	μA		
Operating Current	ICC	Device Selected, IOUT=0mA, ZZ≤VIL, Cycle Time ≥ tcyc Min	-25	-	360	mA	1,2
			-16	-	300		
Standby Current	ISB	Device deselected, IOUT=0mA, ZZ≤VIL, f=Max, All Inputs≤0.2V or ≥ VDD-0.2V	-	170	mA		
	ISB1	Device deselected, IOUT=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (VDD-0.2V or 0.2V)	-	150	mA		
	ISB2	Device deselected, IOUT=0mA, ZZ≥VDD-0.2V, f=Max, All Inputs≤VIL or ≥VIH	-	130	mA		
Output Low Voltage(3.3V I/O)	VOL	IOL=8.0mA	-	0.4	V		
Output High Voltage(3.3V I/O)	VOH	IOH=-4.0mA	2.4	-	V		
Output Low Voltage(2.5V I/O)	VOL	IOL=1.0mA	-	0.4	V		
Output High Voltage(2.5V I/O)	VOH	IOH=-1.0mA	2.0	-	V		
Input Low Voltage(3.3V I/O)	VIL		-0.3*	0.8	V		
Input High Voltage(3.3V I/O)	VIH		2.0	VDD+0.3**	V	3	
Input Low Voltage(2.5V I/O)	VIL		-0.3*	0.7	V		
Input High Voltage(2.5V I/O)	VIH		1.7	VDD+0.3**	V	3	

- Notes :** 1. The above parameters are also guaranteed at industrial temperature range.  
 2. Reference AC Operating Conditions and Characteristics for input and timing.  
 3. Data states are all zero.  
 4. In Case of I/O Pins, the Max. VIH=VDDQ+0.3V

**TEST CONDITIONS**

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	VDDQ/2
Output Load	See Fig. 1

\* The above parameters are also guaranteed at industrial temperature range.



\* Including Scope and Jig Capacitance

Fig. 1

## AC TIMING CHARACTERISTICS

PARAMETER	SYMBOL	-25		-16		UNIT
		MIN	MAX	MIN	MAX	
Cycle Time	tCYC	4.0	-	6.0	-	ns
Clock Access Time	tCD	-	2.6	-	3.5	ns
Output Enable to Data Valid	tOE	-	2.6	-	3.5	ns
Clock High to Output Low-Z	tLZC	1.5	-	1.5	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	2.6	-	3.0	ns
Clock High to Output High-Z	tHZC	-	2.6	-	3.0	ns
Clock High Pulse Width	tCH	1.7	-	2.2	-	ns
Clock Low Pulse Width	tCL	1.7	-	2.2	-	ns
Address Setup to Clock High	tAS	1.2	-	1.5	-	ns
$\overline{\text{CKE}}$ Setup to Clock High	tCES	1.2	-	1.5	-	ns
Data Setup to Clock High	tDS	1.2	-	1.5	-	ns
Write Setup to Clock High ( $\overline{\text{WE}}$ , $\overline{\text{BWx}}$ )	tWS	1.2	-	1.5	-	ns
Address Advance Setup to Clock High	tADVS	1.2	-	1.5	-	ns
Chip Select Setup to Clock High	tCSS	1.2	-	1.5	-	ns
Address Hold from Clock High	tAH	0.3	-	0.5	-	ns
$\overline{\text{CKE}}$ Hold from Clock High	tCEH	0.3	-	0.5	-	ns
Data Hold from Clock High	tDH	0.3	-	0.5	-	ns
Write Hold from Clock High ( $\overline{\text{WE}}$ , $\overline{\text{BWx}}$ )	tWH	0.3	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.3	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.3	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

Notes : 1. The above parameters are also guaranteed at industrial temperature range.

2. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and  $\overline{\text{CS}}$  is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

3. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.

4. A write cycle is defined by  $\overline{\text{WE}}$  low having been registered into the device at ADV Low, A Read cycle is defined by  $\overline{\text{WE}}$  High with ADV Low, Both cases must meet setup and hold times.

5. To avoid bus contention, At a given voltage and temperature tLZC is more than tHZC.

The specs as shown do not imply bus contention because tLZC is a Min. parameter that is worst case at totally different test conditions (0°C,3.465V) than tHZC, which is a Max. parameter(worst case at 70°C,3.135V)

It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

**SLEEP MODE**

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to  $I_{SB2}$ . The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z

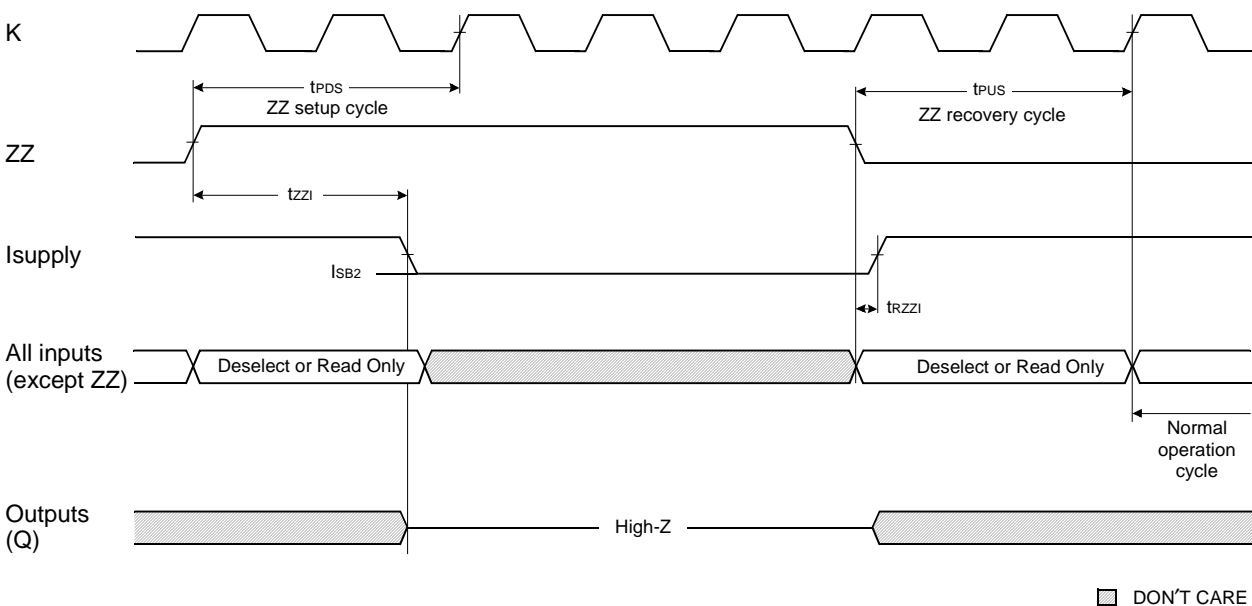
The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

When the ZZ pin becomes a logic High,  $I_{SB2}$  is guaranteed after the time  $t_{ZZ1}$  is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SLEEP MODE during  $t_{PUS}$ , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

**SLEEP MODE ELECTRICAL CHARACTERISTICS**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	$ZZ \geq V_{IH}$	$I_{SB2}$		TBD	mA
ZZ active to input ignored		$t_{PDS}$	2		cycle
ZZ inactive to input sampled		$t_{PUS}$	2		cycle
ZZ active to SLEEP current		$t_{ZZ1}$		2	cycle
ZZ inactive to exit SLEEP current		$t_{RZZ1}$	0		

**SLEEP MODE WAVEFORM**

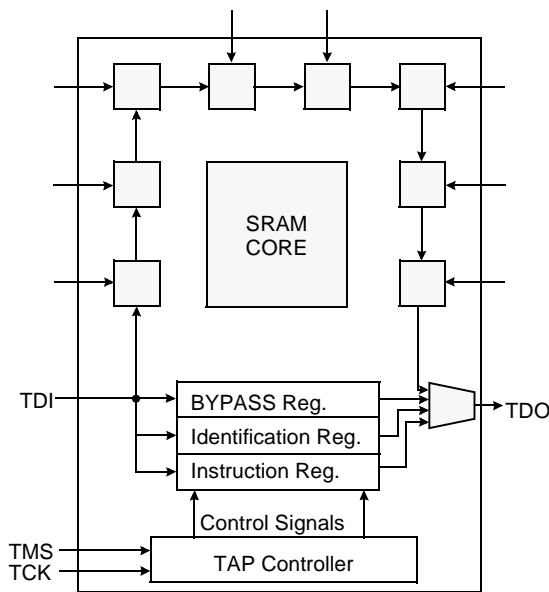


□ DON'T CARE

### IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

### JTAG Block Diagram



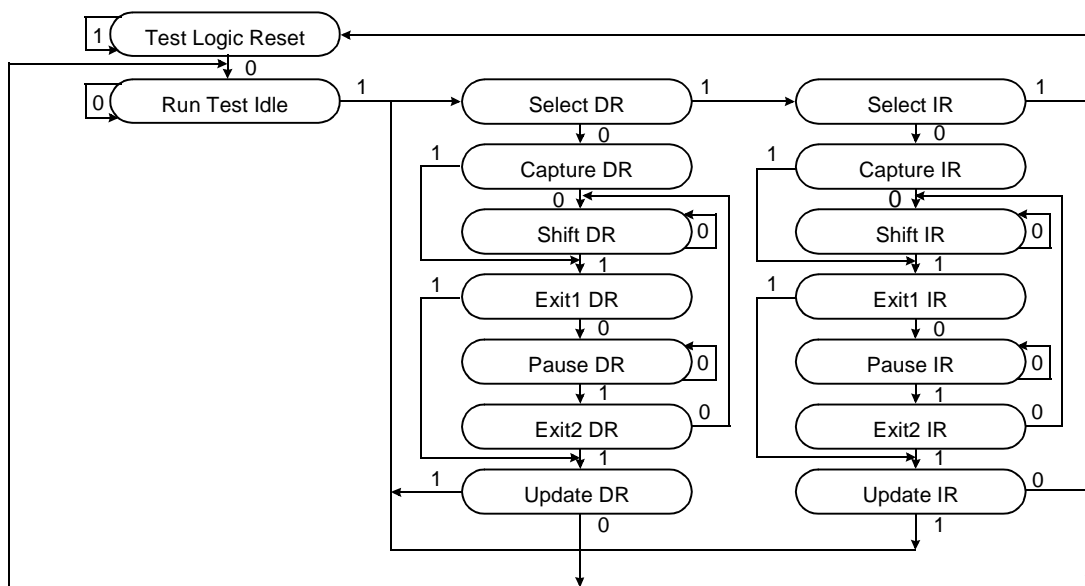
### JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	BYPASS	Bypass Register	4
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	BYPASS	Bypass Register	4
1	1	1	BYPASS	Bypass Register	4

**NOTE :**

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

### TAP Controller State Diagram



**SCAN REGISTER DEFINITION**

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
512Kx36	3 bits	1 bits	32 bits	75 bits
1Mx18	3 bits	1 bits	32 bits	75 bits

**ID REGISTER DEFINITION**

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
512Kx36	0000	00111 00100	XXXXXX	00001001110	1
1Mx18	0000	01000 00011	XXXXXX	00001001110	1

**165FBGA BOUNDARY SCAN EXIT ORDER(x36)**

1	1R	$\overline{\text{LBO}}$		CLK	6B	39
2	6N	NC		NC	11B	40
3	11P	NC		NC	1A	41
4	8P	A		$\overline{\text{CS2}}$	6A	42
5	8R	A		$\overline{\text{BWa}}$	5B	43
6	9R	A		$\overline{\text{BWb}}$	5A	44
7	9P	A		$\overline{\text{BWc}}$	4A	45
8	10P	A		$\overline{\text{BWd}}$	4B	46
9	10R	A		CS2	3B	47
10	11R	A		$\overline{\text{CS1}}$	3A	48
11	11H	ZZ		A	2A	49
12	11N	DQa		A	2B	50
13	11M	DQa		NC	1B	51
14	11L	DQa		DQc	1C	52
15	11K	DQa		DQc	1D	53
16	11J	DQa		DQc	1E	54
17	10M	DQa		DQc	1F	55
18	10L	DQa		DQc	1G	56
19	10K	DQa		DQc	2D	57
20	10J	DQa		DQc	2E	58
21	11G	DQb		DQc	2F	59
22	11F	DQb		DQc	2G	60
23	11E	DQb		DQd	1J	61
24	11D	DQb		DQd	1K	62
25	10G	DQb		DQd	1L	63
26	10F	DQb		DQd	1M	64
27	10E	DQb		DQd	2J	65
28	10D	DQb		DQd	2K	66
29	11C	DQb		DQd	2L	67
30	11A	NC		DQd	2M	68
31	10A	A		DQd	1N	69
32	10B	A		A	3P	70
33	9A	A		A	3R	71
34	9B	A		A	4R	72
35	8A	ADV		A	4P	73
36	8B	$\overline{\text{OE}}$		A1	6P	74
37	7A	$\overline{\text{CKE}}$		A0	6R	75
38	7B	$\overline{\text{WE}}$				

**165FBGA BOUNDARY SCAN EXIT ORDER(x18)**

1	1R	$\overline{\text{LBO}}$		CLK	6B	39
2	6N	NC		NC	11B	40
3	11P	NC		NC	1A	41
4	8P	A		$\overline{\text{CS2}}$	6A	42
5	8R	A		$\overline{\text{BWa}}$	5B	43
6	9R	A		$\overline{\text{NC}}$	5A	44
7	9P	A		$\overline{\text{BWb}}$	4A	45
8	10P	A		$\overline{\text{NC}}$	4B	46
9	10R	A		CS2	3B	47
10	11R	A		$\overline{\text{CS1}}$	3A	48
11	11H	ZZ		A	2A	49
12	11N	NC		A	2B	50
13	11M	NC		NC	1B	51
14	11L	NC		NC	1C	52
15	11K	NC		NC	1D	53
16	11J	NC		NC	1E	54
17	10M	DQa		NC	1F	55
18	10L	DQa		NC	1G	56
19	10K	DQa		DQb	2D	57
20	10J	DQa		DQb	2E	58
21	11G	DQa		DQb	2F	59
22	11F	DQa		DQb	2G	60
23	11E	DQa		DQb	1J	61
24	11D	DQa		DQb	1K	62
25	11C	DQa		DQb	1L	63
26	10F	NC		DQb	1M	64
27	10E	NC		DQb	1N	65
28	10D	NC		NC	2K	66
29	10G	NC		NC	2L	67
30	11A	A		NC	2M	68
31	10A	A		NC	2J	69
32	10B	A		A	3P	70
33	9A	A		A	3R	71
34	9B	A		A	4R	72
35	8A	ADV		A	4P	73
36	8B	$\overline{\text{OE}}$		A1	6P	74
37	7A	$\overline{\text{CKE}}$		A0	6R	75
38	7B	$\overline{\text{WE}}$				

NOTE, NC ; Don't Care



**JTAG DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	3.135/2.375	3.3/2.5	3.465/2.625	V	
Input High Level	V <sub>IH</sub>	2.0/1.7	-	V <sub>DD</sub> +0.3	V	
Input Low Level	V <sub>IL</sub>	-0.3	-	0.8/0.7	V	
Output High Voltage	V <sub>OH</sub>	2.4/2.0	-	-	V	
Output Low Voltage	V <sub>OL</sub>	-	-	0.4/0.4	V	

**NOTE :** The input level of SRAM pin is to follow the SRAM DC specification.

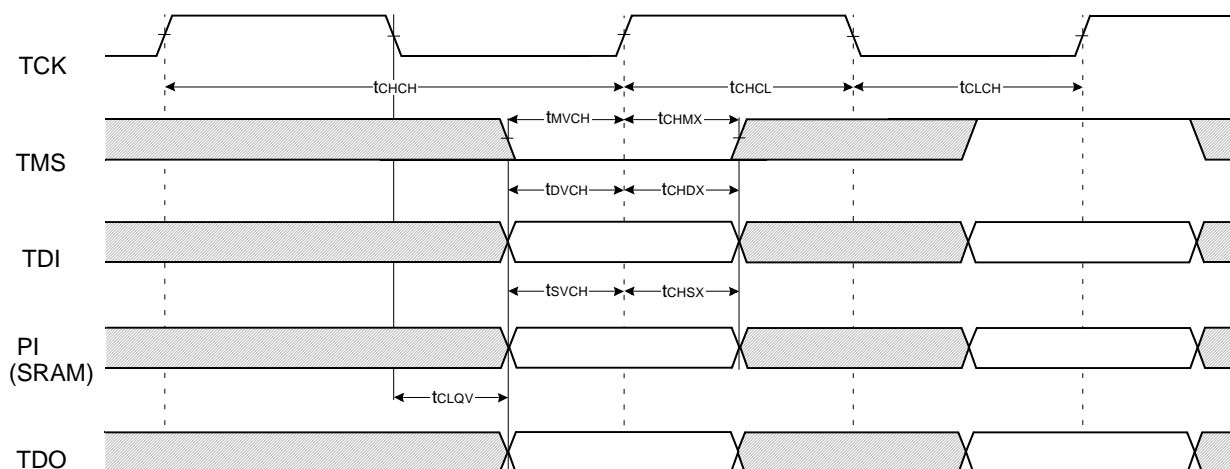
**JTAG AC TEST CONDITIONS**

Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V <sub>IH</sub> /V <sub>IL</sub>	3.0/0 , 2.5/0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0 , 1.0/1.0	ns	
Input and Output Timing Reference Level		V <sub>DDQ</sub> /2	V	

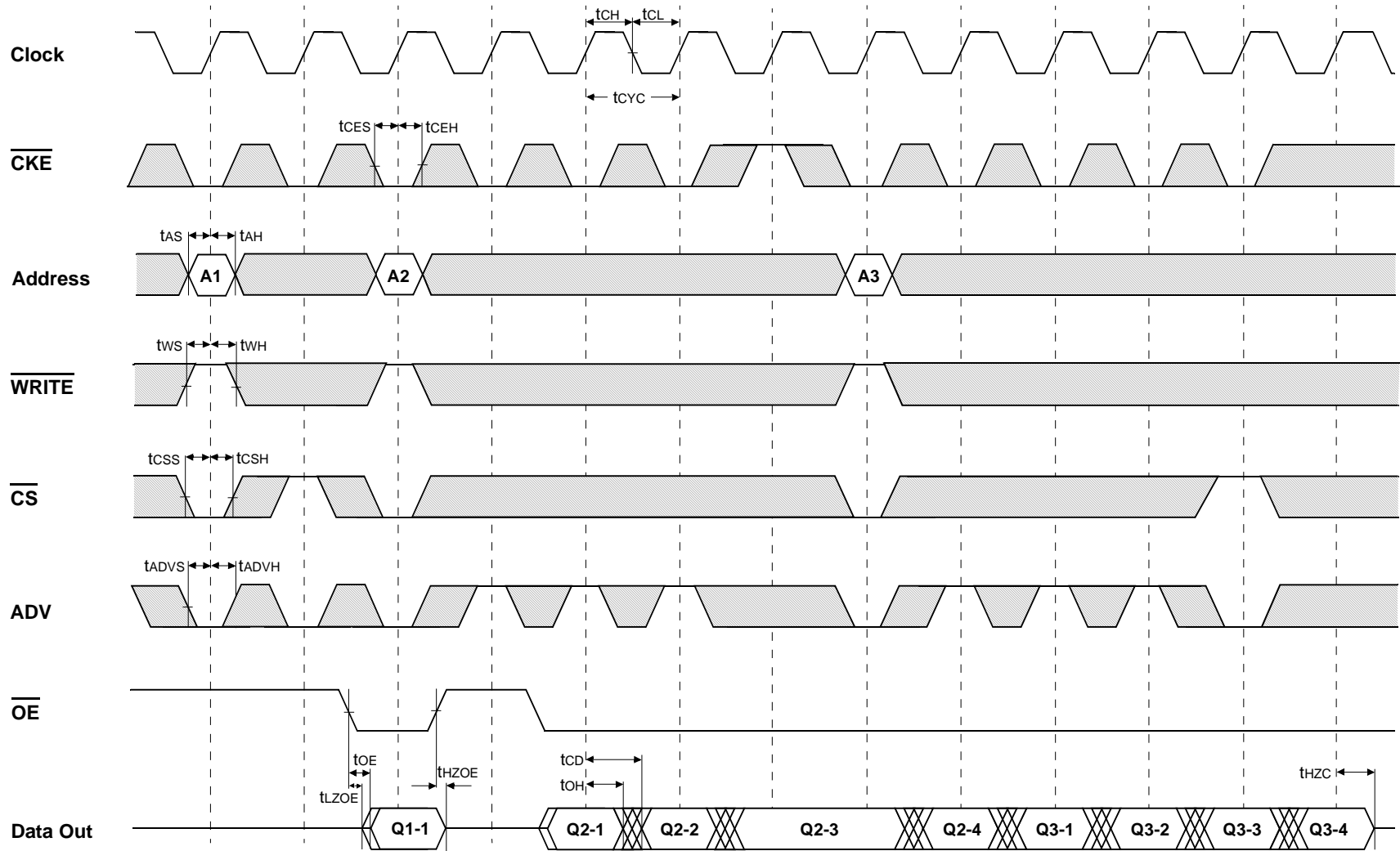
**JTAG AC Characteristics**

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t <sub>CHCH</sub>	50	-	ns	
TCK High Pulse Width	t <sub>CHCL</sub>	20	-	ns	
TCK Low Pulse Width	t <sub>CLCH</sub>	20	-	ns	
TMS Input Setup Time	t <sub>MVCH</sub>	5	-	ns	
TMS Input Hold Time	t <sub>CHMX</sub>	5	-	ns	
TDI Input Setup Time	t <sub>dvCH</sub>	5	-	ns	
TDI Input Hold Time	t <sub>CHDX</sub>	5	-	ns	
SRAM Input Setup Time	t <sub>svCH</sub>	5	-	ns	
SRAM Input Hold Time	t <sub>chsX</sub>	5	-	ns	
Clock Low to Output Valid	t <sub>CLQV</sub>	0	10	ns	

**JTAG TIMING DIAGRAM**



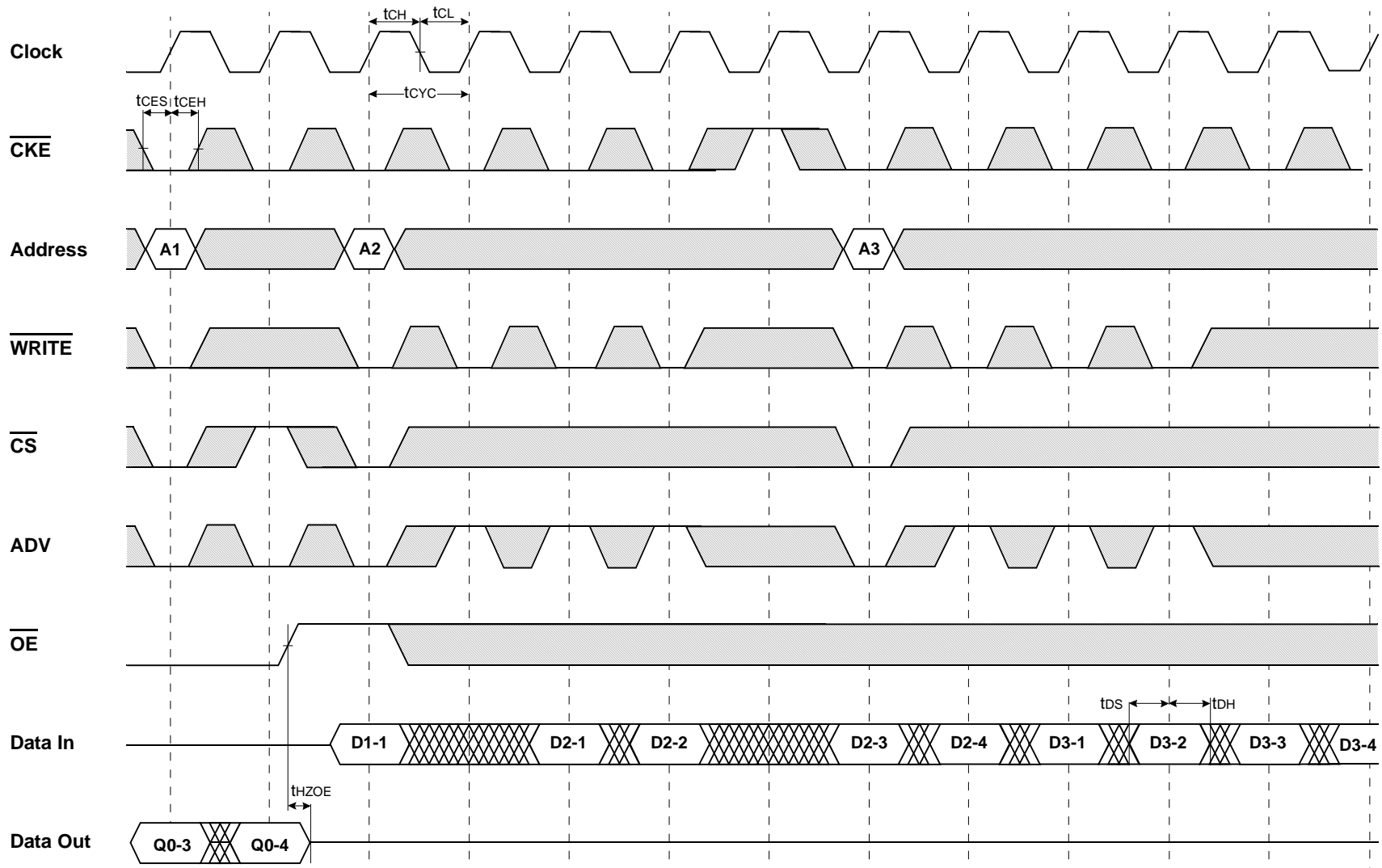
### TIMING WAVEFORM OF READ CYCLE



NOTES:  $\overline{\text{WRITE}} = \text{L}$  means  $\overline{\text{WE}} = \text{L}$ , and  $\overline{\text{BW}}x = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\text{CS}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\text{CS}_2 = \text{L}$

□ Don't Care  
 ⊗ Undefined

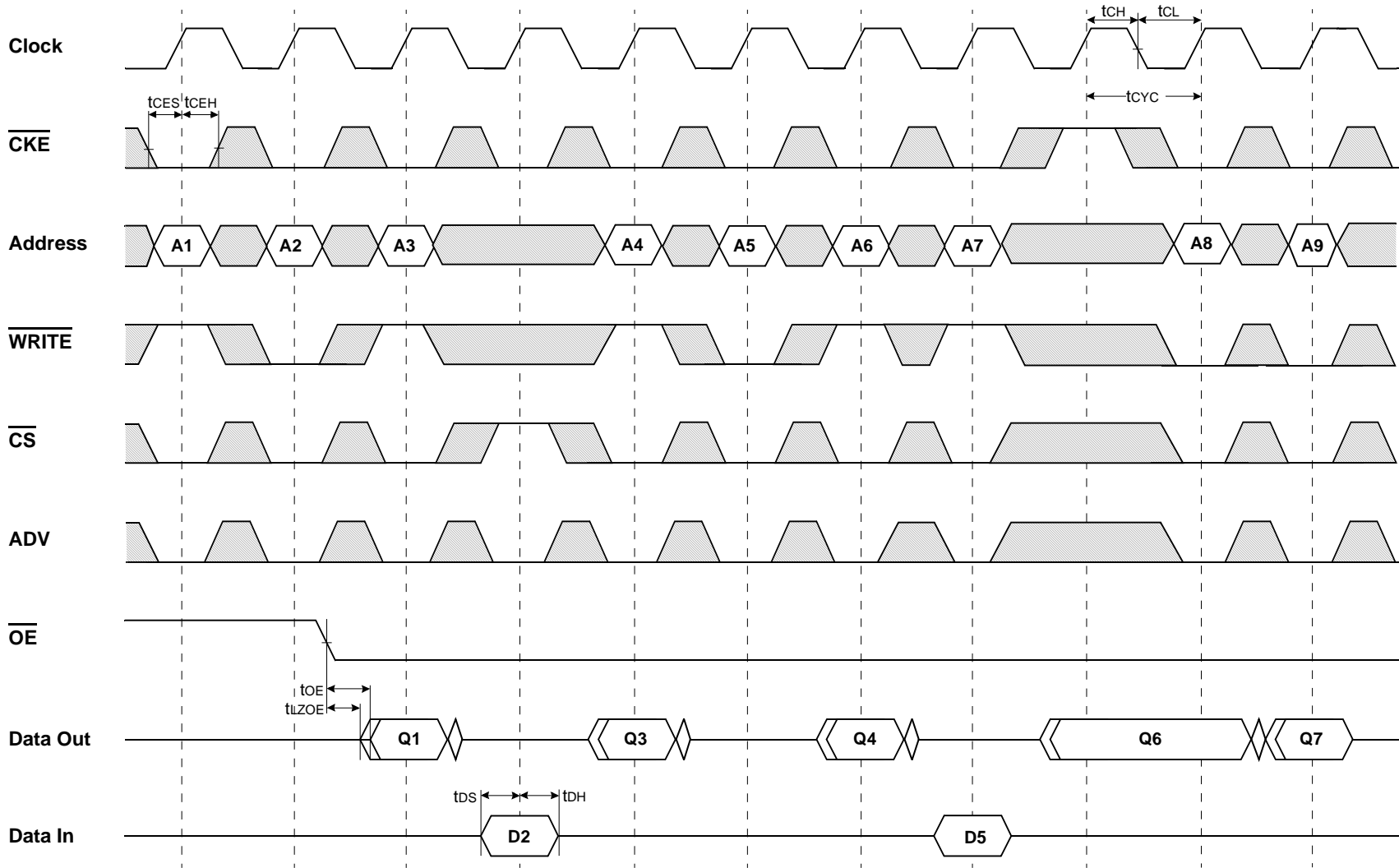
### TIMING WAVEFORM OF WRTE CYCLE



NOTES:  $\overline{WRITE} = L$  means  $\overline{WE} = L$ , and  $\overline{BWx} = L$   
 $\overline{CS} = L$  means  $\overline{CS}_1 = L$ ,  $CS_2 = H$  and  $\overline{CS}_2 = L$   
 $\overline{CS} = H$  means  $\overline{CS}_1 = H$ , or  $\overline{CS}_1 = L$  and  $\overline{CS}_2 = H$ , or  $\overline{CS}_1 = L$ , and  $CS_2 = L$

□ Don't Care  
 ⊠ Undefined

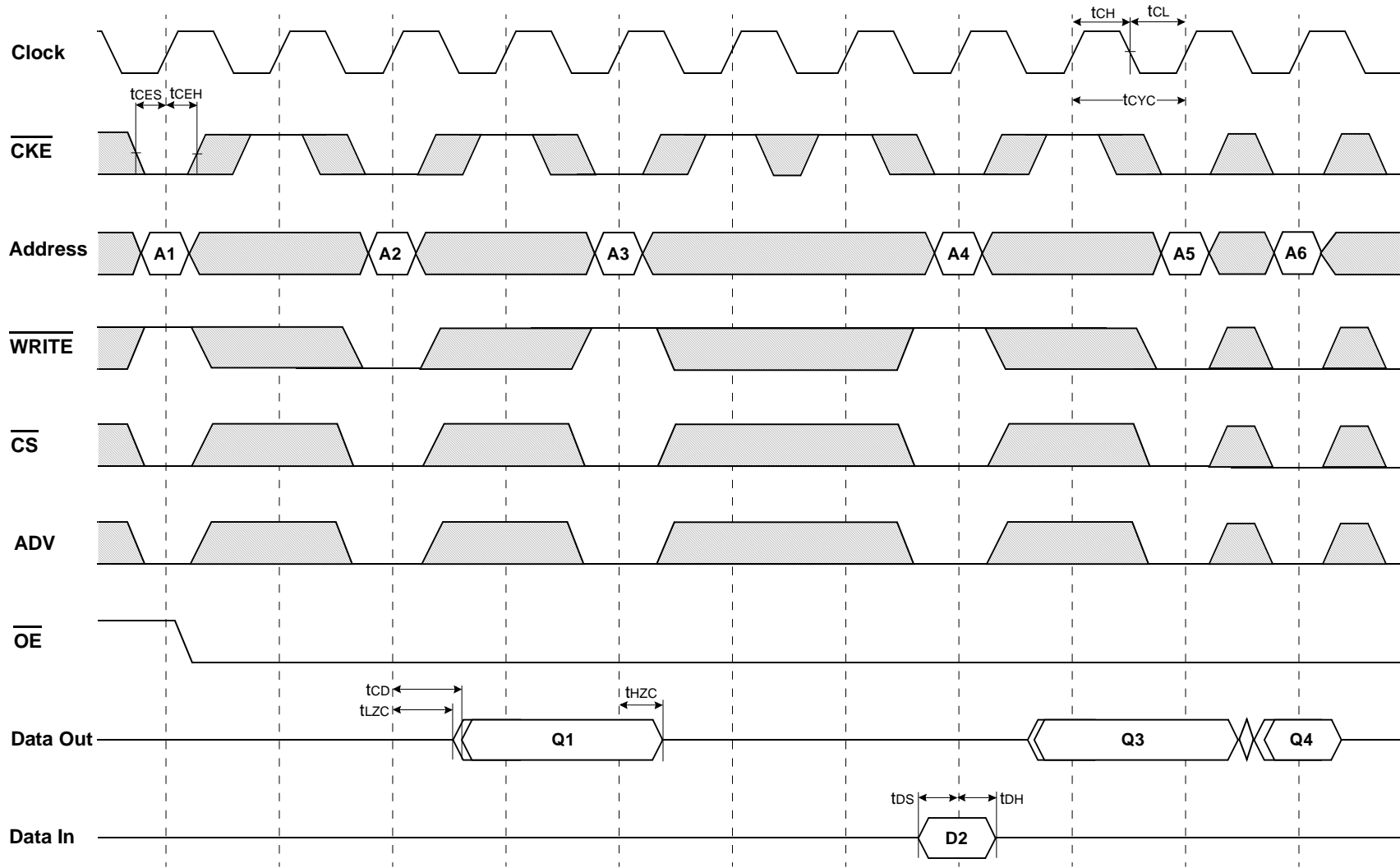
### TIMING WAVEFORM OF SINGLE READ/WRITE



NOTES :  $\overline{\text{WRITE}} = \text{L}$  means  $\overline{\text{WE}} = \text{L}$ , and  $\overline{\text{BWx}} = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\text{CS}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\text{CS}_2 = \text{L}$

□ Don't Care  
 ⊗ Undefined

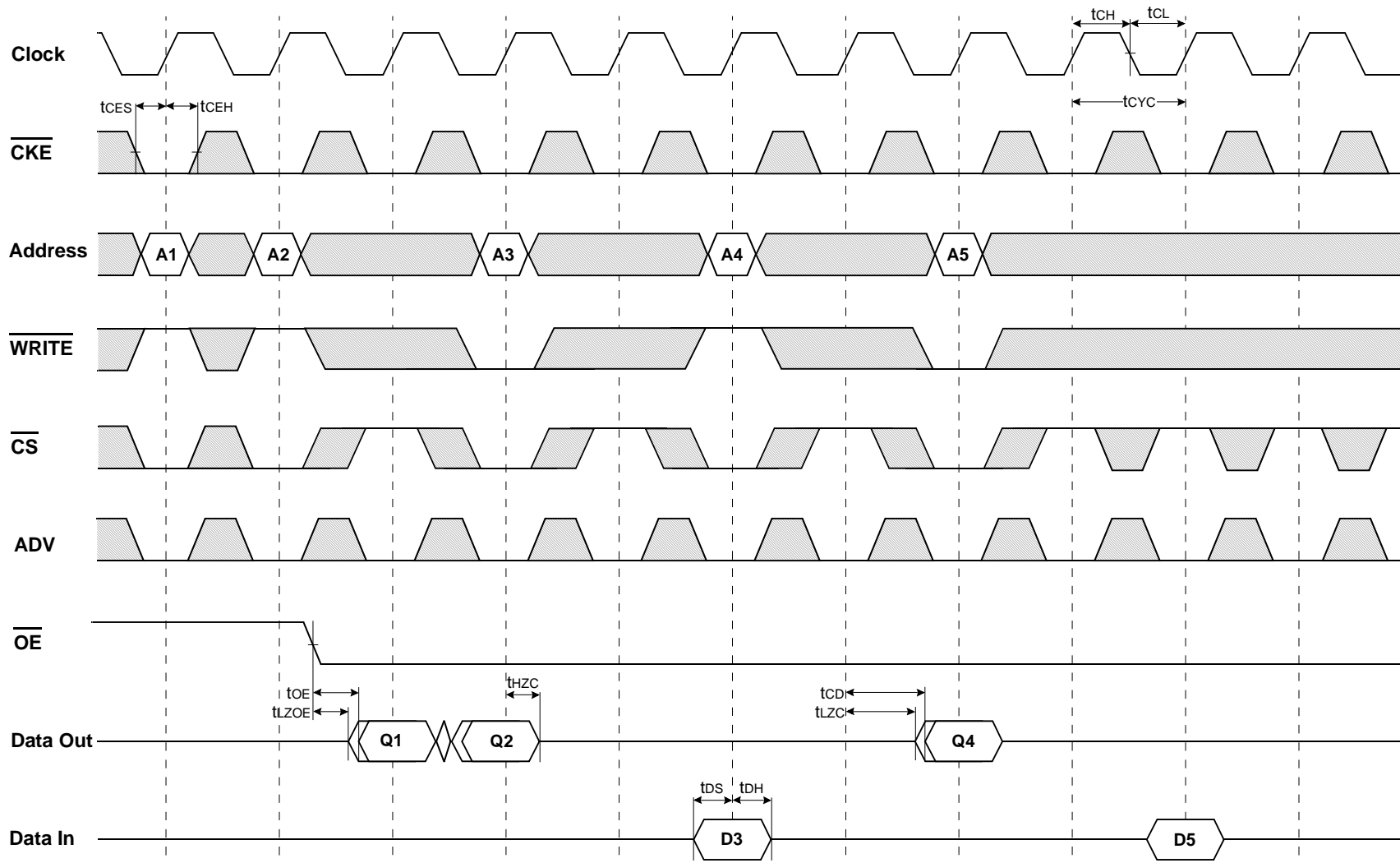
### TIMING WAVEFORM OF $\overline{\text{CKE}}$ OPERATION



NOTES :  $\overline{\text{WRITE}} = \text{L}$  means  $\overline{\text{WE}} = \text{L}$ , and  $\overline{\text{BW}}_x = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\text{CS}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\text{CS}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\text{CS}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\text{CS}_2 = \text{L}$

□ Don't Care  
 ⊠ Undefined

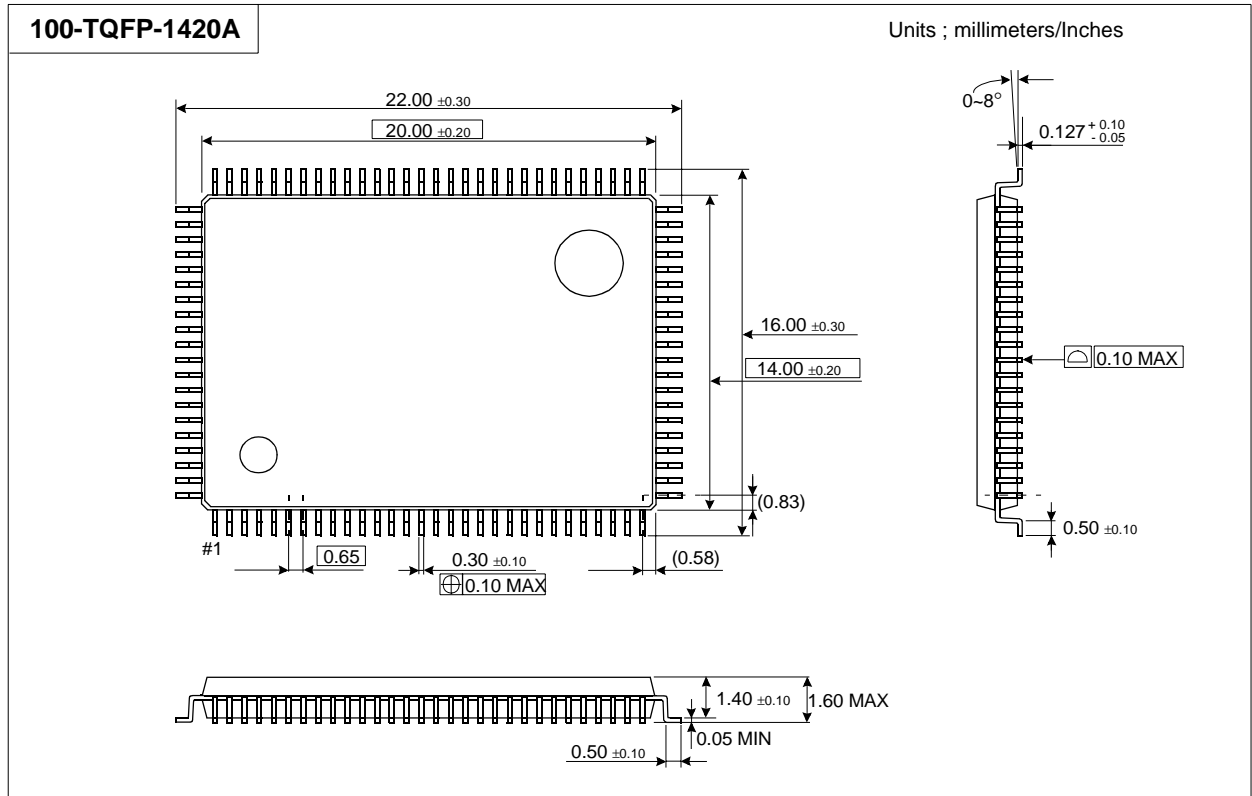
### TIMING WAVEFORM OF $\overline{CS}$ OPERATION



NOTES :  $\overline{WRITE} = L$  means  $\overline{WE} = L$ , and  $\overline{BWx} = L$   
 $\overline{CS} = L$  means  $\overline{CS}_1 = L$ ,  $CS_2 = H$  and  $\overline{CS}_2 = L$   
 $CS = H$  means  $CS_1 = H$ , or  $\overline{CS}_1 = L$  and  $CS_2 = H$ , or  $\overline{CS}_1 = L$ , and  $CS_2 = L$

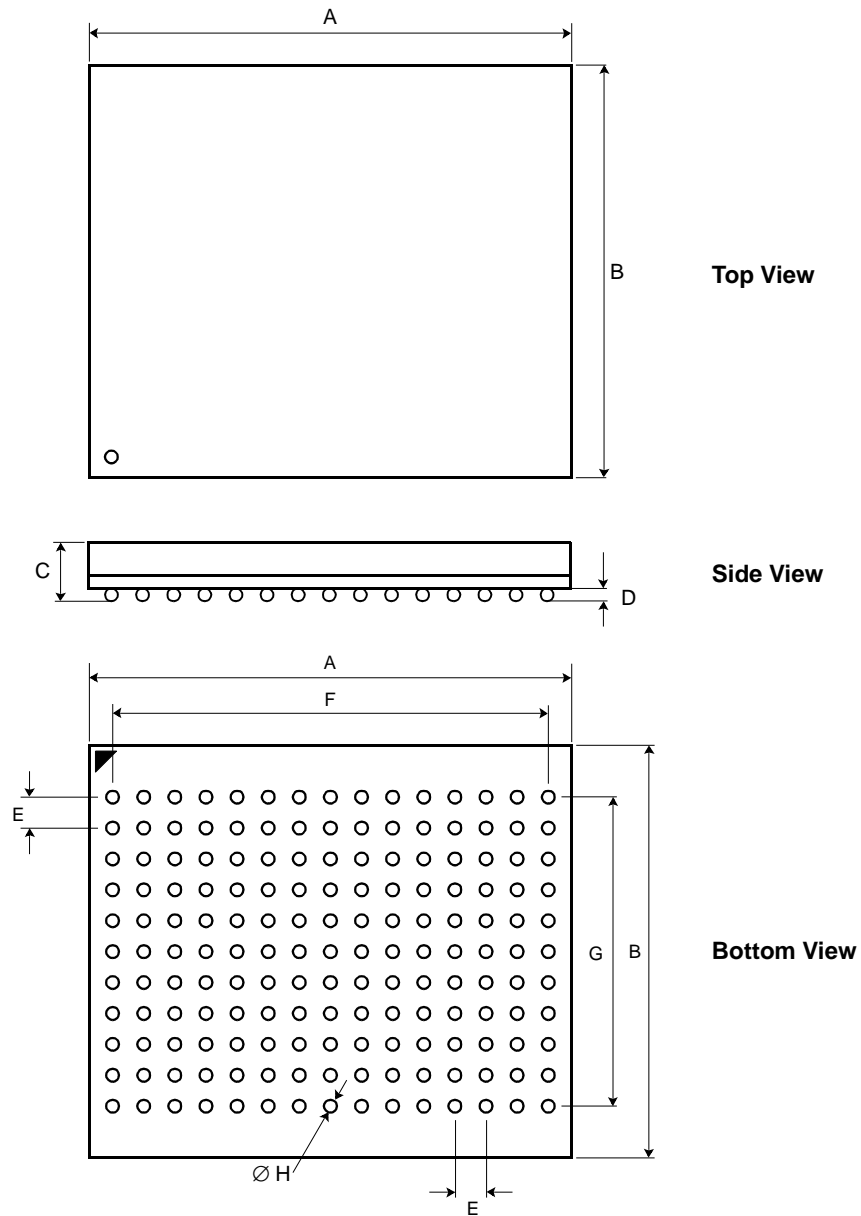
□ Don't Care  
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**PACKAGE DIMENSIONS**



165 FBGA PACKAGE DIMENSIONS

13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Array



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	15 ± 0.1	mm		E	1.0	mm	
B	13 ± 0.1	mm		F	14.0	mm	
C	1.3 ± 0.1	mm		G	10.0	mm	
D	0.35 ± 0.05	mm		H	0.5 ± 0.05	mm	