128K XM20C128S 16K x 8

High Speed AUTOSTORE™ NOVRAM

FEATURES

- High Speed: T_{AA} = 55ns
- NO! Batteries!!
- Low Power CMOS
- AUTOSTORE™ NOVRAM
  - —Automatically Stores RAM Data to E^2PROM upon Power-fail Detection
- Open Drain AUTOSTORE Output Pin
  - —Interrupt or Status Information
  - —Linkable to System Reset Circuitry
- Auto Recall
  - —Automatically Recalls E^2PROM Data During Power-on
- Fully Decoded Module
- Three Temperature Ranges
  - —Commercial
  - —Industrial
- High Reliability
  - —Endurance: 1,000,000 Store Cycles
  - —Data Retention: 100 Years
- ESD Protection
  - —≥2KV All Pins

DESCRIPTION

The XM20C128S is a high speed nonvolatile RAM Module. It is comprised of eight Xicor X20C16 high speed NOVRAMs, a high speed "ACT" decoder and decoupling capacitors mounted on a FR-4 substrate. The XM20C128S is configured 16K x 8 and is fully decoded. The module is a 36-pin SIP conforming to the industry standard pinout for SRAMS.

The XM20C128S fully supports the AUTOSTORE feature, providing hands-off automatic storing of RAM data into E^2PROM when VCC falls below the AUTOSTORE threshold.

The XM20C128S is a highly reliable memory component, supporting unlimited writes to RAM, a minimum 1,000,000 store cycles and a minimum 100 year data retention.

6

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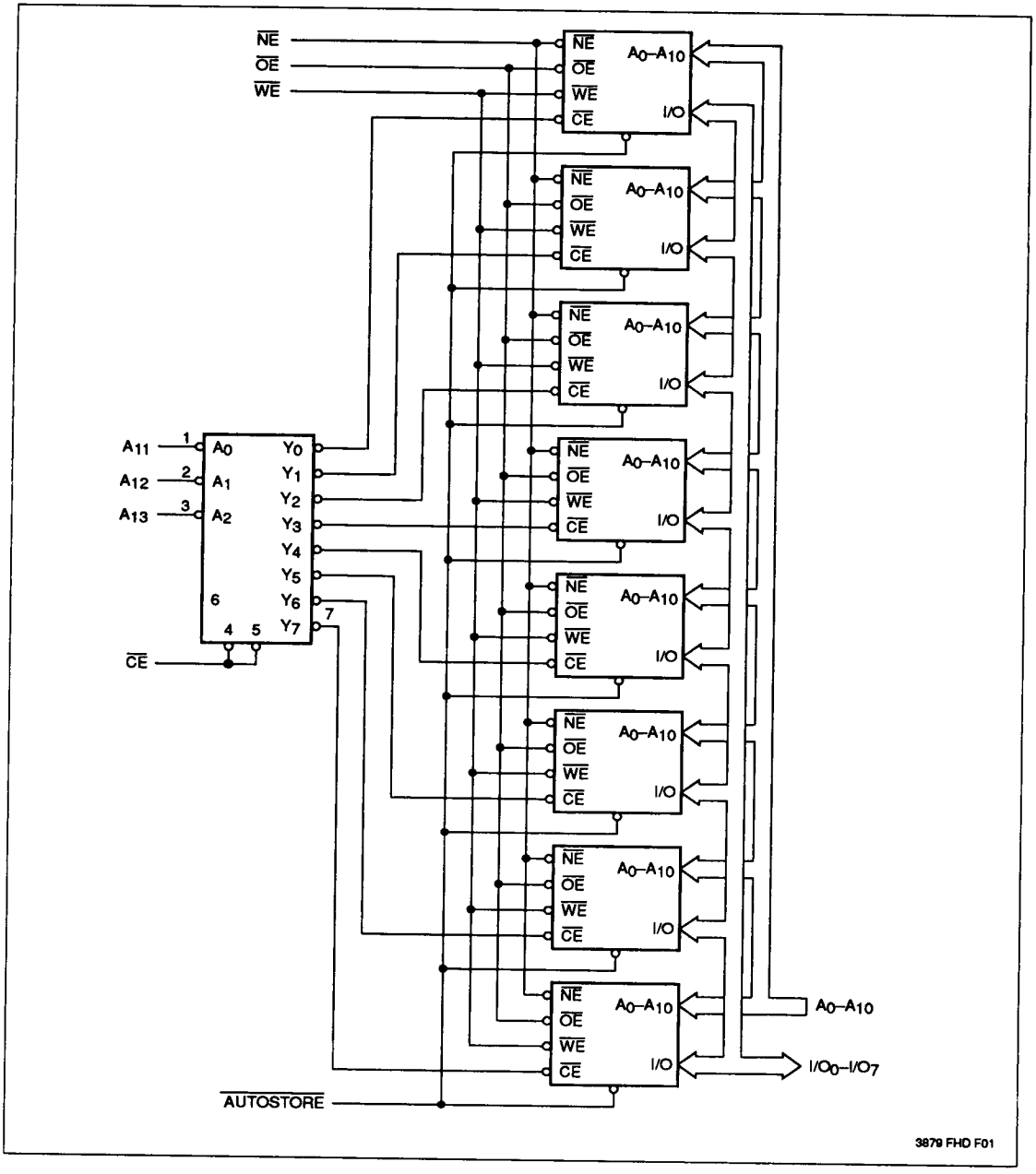
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Addresses (A_0–A_{13})

The address inputs select an 8-bit memory location during read and write operations.

Chip Enable ($\overline{CE}$)

The chip enable input must be LOW to enable all read, write and user requested nonvolatile operations.

Output Enable ($\overline{OE}$)

During normal RAM operations $\overline{OE}$ controls the data output buffers. If a hardware nonvolatile operation is selected ($\overline{NE} = \overline{CE} =$ LOW) and $\overline{WE}$ strobes LOW a recall operation will be initiated.

$\overline{OE}$ LOW will always disable a STORE operation regardless of the state of $\overline{NE}$, $\overline{WE}$, and $\overline{CE}$ so long as the internal transfer has not commenced.

Write Enable ($\overline{WE}$)

During normal RAM operations $\overline{WE} = \overline{CE}$ = LOW will cause data to be written to the RAM address pointed to by the A_0–A_{12} inputs.

Nonvolatile Enable ($\overline{NE}$)

The nonvolatile input controls the transfer of data from the E²PROM array to the RAM array, when strobed LOW in conjunction with $\overline{CE} = \overline{OE}$ = LOW.

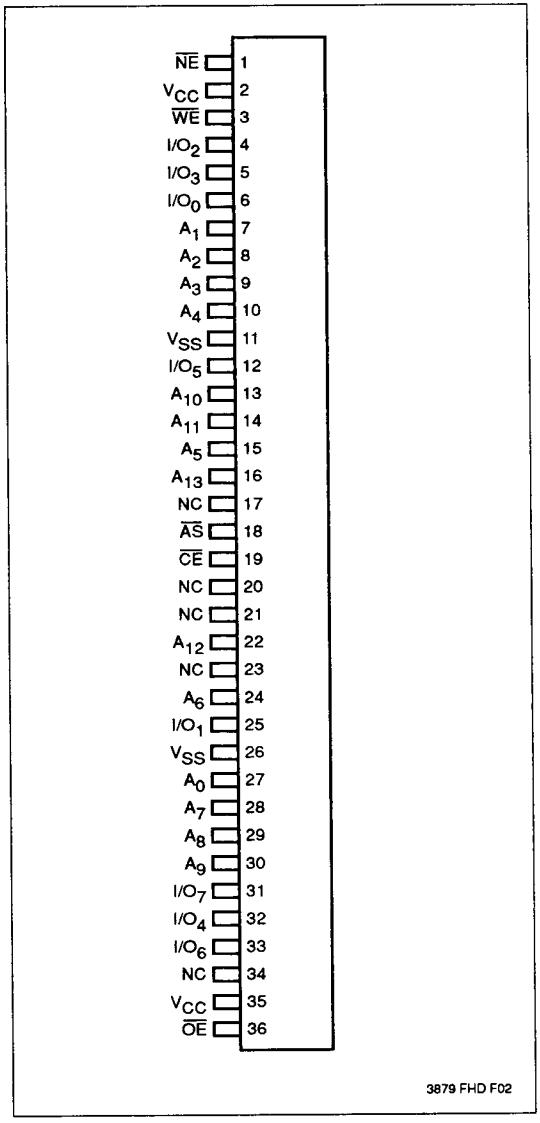
Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20C128S through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

AUTOSTORE Output ($\overline{AS}$)

$\overline{AS}$ is an open drain output. When it is asserted (driving LOW) it indicates V_{CC} has fallen below the AUTOSTORE threshold and an internal store operation has been initiated. Because $\overline{AS}$ is an open drain output it may be wire-ORed with multiple open drain outputs and used as an interrupt input or as an input to a power on reset circuit.

PIN CONFIGURATION



DEVICE OPERATION

RAM operations are identical to those of a standard SRAM. When $\overline{OE}$ and $\overline{CE}$ are asserted data is presented at the I/Os from the address location pointed to by the A_0–A_{13} inputs.

RAM write operations are initiated and the address input is latched by the HIGH to LOW transition of $\overline{CE}$ or $\overline{WE}$, Whichever occurs last. Data are latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

An array recall, E²PROM data transferred to RAM, is initiated whenever $\overline{OE} = \overline{NE} = \overline{CE}$ = LOW. A recall is also performed automatically upon power up.

Command Sequence Operations

The X20C128S employs a version of the industry standard Software Data Protection (SDP). The end user can select various options for transferring data from RAM into the E²PROM array.

All command sequences are comprised of three specific data/address write operations performed with $\overline{NE}$ LOW. A Store operation can be directly selected by issuing an Immediate Store command. The user may also enable and disable the AUTOSTORE function through the software data protection sequence.

Operational Notes

The X20C128S should be viewed as a subsystem when writing software for the various store operations. The module contains eight discrete components each needing to be set to the required state individually. The three high order address bits (A_{11}, A_{12} and A_{13}) select only one of the eight components.

TABLE 1. COMMAND SEQUENCE

Step	Operation	A_0–A_{10}*	Data Pattern	Command [Hex]	Function
1	Write	555	AA	CC	Enable AUTOSTORE
2	Write	2AA	55	CD	Disable AUTOSTORE
3	Write	555	Command	33	Perform Immediate Store

**It should be noted, the high order addresses should remain stable during the operations. It should also be noted that these commands are not global, that is only one device on the module will be affected by each command operation.*

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O State	Power
H	X	X	X	Module Not Selected	High Z	Standby
L	H	H	L	Read RAM	Data Output	Active
L	L	H	X	Write RAM	Data Input	Active
L	L	L	H	Issue Software Command	Data Input	Active
L	H	H	H	Output Disabled	High Z	Active
L	H	L	L	Hardware Array Recall	High Z	Active
L	H	L	H	No Op	High Z	Active
L	L	L	L	Not Allowed	High Z	Active

3879 PGM T04

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–65°C to +125°C
Storage Temperature .....–65°C to +125°C
Voltage on any Pin with
Respect to Ground .....–1.0V to +7V

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

3879 PGM T06

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the module. This is a stress rating only and the functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect module reliability.

Supply Voltage	Limits
XM20C128S	5V ±10%

3879 PGM T07

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC1}	V_{CC} Active Current		200	mA	$\overline{NE} = \overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = TTL Inputs @ f = 20MHz All I/Os = Open
I_{CC2}	V_{CC} Active Current (AUTOSTORE)		20	mA	All Inputs = V_{IH}, All I/Os - Open
I_{SB}	V_{CC} Standby Current		3.0	mA	All Inputs = V_{CC}–0.3V All I/Os = Open
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{IN} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input Low Voltage	–0.5	0.8	V	
V_{IH}(1)	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 5mA
V_{OLAS}	AUTOSTORE Output Voltage		0.4	V	I_{OLAS} = 1mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –4mA

3879 PGM T08

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up (V_{CC} Min.) to RAM Operation	500	µs
t_{PUST}	Power-Up (V_{CC} Min.) to Store Operation	5	ms

3879 PGM T09

CAPACITANCE T_A = 25°C, F = 1.0MHZ, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	80	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	48	pF	V_{IN} = 0V

3879 PGM T10

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

6

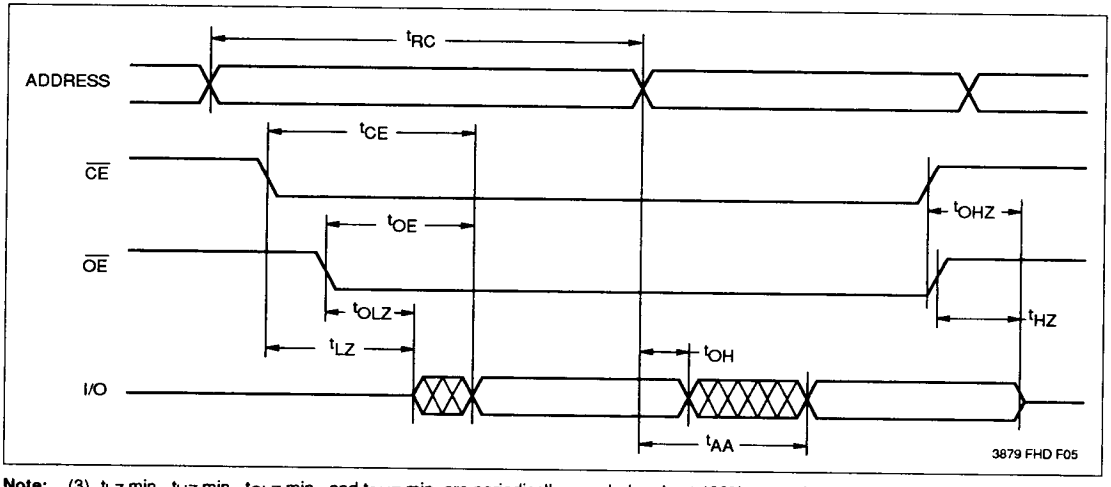
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{RC}	Read Cycle Time	55		ns
t_{CE}	Chip Enable Access Time		55	ns
t_{AA}	Address Access Time		55	ns
t_{OE}	Output Enable Access Time		30	ns
t_{LZ}(3)	$\overline{CE}$ Low to Output in Low Z	0		ns
t_{OLZ}(3)	$\overline{OE}$ Low to Output in Low Z	0		ns
t_{HZ}(3)	$\overline{CE}$ High to Output in Low Z	0	25	ns
t_{OHZ}(3)	$\overline{OE}$ High to Output in Low Z	0	25	ns
t_{OH}	Output Hold	0		ns

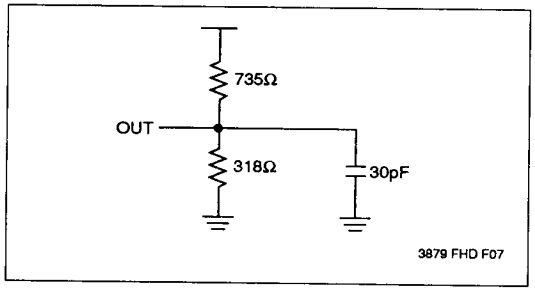
3879 PGM T03

Read Cycle Timing Diagram



Note: (3) t_{LZ} min., t_{HZ} min., t_{OLZ} min., and t_{OHZ} min. are periodically sampled and not 100% teseted. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outptus are no longer driven.

EQUIVALENT TEST LOAD CIRCUIT

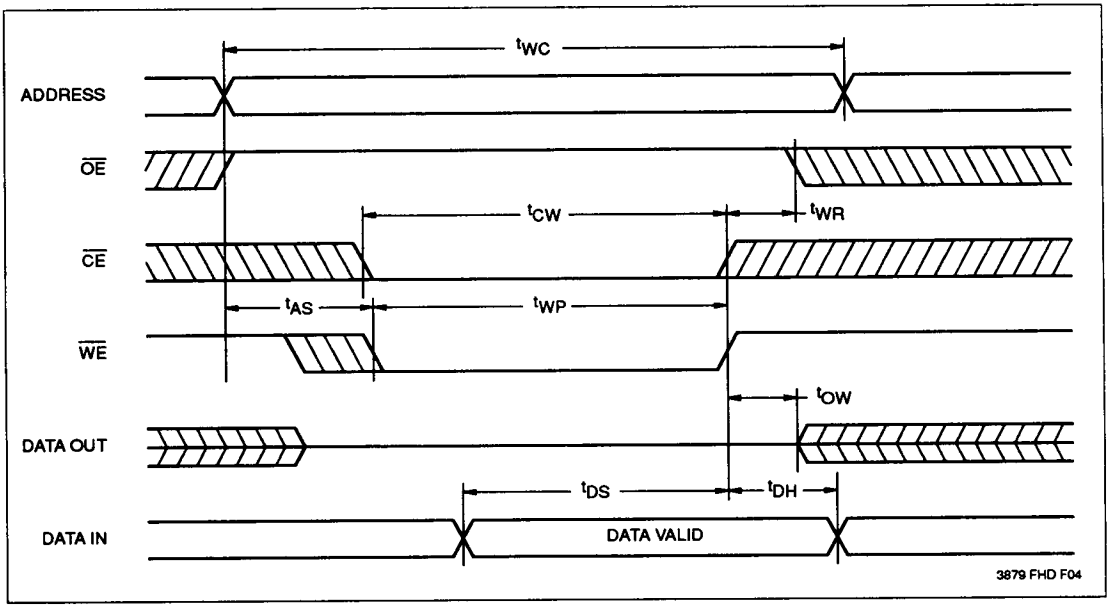


Write Cycle Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{WC}	Write Cycle Time	55		ns
t_{WP}	$\overline{WE}$ Pulse Width	40		ns
t_{CW}	$\overline{CE}$ Pulse Width	40		ns
t_{AS}	Address Setup	0		ns
t_{DS}	Data Setup	25		ns
t_{DH}	Data Hold	0		ns
t_{OW}	Output Active from End of Write		5	ns
t_{WR}	End of Write to Read	0		ns

3879 PGM T02

Write Cycle Timing Diagram



3879 FHD F04

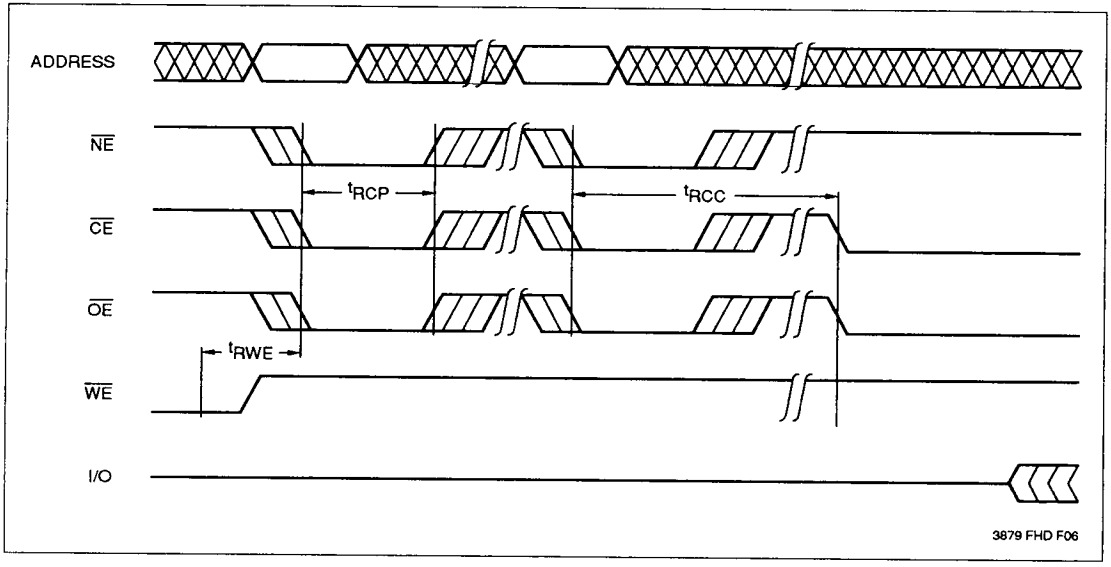
Array Recall Timing

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{RCC}	Array Recall Time		10	
t_{RCP}	Recall Strobe Pulse Width	50		
t_{RWE}	Delay From $\overline{WE}$ HIGH to Recall	0		

3879 PGM T05

Note: The recall sequence must be repeated for each memory component individually. This is accolmplished by sequencing through the Array Recall Cycle with all eight combinations of A_{11}, A_{12} and A_{13}.

Array Recall Cycle



Command Sequence Timing Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{STO}	Store Time		5	ns
t_{SP}	Command Write Pulse Width	50		ns
t_{SPH}	Inter Command Delay	55		ns

Note: All write command sequence timings must confrom to the standard write timing requirements.

3879 PGM T01

Command Write Sequence