



# CMOS, 12-Bit, Single-Supply Complete Voltage-Output DACs

MX7245/MX7248/883B

## 1.0 SCOPE

**1.1** This specification covers the detail requirements for two 12-bit digital-to-analog converters (DACs). The MX7245 has a parallel-loading structure while the MX7248 has an (8 + 4) loading structure. These circuits are processed in accordance with MIL-STD-883 and are fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

## 1.2 Part Numbers

Device	Part Number
-1	MX7245S(X)/883B
-2	MX7248S(Y)/883B

## 1.3 Package

(X)	Package	Description
Q	Q-24	24-Pin Ceramic Dual-In-Line Package (CERDIP)
E	E-28	28-Pin Ceramic Leadless Chip Carrier (LCC)
(Y)	Package	Description
Q	Q-20	20-Pin Ceramic Dual-In-Line Package (CERDIP)
E	E-20	20-Pin Ceramic Leadless Chip Carrier (LCC)

**Note:** See *Package Information* section for package drawings and dimensions.

## 1.4 Absolute Maximum Ratings

(T<sub>A</sub> = +25°C, unless otherwise noted.)

V <sub>DD</sub> to AGND	-0.3V, +17V
V <sub>DD</sub> to DGND	-0.3V, +17V
V <sub>DD</sub> to V <sub>SS</sub>	-0.3V, +34V
REFOUT to AGND (Note 1)	0V, V <sub>DD</sub>
V <sub>OUT</sub> to AGND (Note 1)	V <sub>SS</sub> , V <sub>DD</sub>
V <sub>OUT</sub> to V <sub>SS</sub> (Note 1)	0V, +24V
V <sub>OUT</sub> to V <sub>DD</sub> (Note 1)	-32V, 0V
Digital Input Voltage to DGND	-0.3V, (V <sub>DD</sub> + 0.3V)
AGND to DGND	-0.3V, V <sub>DD</sub>

**Note 1:** The outputs may be shorted to voltages in this range, provided the power dissipation of the package is not exceeded.

8



# CMOS, 12-Bit, Single-Supply Complete Voltage-Output DACs

## 1.4 Absolute Maximum Ratings (continued)

Power Dissipation ( $T_A = +70^\circ\text{C}$ , $T_j = +150^\circ\text{C}$ )	
24-Pin CERDIP (derate 12.50mW/°C above +70°C)	1000mW
28-Pin LCC (derate 10.20mW/°C above +70°C)	816mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C)	889mW
20-Pin LCC (derate 9.09mW/°C above +70°C)	727mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 sec)	+300°C

**1.5 Thermal Resistance**

$\Theta_{JC} = 40^\circ\text{C/W}$ for Q-24
$\Theta_{JC} = 50^\circ\text{C/W}$ for E-28
$\Theta_{JC} = 40^\circ\text{C/W}$ for Q-20
$\Theta_{JC} = 55^\circ\text{C/W}$ for E-20
$\Theta_{JA} = 80^\circ\text{C/W}$ for Q-24
$\Theta_{JA} = 98^\circ\text{C/W}$ for E-28
$\Theta_{JA} = 90^\circ\text{C/W}$ for Q-20
$\Theta_{JA} = 110^\circ\text{C/W}$ for E-20

## 2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

**TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS—Dual Supplies (Note 2)**

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS
					MIN	MAX	
Resolution	N		All	1, 2, 3	12		Bits
Relative Accuracy	INL	$V_{DD} = 11.4\text{V}$ , $V_{SS} = -11.4\text{V}$ $V_{DD} = 14.25\text{V}$ , $V_{SS} = -14.25\text{V}$	All	1, 2, 3	-1	1	LSB
		$V_{DD} = 14.25\text{V}$ , $V_{SS} = -14.25\text{V}$ $V_{DD} = 15.75\text{V}$ , $V_{SS} = -15.75\text{V}$			-1 1/2	1 1/2	
Differential Nonlinearity	DNL	Guaranteed monotonic	All	1, 2, 3	-1	1	LSB
Bipolar Offset Error			All	1	-3	3	LSB
				2, 3	-5	5	
DAC Gain Error (Note 3)	FSE		All	1, 2, 3	-2	2	LSB
Full-Scale Output Voltage Error (Note 4)		$V_{DD} = 12\text{V}$ , $V_{SS} = -12\text{V}$ $V_{DD} = 15\text{V}$ , $V_{SS} = -15\text{V}$	All	1	-0.2	0.2	%FSR
				2, 3	-0.6	0.6	
$\Delta\text{Full Scale}/\Delta V_{DD}$		$V_{DD} = \pm 5\%$	All	1	-0.12	0.12	%FSR/V
$\Delta\text{Full Scale}/\Delta V_{SS}$		$V_{SS} = \pm 5\%$	All	1	-0.1	0.1	%FSR/V
$\Delta\text{Offset}/\Delta V_{DD}$		$V_{DD} = \pm 5\%$	All	1, 2, 3	-2	2	mV
$\Delta\text{Offset}/\Delta V_{SS}$		$V_{SS} = \pm 5\%$	All	1, 2, 3	-1	1	mV
Reference Output		$V_{DD} = 12\text{V}$ and $15\text{V}$ $V_{SS} = -12\text{V}$ and $-15\text{V}$	All	1	4.99	5.01	V

# CMOS, 12-Bit, Single-Supply Complete Voltage-Output DACs

MX7245/MX7248/883B

**TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS—Dual Supplies (Note 2)  
(continued)**

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS
					MIN	MAX	
$\Delta$ Reference/ $\Delta V_{DD}$		$V_{DD} = \pm 5\%$	All	1		6	mV/V
Reference Load Sensitivity		Reference load current change (0 $\mu$ A to 100 $\mu$ A) not including $R_{OFS}$ current	All	1, 2, 3	-1.5	1.5	mV
Digital Input High Voltage	$V_{INH}$		All	1, 2, 3	2.4		V
Digital Input Low Voltage	$V_{INL}$		All	1, 2, 3		0.8	V
Digital Input Current – Data Inputs	$I_{IN}$	$V_{IN} = 0V$ or $V_{DD}$	All	1, 3	-1	1	$\mu$ A
				2	-10	10	
Digital Input High Current – Control Inputs (Note 5)	$I_{INH}$	$V_{IN} = V_{DD}$	All	1, 3	-1	1	$\mu$ A
				2	-10	10	
Digital Input Low Current – Control Inputs	$I_{INL}$	$V_{IN} = 0V$	All	1, 3		150	$\mu$ A
				2		200	
Digital Input Capacitance	$C_{IN}$		-1	4		8	pF
			-2				
Output Range Resistors	$R_{OUT}$		All	1, 2, 3	15	30	k $\Omega$
Output Voltage Ranges (Note 6)		Pin strappable. Minimum load resistance is 2k $\Omega$ to GND	All	1, 2, 3	0	5	V
					0	10	
					-5	-10	
Power-Supply Current	$I_{DD}$	Outputs unloaded	All	1		9	mA
				2, 3		12	
Output Voltage Settling Time (Note 7)	$t_S$	To $\pm 1$ LSB, $R_L = 5k\Omega$	All	4		5	$\mu$ s
Output Voltage Slew Rate	SR		All	4	2		V/ $\mu$ s
Chip-Select Pulse Width	$t_1$	Figure 1	All	9	80		ns
Write Pulse Width	$t_2$	Figure 1	All	9	80		ns
Chip-Select to Write-Setup Time	$t_3$	Figure 1	All	9	0		ns
Chip-Select to Write-Hold Time	$t_4$	Figure 1	All	9	0		ns
Data Valid to Write-Setup Time	$t_5$	Figure 1	-1	9		100	ns
			-2				
Data Valid to Write-Hold Time	$t_6$	Figure 1	All	9	10		ns
Load DAC Pulse Width	$t_7$	Figure 1	All	9	80		ns
Clear Pulse Width	$t_8$	Figure 1	All	9	80		ns

**Note 2:**  $V_{DD} = 11.4V$ ,  $V_{SS} = -11.4V$ ;  $V_{DD} = 15.75V$ ,  $V_{SS} = -15.75V$ , AGND = DGND = 0V,  $R_L = 2k\Omega$  to GND,  $C_L = 100pF$  to GND, REF unloaded, unless otherwise noted. Characterized at initial design and after any subsequent redesigns.

**Note 3:** Calculated with respect to the reference voltage and measured with an allowance for the offset error.

**Note 4:** Calculated with an ideal 4.9988V or 9.9976V, depending on the range.

**Note 5:** Control inputs are CS, WR, LDAC, and CLR for MX7245 and CSMSB, CSLSB, WR, and LDAC for MX7248.

**Note 6:** 0V to 10V applies to  $V_{DD} = 15V \pm 5\%$  and  $V_{SS} = -15V \pm 5\%$  only.

**Note 7:** For positive full-scale change, the DAC register is loaded with all 0s, then all 1s. For negative full-scale change, the DAC register is loaded with all 1s, then all 0s.

**MAXIM**

8-55

8

# CMOS, 12-Bit, Single-Supply Complete Voltage-Output DACs

**TABLE 2. ELECTRICAL PERFORMANCE CHARACTERISTICS—Single Supply (Note 8)**

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS
					MIN	MAX	
Resolution	N		All	1, 2, 3	12		Bits
Relative Accuracy	INL	$V_{DD} = 11.4V$ and $14.25V$	All	1, 2, 3	-1	1	LSB
		$V_{DD} = 14.25V$ and $15.75V$			-1 1/2	1 1/2	
Differential Nonlinearity	DNL	Guaranteed monotonic	All	1, 2, 3	-1	1	LSB
Unipolar Offset Error			All	1	-3	3	LSB
				2, 3	-5	5	
DAC Gain Error (Note 3)	FSE		All	1, 2, 3	-2	2	LSB
Full-Scale Output Voltage Error (Note 4)		$V_{DD} = 12V$ and $15V$	All	1	-0.2	0.2	%FSR
				2, 3	-0.6	0.6	
$\Delta$ Full Scale/ $\Delta V_{DD}$		$V_{DD} = \pm 5\%$	All	1	-0.12	0.12	%FSR/V
$\Delta$ Offset/ $\Delta V_{DD}$		$V_{DD} = \pm 5\%$	All	1, 2, 3	-2	2	mV
Reference Output		$V_{DD} = 12V$ and $15V$	All	1	4.99	5.01	V
$\Delta$ Reference/ $\Delta V_{DD}$		$V_{DD} = \pm 5\%$	All	1		6	mV/V
Reference Load Sensitivity		Reference load current change (0 $\mu$ A to 100 $\mu$ A) not including $R_{OFS}$ current	All	1, 2, 3	-1.5	1.5	mV
Digital Input High Voltage	$V_{INH}$		All	1, 2, 3	2.4		V
Digital Input Low Voltage	$V_{INL}$		All	1, 2, 3		0.8	V
Digital Input Current – Data Inputs	$I_{IN}$	$V_{IN} = 0V$ or $V_{DD}$	All	1, 3	-1	1	$\mu$ A
				2	-10	10	
Digital Input High Current – Control Inputs (Note 5)	$I_{INH}$	$V_{IN} = V_{DD}$	All	1, 3	-1	1	$\mu$ A
				2	-10	10	
Digital Input Low Current – Control Inputs	$I_{INL}$	$V_{IN} = 0V$	All	1, 3		150	$\mu$ A
				2		200	
Digital Input Capacitance	$C_{IN}$		-1	4		8	pF
			-2			16	
Output Range Resistors	$R_{OUT}$		All	1, 2, 3	15	30	k $\Omega$
Output Voltage Ranges (Note 6)		Pin strappable. Minimum load resistance is 2k $\Omega$ to GND	All	1, 2, 3	0	5	V
					0	10	
Power-Supply Current	$I_{DD}$	Outputs unloaded	All	1		9	mA
				2, 3		12	
Output Voltage Settling Time (Note 7)	$t_s$	To $\pm 1$ LSB, $R_L = 5k\Omega$	All	4		5	$\mu$ s
Output Voltage Slew Rate	SR		All	4	2		V/ $\mu$ s
Chip-Select Pulse Width	$t_1$	Figure 1	All	9	105		ns
Write Pulse Width	$t_2$	Figure 1	All	9	105		ns
Chip-Select to Write-Setup Time	$t_3$	Figure 1	All	9	0		ns
Chip-Select to Write-Hold Time	$t_4$	Figure 1	All	9	0		ns

# CMOS, 12-Bit, Single-Supply Complete Voltage-Output DACs

MX7245/MX7248/883B

**TABLE 2. ELECTRICAL PERFORMANCE CHARACTERISTICS—Single Supply (Note 8)**  
(continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS
					MIN	MAX	
Data Valid to Write-Setup Time	$t_5$	Figure 1	-1	9	155		ns
			-2	9	180		
Data Valid to Write-Hold Time	$t_6$	Figure 1	All	9	0		ns
Load DAC Pulse Width	$t_7$	Figure 1	All	9	90		ns
Clear Pulse Width	$t_8$	Figure 1	All	9	140		ns

**Note 3:** Calculated with respect to the reference voltage and measured with an allowance for the offset error.

**Note 4:** Calculated with an ideal 4.9988V or 9.9976V, depending on the range.

**Note 5:** Control inputs are CS, WR, LDAC, and CLR for MX7245 and CSMSB, CSLSB, WR, and LDAC for MX7248.

**Note 6:** 0V to 10V applies to  $V_{DD} = 15V \pm 5\%$ .

**Note 7:** For positive full-scale change, the DAC register is loaded with all 0s, then all 1s. For negative full-scale change, the DAC register is loaded with all 1s, then all 0s.

**Note 8:**  $V_{DD} = 11.4V$  and  $15.75V$ ,  $AGND = DGND = 0V$ ,  $R_L = 2k\Omega$  to GND,  $C_L = 100pF$  to GND, REF unloaded, unless otherwise noted. Characterized at initial design and after any subsequent redesigns.

# CMOS, 12-Bit, Single-Supply Complete Voltage-Output DACs

## 3.0 QUALITY ASSURANCE

- 3.1** Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.
- 3.2** Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
- (1) Test condition A, B, C, or D.
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
  - (3) Interim and final electrical test requirements shall be as specified in Table 3.
- 3.3** Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
- Group A inspection:
- (1) Tests as specified in Table 3.
  - (2) Selected subgroups in Tables 1 and 2, Method 5005 of MIL-STD-883 shall be omitted.
- 3.4** Groups C and D inspections:
- a. End-point electrical parameters shall be specified in Tables 1 and 2.
  - b. Steady-state life test (Method 1005 of MIL-STD-883):
    - (1) Test condition A, B, C, or D.
    - (2)  $T_A = +125^\circ\text{C}$ , minimum.
    - (3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

**TABLE 3. ELECTRICAL TEST REQUIREMENTS**

MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Tables 1 and 2)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1*, 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 4,** 9, 10,*** 11****
Groups C and D End-Point Electrical Parameters (Method 5005)	1

\* PDA applies to Subgroup 1 only.

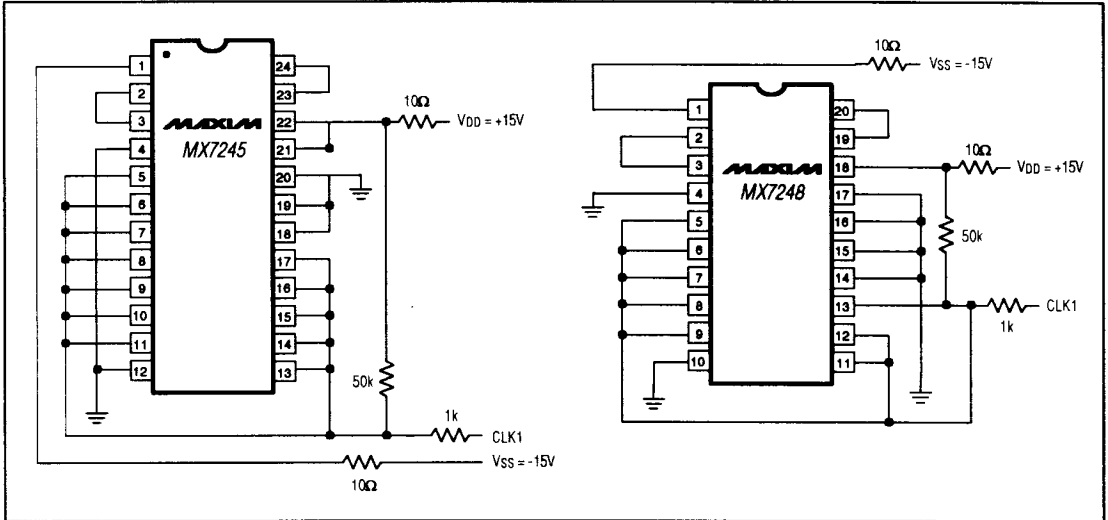
\*\* Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 5 units.

\*\*\* Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table 1.

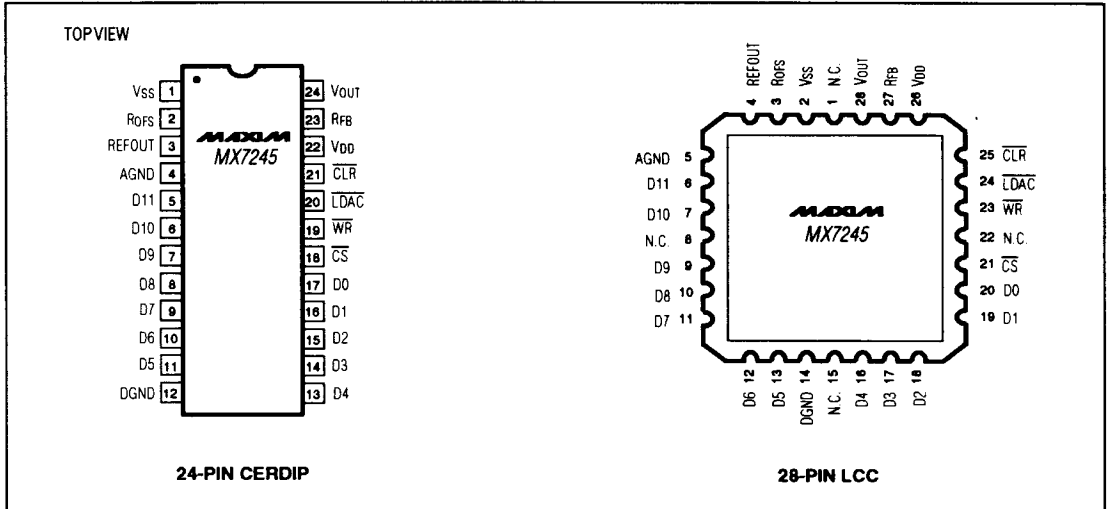
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MX7245/MX7248/883B

## 4.0 Life Test/Burn-In Circuits



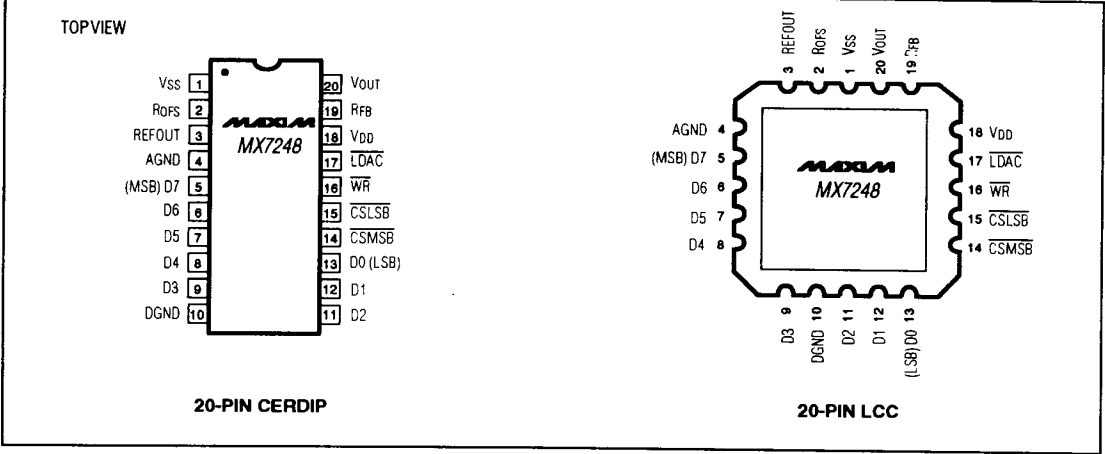
## 4.1 Pin Configurations



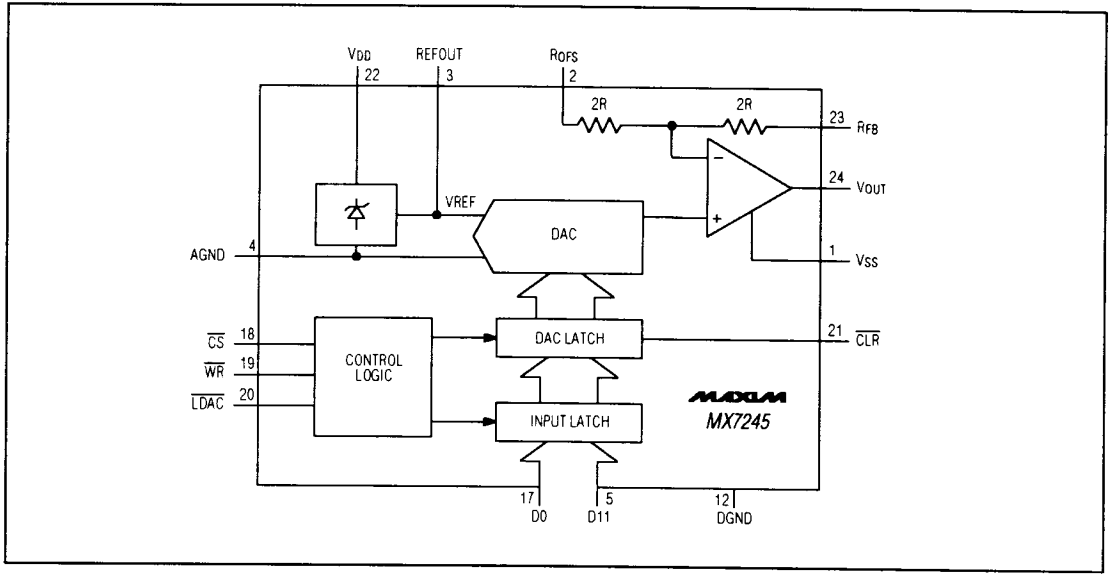
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## 4.1 Pin Configurations (continued)



## 4.2 Functional Diagrams

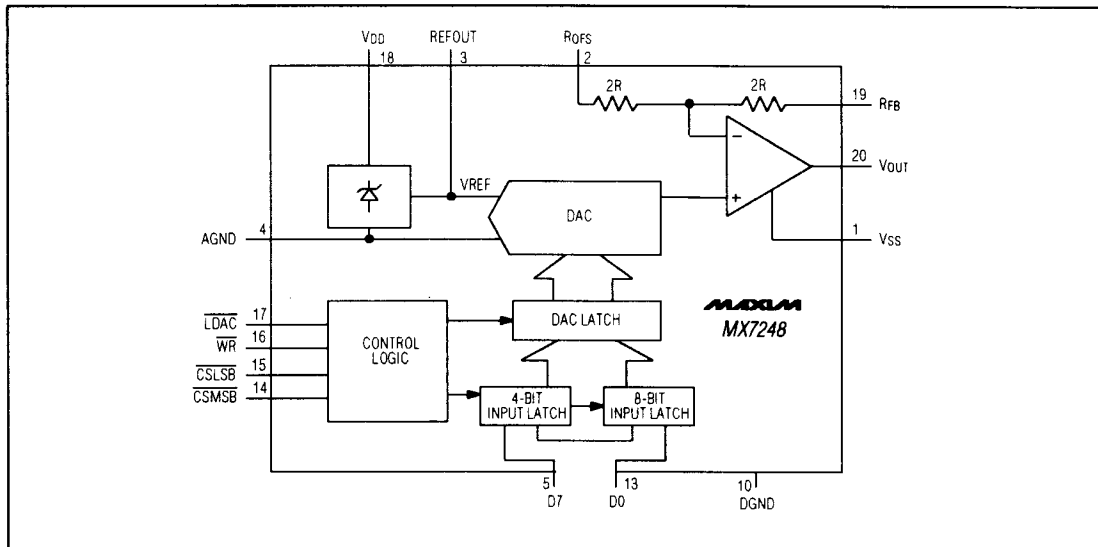




# CMOS, 12-Bit, Single-Supply Complete Voltage-Output DACs

MX7245/MX7248/883B

## 4.2 Functional Diagrams (continued)



## 4.3 Timing Diagrams

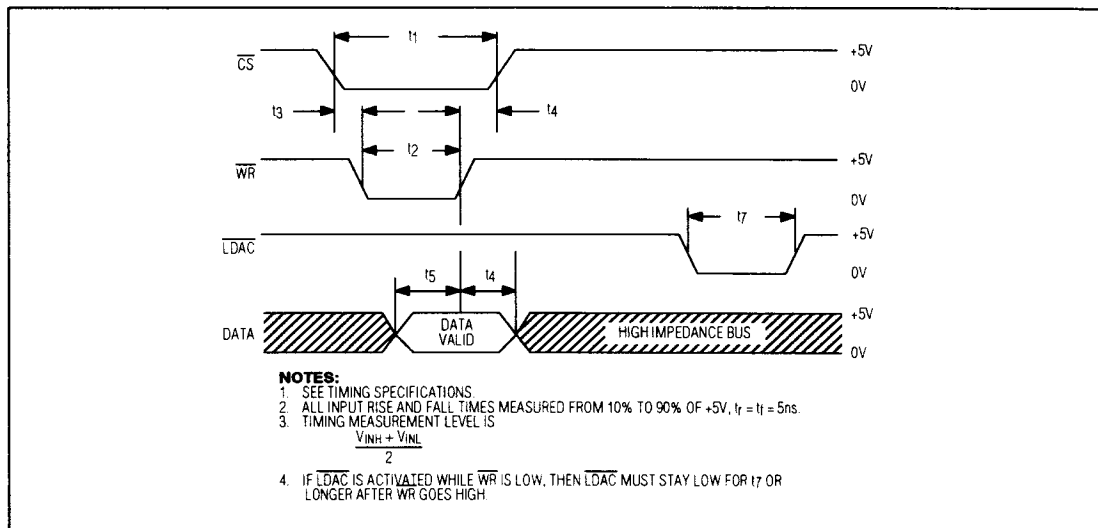


Figure 1a. MX7245 Write-Cycle Timing Diagram

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8-61

8

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## 4.3 Timing Diagrams (continued)

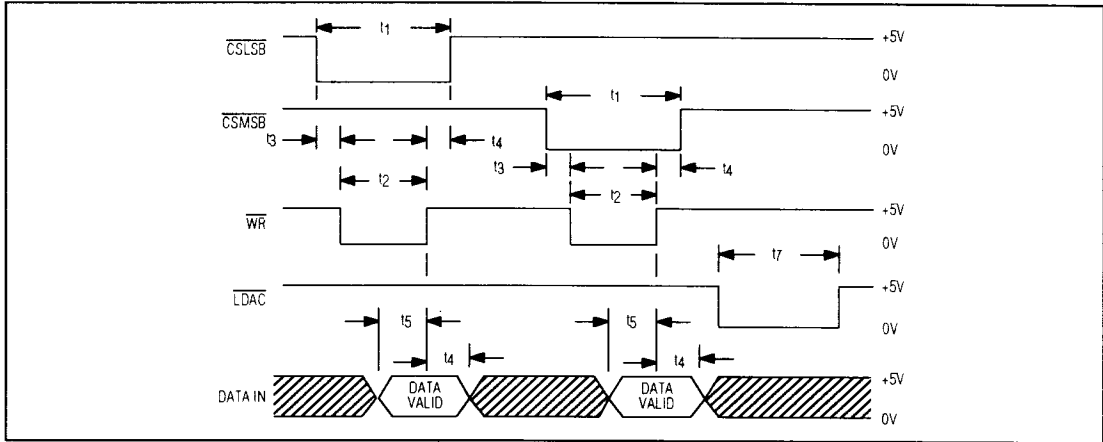


Figure 1b. MX7248 Write-Cycle Timing Diagram

## 4.4 Mode Control Tables

MX7245				Function
CLR	LDAC	WR	CS	
H	L	L	L	Both latches transparent
H	H	H	X	Both latches latched
H	H	X	H	Both latches latched
H	H	L	L	Input latches transparent
H	H		L	Input latches latched
H	L	H	H	DAC latches transparent
H		H	H	DAC latches latched

MX7248				Function
CSLSB	CSMSB	WR	LDAC	
L	H	L	H	Loads LS byte into input latch
L	H		H	Latches LS byte into input latch
	H	L	H	Latches LS byte into input latch
H	L	L	H	Loads MS nibble into input latch
H	L		H	Latches MS nibble into input latch
H		L	H	Latches MS nibble into input latch
H	H	H	L	Loads input latch into DAC latch

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